fp1. Introduction

This design document serves as a guidance for our future implementations. Its intended audiences are our team and 3410 staff who are masters of pipelined mips processors.

2. Overview
  1) design of control signal
3.

instruction	31-26	25-21	20-16	15-11	10-6	5-0
ADDIU	001001	src	dest	signed imm		
ANDI	001100	src	dest	zero imm		
ORI	001101	src	dest	zero imm		
XORI	001110	src	dest	zero imm		
SLTI	001010	src	dest	signed imm		
SLTIU	001011	src	dest	signed imm		
ADDU	000000	src1	src2	dest	000000	100001
SUBU	000000	src1	src2	dest	000000	100011
AND	000000	src1	src2	dest	000000	100100
OR	000000	src1	src2	dest	000000	100101
XOR	000000	src1	src2	dest	000000	100110
NOR	000000	src1	src2	dest	000000	100111
SLT	000000	src1	src2	dest	000000	101010
SLTU	000000	src1	src2	dest	000000	101011
MOVN	000000	src1	src2	dest	000000	001011
MOVZ	000000	src1	src2	dest	000000	001010
SLL	000000	000000	src	dest	shamt	000000
SRL	000000	000000	src	dest	shamt	000010
SRA	000000	000000	src	dest	shame	000011
SLLV	000000	src1	src2	dest	000000	000100
SRLV	000000	src1	src2	dest	000000	000110
SRAV	000000	src1	src2	dest	000000	000111
LUI	001111	00000	dest	imm		

J	000010	target				
JR	000000	src	00000	00000	00000	
JAL	000011	target				
JALR	000000	src	00000	001001		
BEQ	000100	src1	src2	signed off		
BNE	000101	src1	src2	signed off		
BGTZ	000111	src	00000	signed off		
BLTZ	000001	src	00000	signed off		
BGEZ	000001	src	00001	signed off		
LW	100011	base	dest	signed off		
LB	100000	base	dest	signed off		
LBU	100100	base	dest	signed off		
SW	101011	base	dest	signed off		
SB	101000	base	dest	signed off		

1. R type $ I type instruction
The difference between R type instruction Opcode and I type instructions Opcode is the 29th bit in the instruction, which is 1 in R type instructions and 0 in I type instructions.

a. the rd port connection
As illustrated in the diagram, there is a 2-1 mix before the rd port. When the control signal is 1(i.e we are executing R type instruction, the MUX chooses the 15th -11th bits of instruction, which is the rd for R type instruction. When the control signal is 0 (i.e. we are executing I type instruction), the MUX chooses the 21th - 16 th bits of instruction, which is rd for I type instruction.

d. the 2nd input of ALU
When the control signal is 0 (i.e. we are executing R type instruction), we select the value in register B to further perform operation with the value in register A.
When the control signal is 1 (i.e. we are executing I type instruction), we select the value in immediate field to further perform operation with the value in register A.

c. the op code in ALU

Let's first make some observations.

R type instruction : the mips instruction op code for XORI is 001110. The ALU opcode for XOR is 1110.
the mips instruction op code for ANDI is 001100. The ALU opcode for for AND is 1000.

So, the ALU opcode is obtained by taking the least significant three bits of mips instruction opcode and add a zero at the least significant bit.