



KVM/ARM: The Design and Implementation of the Linux ARM Hypervisor

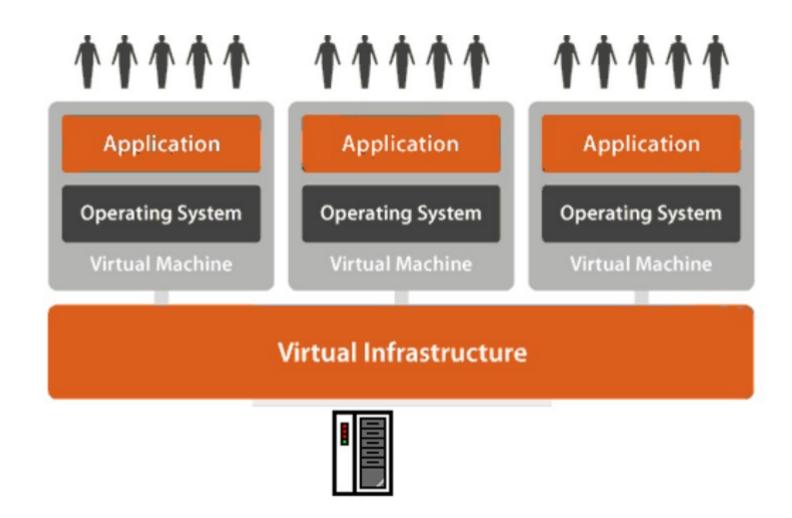
Fall 2014

Presented By: Probir Roy



Virtualization & Hypervisor







Virtualization & Hypervisor (cont.)



Which type of Hypervisor is better?

VM OS / App

VM OS / App

Bare Metal Hypervisor

Hardware

Virtual Machine
OS / App

Hardware Emulation

Operating System

Hardware

Bare Metal / Native Hypervisor

Hosted Hypervisor

Xen, VMWare ESX

VMWare Workstation

www.software.intel.com





KVM/ARM: The Design and Implementation of the Linux ARM Hypervisor

Apps

Apps

Guest OS

Guest OS

QEMU

QEMU

Linux Kernel

Hypervisor (KVM)

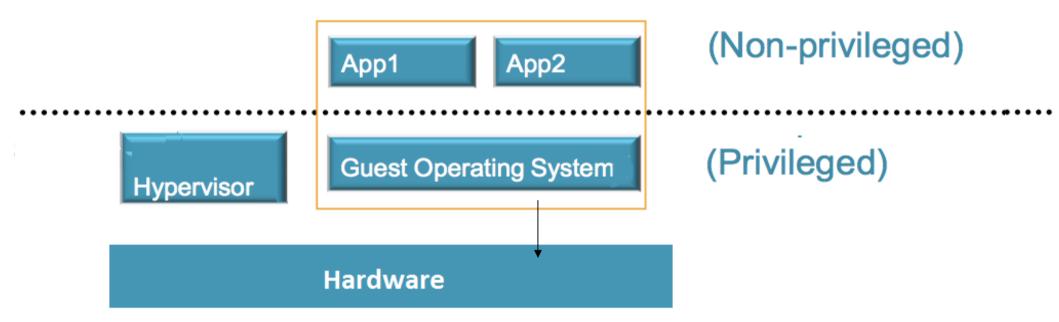
Full Virtualization

ARM



Prior ARMV7





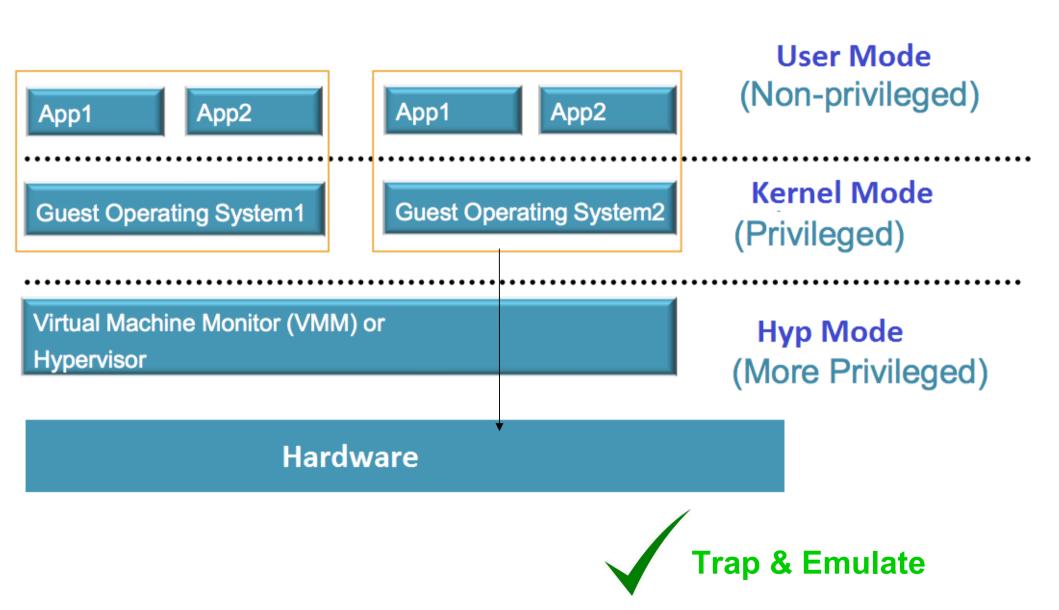
Not Classically Virtualizable





ARM V7 Virtualization Extension



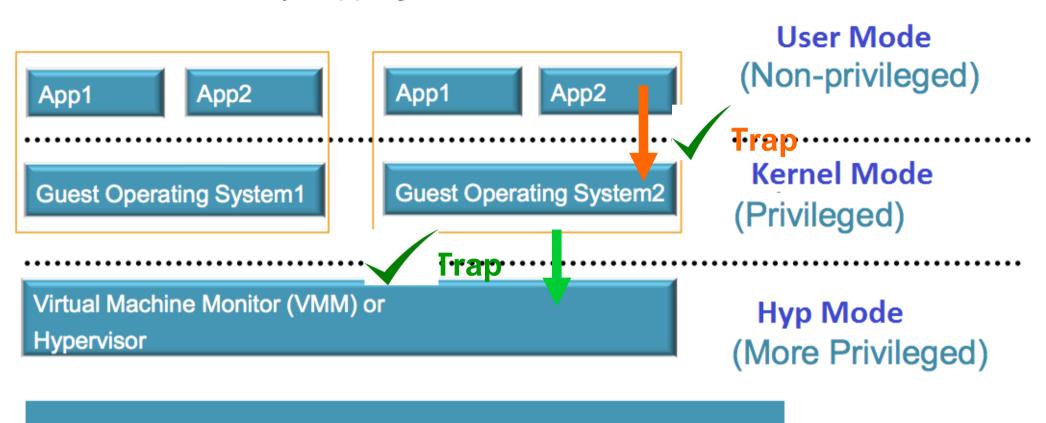




CPU Virtualization



Why trapping at Kernel Mode is useful?



Hardware

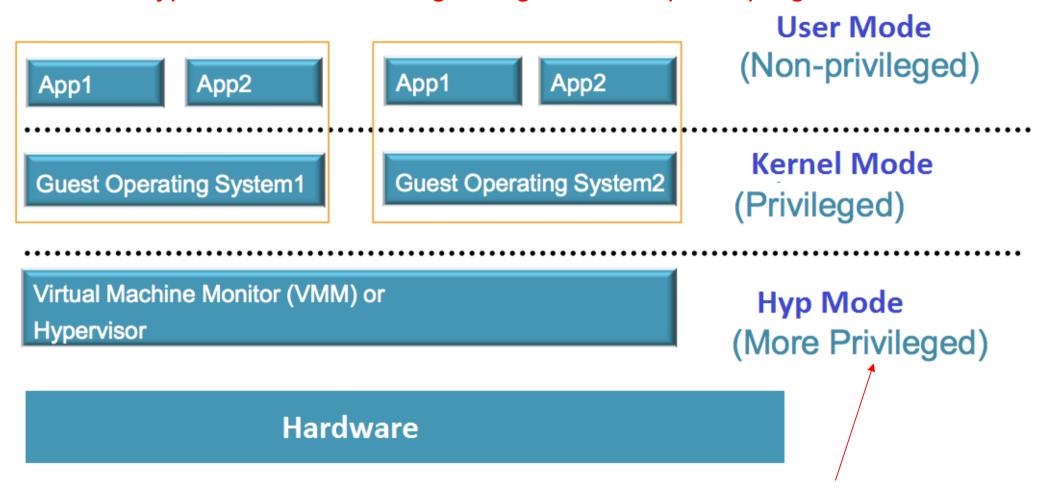
From Hyp Mode, hardware Configurable to trap sensitive instructions and interrupt to Hyp Mode Hardware Configurable to trap sensitive instructions and interrupt directly to VM's Kernel mode



CPU Virtualization



Hypervisor should be lightweight and simple to program



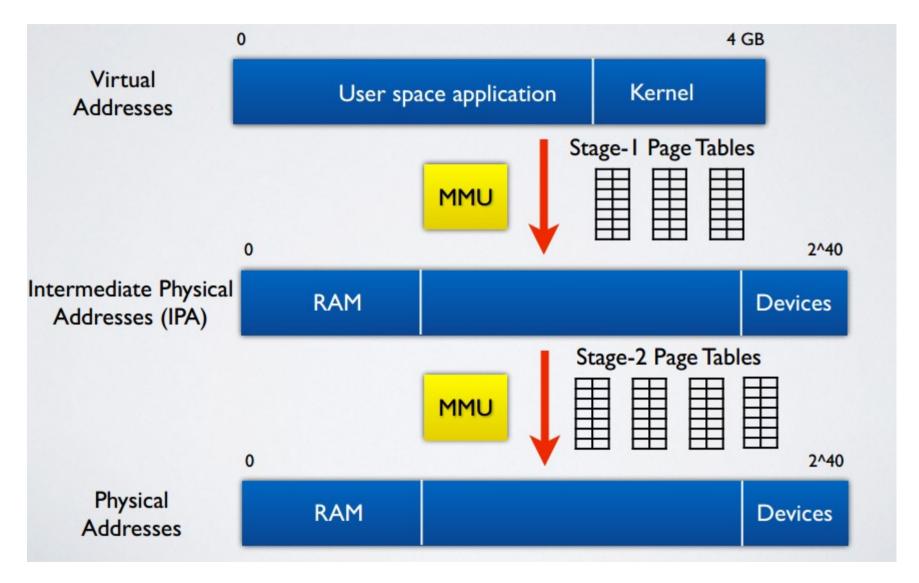
Reduced Number of Control Registers

Hyp mode has its own separate address space

Page tables entries is protected from user mode, as they should not be shared with user mode





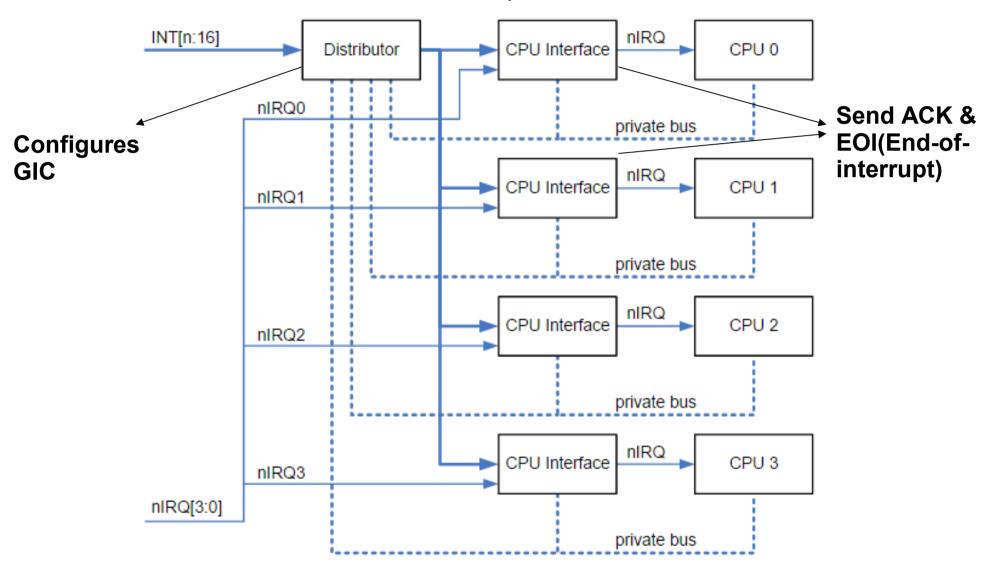


Hardware support to virtualize physical memory: Stage 2 Page Tables Enabled/Disabled from Hyp Mode





Generic Interrupt Controller



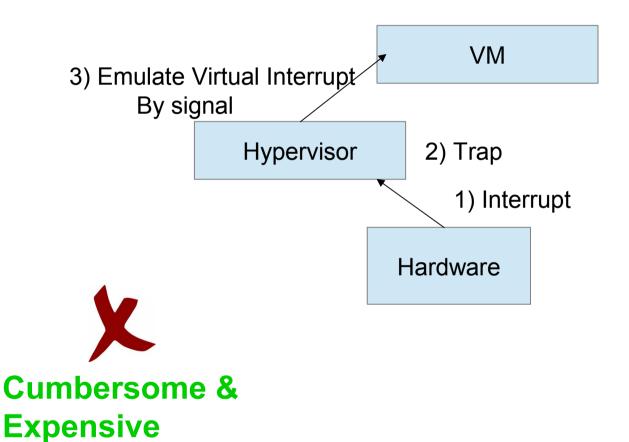
http://infocenter.arm.com





Generic Interrupt Controller

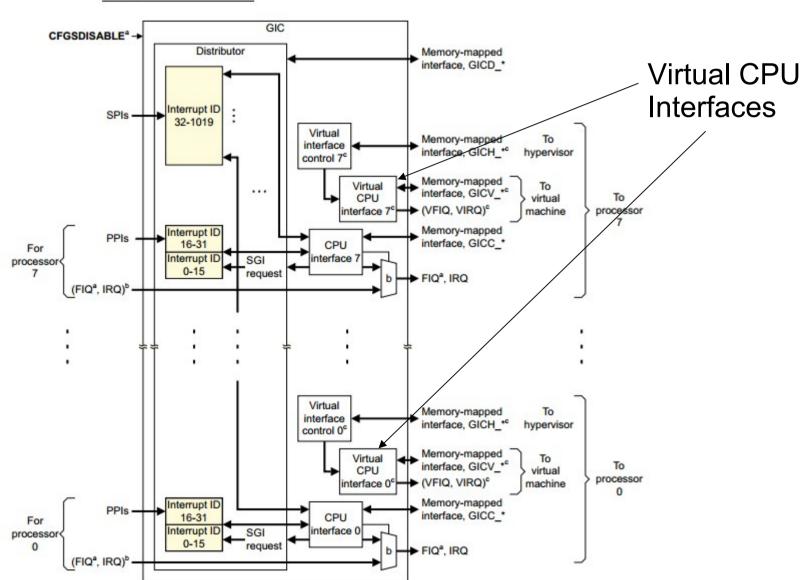
Trapping Interrupt in Hyp Mode







Generic Interrupt Controller (V2.0) Virtual GIC Why Virtual Distributor is required?



But No Virtual Distributor

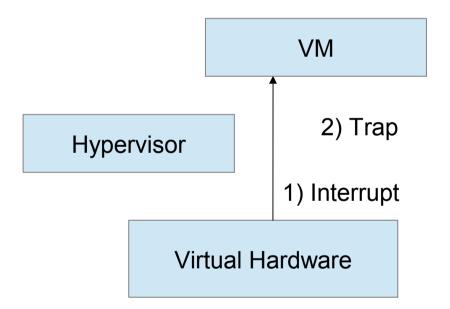
http://infocenter.arm.com





Generic Interrupt Controller (V2.0) Virtual GIC

Trapping Interrupt in Kernel Mode







Generic Timer support

Timer 0 CPU 0

Timer 1 CPU 1

Counter

Timer 2 CPU 2

Timer 3 CPU 3

Can be configured from Hyp Mode

But requires Timer operations to be performed by Hyp

ARM introduces Virtual Timer and Counter





Generic and Virtualized Timer support

CPU 0 Timer 0 Timer 1 CPU 1 Accessible Counter from Hyp mode Timer 2 CPU₂ Timer 3 CPU₃ Virtual CPU Virtual Counter Virtual Timer 0 Virtual CPU Virtual Counter Virtual Timer 1 Accessible from VMs Virtual CPU Virtual Timer 2 Virtual Counter Virtual CPU **Virtual Counter** Virtual Timer 3 3

Why Virtual Timer support is required?





PL0 User

PL1 Kernel

PL2 Hyp

Linux Kernel KVM

Firstly, Linux is written to work in kernel mode and would not run unmodified in Hyp Mode

Some registers and table formats are different in Hyp mode than in kernel mode

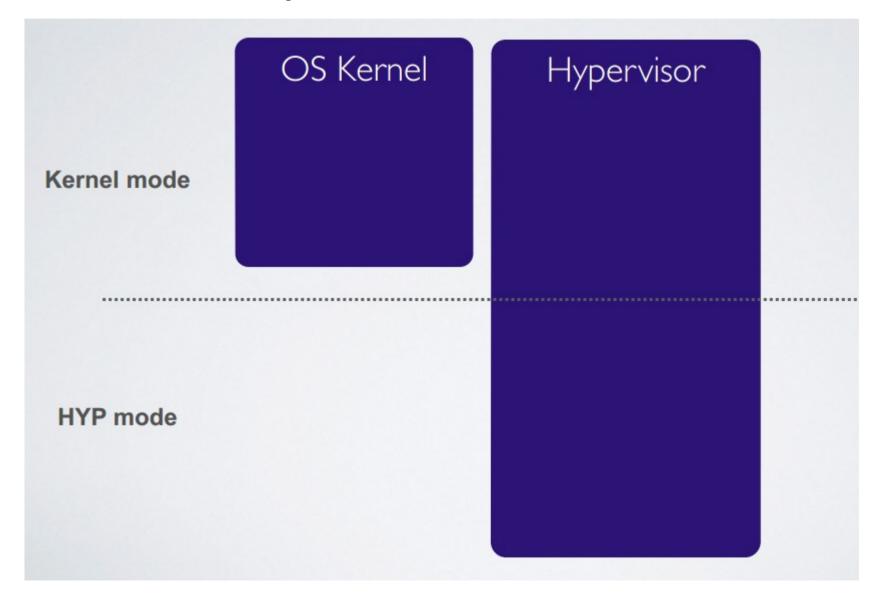
Secondly, Running entire kernel in Hyp Mode would adversely affect native performance

Hyp mode has its own separate address space. This requires explicitly map user space data while accessing user space memory



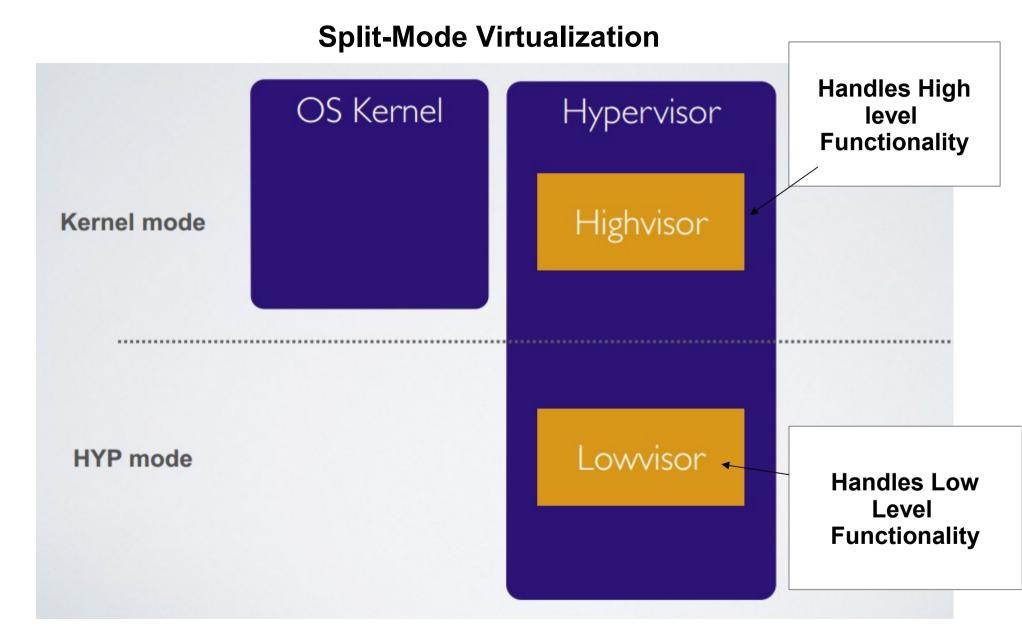


Split-Mode Virtualization





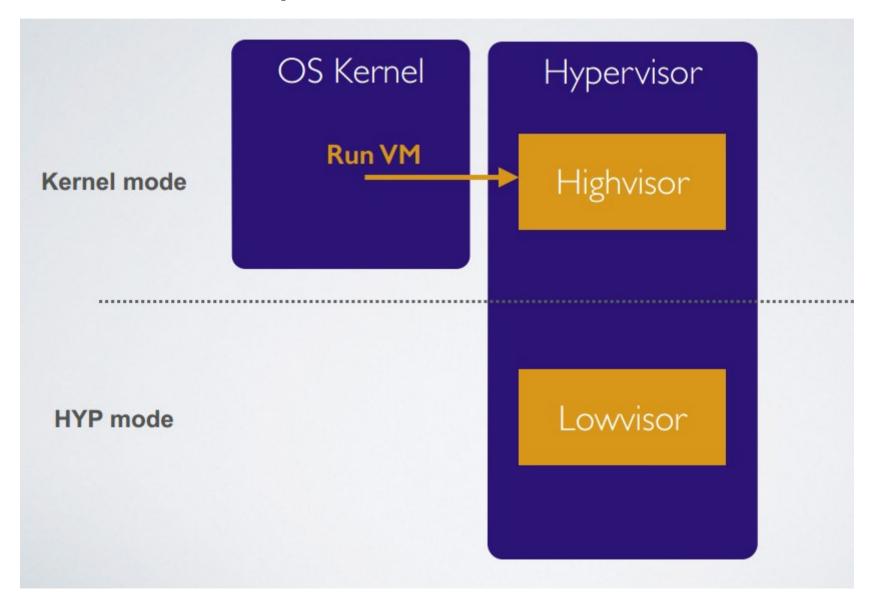








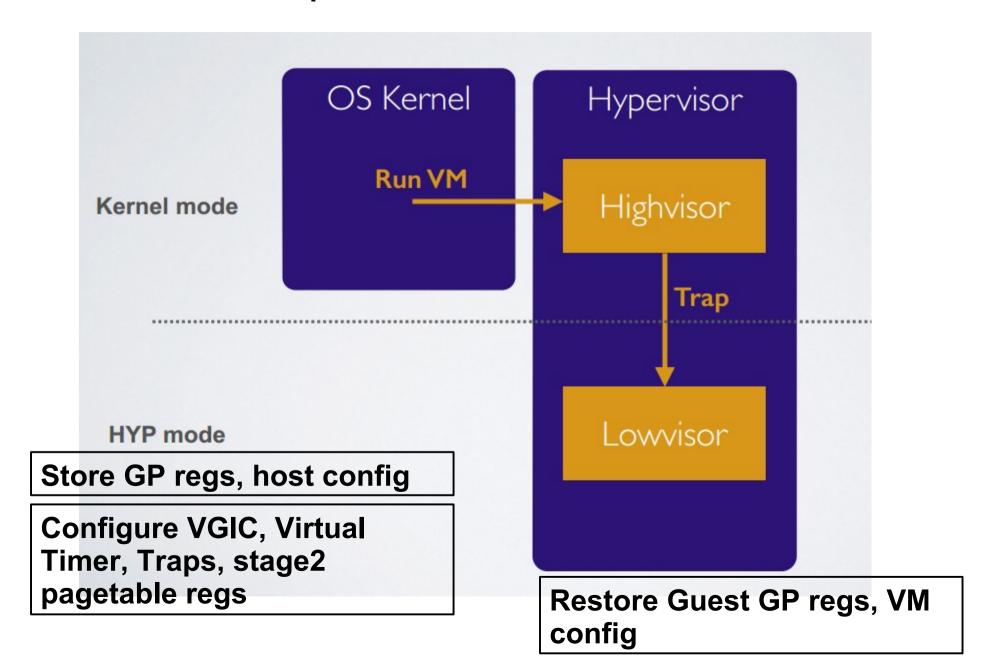
Split-Mode Virtualization







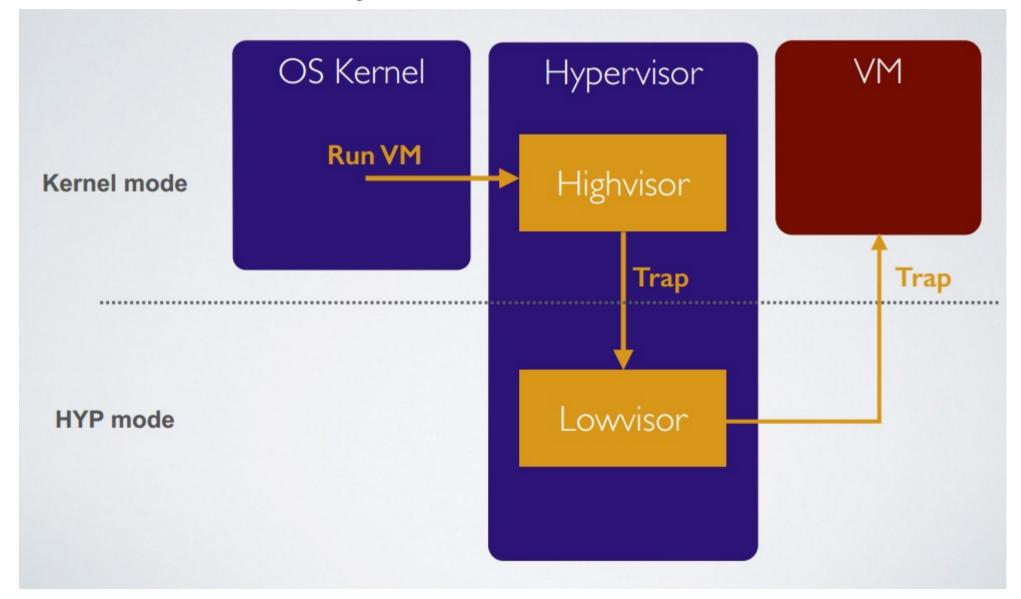
Split-Mode Virtualization







Split-Mode Virtualization

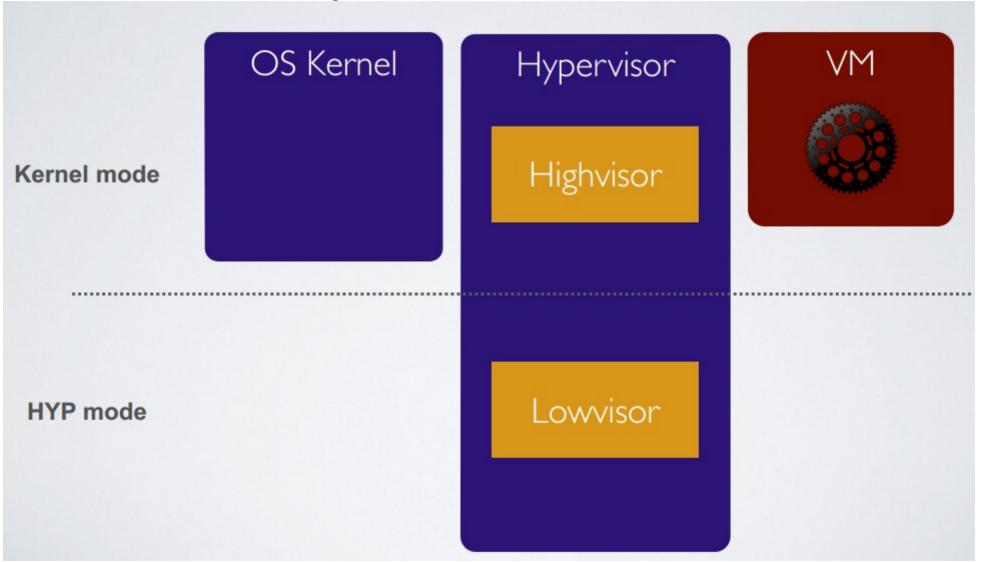


Lowvisor creates correct execution context by configuring hardware





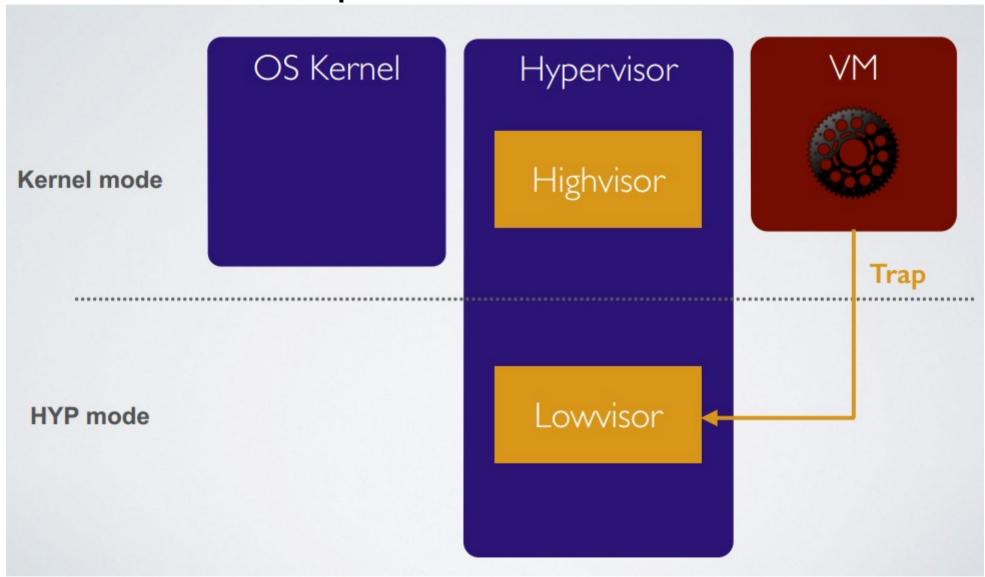
Split-Mode Virtualization







Split-Mode Virtualization

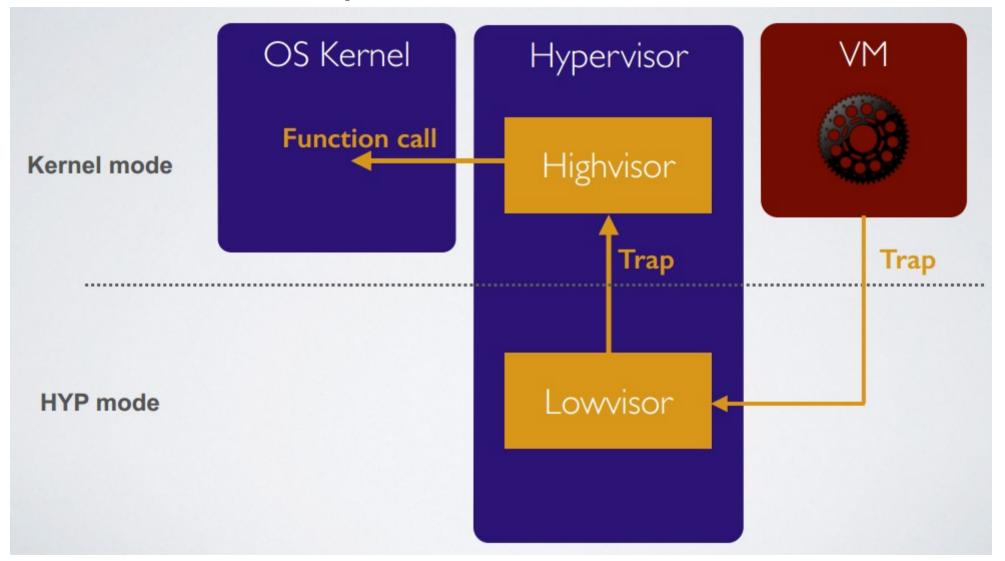


Lowvisor: Handles Interrupts and Exceptions





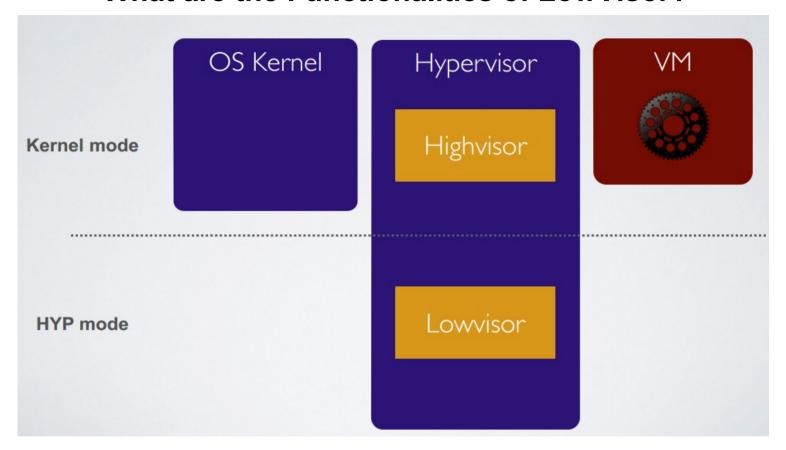
Split-Mode Virtualization







What are the Functionalities of LowVisor?

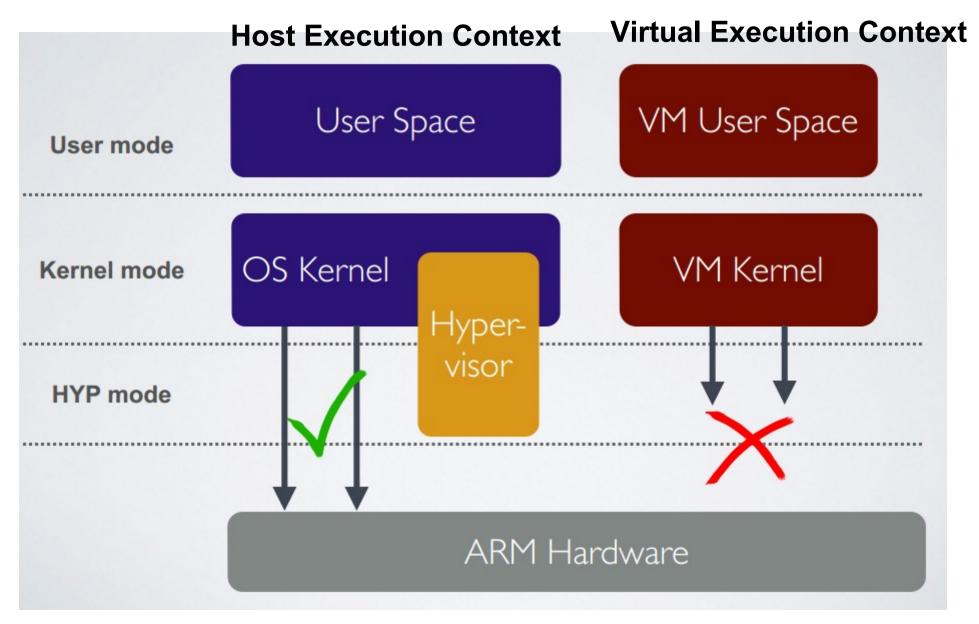


Trap handler: Handles Interrupt and Exception

Set Correct Execution context by configuring hardware



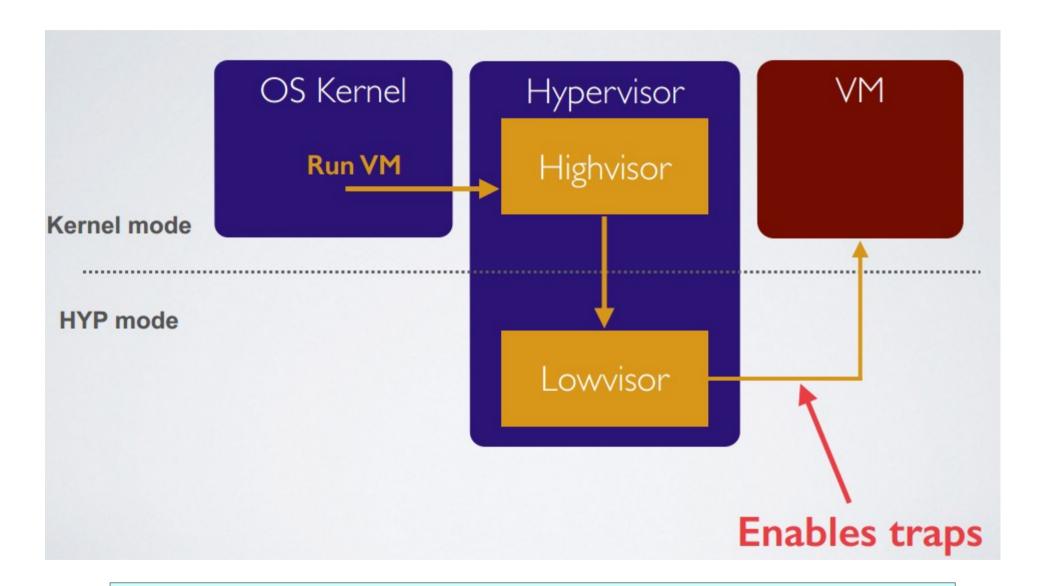






CPU Virtualization

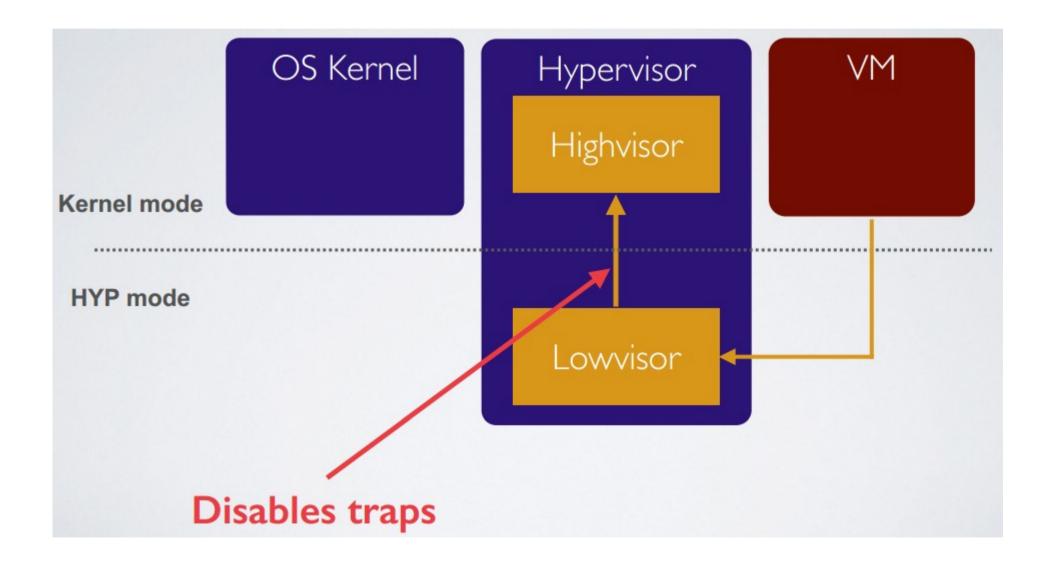






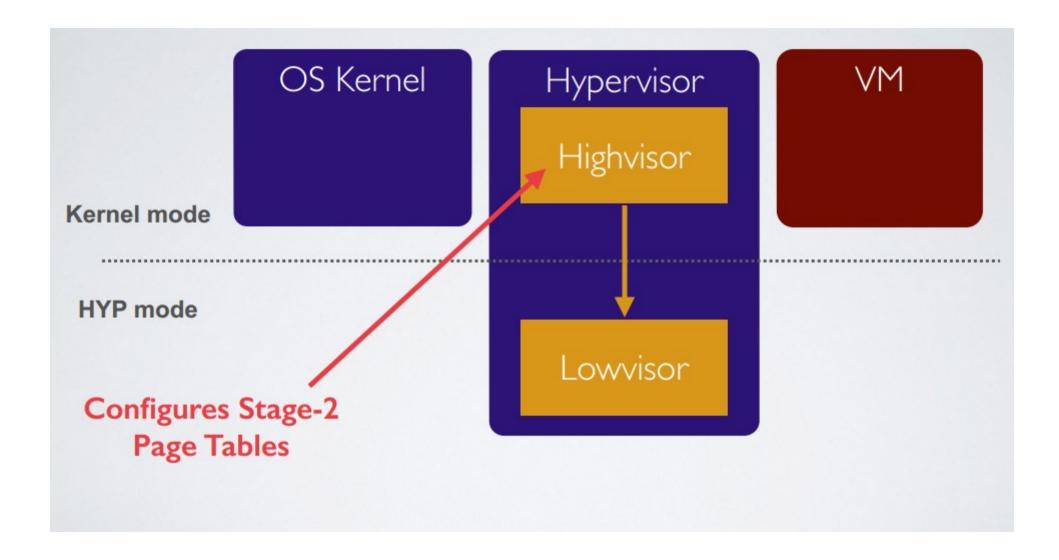
CPU Virtualization







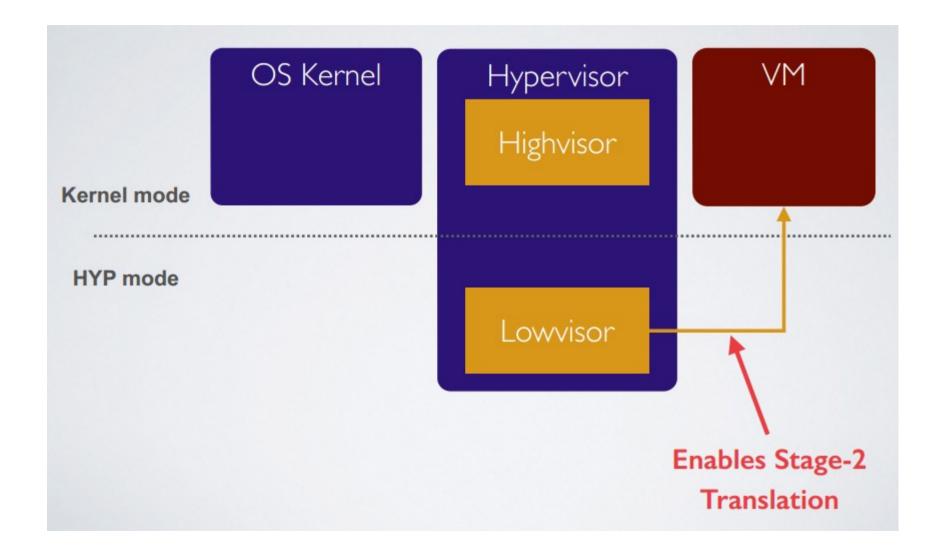




Configuring page tables is a high level Functionality



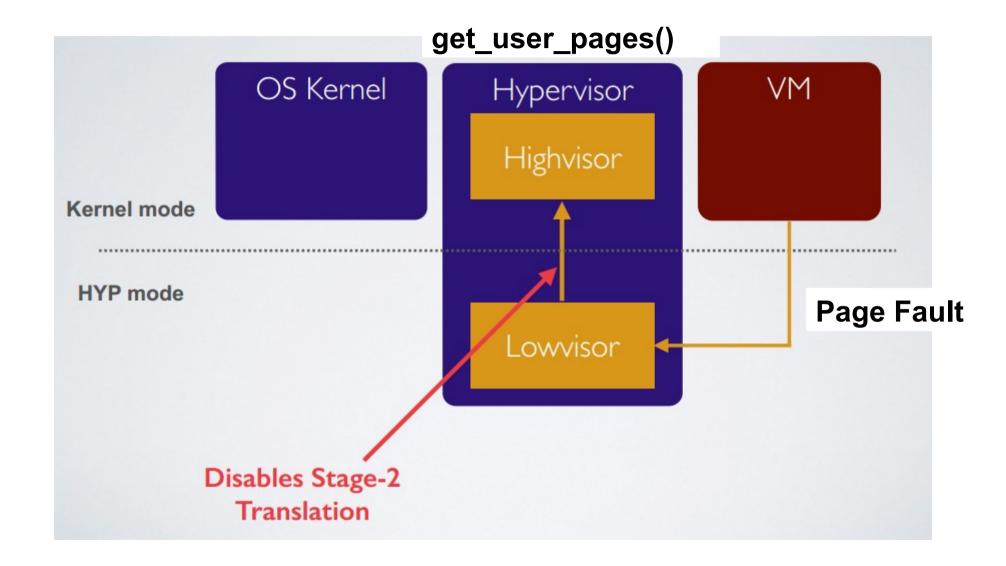




But LowVisor has hardware access as it runs in Hyp Mode

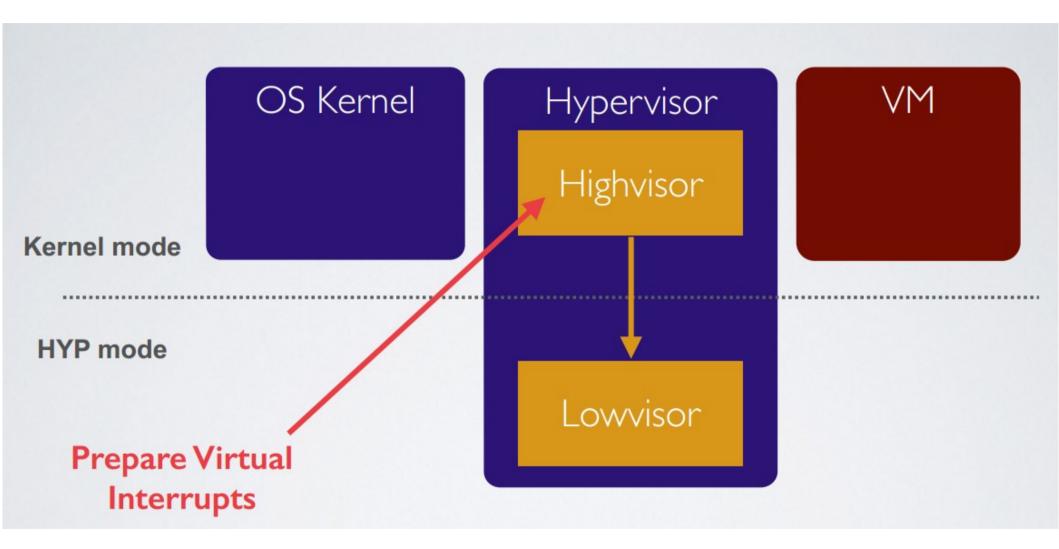






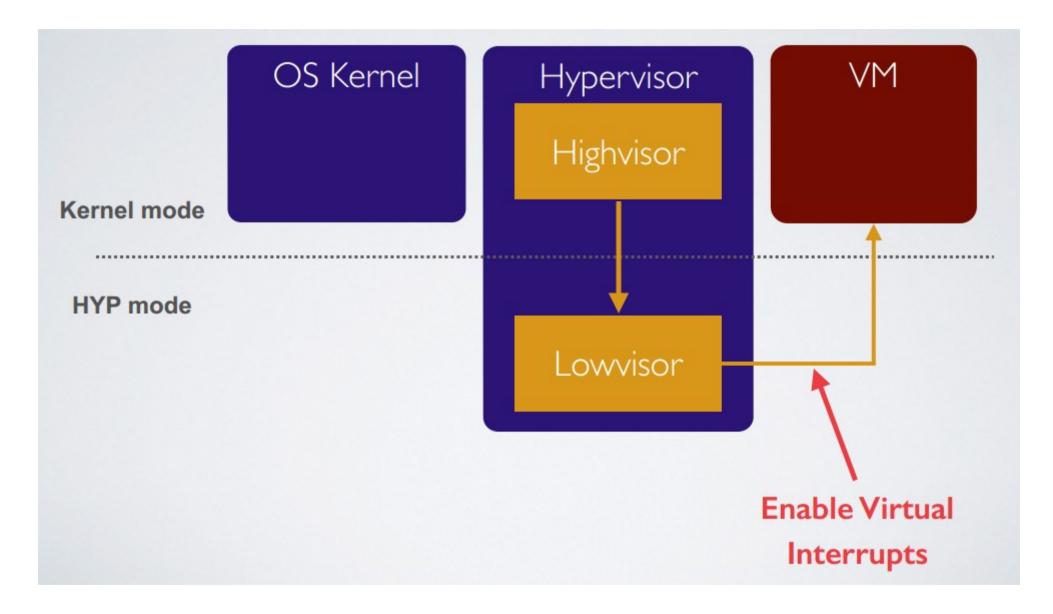






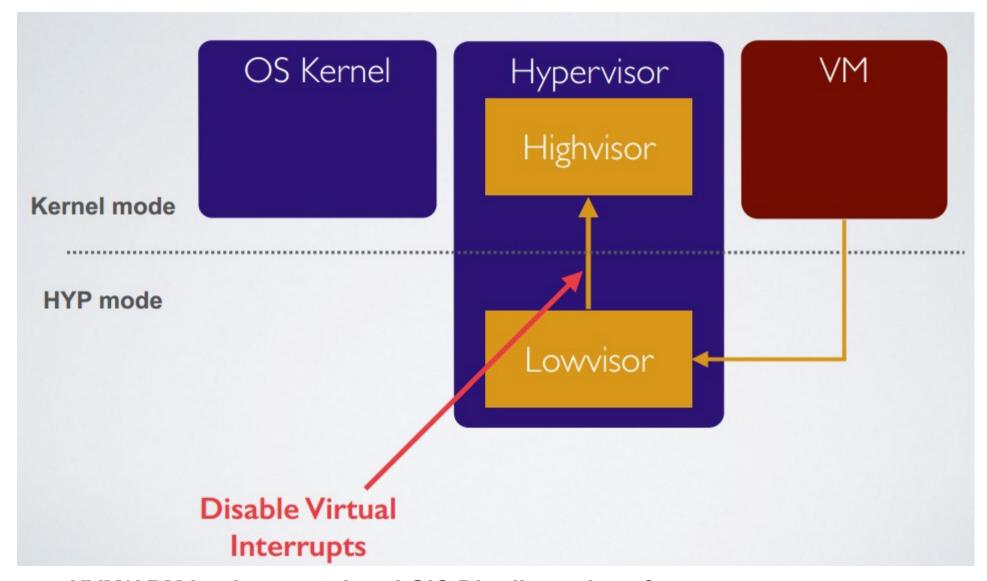










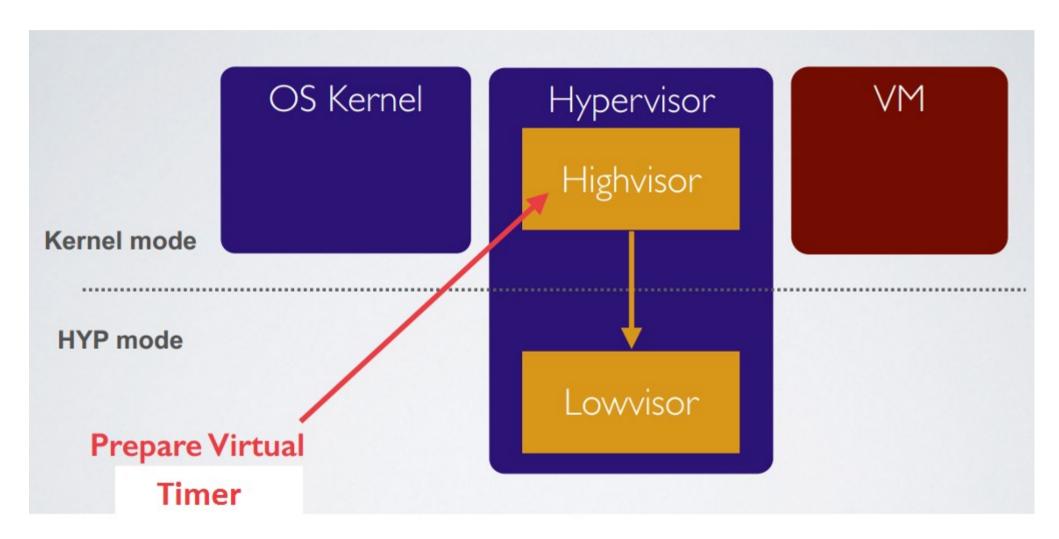


KVM/ARM implements virtual GIC Distributor in software

What happens when a virtual interrupt occurs?

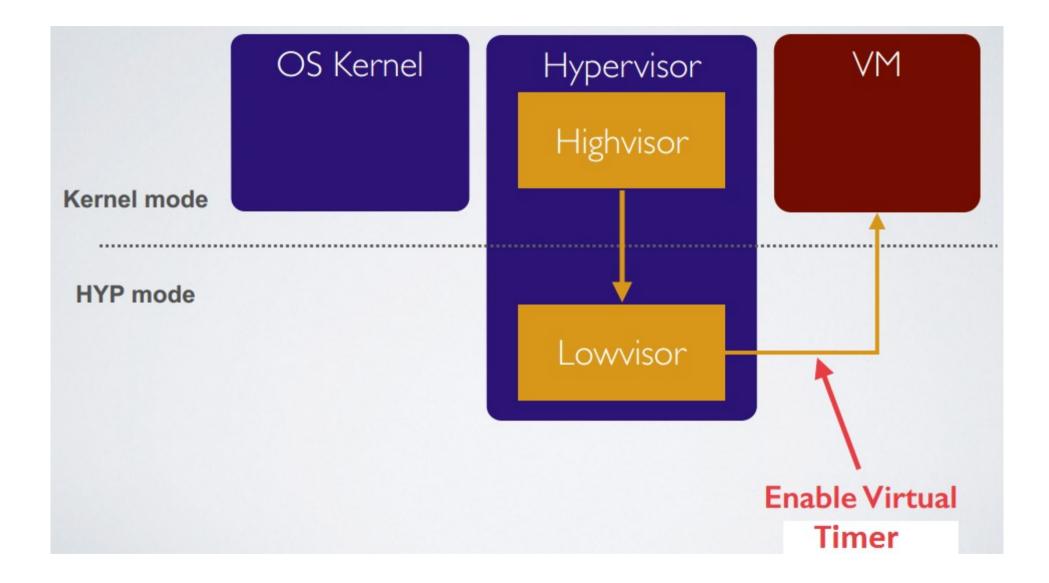






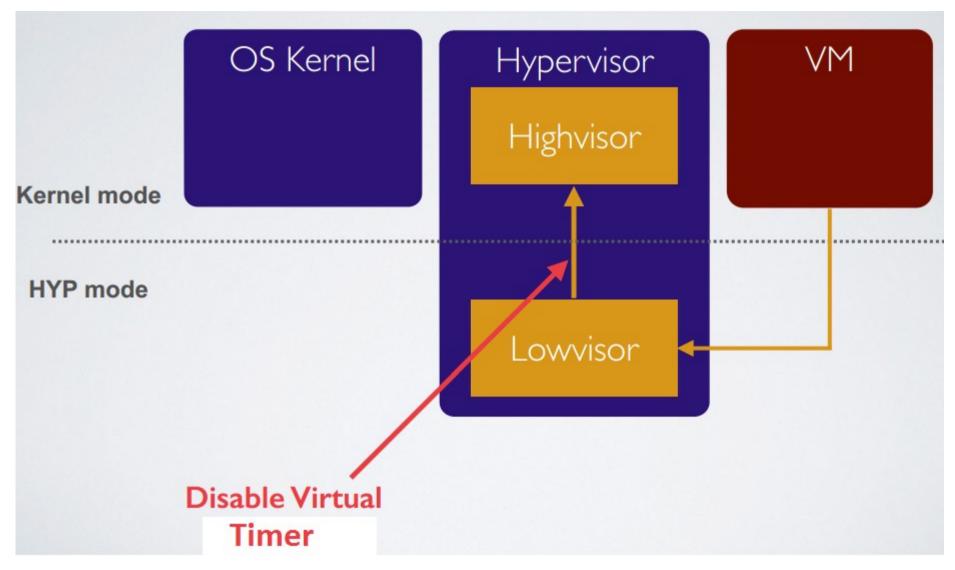










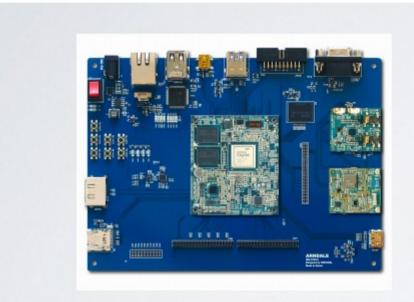


Virtual timers cannot directly raise virtual interrupts, but always raise hardware interrupts



mplementation & Experimental Setup





Arndale Board - Exynos 5250 Dual-Core Cortex A-15 @ 1.4 GHz eSATA SSD



MacBook Air Dual-Core Intel i7 @1.8 GHz SATA SSD



mplementation & Experimental Setup





version 12.10 (Quantal Quetzal)



Same amount of memory across all runs



Kernel version 3.10



Same kernel config





Two world switches

Micro Test	ARM	ARM no VGIC/vtimers	x86 laptop	x86 server
Hypercall	5,326	2,270	1,336	1,638
Trap	27	27	632	821
I/O Kerp	5,990	2,850	3,19	3,291
I/O V	10,119	6,704	10,9	12,218
7	14,366	32,951	17,1	21,177
∠OI+ACK	427	13,726	2	2,305

Table 3: Micro-Architectural Cycle ints

Cost of saving and restoring VGIC states

hardware support to save and restore state





Switching the hardware mode

Micro Test	ARM	ARM no VGIC/vtimers	x86 laptop	x86 server
Hypercall	5,326	2,270	1,336	1,638
Trap	27	27	632	821
I/O Kernel	5,990	2,850	3,190	3,291
I/O Use	10,119	6,704	10,9	12,218
IP ^r	14,366	32,951	17,1	21,177
JI+ACK	427	13,726	2	2,305

Table 3: Micro-Architectural Cycle ints

Manipulate two registers to trap

hardware supported save and restore state





cost of an I/O operation from the VM to a device

Micro Test	ARM	ARM no VGIC/vtimers	x86 laptop	x86 server
Hypercall	5,326	2,270	1,336	1,638
Trap	27	27	632	821
I/O Kernel	5,990	2,850	3,190	3,291
I/O User	10,119	6,704	10,985	12,218
IPI	14,366	32,951	17,138	21,177
1+ACK	427	13 26	2,043	2,305

Table 3: Micro-Are' ctural Cycle Cou

saving and restoring VGIC

x86 KVM saves and restores additional state lazily

hardware supported save and restore state





cost of Inter-processor Interrupt

Micro Test	ARM	ARM no VGIC/vtimers	x86 laptop	x86 server
Hypercall	5,326	2,270	1,336	1,638
Trap	27	27	632	821
I/O Kernel	5,990	2,850	3,190	3,291
I/O User	10,119	6,704	10,985	12,218
IPI	14,366	32,951	17,138	21,177
EOI+ACK	427	13,726	2,043	2,305

Table 3: Micro-Architectural Cycle unts

Hardware supported VGIC

EOI/ACK must be handled in Root mode in x86



Recommendation to Hardware Designers



Share Kernel Mode Memory Model in Hyp Mode

- Current implementation is different and require extra effort for memory management

Make VGIC state access fast, or at least infrequent

 Cause overhead because of slow MMIO access. Summary registers describing virtual interrupt state could be an improvement

Completely avoid IPI traps

- As Virtual Distributors are implemented in software, this cause some overhead.



Summary



KVM/ARM was the first system to run unmodified guests on hardware

Facilitated by split-mode virtualization

Comparison with KVM





Questions?