Distribution Substation Protection Improvement Using Logic Processors

High Value Solutions With Low Incremental Costs

One of the seldom recognized benefits of multifunction relaying systems is the low incremental cost of implementing advanced protection, control and automation functions. Many of the capabilities discussed below do not even require additional wiring. Once the new relays, logic processor, and communication processor are installed for basic protection; advanced protection, control, and automation functions usually require only a few more settings. The additional engineering cost is a fraction of engineering costs associated with the basic wiring, installation and setting of the devices.

There are several major concerns in the protection of complex distribution substations equipped with a bus-tie breaker and served by two transformers, such as in Figure 1.
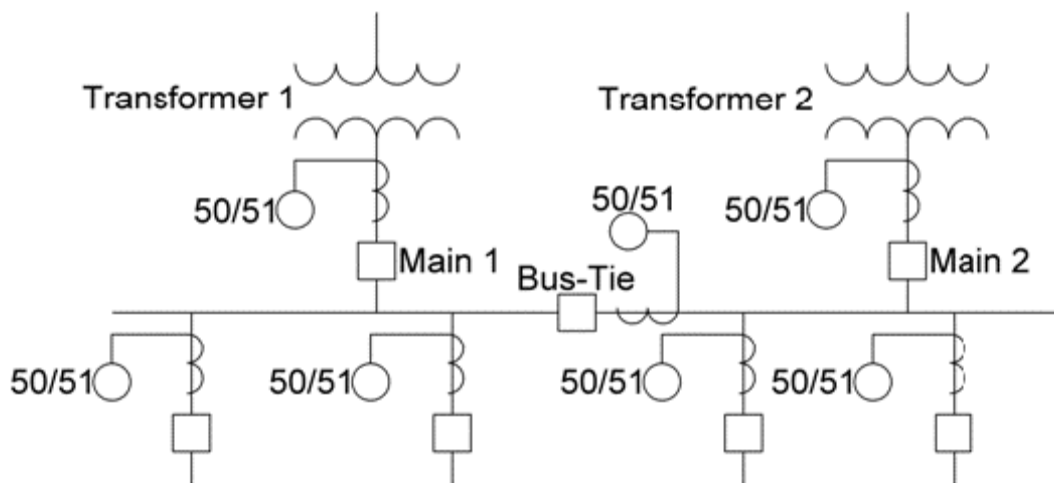

Figure 1: Distribution Substation Having Two Transformers, Two Buses, and a Bus-Tie Breaker

Some key protection and operational issues are:

- Operating with a closed bus-tie breaker increases the fault duty for bus faults and close-in feeder faults while fault current measured by an individual transformer secondary main breaker is reduced (as compared to operating with the bus-tie open). Coordination of discrete secondary main breaker relays for the bus-tie closed condition compromises either fault clearing time or security when the bus-tie is open or one transformer is out-of-service.
- For a fault in the transformer zone, the bus served by the faulted transformer experiences an outage if the bus-tie breaker is operated normally open. With discrete relays, this outage lasts until a crew can be dispatched to the substation to manually reenergize the bus by closing the bus-tie breaker.
- When the bus-tie breaker is operated normally closed, the transformers share the total station load more evenly.
- Long bus-fault clearing times increase the substation arc flash hazard to personnel and increase the potential for switchgear damage if a fault occurs.

When the substation overcurrent protection is based on newer multifunction relays, there are opportunities to improve protection and operation through installation of substation logic processors with the new protective relays. These devices use real-time data collected from substation relays to enhance

protection performance and offer several control capabilities that enhance substation operation. Following are some protection and operational enhancements to consider:

- Fast-bus tripping significantly reduces bus fault clearing times
- Secondary main breaker relay settings optimize automatically for bus-tie breaker position
- Automatic bus restoration reduces outage length following transformer-zone fault clearance
- Selective load-sharing and load-shedding functions prevent transformer overload

To implement these capabilities, the logic processor trades data and control signals with each of the substation secondary-voltage protective relays, including the relay monitoring the bus-tie breaker. Our preference for this function is the SEL-2100 Logic Processor which communicates using SEL's Mirrored Bit protocol with feeder protection modules such as the ELOCS.

Fast Bus Tripping

In traditional distribution bus protection schemes the secondary main breaker relay operates with coordinated time-delay to clear bus faults and to provide backup protection for uncleared feeder faults. This coordination can produce bus-fault clearing times on the order of 0.5 – 0.75 seconds, depending on feeder protection settings.

In a fast bus tripping application, the secondary main relay (and the bus-tie relay, if present) is blocked from tripping for any feeder fault, but allowed to trip with a short, definite-time delay for any bus fault. By using a logic processor to steer the feeder relay block-trip signals, a fast bus tripping scheme can be implemented that automatically adjusts its performance for changing bus topologies, providing coordinated primary bus-fault tripping and backup protection, regardless of which main breakers are closed. Typical bus fault clearing times are reduced to less than 10 cycles, a savings of 0.35 – 0.6 seconds. This time savings represents a major reduction in switchgear damage potential and arc flash hazard for bus faults.

Automatic Main Breaker Relay Setting Revision

Because the fault duty and fault current distribution changes dramatically for faults at or near the substation depending on which main and bus-tie breakers are closed when the fault occurs, the discrete relay coordination is a compromise of either sensitivity or security, depending on the selected philosophy and the assumed station topology used for the coordination. A substation logic processor applied with multifunction main breaker and bus-tie breaker relays allows these compromises to be avoided. Two or more coordination approaches are defined in advance by protection engineers for the various station topologies. Using breaker positions reported by each main and bus-tie relay, the logic processor commands each relay to use the appropriate protection element set that provides best coordination for the active topology. This may or may not involve multiple setting groups within the relays, depending on availability of multiple overcurrent protection elements within an individual setting group.

Automatic Bus Restoration

If a transformer zone fault is cleared while the bus-tie breaker is open, the bus and feeders served by the faulted transformer are left deenergized until the bus-tie breaker is closed. If this is done manually, the resulting outage can be long, recommending operation of the substation with the bus-tie breaker closed and subjecting the station to the consequential higher fault duties. A substation logic processor monitoring the main breaker positions and the transformer lockout relay positions can automatically close a normally open bus-tie breaker following the transformer zone trip. This shortens the resulting outage length from minutes or hours to cycles and permits operation of the bus-tie breaker normally open.

Automatic Load Shedding and Load Sharing

A further advantage afforded by the substation logic processor is in the loading of the substation transformers. When the bus-tie breaker is operated normally open, the transformers do not share the station load evenly since each transformer carries only its own bus. A substation logic processor provides the opportunity to automatically close the bustie breaker (and adjust the secondary main breaker relay settings accordingly) if either of the transformers reaches a significant fraction of its rated load. If both transformers reach maximum load, or if one transformer reaches maximum load while serving both buses, the logic processor can initiate automatic load shedding to reduce load to acceptable values.