











#### LM224K, LM224KA, LM324, LM324A, LM324K, LM324KA, LM2902 LM124, LM124A, LM224, LM224A, LM2902V, LM2902K, LM2902KV, LM2902KAV

SLOS066W - SEPTEMBER 1975-REVISED MARCH 2015

# LMx24, LMx24x, LMx24xx, LM2902, LM2902x, LM2902xx, LM2902xxx Quadruple **Operational Amplifiers**

#### **Features**

- 2-kV ESD Protection for:
  - LM224K, LM224KA
  - LM324K, LM324KA
  - LM2902K, LM2902KV, LM2902KAV
- Wide Supply Ranges
  - Single Supply: 3 V to 32 V (26 V for LM2902)
  - Dual Supplies: ±1.5 V to ±16 V (±13 V for LM2902)
- Low Supply-Current Drain Independent of Supply Voltage: 0.8 mA Typical
- Common-Mode Input Voltage Range Includes Ground, Allowing Direct Sensing Near Ground
- Low Input Bias and Offset Parameters
  - Input Offset Voltage: 3 mV Typical A Versions: 2 mV Typical
  - Input Offset Current: 2 nA Typical
  - Input Bias Current: 20 nA Typical A Versions: 15 nA Typical
- Differential Input Voltage Range Equal to Maximum-Rated Supply Voltage: 32 V (26 V for LM2902)
- Open-Loop Differential Voltage Amplification: 100 V/mV Typical
- Internal Frequency Compensation
- On Products Compliant to MIL-PRF-38535, All Parameters are Tested Unless Otherwise Noted, On All Other Products, Production Processing Does Not Necessarily Include Testing of All Parameters.

## 2 Applications

- Blu-ray Players and Home Theaters
- Chemical and Gas Sensors
- **DVD Recorders and Players**
- Digital Multimeter: Bench and Systems
- Digital Multimeter: Handhelds
- Field Transmitter: Temperature Sensors
- Motor Control: AC Induction, Brushed DC, Brushless DC, High-Voltage, Low-Voltage, Permanent Magnet, and Stepper Motor
- Oscilloscopes
- TV: LCD and Digital
- Temperature Sensors or Controllers Using
- Weigh Scales

## 3 Description

These devices consist of four independent high-gain frequency-compensated operational amplifiers that are designed specifically to operate from a single supply or split supply over a wide range of voltages.

#### Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)				
	SOIC (14)	8.65 mm × 3.91 mm				
	CDIP (14)	19.56 mm × 6.67 mm				
LMx24, LMx24x, LMx24xx, LM2902,	PDIP (14)	19.30 mm × 6.35 mm				
LM2902x,	CFP (14)	9.21 mm × 5.97 mm				
LM2902xx, LM2902xxx	TSSOP (14)	5.00 mm × 4.40 mm				
LIVIZOZXXX	SO (14)	9.20 mm × 5.30 mm				
	SSOP (14)	6.20 mm × 5.30 mm				
LM124, LM124A	LCCC (20)	8.90 mm × 8.90 mm				

<sup>(1)</sup> For all available packages, see the orderable addendum at the end of the data sheet.

#### Symbol (Each Amplifier)







SLOS066W - SEPTEMBER 1975-REVISED MARCH 2015

www.ti.com

## **Table of Contents**

1	Features 1		8.1 Overview	10
2	Applications 1		8.2 Functional Block Diagram	10
3	Description 1		8.3 Feature Description	11
4	Revision History2		8.4 Device Functional Modes	11
5	Pin Configuration and Functions	9	Application and Implementation	12
6	Specifications4		9.1 Application Information	12
٠	6.1 Absolute Maximum Ratings		9.2 Typical Application	12
	6.2 ESD Ratings	10	Power Supply Recommendations	13
	6.3 Recommended Operating Conditions	11	Layout	13
	6.4 Thermal Information		11.1 Layout Guidelines	13
	6.5 Electrical Characteristics for LMx24 and LM324K 5		11.2 Layout Examples	14
	6.6 Electrical Characteristics for LM2902 and LM2902V 6	12	Device and Documentation Support	15
	6.7 Electrical Characteristics for LMx24A and		12.1 Documentation Support	
	LM324KA 6		12.2 Related Links	15
	6.8 Operating Conditions		12.3 Trademarks	15
	6.9 Typical Characteristics 8		12.4 Electrostatic Discharge Caution	15
7	Parameter Measurement Information 9		12.5 Glossary	
8	Detailed Description 10	13	Mechanical, Packaging, and Orderable Information	15

## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

С	changes from Revision V (January 2014) to Revision W	Page
•	Added Applications	1
•	Added Device Information table	1
•	Added Device and Documentation Support section	15
•	Added Mechanical, Packaging, and Orderable Information section	15
С	changes from Revision U (August 2010) to Revision V	Page
•	Updated document to new TI data sheet format - no specification changes	1
•	Updated Features	1
•		
•	Removed Ordering Information table	



## 5 Pin Configuration and Functions





#### **Pin Functions**

	PIN			
NAME	LCCC NO.	SOIC, SSOP, CDIP, PDIP, SO, TSSOP, CFP NO.	I/O	DESCRIPTION
1IN-	3	2	I	Negative input
1IN+	4	3	1	Positive input
10UT	2	1	0	Output
2IN-	9	6	1	Negative input
2IN+	8	5	1	Positive input
2OUT	10	7	0	Output
3IN-	13	9	I	Negative input
3IN+	14	10	1	Positive input
3OUT	12	8	0	Output
4IN-	19	13	1	Negative input
4IN+	18	12	I	Positive input
4OUT	20	14	0	Output
GND	16	11	_	Ground
	1			
	5			
NC	7			Do not connect
NC	11	_	_	Do not connect
	15			
	17			
V <sub>CC</sub>	6	4	_	Power supply



## 6 Specifications

#### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		LM2	902	LMx24xx,	LMx24, LMx24x, LMx24xx, LM2902x, LM2902xx, LM2902xxx			
		MIN	MAX	MIN	MAX			
Supply voltage, V <sub>CC</sub> <sup>(2)</sup>		±13	26	±16	32	V		
Differential input voltage, V <sub>ID</sub> <sup>(3)</sup>			±26		±32	V		
Input voltage, V <sub>I</sub> (either input)	-0.3	26	-0.3	to 32	V			
Duration of output short circuit (one amp below) $T_A = 25$ °C, $V_{CC} \le 15$ V <sup>(4)</sup>	lifier) to ground at (or	Unlir	nited	Unli	mited			
Operating virtual junction temperature, T	J		150		150	°C		
Case temperature for 60 seconds	FK package				260	°C		
Lead temperature 1.6 mm (1/16 inch) from case for 60 seconds	J or W package		300		300	°C		
Storage temperature, T <sub>stg</sub>		-65	150	-65	150	°C		

<sup>(1)</sup> Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### 6.2 ESD Ratings

			VALUE	UNIT
LM224K	K, LM224KA, LM324K, LM324	KA, LM2902K, LM2902KV, LM2902KAV		
\ /		Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	
V <sub>(ESD)</sub>	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101	±1000	V
LM124,	LM124A, LM224, LM224A, LM	И324, LM324A, LM2902, LM2902V		
V	Clastrostatia diasharas	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±500	\/
V <sub>(ESD)</sub>	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101	±1000	٧

<sup>(1)</sup> JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

#### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		LM2	902	LMx24, LMx24 LM2902x, LM2902		UNIT
		MIN	MAX	MIN	MAX	
V <sub>CC</sub> Supply voltage		3	26	3	30	V
V <sub>CM</sub> Common-mode voltage		0	V <sub>CC</sub> – 2	0	V <sub>CC</sub> – 2	V
	LM124			-55	125	
T <sub>A</sub> Operating free air	LM2904	-40	125			00
temperature	LM324			0	70	°C
	LM224			-25	85	

<sup>(2)</sup> All voltage values (except differential voltages and V<sub>CC</sub> specified for the measurement of I<sub>OS</sub>) are with respect to the network GND.

<sup>(3)</sup> Differential voltages are at IN+, with respect to IN-.

<sup>(4)</sup> Short circuits from outputs to VCC can cause excessive heating and eventual destruction.



SLOS066W - SEPTEMBER 1975-REVISED MARCH 2015

## 6.4 Thermal Information

STRUMENTS

			L	.Mx24, LM2	902					
THERMAL METRIC <sup>(1)</sup>		D (SOIC)	DB (SSOP)	N (PDIP)	NS (SO)	PW (TSSOP)	FK (LCCC)	J (CDIP)	W (CFP)	UNIT
		14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	20 PINS	14 PINS	14 PINS	
R <sub>0JA</sub> (2)(3)	Junction-to- ambient thermal resistance	86	86	80	76	113	_	_	_	9000
R <sub>0JC</sub> (4)	Junction-to-case (top) thermal resistance	_	_	_	_	_	5.61	15.05	14.65	°C/W

- For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.
- Short circuits from outputs to VCC can cause excessive heating and eventual destruction.
- Maximum power dissipation is a function of  $T_{J(max)}$ ,  $R_{\theta JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_{J(max)} T_A)/R_{\theta JA}$ . Operating at the absolute maximum  $T_J$  of 150°C can affect reliability. Maximum power dissipation is a function of  $T_{J(max)}$ ,  $R_{\theta JA}$ , and  $T_C$ . The maximum allowable power dissipation at any allowable case temperature is  $P_D = (T_{J(max)} T_C)/R_{\theta JC}$ . Operating at the absolute maximum  $T_J$  of 150°C can affect reliability.

#### 6.5 Electrical Characteristics for LMx24 and LM324K

at specified free-air temperature,  $V_{CC} = 5 \text{ V}$  (unless otherwise noted)

	PARAMETER	TEST COME	NTIONS(1)	T (2)	LM1	24, LM224		LM3	24, LM324K		UNIT
	PARAMETER	TEST COND	IIION5\"	T <sub>A</sub> <sup>(2)</sup>	MIN	TYP <sup>(3)</sup>	MAX	MIN	TYP <sup>(3)</sup>	MAX	UNII
.,	lanut offect valte as	V <sub>CC</sub> = 5 V to MAX,	$V_{IC} = V_{ICR}min,$	25°C		3	5		3	7	\/
V <sub>IO</sub>	Input offset voltage	V <sub>O</sub> = 1.4 V		Full range			7			9	mV
	land offer toward	V <sub>O</sub> = 1.4 V		25°C		2	30		2	50	^
I <sub>IO</sub>	Input offset current	V <sub>O</sub> = 1.4 V		Full range			100			150	nA
	Input bing gurent	V 44V		25°C		-20	-150		-20	-250	- ^
l <sub>IB</sub>	Input bias current	V <sub>O</sub> = 1.4 V		Full range			-300			-500	nA
v	Common mode input valteer range	V 5 V to MAY		25°C	0 to V <sub>CC</sub> – 1.5			0 to V <sub>CC</sub> – 1.5			V
V <sub>ICR</sub>	Common-mode input voltage range	V <sub>CC</sub> = 5 V to MAX		Full range	0 to V <sub>CC</sub> - 2			0 to V <sub>CC</sub> - 2			V
		$R_L = 2 k\Omega$		25°C	V <sub>CC</sub> - 1.5			V <sub>CC</sub> - 1.5			
\/	High level autout valtage	R <sub>L</sub> = 10 kΩ		25°C							V
V <sub>OH</sub>	High-level output voltage	V MAN	$R_L = 2 k\Omega$	Full range	26			26			V
		V <sub>CC</sub> = MAX	R <sub>L</sub> ≥ 10 kΩ	Full range	27	28		27	28		
V <sub>OL</sub>	Low-level output voltage	R <sub>L</sub> ≤ 10 kΩ		Full range		5	20		5	20	mV
^	Large-signal differential voltage	V <sub>CC</sub> = 15 V, V <sub>O</sub> = 1	V to 11 V,	25°C	50	100		25	100		V/mV
$A_{VD}$	amplification	R <sub>L</sub> ≥ 2 kΩ		Full range	25			15			V/IIIV
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}min$		25°C	70	80		65	80		dB
k <sub>svr</sub>	Supply-voltage rejection ratio $(\Delta V_{CC}/\Delta VIO)$			25°C	65	100		65	100		dB
V <sub>O1</sub> / V <sub>O2</sub>	Crosstalk attenuation	f = 1 kHz to 20 kHz		25°C		120			120		dB
		V <sub>CC</sub> = 15 V,		25°C	-20	-30	-60	-20	-30	-60	
		$V_{ID} = 1 V,$ $V_{O} = 0$	Source	Full range	-10			-10			mA
lo	Output current	V <sub>CC</sub> = 15 V,		25°C	10	20		10	20		ША
		$V_{ID} = -1 \text{ V},$ $V_{O} = 15 \text{ V}$	Sink	Full range	5			5			
		$V_{ID} = -1 \ V, \ V_{O} = 20$	00 mV	25°C	12	30		12	30		μΑ
los	Short-circuit output current	$V_{CC}$ at 5 V, $V_{O}$ = 0, GND at -5 V		25°C		±40	±60		±40	±60	mA
		V <sub>O</sub> = 2.5 V, no load		Full range		0.7	1.2		0.7	1.2	
I <sub>CC</sub>	Supply current (four amplifiers)	V <sub>CC</sub> = MAX, V <sub>O</sub> = 0 no load	.5 V <sub>CC</sub> ,	Full range		1.4	3		1.4	3	mA

All characteristics are measured under open-loop conditions, with zero common-mode input voltage, unless otherwise specified. MAX V<sub>CC</sub> for testing purposes is 26 V for LM2902 and 30 V for the others.

Full range is -55°C to 125°C for LM124, -25°C to 85°C for LM224, and 0°C to 70°C for LM324.

All typical values are at  $T_A = 25$ °C



#### 6.6 Electrical Characteristics for LM2902 and LM2902V

at specified free-air temperature,  $V_{CC} = 5 \text{ V}$  (unless otherwise noted)

	DADAMETED	TEAT ACTION	TION(1)	<b>T</b> (2)	L	M2902		LI	/I2902V		LINIT
	PARAMETER	TEST CONDI	TIONS	T <sub>A</sub> <sup>(2)</sup>	MIN	TYP <sup>(3)</sup>	MAX	MIN	TYP <sup>(3)</sup>	MAX	UNIT
			Non-A-suffix	25°C		3	7		3	7	
	land offertually as	$V_{CC} = 5 \text{ V to MAX},$	devices	Full range			10			10	\/
V <sub>IO</sub>	Input offset voltage	$V_{IC} = V_{ICR} min,$ $V_{O} = 1.4 \text{ V}$	A-suffix	25°C					1	2	mV
		devices		Full range						4	
$\Delta V_{IO}/\Delta T$	Input offset voltage temperature drift	$R_S = 0 \Omega$		Ful range					7		μV/°C
I <sub>IO</sub>	Input offset current	V <sub>O</sub> = 1.4 V		25°C		2	50		2	50	nA
10	input onset current	VO = 1.4 V		Full range			300			150	ПА
$\Delta I_{IO}/\Delta T$	Input offset voltage temperature drift			Ful range					10		pA/°C
I <sub>IB</sub>	Input bias current	V <sub>O</sub> = 1.4 V		25°C		-20	-250		-20	-250	nA
ΊΒ	input bias current	VO = 1.4 V		Full range			-500			-500	ША
V	Common-mode input voltage range	V <sub>CC</sub> = 5 V to MAX		25°C	0 to V <sub>CC</sub> – 1.5			0 to V <sub>CC</sub> – 1.5			٧
V <sub>ICR</sub>	Common-mode input voltage range	V <sub>CC</sub> = 5 V to IVIAX		Full range	0 to V <sub>CC</sub> – 2			0 to V <sub>CC</sub> – 2			V
		$R_L = 2 k\Omega$		25°C							
V	High lavel cutout valtage	R <sub>L</sub> = 10 kΩ		25°C	V <sub>CC</sub> - 1.5			V <sub>CC</sub> - 1.5			V
$V_{OH}$	High-level output voltage	V <sub>CC</sub> = MAX	$R_L = 2 k\Omega$	Full range	22			26			V
		V <sub>CC</sub> = IVIAX	$R_L \ge 10 \text{ k}\Omega$	Full range	23	24		27			
$V_{OL}$	Low-level output voltage	$R_L \le 10 \text{ k}\Omega$		Full range		5	20		5	20	mV
	Large-signal differential voltage	V <sub>CC</sub> = 15 V,		25°C	25	100		25	100		
A <sub>VD</sub>	amplification	$V_O = 1 \text{ V to } 11 \text{ V},$ $R_L \ge 2 \text{ k}\Omega$		Full range	15			15			V/mV
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}min$		25°C	50	80		60	80		dB
$k_{\text{SVR}}$	Supply-voltage rejection ratio $(\Delta V_{CC} / \Delta VIO)$			25°C	50	100		60	100		dB
V <sub>O1</sub> / V <sub>O2</sub>	Crosstalk attenuation	f = 1 kHz to 20 kHz		25°C		120			120		dB
		V <sub>CC</sub> = 15 V,		25°C	-20	-30	-60	-20	-30	-60	
		$V_{ID} = 1 V,$ $V_{O} = 0$	Source	Full range	-10			-10			mA
Io	Output current	V <sub>CC</sub> = 15 V,		25°C	10	20		10	20		ША
		V <sub>ID</sub> = -1 V, V <sub>O</sub> = 15 V		Full range	5			5			
		$V_{ID} = -1 \text{ V}, V_{O} = 200 \text{ mV}$		25°C		30		12	40		μΑ
I <sub>OS</sub>	Short-circuit output current	$V_{CC}$ at 5 V, $V_{O}$ = 0,	GND at -5 V	25°C		±40	±60		±40	±60	mA
		V <sub>O</sub> = 2.5 V, no load		Full range		0.7	1.2		0.7	1.2	
I <sub>cc</sub>	Supply current (four amplifiers)	$V_{CC} = MAX, V_{O} = 0$ no load	.5 V <sub>CC</sub> ,	Full range		1.4	3		1.4	3	mA

All characteristics are measured under open-loop conditions, with zero common-mode input voltage, unless otherwise specified. MAX V<sub>CC</sub> for testing purposes is 26 V for LM2902 and 32 V for LM2902V.

## 6.7 Electrical Characteristics for LMx24A and LM324KA

at specified free-air temperature, V<sub>CC</sub> = 5 V (unless otherwise noted)

	PARAMETER	TEST CONDITIONS(1)	T <sub>A</sub> <sup>(2)</sup>	L	M124A			LM224A		LM324A	LM324F	(A	UNIT
	PARAMETER TEST CONDITIONS		IA''	MIN	TYP(3)	MAX	MIN	TYP(3)	MAX	MIN	TYP(3)	MAX	UNII
	Input offset	V <sub>CC</sub> = 5 V to 30 V,	25°C			2		2	3		2	3	
V <sub>IO</sub>	voltage	$V_{IC} = V_{ICR}min,$ $V_{O} = 1.4 \text{ V}$	Full range			4			4			5	mV
	Input offset	V <sub>O</sub> = 1.4 V	25°C			10		2	15		2	30	nA
IO	current	V <sub>O</sub> = 1.4 V	Full range			30			30			75	IIA
	Input bias	V <sub>O</sub> = 1.4 V	25°C			-50		-15	-80		-15	-100	
IB	I <sub>IB</sub> current	V <sub>O</sub> = 1.4 V	Full range			-100			-100			-200	nA

<sup>(1)</sup> All characteristics are measured under open-loop conditions, with zero common-mode input voltage, unless otherwise specified.

<sup>(2)</sup> Full range is -40°C to 125°C for LM2902.

<sup>(3)</sup> All typical values are at  $T_A = 25$ °C.

<sup>(2)</sup> Full range is -55°C to 125°C for LM124A, -25°C to 85°C for LM224A, and 0°C to 70°C for LM324A.

<sup>(3)</sup> All typical values are at  $T_A = 25$ °C.



## Electrical Characteristics for LMx24A and LM324KA (continued)

at specified free-air temperature,  $V_{CC} = 5 \text{ V}$  (unless otherwise noted)

PARAMETER TEST CONDITION		DITIONO(1)	<b>-</b> (2)	ı	_M124A			LM224A		LM324A, LM324KA			LINUT	
PA	ARAMETER	TEST CON	DITIONS	T <sub>A</sub> <sup>(2)</sup>	MIN	TYP <sup>(3)</sup>	MAX	MIN	TYP <sup>(3)</sup>	MAX	MIN	TYP <sup>(3)</sup>	MAX	UNIT
V	Common-mode			25°C	0 to V <sub>CC</sub> - 1.5			0 to V <sub>CC</sub> – 1.5			0 to V <sub>CC</sub> – 1.5			V
$V_{ICR}$	input voltage range	V <sub>CC</sub> = 30 V		Full range	0 to V <sub>CC</sub> - 2			0 to V <sub>CC</sub> – 2			0 to V <sub>CC</sub> – 2			V
		$R_L = 2 k\Omega$		25°C	V <sub>CC</sub> - 1.5			V <sub>CC</sub> - 1.5			V <sub>CC</sub> - 1.5			
$V_{OH}$	High-level output voltage	V 20 V	$R_L = 2 k\Omega$	Full range	26			26			26			V
	output romago	V <sub>CC</sub> = 30 V	R <sub>L</sub> ≥ 10 kΩ	Full range	27			27	28		27	28		
V <sub>OL</sub>	Low-level output voltage	R <sub>L</sub> ≤ 10 kΩ		Full range			20		5	20		5	20	mV
	Large-signal	V <sub>CC</sub> = 15 V,		25°C	50	100		50	100		25	100		
$A_{VD}$	differential voltage amplification	$V_0 = 1 \text{ V to } 1$ $R_L \ge 2 \text{ k}\Omega$	1 V,	Full range	25			25			15			V/mV
CMRR	Common-mode rejection ratio	V <sub>IC</sub> = V <sub>ICR</sub> min		25°C	70			70	80		65	80		dB
k <sub>SVR</sub>	Supply-voltage rejection ratio $(\Delta V_{CC}/\Delta V_{IO})$			25°C	65			65	100		65	100		dB
$V_{O1}/V_{O2}$	Crosstalk attenuation	f = 1 kHz to 2	0 kHz	25°C		120			120			120		dB
		V <sub>CC</sub> = 15 V,		25°C	-20			-20	-30	-60	-20	-30	-60	
		$V_{ID} = 1 V,$ $V_{O} = 0$	Source	Full range	-10			-10			-10			mA
Io	Output current	V <sub>CC</sub> = 15 V,		25°C	10			10	20		1	20		IIIA
		$V_{ID} = -1 \text{ V},$ $V_{O} = 15 \text{ V}$	Sink	Full range	5			5			5			
		V <sub>ID</sub> = −1 V, V <sub>0</sub>	o = 200 mV	25°C	12			12	30		12	30		μA
I <sub>os</sub>	Short-circuit output current	V <sub>CC</sub> at 5 V, G V <sub>O</sub> = 0	ND at -5 V,	25°C		±40	±60		±40	±60		±40	±60	mA
	0	V <sub>O</sub> = 2.5 V, no	o load	Full range		0.7	1.2		0.7	1.2		0.7	1.2	
I <sub>CC</sub>	Supply current (four amplifiers)	V <sub>CC</sub> = 30 V, V no load	<sub>O</sub> = 15 V,	Full range		1.4	3.		1.4	3		1.4	3	mA

## 6.8 Operating Conditions

 $V_{CC} = \pm 15 \text{ V}, T_A = 25^{\circ}\text{C}$ 

	- 7			
	PARAMETER	TEST CONDITIONS	TYP	UNIT
SR	Slew rate at unity gain	$R_L = 1 \text{ M}\Omega$ , $C_L = 30 \text{ pF}$ , $V_I = \pm 10 \text{ V}$ (see Figure 7)	0.5	V/µs
B <sub>1</sub>	Unity-gain bandwidth	$R_L = 1 \text{ M}\Omega$ , $C_L = 20 \text{ pF}$ (see Figure 7)	1.2	MHz
V <sub>n</sub>	Equivalent input noise voltage	$R_S = 100 \Omega$ , $V_I = 0 V$ , $f = 1 kHz$ (see Figure 8)	35	nV/√Hz



#### 6.9 Typical Characteristics





## 7 Parameter Measurement Information



Figure 7. Unity-Gain Amplifier

Figure 8. Noise-Test Circuit



#### 8 Detailed Description

#### 8.1 Overview

These devices consist of four independent high-gain frequency-compensated operational amplifiers that are designed specifically to operate from a single supply over a wide range of voltages. Operation from split supplies also is possible if the difference between the two supplies is 3 V to 32 V (3 V to 26 V for the LM2902 device), and  $V_{CC}$  is at least 1.5 V more positive than the input common-mode voltage. The low supply-current drain is independent of the magnitude of the supply voltage.

Applications include transducer amplifiers, DC amplification blocks, and all the conventional operational-amplifier circuits that now can be more easily implemented in single-supply-voltage systems. For example, the LM124 device can be operated directly from the standard 5-V supply that is used in digital systems and provides the required interface electronics, without requiring additional ±15-V supplies.

#### 8.2 Functional Block Diagram



<sup>&</sup>lt;sup>†</sup> ESD protection cells - available on LM324K and LM324KA only



SLOS066W - SEPTEMBER 1975-REVISED MARCH 2015

#### 8.3 Feature Description

INSTRUMENTS

#### 8.3.1 Unity-Gain Bandwidth

Gain bandwidth product is found by multiplying the measured bandwidth of an amplifier by the gain at which that bandwidth was measured. These devices have a high gain bandwidth of 1.2 MHz.

#### 8.3.2 Slew Rate

The slew rate is the rate at which an operational amplifier can change its output when there is a change on the input. These devices have a 0.5-V/µs slew rate.

#### 8.3.3 Input Common Mode Range

The valid common mode range is from device ground to  $V_{CC}-1.5\ V$  ( $V_{CC}-2\ V$  across temperature). Inputs may exceed  $V_{CC}$  up to the maximum  $V_{CC}$  without device damage. At least one input must be in the valid input common mode range for output to be correct phase. If both inputs exceed valid range then output phase is undefined. If either input is less than -0.3 V then input current should be limited to 1 mA and output phase is undefined.

#### 8.4 Device Functional Modes

These devices are powered on when the supply is connected. This device can be operated as a single supply operational amplifier or dual supply amplifier depending on the application.



## Application and Implementation

#### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

#### 9.1 Application Information

The LMx24 and LM2902 operational amplifiers are useful in a wide range of signal conditioning applications. Inputs can be powered before VCC for flexibility in multiple supply circuits.

## 9.2 Typical Application

A typical application for an operational amplifier in an inverting amplifier. This amplifier takes a positive voltage on the input, and makes it a negative voltage of the same magnitude. In the same manner, it also makes negative voltages positive.



Figure 9. Application Schematic

#### 9.2.1 Design Requirements

The supply voltage must be chosen such that it is larger than the input voltage range and output range. For instance, this application will scale a signal of ±0.5 V to ±1.8 V. Setting the supply at ±12 V is sufficient to accommodate this application.

#### 9.2.2 Detailed Design Procedure

Determine the gain required by the inverting amplifier using Equation 1 and Equation 2:

$$A_{v} = \frac{VOUT}{VIN}$$

$$A_{v} = \frac{1.8}{-0.5} = -3.6$$
(1)

Once the desired gain is determined, choose a value for RI or RF. Choosing a value in the kilohm range is desirable because the amplifier circuit will use currents in the milliamp range. This ensures the part will not draw too much current. This example will choose 10 k $\Omega$  for RI which means 36 k $\Omega$  will be used for RF. This was determined by Equation 3.

$$A_{v} = -\frac{RF}{RI} \tag{3}$$

(2)



## **Typical Application (continued)**

#### 9.2.3 Application Curve



Figure 10. Input and Output Voltages of the Inverting Amplifier

## 10 Power Supply Recommendations

#### **CAUTION**

Supply voltages larger than 32 V for a single supply, or outside the range of ±16 V for a dual supply can permanently damage the device (see the *Absolute Maximum Ratings*).

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, refer to the *Layout*.

## 11 Layout

#### 11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the
  operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance
  power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-μF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If
  it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as
  opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting
  input minimizes parasitic capacitance, as shown in Layout Examples.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.



## 11.2 Layout Examples



Figure 11. Operational Amplifier Board Layout for Noninverting Configuration



Figure 12. Operational Amplifier Schematic for Noninverting Configuration



## 12 Device and Documentation Support

## 12.1 Documentation Support

#### 12.1.1 Related Documentation

For related documentation, see the following:

Circuit Board Layout Techniques, SLOA089

#### 12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LM124	Click here	Click here	Click here	Click here	Click here
LM124A	Click here	Click here	Click here	Click here	Click here
LM224	Click here	Click here	Click here	Click here	Click here
LM224A	Click here	Click here	Click here	Click here	Click here
LM324	Click here	Click here	Click here	Click here	Click here
LM324A	Click here	Click here	Click here	Click here	Click here
LM2902	Click here	Click here	Click here	Click here	Click here
LM2902V	Click here	Click here	Click here	Click here	Click here
LM224K	Click here	Click here	Click here	Click here	Click here
LM224KA	Click here	Click here	Click here	Click here	Click here
LM324K	Click here	Click here	Click here	Click here	Click here
LM324KA	Click here	Click here	Click here	Click here	Click here
LM2902K	Click here	Click here	Click here	Click here	Click here
LM2902KV	Click here	Click here	Click here	Click here	Click here
LM2902KAV	Click here	Click here	Click here	Click here	Click here

#### 12.3 Trademarks

All trademarks are the property of their respective owners.

## 12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

#### 12.5 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.





6-Feb-2020

## **PACKAGING INFORMATION**

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish (6)	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Sample
5962-7704301VCA	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-7704301VC A LM124JQMLV	Sample
5962-9950403V9B	ACTIVE	XCEPT	KGD	0	100	TBD	Call TI	N / A for Pkg Type	-55 to 125		Sample
5962-9950403VCA	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-9950403VC A LM124AJQMLV	Sample
77043012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	77043012A LM124FKB	Sample
7704301CA	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	7704301CA LM124JB	Sample
7704301DA	ACTIVE	CFP	W	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	7704301DA LM124WB	Sample
77043022A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	77043022A LM124AFKB	Sample
7704302CA	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	7704302CA LM124AJB	Sample
7704302DA	ACTIVE	CFP	W	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	7704302DA LM124AWB	Sample
JM38510/11005BCA	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	JM38510 /11005BCA	Sample
LM124AFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	77043022A LM124AFKB	Sample
LM124AJ	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	LM124AJ	Sample
LM124AJB	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	7704302CA LM124AJB	Sample
LM124AWB	ACTIVE	CFP	W	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	7704302DA LM124AWB	Sample
LM124D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LM124	Sample
LM124DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LM124	Sample





Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish (6)	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
LM124DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LM124	Samples
LM124DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LM124	Samples
LM124FKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	77043012A LM124FKB	Samples
LM124J	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	LM124J	Samples
LM124JB	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	7704301CA LM124JB	Samples
LM124W	ACTIVE	CFP	W	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	LM124W	Samples
LM124WB	ACTIVE	CFP	W	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	7704301DA LM124WB	Samples
LM224AD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM224A	Samples
LM224ADR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU   SN	Level-1-260C-UNLIM	-25 to 85	LM224A	Samples
LM224ADRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM224A	Samples
LM224ADRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM224A	Samples
LM224AN	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-25 to 85	LM224AN	Samples
LM224D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM224	Samples
LM224DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM224	Samples
LM224DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU   SN	Level-1-260C-UNLIM	-25 to 85	LM224	Samples
LM224DRG3	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-25 to 85	LM224	Samples
LM224DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM224	Samples
LM224KAD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM224KA	Samples



Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
LM224KADG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM224KA	Sample
LM224KADR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM224KA	Sample
LM224KADRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM224KA	Sample
LM224KAN	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-25 to 85	LM224KAN	Sample
LM224KDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM224K	Sample
LM224KDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM224K	Sample
LM224KN	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-25 to 85	LM224KN	Sample
LM224N	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-25 to 85	LM224N	Sample
LM224NE4	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-25 to 85	LM224N	Sample
LM2902D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2902	Sample
LM2902DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	LM2902	Sample
LM2902DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2902	Sample
LM2902DRG3	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	LM2902	Sample
LM2902DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2902	Sample
LM2902KAVQDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2902KA	Sample
LM2902KAVQDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2902KA	Sample
LM2902KAVQPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2902KA	Sample
LM2902KAVQPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2902KA	Sample



Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
LM2902KD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2902K	Samples
LM2902KDB	ACTIVE	SSOP	DB	14	80	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2902K	Samples
LM2902KDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2902K	Samples
LM2902KDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2902K	Samples
LM2902KN	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-40 to 125	LM2902KN	Samples
LM2902KNSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2902K	Samples
LM2902KNSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2902K	Samples
LM2902KPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2902K	Samples
LM2902KPWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2902K	Samples
LM2902KPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2902K	Samples
LM2902KVQDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2902KV	Samples
LM2902KVQDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2902KV	Samples
LM2902KVQPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2902KV	Samples
_M2902KVQPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2902KV	Samples
LM2902N	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	NIPDAU   SN	N / A for Pkg Type	-40 to 125	LM2902N	Samples
LM2902NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	NIPDAU	N / A for Pkg Type	-40 to 125	LM2902N	Samples
LM2902NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2902	Samples
LM2902PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2902	Samples



Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
LM2902PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	L2902	Samples
LM2902PWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2902	Samples
LM2902PWRG3	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	L2902	Samples
LM2902PWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2902	Samples
LM324AD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM324A	Samples
LM324ADBR	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM324A	Samples
LM324ADE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM324A	Samples
LM324ADR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU   SN	Level-1-260C-UNLIM	0 to 70	LM324A	Samples
LM324ADRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM324A	Samples
LM324ADRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM324A	Samples
LM324AN	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	LM324AN	Samples
LM324ANSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM324A	Samples
LM324ANSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM324A	Samples
LM324APW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	L324A	Samples
LM324APWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	L324A	Samples
LM324APWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	NIPDAU   SN	Level-1-260C-UNLIM	0 to 70	L324A	Samples
LM324APWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	L324A	Samples
LM324D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM324	Samples





Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
LM324DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM324	Samples
LM324DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM324	Samples
LM324DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU   SN	Level-1-260C-UNLIM	0 to 70	LM324	Samples
LM324DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM324	Samples
LM324DRG3	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	0 to 70	LM324	Samples
LM324DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM324	Samples
LM324KAD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM324KA	Samples
LM324KADR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM324KA	Samples
LM324KADRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM324KA	Samples
LM324KAN	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	LM324KAN	Samples
LM324KANSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM324KA	Samples
LM324KAPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	L324KA	Samples
LM324KAPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	L324KA	Samples
LM324KAPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	L324KA	Samples
LM324KDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM324K	Samples
LM324KN	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	LM324KN	Samples
LM324KNSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM324K	Samples
LM324KPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	L324K	Samples



6-Feb-2020



www.ti.com

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish (6)	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
LM324KPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	L324K	Samples
LM324N	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	NIPDAU   SN	N / A for Pkg Type	0 to 70	LM324N	Samples
LM324NE3	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	SN	N / A for Pkg Type	0 to 70	LM324N	Samples
LM324NE4	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	LM324N	Samples
LM324NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM324	Sample
LM324NSRE4	ACTIVE	so	NS	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM324	Sample
LM324NSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM324	Sample
LM324PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	L324	Sample
LM324PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	NIPDAU   SN	Level-1-260C-UNLIM	0 to 70	L324	Sample
LM324PWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	L324	Sample
LM324PWRG3	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	0 to 70	L324	Sample
LM324PWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	L324	Sample
M38510/11005BCA	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	JM38510 /11005BCA	Sample

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

## PACKAGE OPTION ADDENDUM



6-Feb-2020

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (CI) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- (3) MSL, Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

#### OTHER QUALIFIED VERSIONS OF LM124, LM124-SP, LM124M, LM2902:

Catalog: LM124, LM124

Automotive: LM2902-Q1

■ Enhanced Product: LM2902-EP

Military: LM124M, LM124M

Space: LM124-SP, LM124-SP

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Automotive Q100 devices qualified for high-reliability automotive applications targeting zero defects



## **PACKAGE OPTION ADDENDUM**

- Enhanced Product Supports Defense, Aerospace and Medical Applications
- Military QML certified for Military and Defense Applications
- Space Radiation tolerant, ceramic packaging and qualified for use in Space-based application

**PACKAGE MATERIALS INFORMATION** 

www.ti.com 28-Dec-2019

## TAPE AND REEL INFORMATION





	Α0	Dimension designed to accommodate the component width
	B0	Dimension designed to accommodate the component length
	K0	Dimension designed to accommodate the component thickness
	W	Overall width of the carrier tape
г	D1	Pitch between successive cavity centers

## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM124DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM224ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM224ADR	SOIC	D	14	2500	330.0	16.8	6.5	9.5	2.1	8.0	16.0	Q1
LM224ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM224ADRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM224ADRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM224DR	SOIC	D	14	2500	330.0	16.8	6.5	9.5	2.1	8.0	16.0	Q1
LM224DR	SOIC	D	14	2500	330.0	17.0	6.4	9.05	2.1	8.0	16.0	Q1
LM224DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM224DRG3	SOIC	D	14	2500	330.0	16.8	6.5	9.5	2.1	8.0	16.0	Q1
LM224DRG3	SOIC	D	14	2500	330.0	17.0	6.4	9.05	2.1	8.0	16.0	Q1
LM224DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM224KADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM224KDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM2902DR	SOIC	D	14	2500	330.0	16.8	6.5	9.5	2.1	8.0	16.0	Q1
LM2902DR	SOIC	D	14	2500	330.0	17.0	6.4	9.05	2.1	8.0	16.0	Q1
LM2902DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM2902DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1



# **PACKAGE MATERIALS INFORMATION**

www.ti.com 28-Dec-2019

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2902DRG3	SOIC	D	14	2500	330.0	16.8	6.5	9.5	2.1	8.0	16.0	Q1
LM2902DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM2902DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM2902KAVQPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2902KAVQPWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2902KDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM2902KNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
LM2902KPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2902KVQPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2902KVQPWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2902NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
LM2902PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2902PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2902PWRG3	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2902PWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM324ADR	SOIC	D	14	2500	330.0	16.8	6.5	9.5	2.1	8.0	16.0	Q1
LM324ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM324ADRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM324ANSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
LM324APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM324APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM324APWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM324DR	SOIC	D	14	2500	330.0	16.8	6.5	9.5	2.1	8.0	16.0	Q1
LM324DR	SOIC	D	14	2500	330.0	17.0	6.4	9.05	2.1	8.0	16.0	Q1
LM324DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM324DRG3	SOIC	D	14	2500	330.0	17.0	6.4	9.05	2.1	8.0	16.0	Q1
LM324DRG3	SOIC	D	14	2500	330.0	16.8	6.5	9.5	2.1	8.0	16.0	Q1
LM324DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM324DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM324KADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM324KANSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
LM324KAPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM324KDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM324KNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
LM324KPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM324PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM324PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM324PWRG3	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM324PWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

www.ti.com 28-Dec-2019



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM124DR	SOIC	D	14	2500	350.0	350.0	43.0
LM224ADR	SOIC	D	14	2500	333.2	345.9	28.6
LM224ADR	SOIC	D	14	2500	364.0	364.0	27.0
LM224ADR	SOIC	D	14	2500	367.0	367.0	38.0
LM224ADRG4	SOIC	D	14	2500	367.0	367.0	38.0
LM224ADRG4	SOIC	D	14	2500	333.2	345.9	28.6
LM224DR	SOIC	D	14	2500	364.0	364.0	27.0
LM224DR	SOIC	D	14	2500	333.2	345.9	28.6
LM224DR	SOIC	D	14	2500	367.0	367.0	38.0
LM224DRG3	SOIC	D	14	2500	364.0	364.0	27.0
LM224DRG3	SOIC	D	14	2500	333.2	345.9	28.6
LM224DRG4	SOIC	D	14	2500	367.0	367.0	38.0
LM224KADR	SOIC	D	14	2500	367.0	367.0	38.0
LM224KDR	SOIC	D	14	2500	367.0	367.0	38.0
LM2902DR	SOIC	D	14	2500	364.0	364.0	27.0
LM2902DR	SOIC	D	14	2500	333.2	345.9	28.6
LM2902DR	SOIC	D	14	2500	367.0	367.0	38.0
LM2902DR	SOIC	D	14	2500	333.2	345.9	28.6
LM2902DRG3	SOIC	D	14	2500	364.0	364.0	27.0
LM2902DRG4	SOIC	D	14	2500	333.2	345.9	28.6



# **PACKAGE MATERIALS INFORMATION**

www.ti.com 28-Dec-2019

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2902DRG4	SOIC	D	14	2500	367.0	367.0	38.0
LM2902KAVQPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
LM2902KAVQPWRG4	TSSOP	PW	14	2000	367.0	367.0	35.0
LM2902KDR	SOIC	D	14	2500	367.0	367.0	38.0
LM2902KNSR	SO	NS	14	2000	367.0	367.0	38.0
LM2902KPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
LM2902KVQPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
LM2902KVQPWRG4	TSSOP	PW	14	2000	367.0	367.0	35.0
LM2902NSR	SO	NS	14	2000	367.0	367.0	38.0
LM2902PWR	TSSOP	PW	14	2000	367.0	367.0	35.0
LM2902PWR	TSSOP	PW	14	2000	364.0	364.0	27.0
LM2902PWRG3	TSSOP	PW	14	2000	364.0	364.0	27.0
LM2902PWRG4	TSSOP	PW	14	2000	367.0	367.0	35.0
LM324ADR	SOIC	D	14	2500	364.0	364.0	27.0
LM324ADR	SOIC	D	14	2500	367.0	367.0	38.0
LM324ADRG4	SOIC	D	14	2500	367.0	367.0	38.0
LM324ANSR	SO	NS	14	2000	367.0	367.0	38.0
LM324APWR	TSSOP	PW	14	2000	364.0	364.0	27.0
LM324APWR	TSSOP	PW	14	2000	367.0	367.0	35.0
LM324APWRG4	TSSOP	PW	14	2000	367.0	367.0	35.0
LM324DR	SOIC	D	14	2500	364.0	364.0	27.0
LM324DR	SOIC	D	14	2500	333.2	345.9	28.6
LM324DR	SOIC	D	14	2500	367.0	367.0	38.0
LM324DRG3	SOIC	D	14	2500	333.2	345.9	28.6
LM324DRG3	SOIC	D	14	2500	364.0	364.0	27.0
LM324DRG4	SOIC	D	14	2500	333.2	345.9	28.6
LM324DRG4	SOIC	D	14	2500	367.0	367.0	38.0
LM324KADR	SOIC	D	14	2500	367.0	367.0	38.0
LM324KANSR	SO	NS	14	2000	367.0	367.0	38.0
LM324KAPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
LM324KDR	SOIC	D	14	2500	367.0	367.0	38.0
LM324KNSR	SO	NS	14	2000	367.0	367.0	38.0
LM324KPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
LM324PWR	TSSOP	PW	14	2000	367.0	367.0	35.0
LM324PWR	TSSOP	PW	14	2000	364.0	364.0	27.0
LM324PWRG3	TSSOP	PW	14	2000	364.0	364.0	27.0
LM324PWRG4	TSSOP	PW	14	2000	367.0	367.0	35.0

# FK (S-CQCC-N\*\*)

## LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004



## **MECHANICAL DATA**

## NS (R-PDSO-G\*\*)

# 14-PINS SHOWN

## PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



# W (R-GDFP-F14)

## CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP1-F14



CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.

4040083-5/G





CERAMIC DUAL IN LINE PACKAGE



- 1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This package is hermitically sealed with a ceramic lid using glass frit.
- His package is remitted by sealed with a ceramic its using glass mit.
   Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
   Falls within MIL-STD-1835 and GDIP1-T14.



CERAMIC DUAL IN LINE PACKAGE



# D (R-PDSO-G14)

## PLASTIC SMALL OUTLINE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.



# D (R-PDSO-G14)

# PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G14)

## PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



# PW (R-PDSO-G14)

# PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



# N (R-PDIP-T\*\*)

## PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

#### **28 PINS SHOWN**



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-150

#### IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

Tl's products are provided subject to Tl's Terms of Sale (<a href="www.ti.com/legal/termsofsale.html">www.ti.com/legal/termsofsale.html</a>) or other applicable terms available either on ti.com or provided in conjunction with such Tl products. Tl's provision of these resources does not expand or otherwise alter Tl's applicable warranties or warranty disclaimers for Tl products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2020, Texas Instruments Incorporated