

Photon Chip Implementation

Johann Pascher

2025

Abstract

This document is part of the T0 Theory Collection.

Abstract

The implementation of photonic components on wafers (e.g., TFLN or Si photonics) enables scalable, low-latency systems for 6G networks. **The global strategy focuses in 2025 on the industrialization of thin-film lithium niobate (TFLN) through specialized foundries [?] and the development of scalable photonic quantum computers (LNOI/PhoQuant) [?].** This introduction is based on current literature (2024–2025) and highlights fabrication processes (ion slicing, wafer bonding), preferred techniques (MZI integration), and relevance for signal processing. Practical: Table of methods, outlook on hybrid PICs. Sources: Nature, ScienceDirect, arXiv. **A new optoelectronic chip that integrates terahertz and optical signals is key to millimeter-precise distance measurement and high-performance 6G mobile communications [?].**

1 Basics: Why Wafer Integration in Communication Engineering?

The fabrication of photonic components on wafers (e.g., thin-film lithium niobate, TFLN) revolutionizes communication engineering: Scalable production of integrated circuits (PICs) for RF signal processing, 6G MIMO, and AI-assisted routing. **The transition to high-volume manufacturing is accelerated by specialized TFLN foundries, such as the QCi Foundry, which will accept the first commercial pilot orders in 2025 [?]. Globally, 2025 (International Year of Quantum Science and Technology) highlights the strategic importance of photonics for competitiveness [?].** Wafer-based processes (e.g., ion slicing + bonding) enable monolithic integration of > 1000 components/wafer, with losses < 1 dB and bandwidths > 100 GHz. Important Note: The technology is hybrid-analog: Optical waveguides for continuous processing, combined with electronic control. This reduces latency (ps range) and energy (pJ/bit), essential for real-time 6G applications.

Current trends (2025): Transition to 300 mm wafers for industrial scaling, focused on flexible, cost-effective processes [?].

2 Realization: Key Processes for Component Integration

The implementation occurs in multi-stage processes, strongly aligned with semiconductor fabrication (e.g., CMOS-compatible). Core steps:

- **Ion Slicing and Wafer Bonding:** For thin films (e.g., LiTaO_3 on Si); enables high density without substrate losses [?].
- **Etching and Lithography:** Mask-CMP for waveguide microstructures; precise structures (< 100 nm) for MZI arrays [?].
- **Monolithic Integration:** Co-packaging of electronics/photonics; reduces latency in hybrid systems [?].
- **Flexible Wafer Scaling:** Mechanically flexible 300 mm platforms for cost-effective production [?].

Example: Wafer bonding for LNOI (Lithium Niobate on Insulator): Thickness $t = 525$ μm , implantation dose $D = 5 \times 10^{16} \text{ cm}^{-2}$, resulting layer thickness $h \approx 400$ nm.

3 Preferred Components and Operations on Wafers

Photonic wafers are suited for linear, frequency-dependent components; analog integration prioritizes interference-based operations for 6G signals. **In addition to TFLN, the silicon nitride (SiN) platform is being promoted to offer PICs for biosciences and sensing [?].**

Preferred: Linear operations (e.g., matrix-vector multiplication via MZI meshes) for AI-assisted routing; non-linear (e.g., logic gates) requires hybrids.

Component	Realization Process	Relevance for Communication Engineering
Mach-Zehnder Interferometer (MZI)	Ion slicing + lithography on TFLN wafers	Phase modulation for demodulation (6G, latency < 1 ps) [?]
Waveguide Arrays	Wafer bonding (LNOI) + etching	Parallel RF filtering (> 100 GHz bandwidth) [?]
Optoelectronic THz Processor	Si photonics/InP hybrid PICs	6G transceivers, millimeter-precise distance measurement [?]
Quantum Dot Integrator (InAs)	Monolithic Si integration	Hybrid signal amplification for optical networks [?]
Meta-Optics Structures	CMP mask etching on LiNbO ₃	Gradient filters for BSS in MIMO systems [?]
LNOI Qubit Structures	Semiconductor fabrication (PhoQuant)	Scalable, room-temperature stable quantum computers [?]
Flexible PICs	300 mm wafers with mechanical flexibility	Mobile 6G edge devices (roll-to-roll fab) [?]

Table 1: Preferred Components: Implementation on Wafers and Applications

4 Literature Review: Latest Documents (2024–2025)

Selected sources on wafer implementation (focused on photonic components; links to PDFs/abstracts):

- **TFLN Foundries and Industrialization:** The **QCi Foundry** (specialized in TFLN) will accept the first pilot orders for commercial production of photonic chips in 2025, marking the industrialization of the platform [?].
- **Mechanically-flexible wafer-scale integrated-photonics fabrication (2024):** First 300 mm platform for flexible PICs; process: bonding + etching. Relevance: Scalable RF chips for mobile networks. [?]
- **Lithium tantalate photonic integrated circuits for volume manufacturing (2024):** Ion slicing + bonding for LiTaO₃ wafers; density > 1000 components/wafer. Relevance: Low losses for 6G transceivers. [?]
- **LNOI for Quantum Computers (PhoQuant):** Fraunhofer IOF is developing a photonic quantum computer based on **LNOI**, where fabrication methods stem from semiconductor manufacturing and are immediately scalable. This demonstrates the deployability of the LNOI platform for highly complex quantum architectures [?].
- **Fabrication of heterogeneous LNOI photonics wafers (2023/2024 Update):** Room-temperature bonding for LNOI; precise waveguides. Relevance: Hybrid opto-electronics for signal processing. [?]
- **Fabrication of on-chip single-crystal lithium niobate waveguide (2025):** Mask-CMP etching for TFLN microstructures. Relevance: Real-time filters for broadband communication. [?]
- **The integration of microelectronic and photonic circuits on a single wafer (2024):** Monolithic co-integration; applications in optical networks. Relevance: Latency reduction in 6G. [?]

These documents show: Transition to high-volume manufacturing (12 000 wafers/year), with a focus on analog precision for communication engineering.

5 Outlook: Photonic Wafers in 6G Networks

Wafer integration enables cost-effective PICs for base stations: E.g., optical MIMO with < 1 dB loss. Challenges: Increase yield (currently < 80%). Future: AI-assisted fab (e.g., for dynamic routing chips). **The THz chip from EPFL/Harvard demonstrates the enormous potential of optoelectronic integration to process high-frequency radio signals with millimeter precision, opening new application fields in robotics and autonomous vehicles [?].**

References

- [1] J. Pascher, *T0 Theory Overview*, 2025.
- [2] A. Einstein, *On the Electrodynamics of Moving Bodies*, Ann. Phys., 1905.
- [3] M. Planck, *On the Law of Distribution of Energy*, 1900.
- [4] R. P. Feynman, *QED: The Strange Theory of Light and Matter*, 2006.
- [5] S. Weinberg, *The Quantum Theory of Fields*, 1995.
- [6] Particle Data Group, *Review of Particle Physics*, 2024.