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CORE-V 180 MCU Proposal

Sorbonne Université & Global Foundries

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April 24, 2023 @Internet

Overview

- Design a CORE-V MCU on Global Foundries 180nm.

- Using the FOSS RTL-to-GDSII Coriolis toolchain.

- The GF 180nm process node is now NDA free.

- The final GDSII layout can be openly published.

- The whole building procedure can be published and reproduced by third parties.

Expected Outcomes

- A free RTL-to-GDSII toolchain, calibrated and proven for use with GF 180nm node.

- A CORE-V MCU chip usable for small applications.

- A CORE-V MCU design tutorial for academics and teaching, along with at least a basic test PCB board.

- A free, CORE-V MCU readily customizable platform for all industrial partners.

Contributions

✐ GF will provide the shuttle to fabricate the design.

✐ SU/LIP6 may punctually contact GF to clarify points on the design kit.

✐ SU/LIP6 will provides the RTL-to-GDSII toolchain, configure it, and build the design tutorial.

✐ In addition SU/LIP6 will provides simple analog blocs, like a PLL.

✐ Various Standard cells library, SRAM and I/O cells will be tested.

✐ The OpenHW Group will provide a scaled down version of the CORE-V MCU.

Tradeoffs

- The CORE-V MCU must be scaled down for two reasons:
  1. A 22nm design cannot fit into the envisionned 180nm area.

  2. The eFPGA will not be available.

- GF will define the alloted area for the design.

- Given the area, a scaled down version must be selected, in accordance to kind of application it is choosen to run.

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The SU/LIP6 Experience
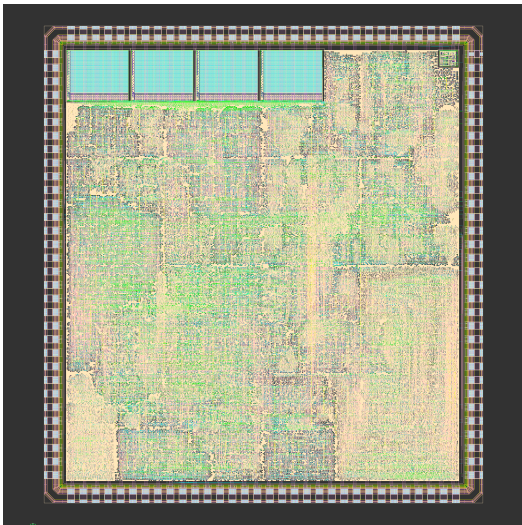
- The LibreSOC chip.
- https://libre-soc.org/.
- TSMC 180nm.
- 1.3 Mt,
  standard cells: 500 Kt,
  SRAM: 800 Kt.
- 120K gates (SRAM excluded).
- 5.1×5.5 mm (28mm^2).

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PROVEN PROCESSOR IP

ASIC Design Flow
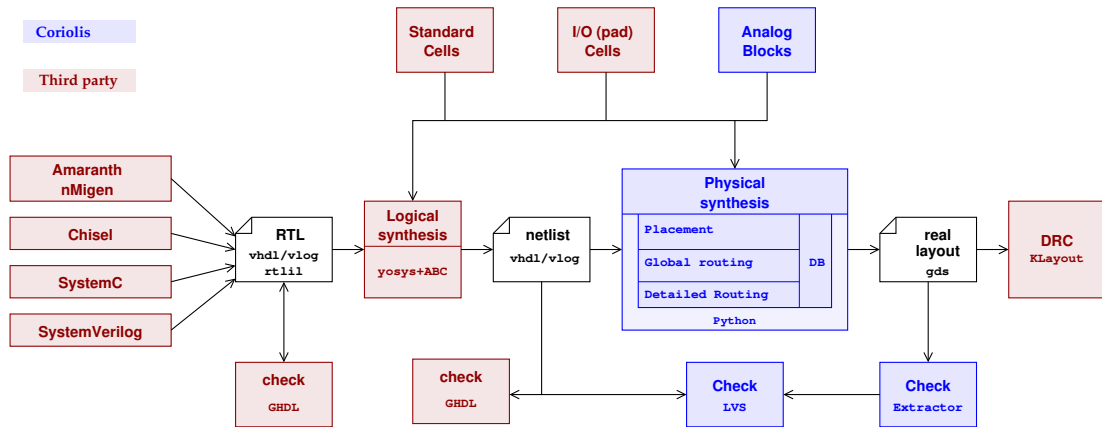
Standard Cells Libraries

✏ As an experiment, we will check three standard cells libraries:

1. The GF library, supplied with the design kit.

2. The portable cells, supplied by Chips4Makers (`https://chips4makers.io`).

3. The SU/LIP6 portable cells (symbolic).

✏ The version to be send to the foundry will be choosen according to overall area and timing results.