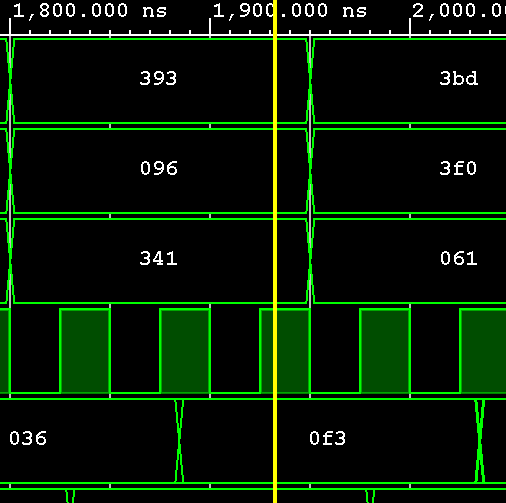
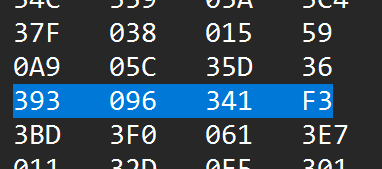
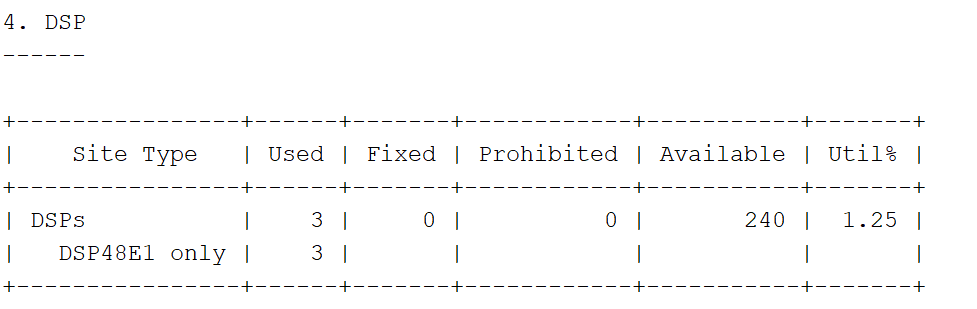
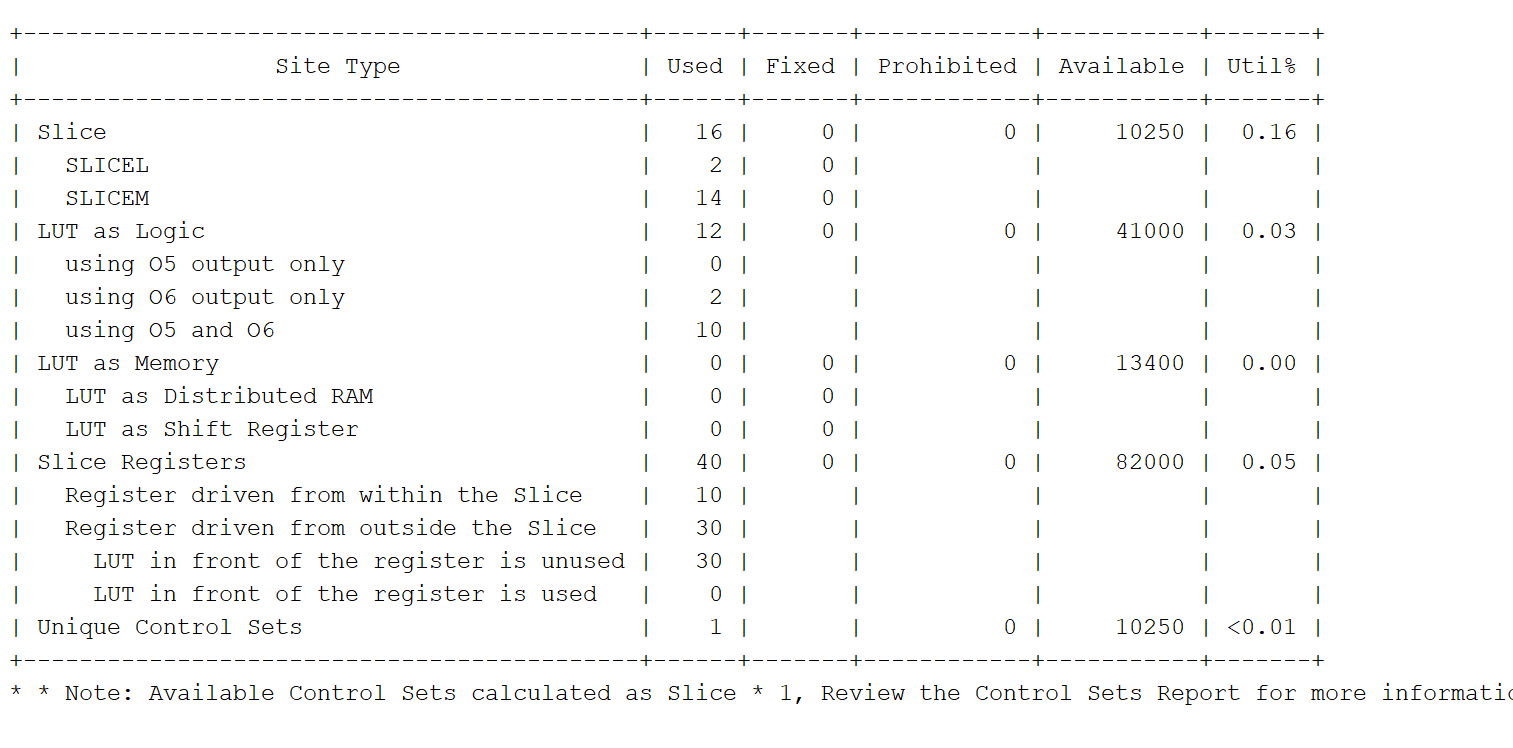
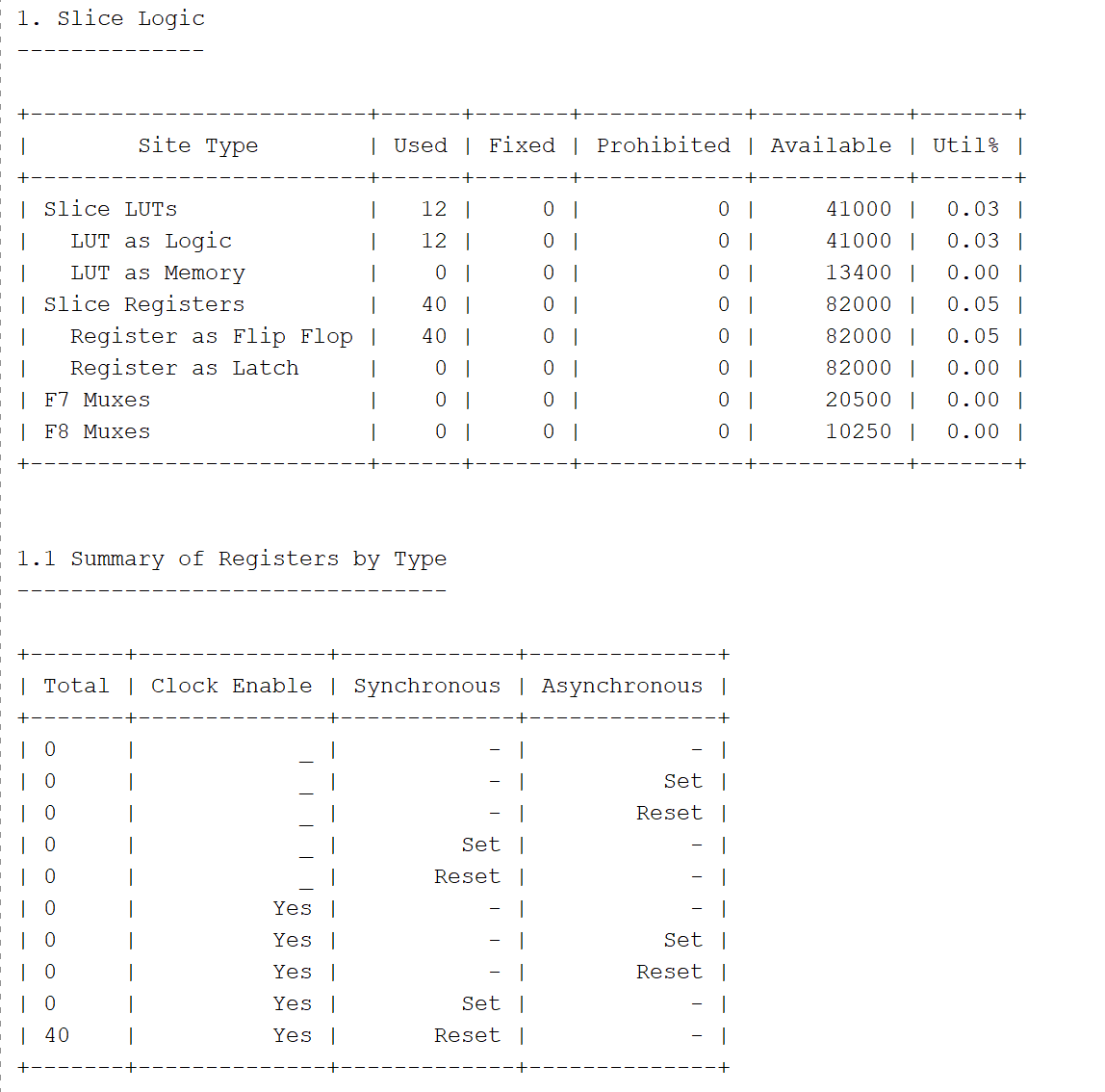
# Name: \_Joseph Coker

# Netid: \_\_ JPC496

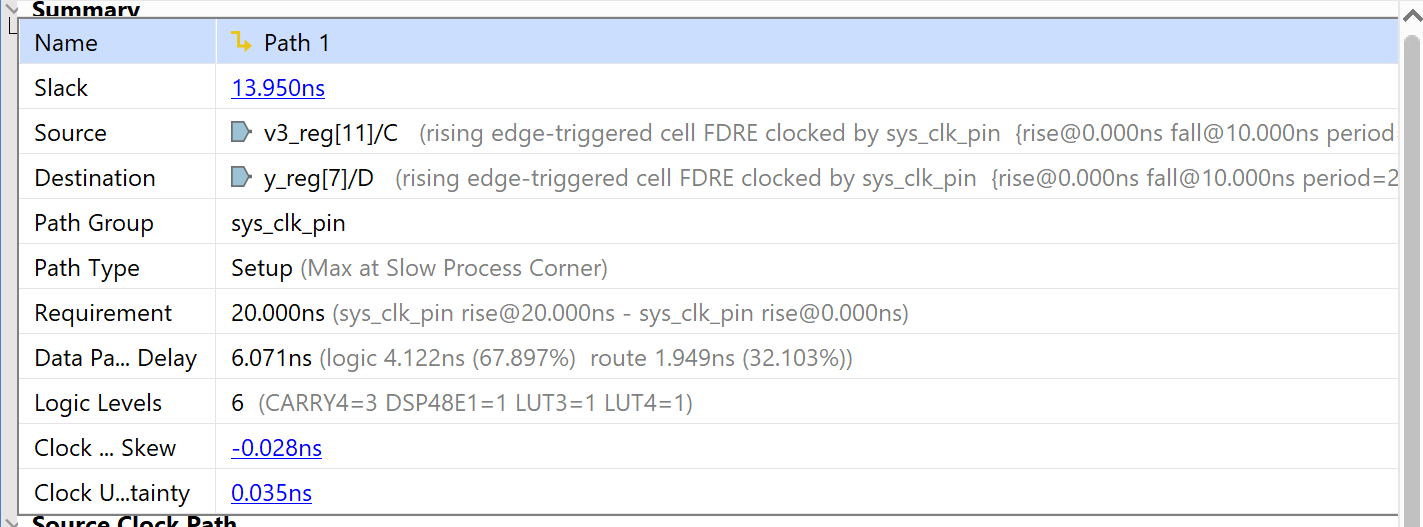
1. Correct Design part 1 (25 pts with simulation screenshot, table data)
   1. Simulation Screenshot (includes screenshot of line from vector file that is being used in the screenshot). Simulation screenshot annotated to show latency. (13 pts)



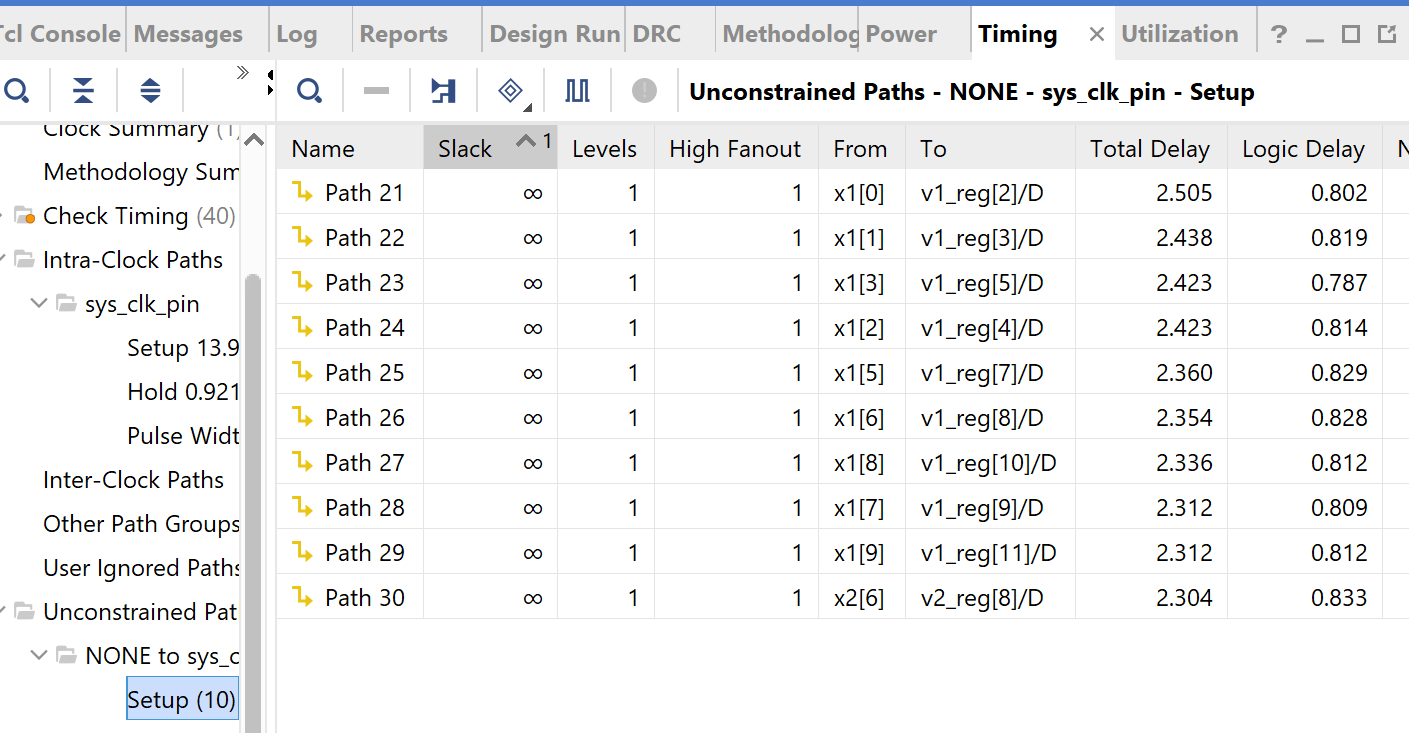
* 1. Resource Tables—Slice Logic, Summary of Registers, DSP Table (3 pts)



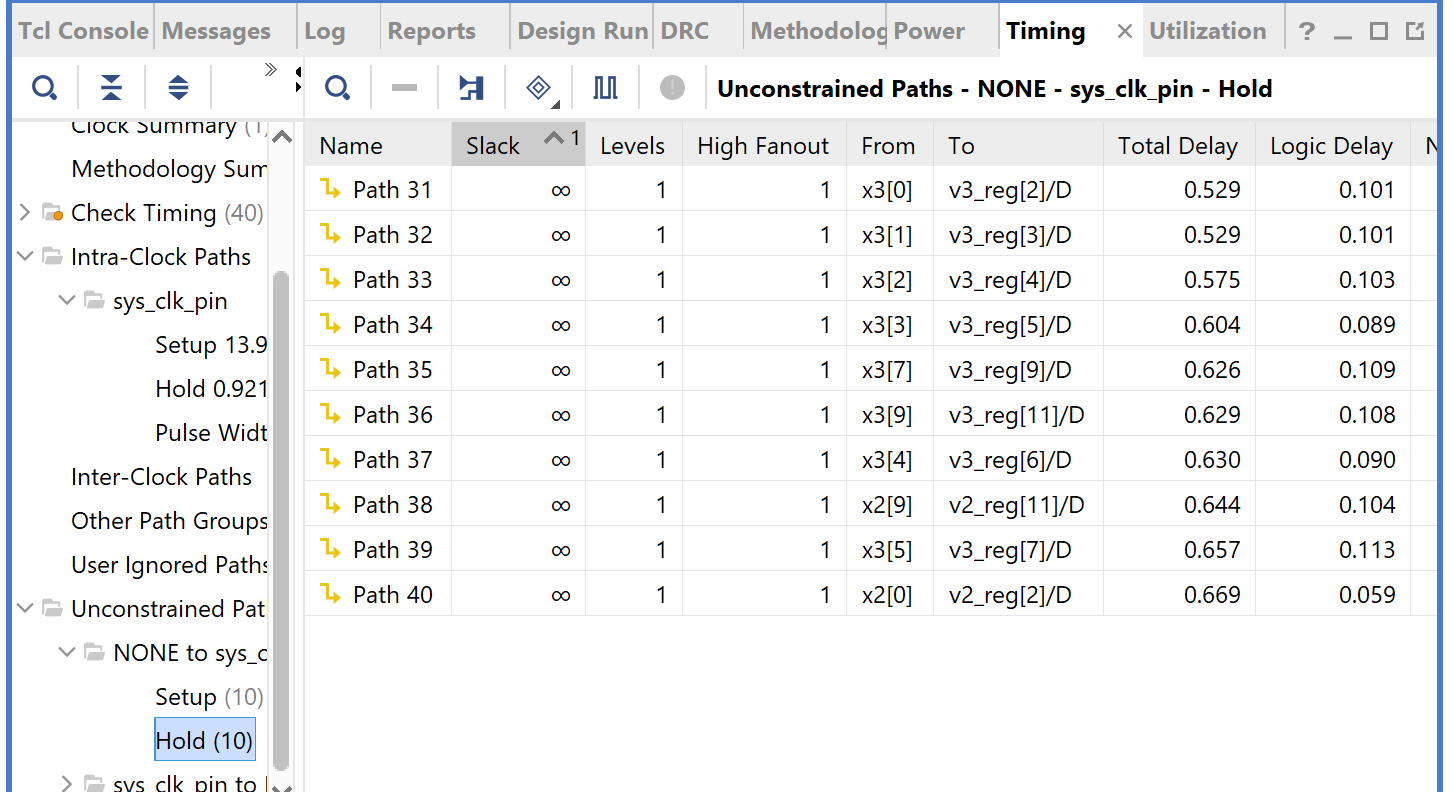
* 1. Timing: longest register to register path: (3 pts)



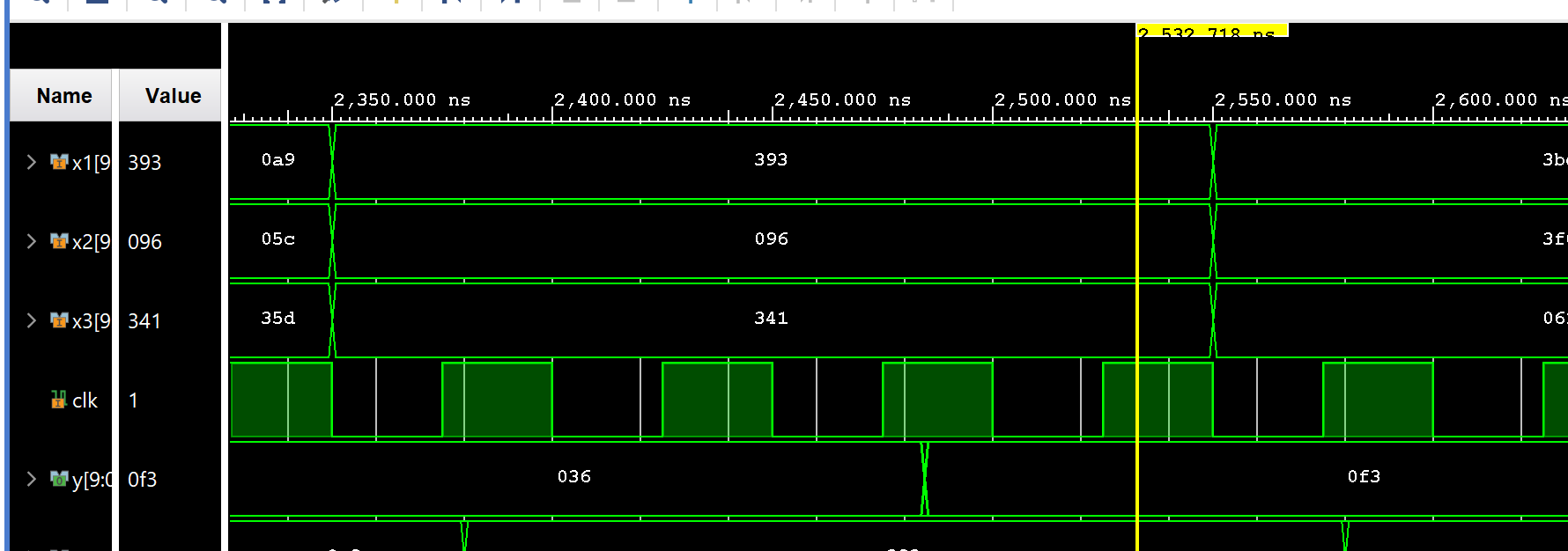
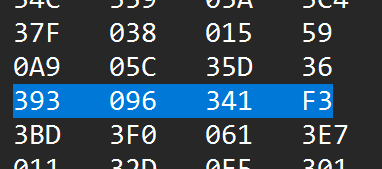
* 1. Timing: longest clock to output path: (3 pts)



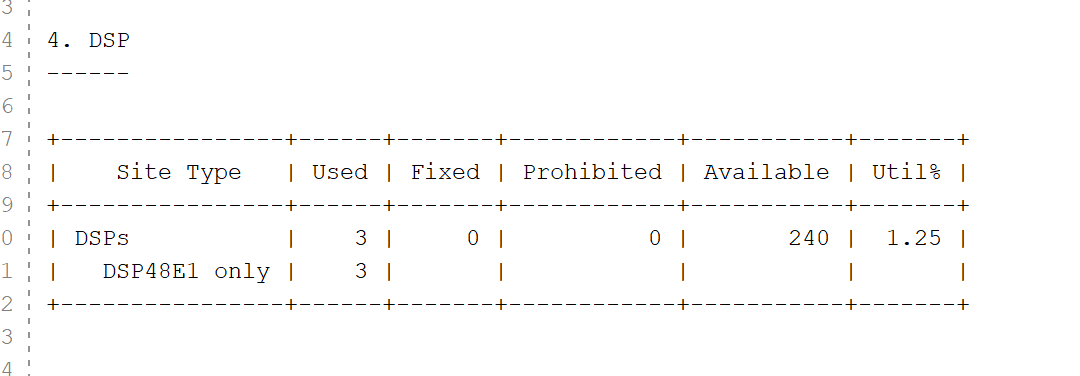
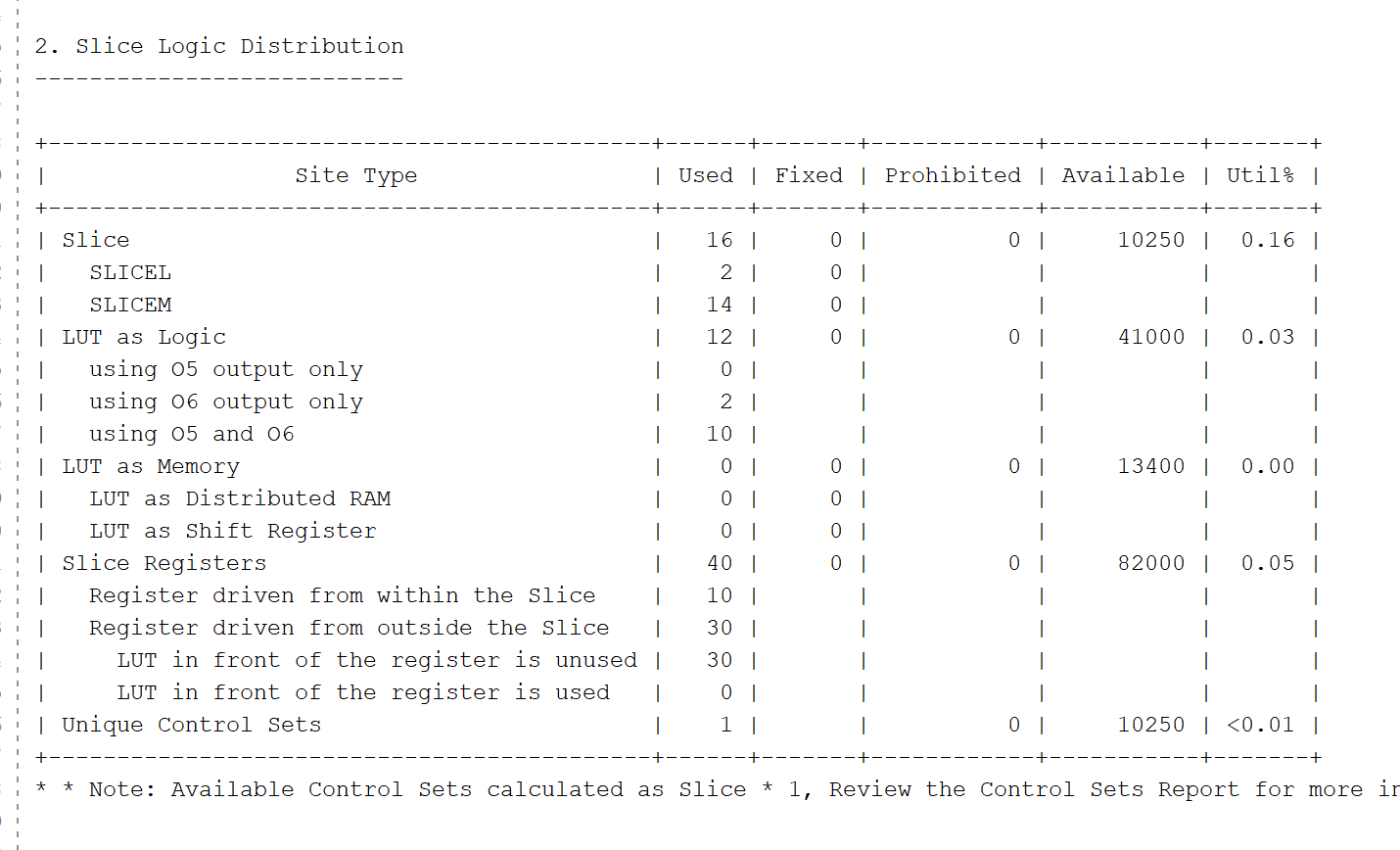
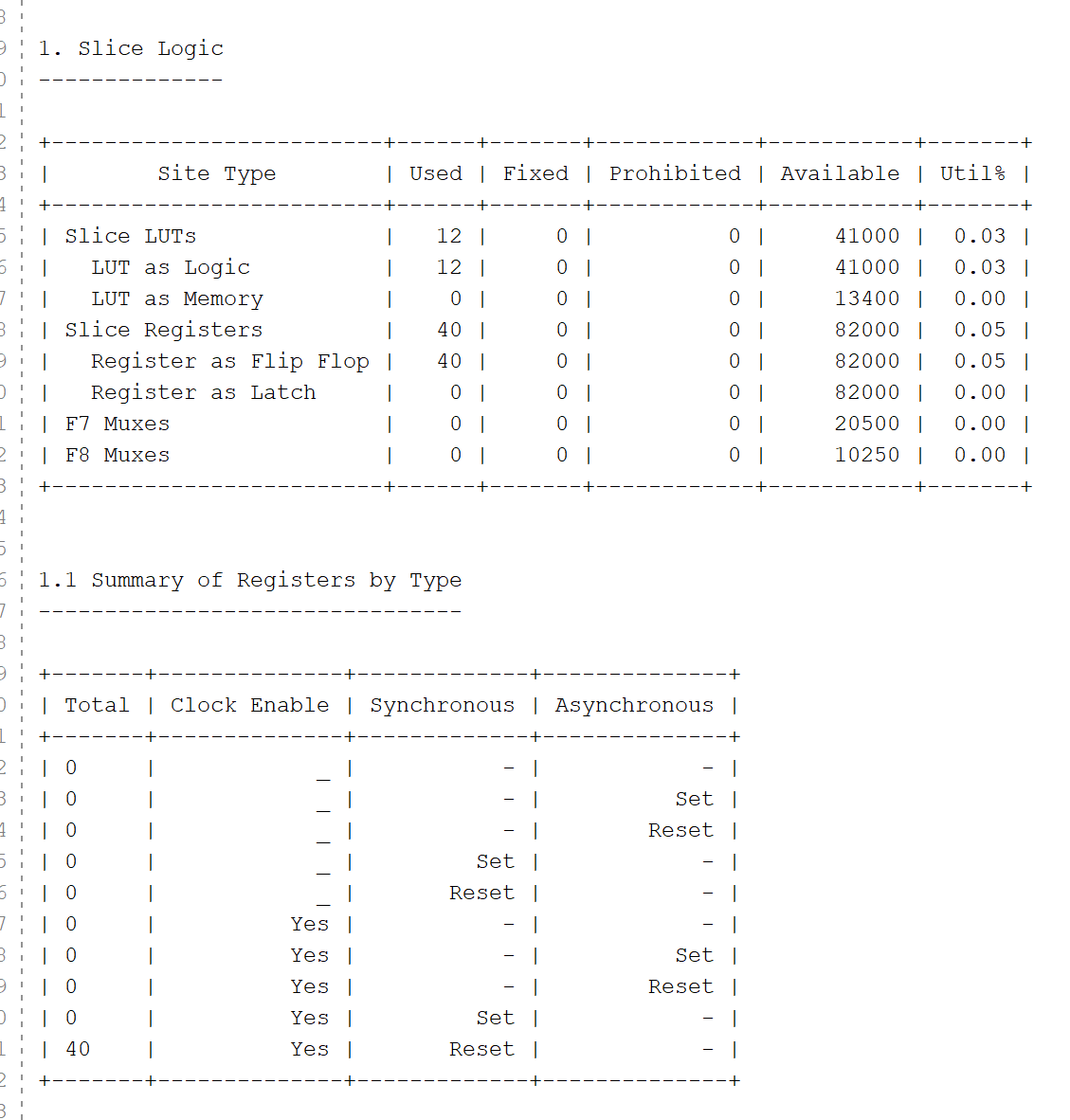
* 1. Timing: longest input pin to input register path: (3 pts)



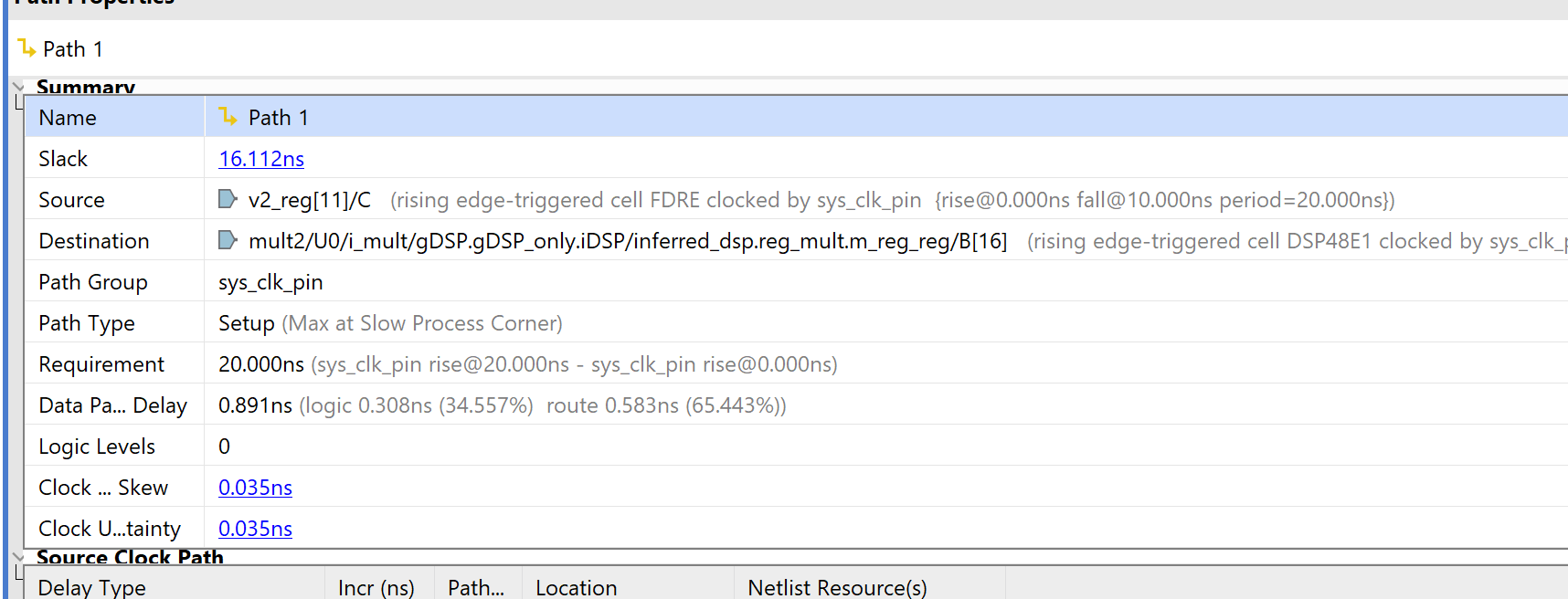
1. Correct Design part 2 (25 pts, with simulation screenshot, table data)
   1. Simulation screenshot (includes screenshot of line from vector file that is being used in the screenshot). Simulation screenshot annotated to show latency. (14 pts)



* 1. Resource usage: Slice Logic, Summary of Registers, DSP Table (3 pts)

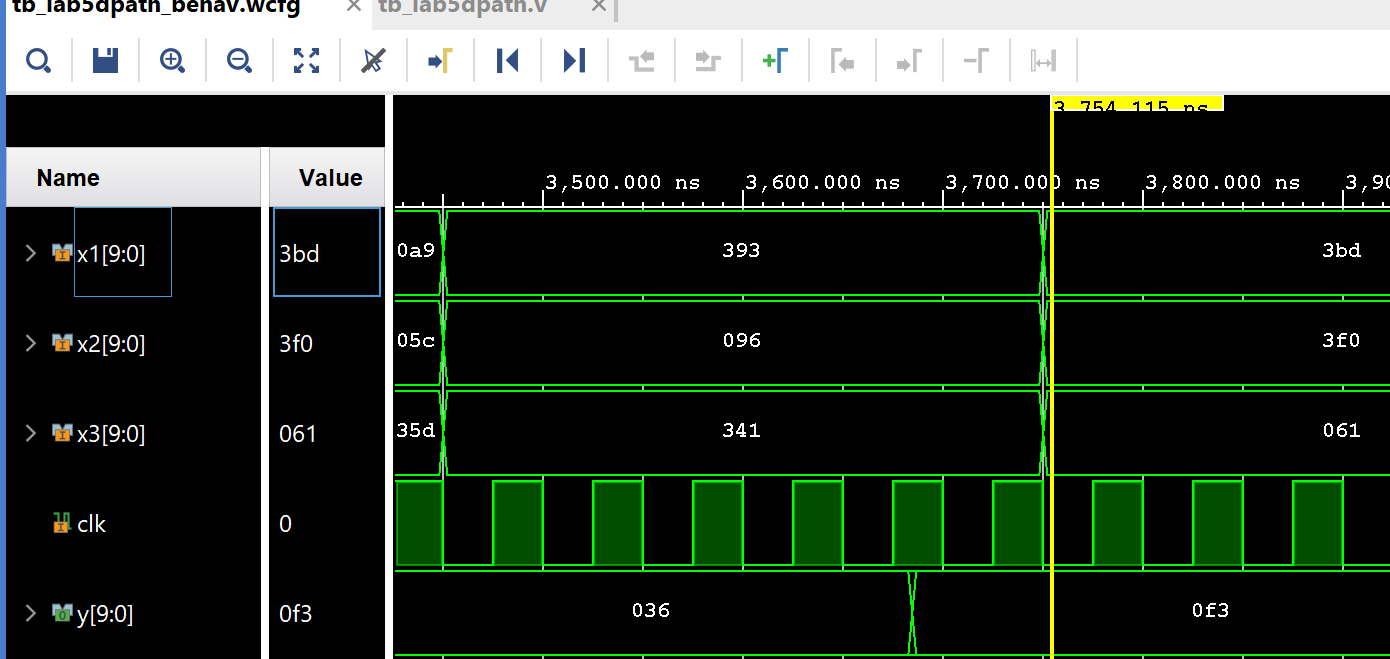
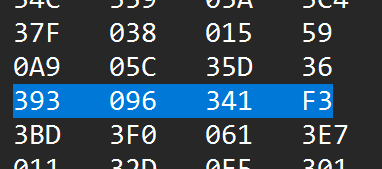


* 1. Timing – longest register to register path (3 pts)

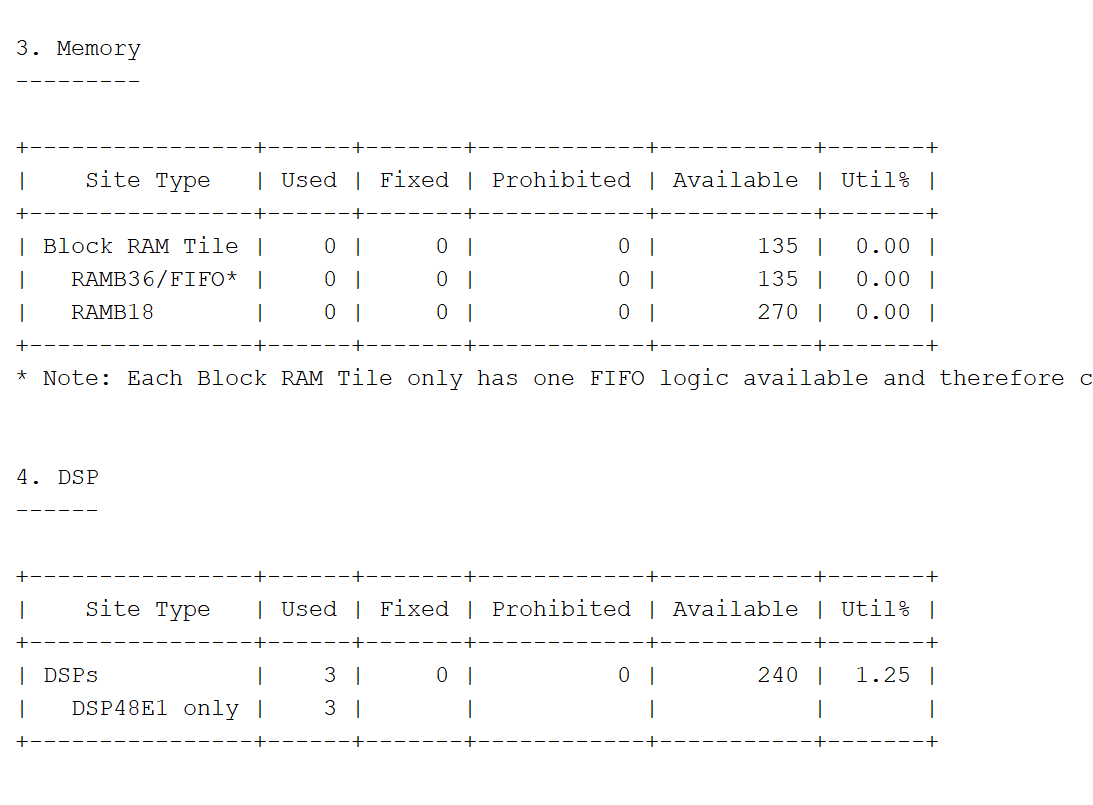
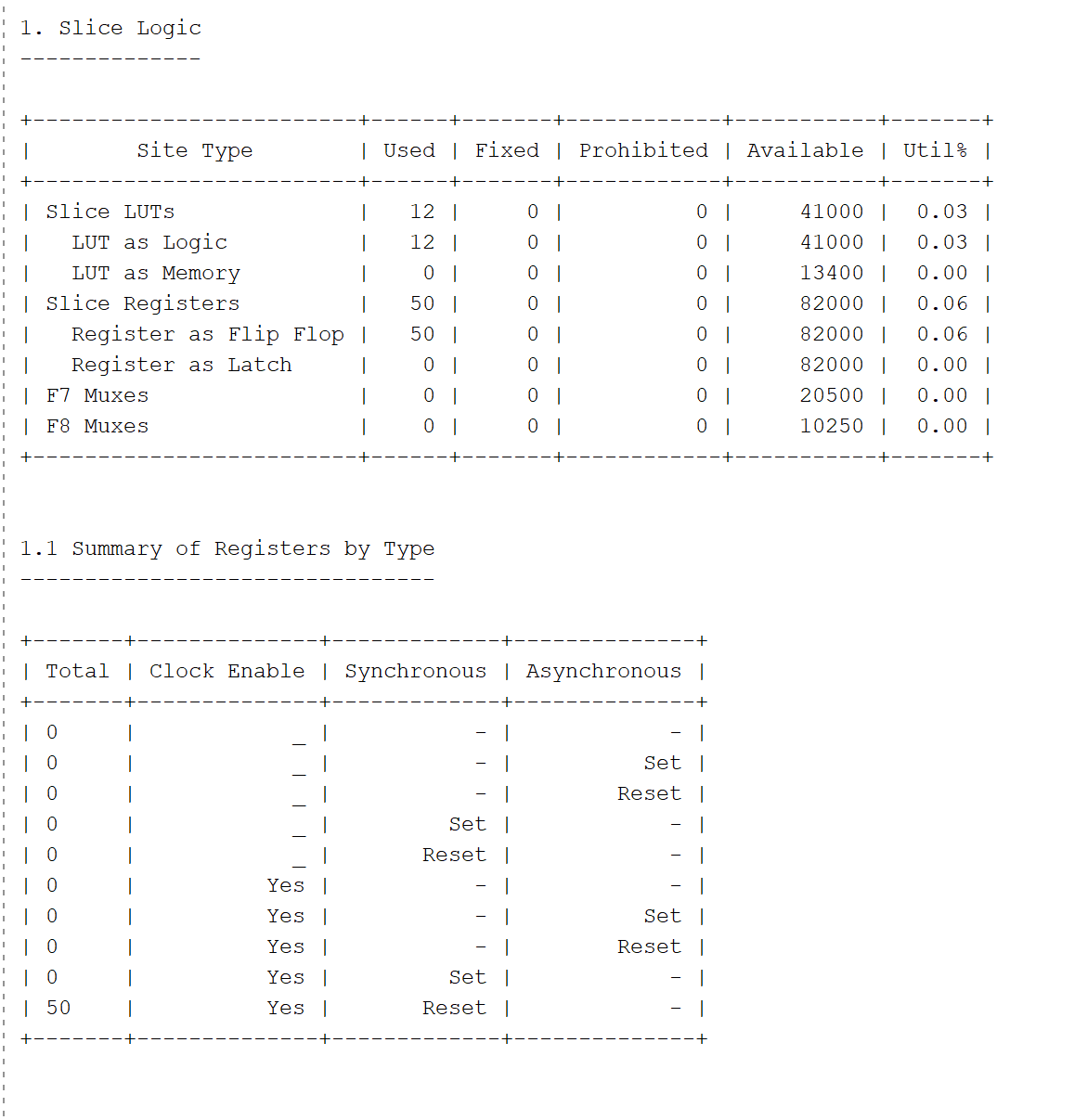


* 1. Is the above path from the output of the input register to the multiplier input or is it from the output of the multiplier to input of the output register? (5 pts)
     1. from the output of the input register to the multiplier input

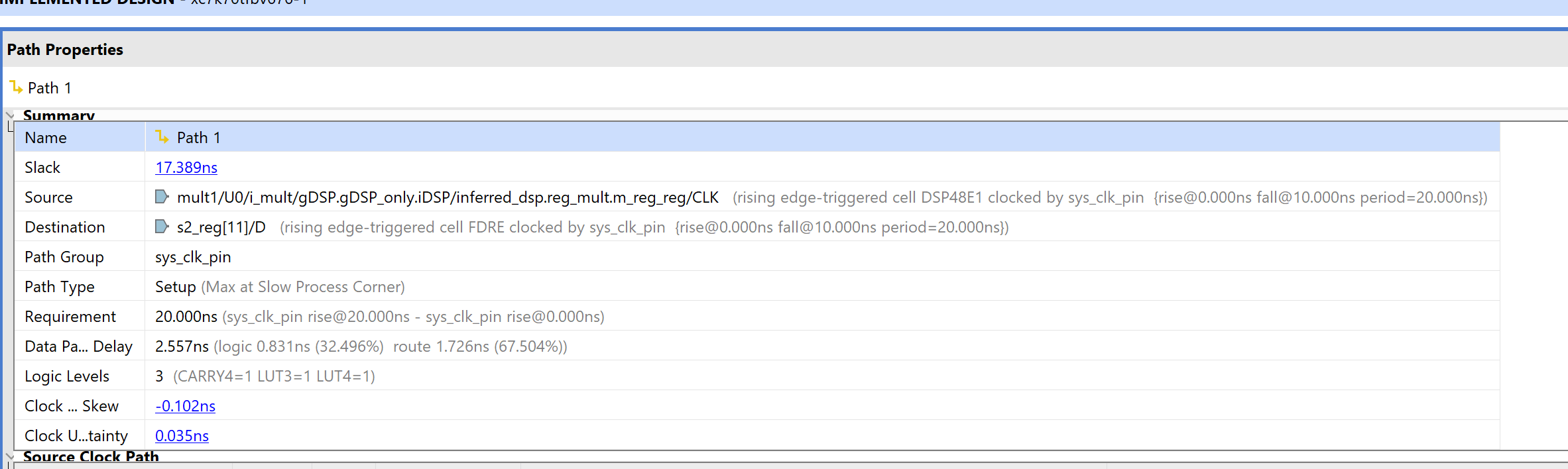
1. Correct Design part 3 (40 pts, with simulation screenshot, table data)
   1. Simulation screenshot (includes screenshot of line from vector file that is being used in the screenshot). Simulation screenshot annotated to show latency. (20 pts)



* 1. Resource Usage: Slice Logic, Summary of Registers, DSP Table (5 pts)



* 1. Timing, longest register to register path: (5 pts)



* 1. Is the above longest registers path in Path group A, B, C, D? Explain your justification. (10 pts)
     1. C, the path from the second multiplier pipeline stage to the adder logic pipeline stage. The screenshot lists the source as the multiplier and the destination as the s2 register.

1. Question (10 pts): From the utilization data for part 1, show a calculation verifying the number of DFFs in the design (these DFFs are all ‘Slice Registers as Flip Flops). FYI, this number does not increase in part 2 because the register used on the output of the Multiplier is inside the DSP48 block, not in the Slices. Also show a calculation verifying the number of Slice Registers (DFFS) for part 3 (do not count any of the registers associated with the multiplier).
   1. 40. Register driven from within the Slice = 10. Register driven from outside the Slice = 30.
   2. 50. Register driven from within the Slice = 10. Register driven from outside the Slice = 40.