UNIVERSIDADE FEDERAL DO RIO GRANDE DO SUL
CIRCUITOS DIGITAIS - INF01058
Laboratório 5 – Projeto de decodificador para 7 segmentos

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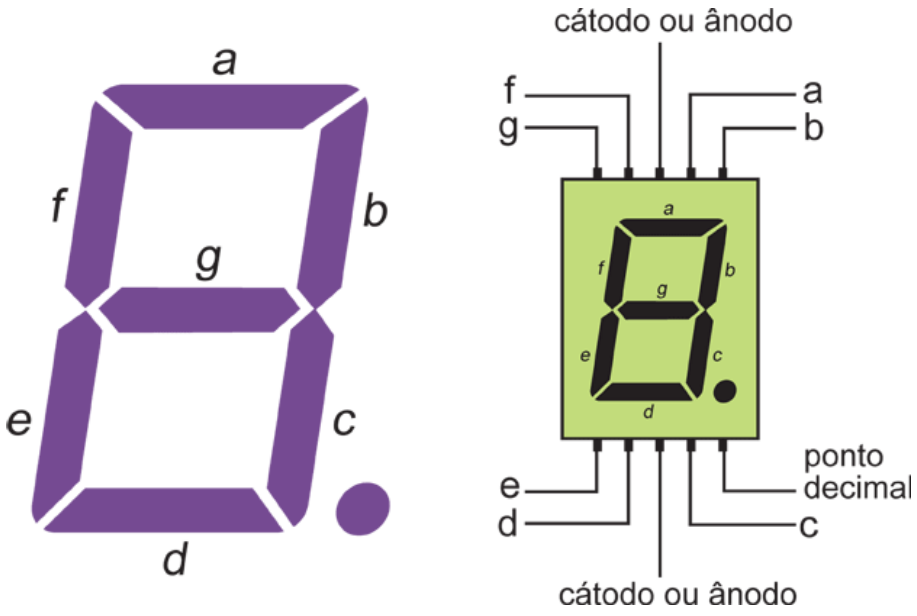
No quinto laboratório da disciplina de Circuitos Digitais, realizamos a montagem de um decodificador para 7 segmentos de um display de leds, cujas entradas geram números hexadecimais (0 à F), no Quartus II. Antes de tudo, montamos uma tabela com as entradas e saídas. Após isso, construímos os mapas de karnaught para cada led do display. Logo em seguida, fizemos as fórmulas lógicas para passar para o nosso circuito. Com isso já feito, montamos o circuito para os leds (do led A até o led G), para depois juntar todos em um único circuito que resultará no decodificador que desejávamos criar. O passo a passo realizado em cada led pode ser visualizado nas imagens abaixo.

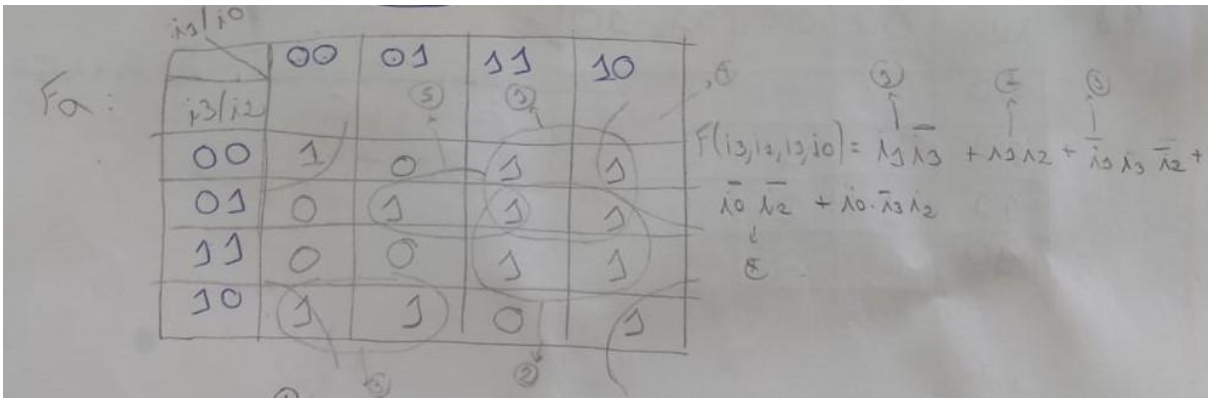


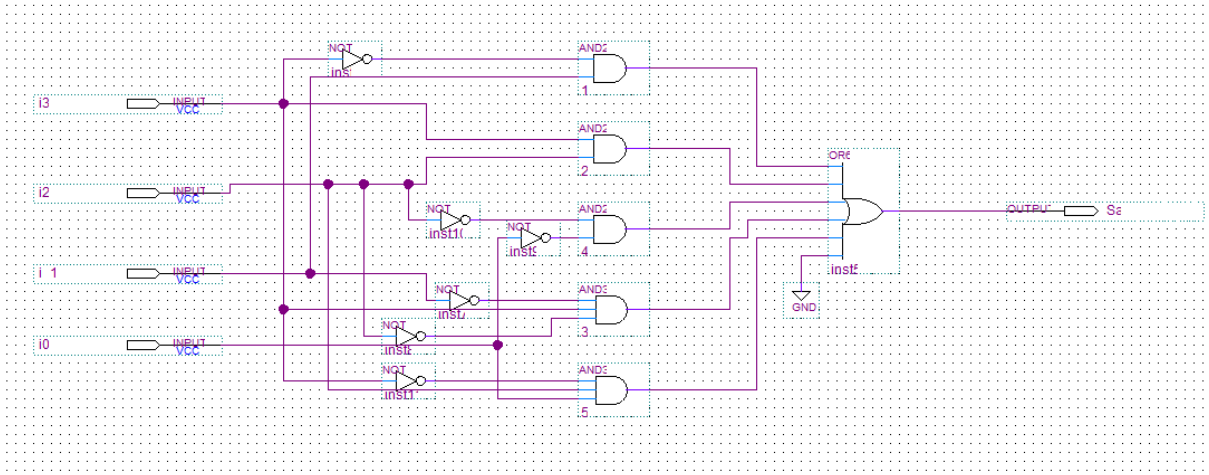
painel led cujo circuito nos baseamos.

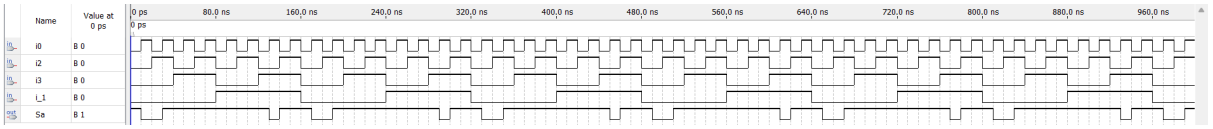
Tabela-verdade dos leds:

n	i3	i2	i1	i0	Fa	Fb	Fc	Fd	Fe	Ff	Fg
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	0	0	1	1
5	0	1	0	1	1	0	1	1	0	1	1
6	0	1	1	0	1	0	1	1	1	1	1
7	0	1	1	1	1	1	1	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	0	0	1	1
A	1	0	1	0	1	1	1	0	1	1	1
B	1	0	1	1	0	0	1	1	1	1	1
C	1	1	0	0	0	0	0	1	1	0	1
D	1	1	0	1	0	1	1	1	1	0	1
E	1	1	1	0	1	0	0	1	1	1	1
F	1	1	1	1	1	0	0	0	1	1	1

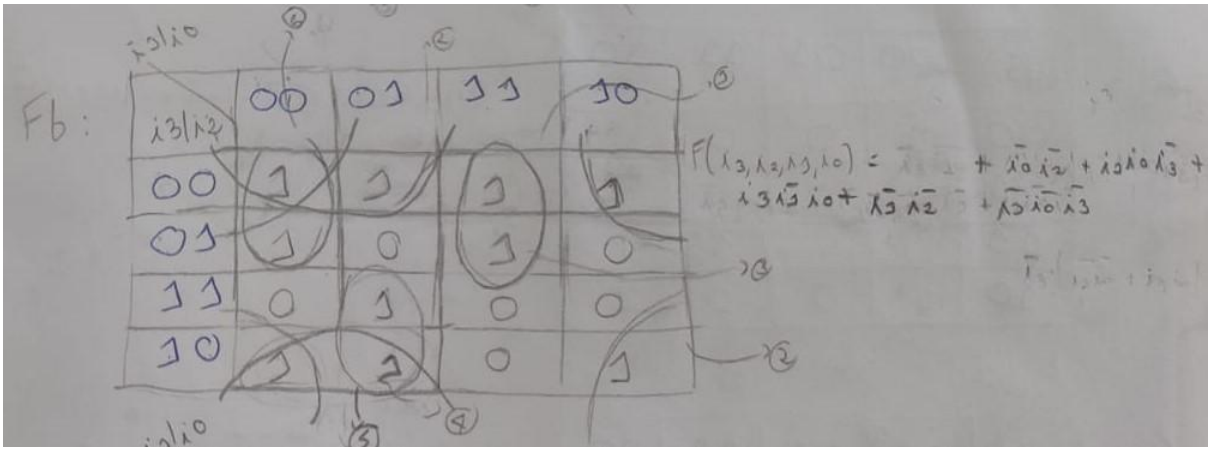
LED A:

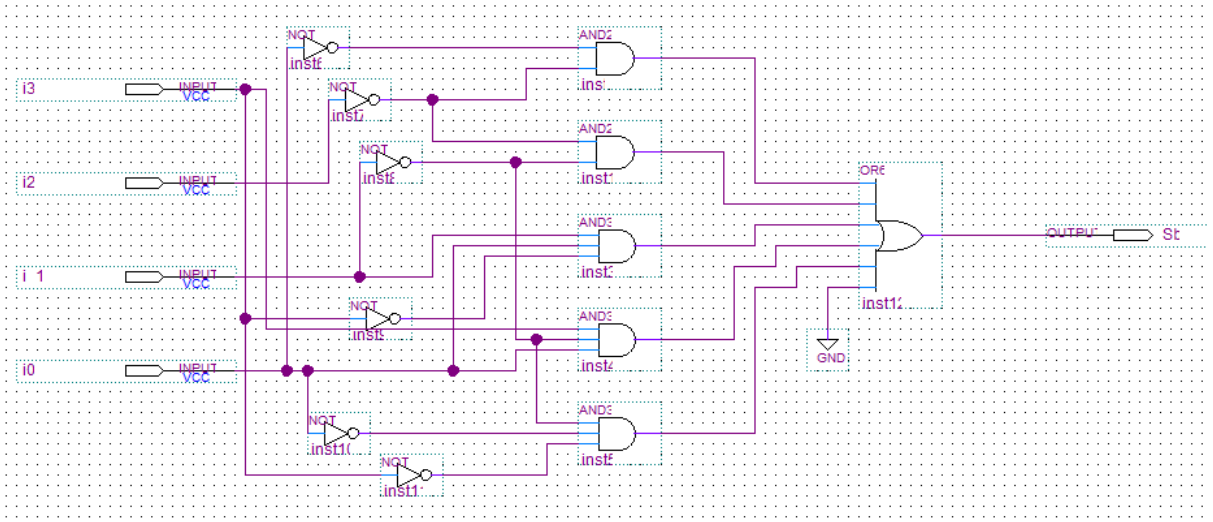

i3/i2
i1/i0
00
01
11
10
Fa :
F(i3,i2,i1,i0) = i3 ī3 + i1 i2 + ī3 i1 ī3 ī2 +
ī0 ī2 + i0 · ī3 i2

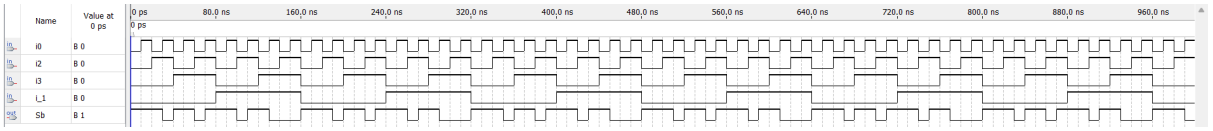

i3
i2
i_1
i0
INPUT
VCC
NOT
AND2
ORG
GND
OUTPU
Sa


Name
Value at 0 ps
i0
i2
i3
i_1
Sa
0 ps
80,0 ns
160,0 ns
240,0 ns
320,0 ns
400,0 ns
480,0 ns
560,0 ns
640,0 ns
720,0 ns
800,0 ns
880,0 ns
960,0 ns

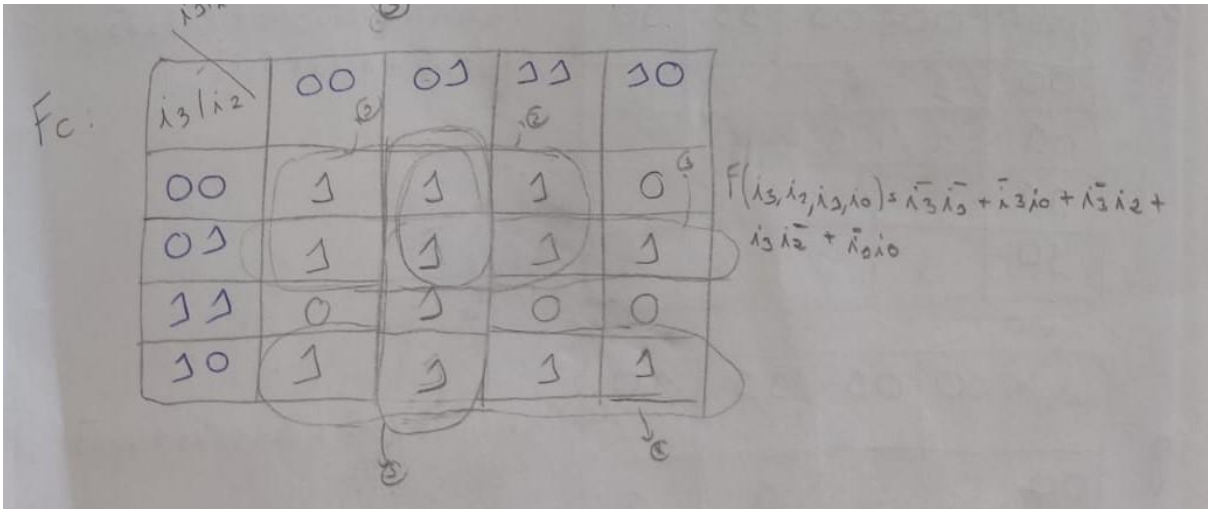
LED B:

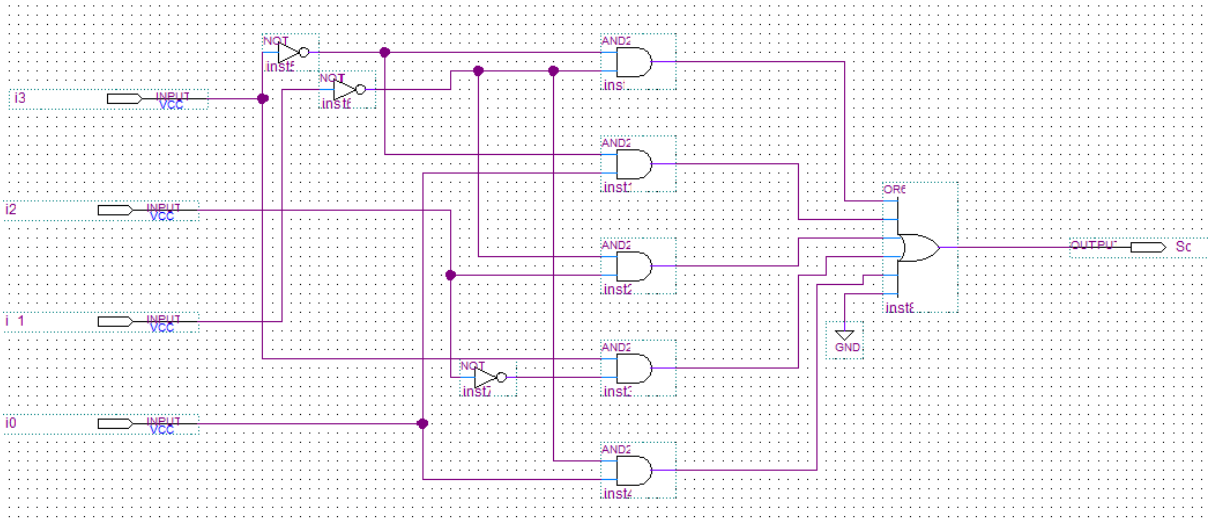

Fb :

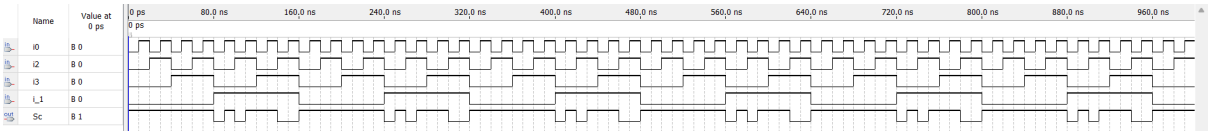

i3
i2
i 1
i0
INPUT
VCC
NOT
AND2
OR2
GND
OUTPU
St


Name
Value at 0 ps
i0
i2
i3
i_1
Sb
0 ps
80,0 ns
160,0 ns
240,0 ns
320,0 ns
400,0 ns
480,0 ns
560,0 ns
640,0 ns
720,0 ns
800,0 ns
880,0 ns
960,0 ns

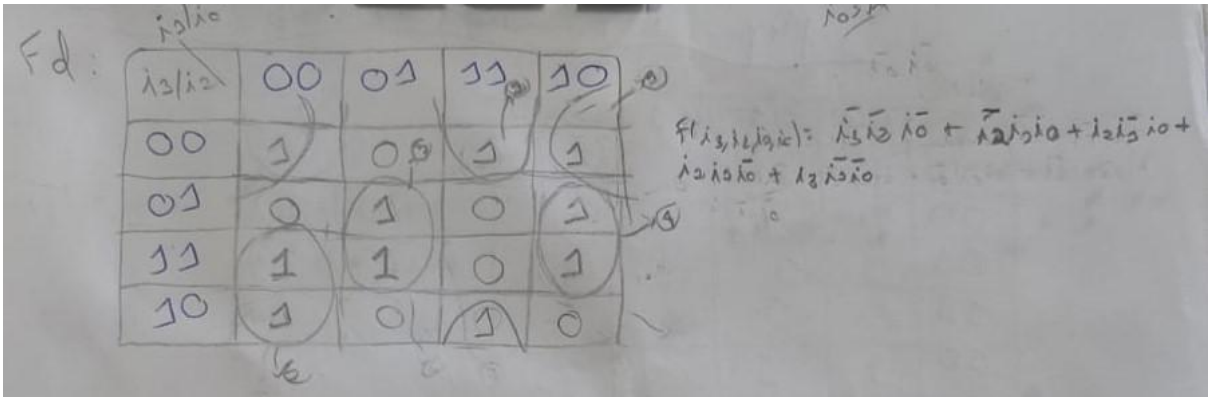
LED C:

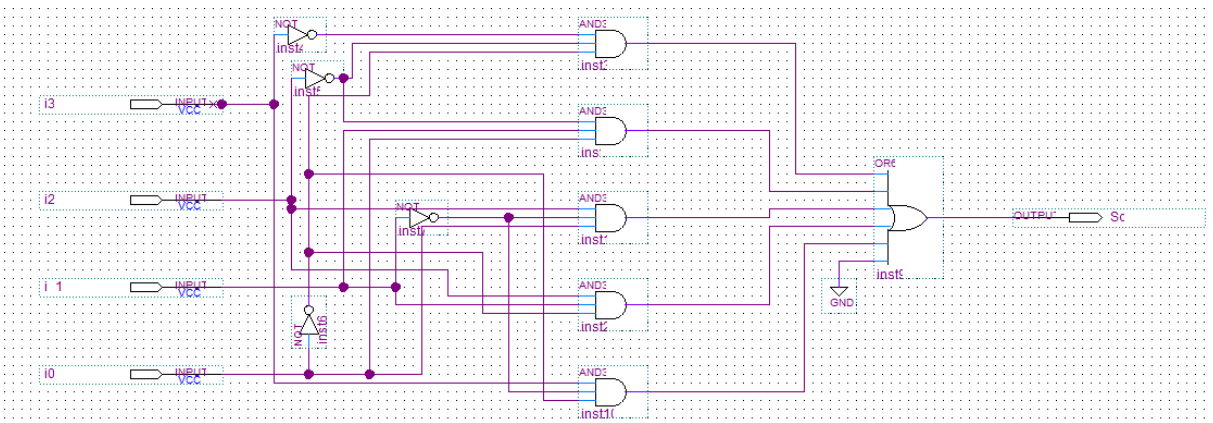

Fc:
F(λ3,λ2,λ1,λ0) = λ̄3λ̄2 + λ̄3λ0 + λ̄3λ2 +
λ1λ̄2 + λ̄0λ0

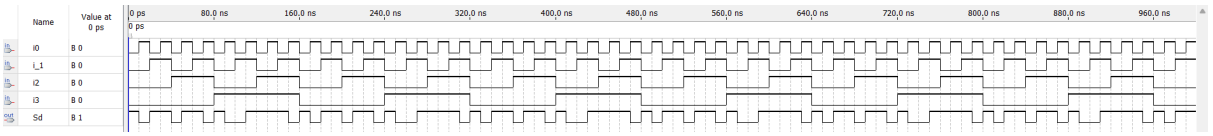

I3
I2
I 1
I0
INPUT
VCC
NOT
AND2
OR4
GND
OUTPUT
Sc


Name
Value at 0 ps
0 ps
80,0 ns
160,0 ns
240,0 ns
320,0 ns
400,0 ns
480,0 ns
560,0 ns
640,0 ns
720,0 ns
800,0 ns
880,0 ns
960,0 ns
I0
I2
I3
I_1
Sc

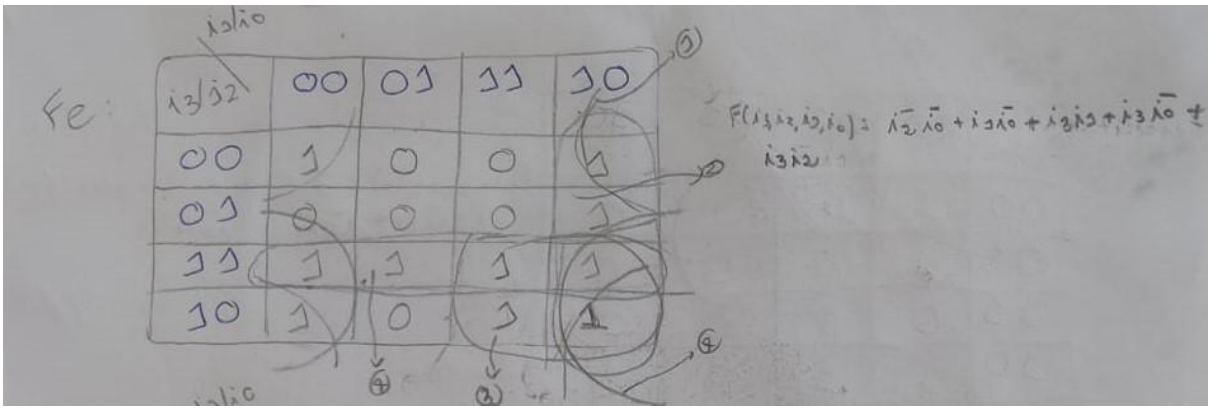
LED D:

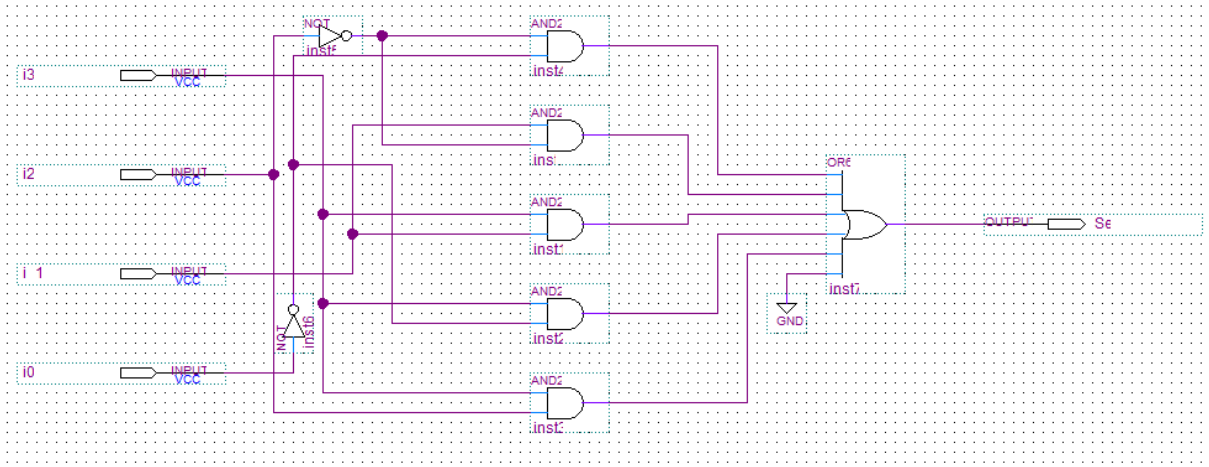

Fd:
F(i3,i2,i1,i0) = i3 i2 i0 + i2 i1 i0 + i2 i1 i0 + i3 i1 i0 + i3 i2 i0

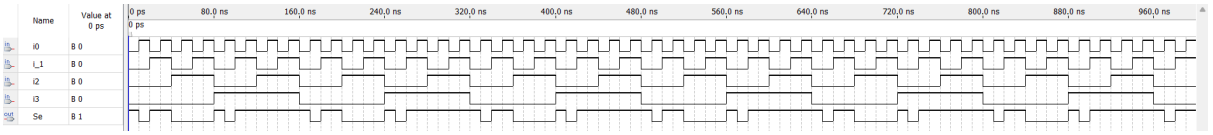

i3
i2
i 1
i0
INPUT
VCC
NOT
AND3
OR4
GND
OUTPUT
Sc


Name
Value at 0 ps
i0
i_1
i2
i3
Sd
0 ps
80,0 ns
160,0 ns
240,0 ns
320,0 ns
400,0 ns
480,0 ns
560,0 ns
640,0 ns
720,0 ns
800,0 ns
880,0 ns
960,0 ns

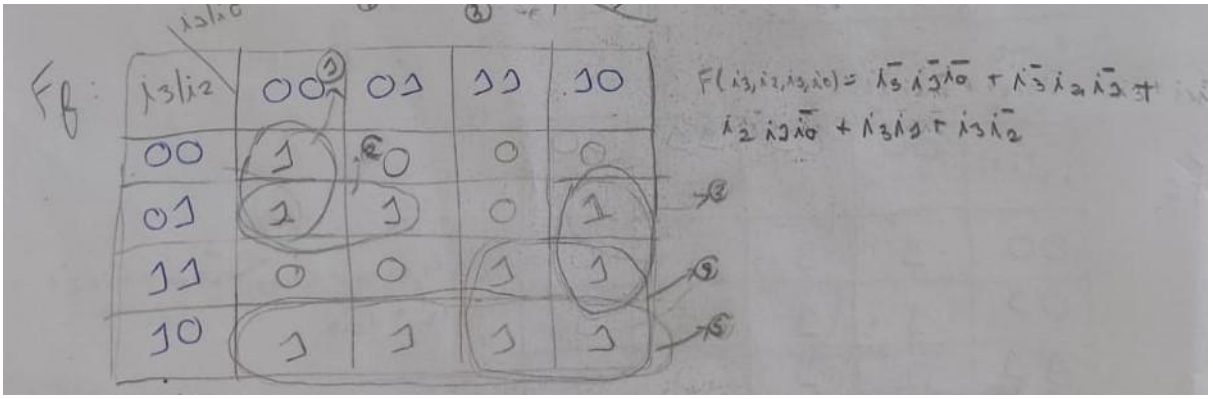
LED E:

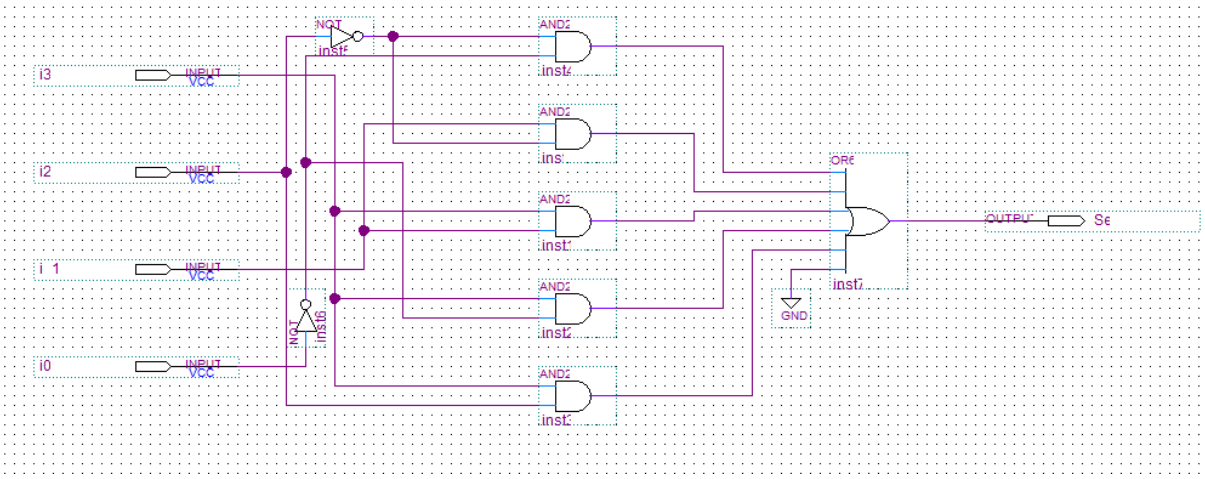


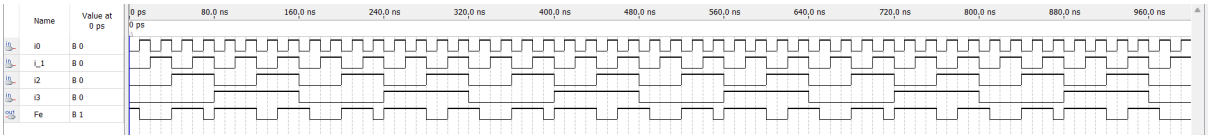

i3
i2
i 1
i0
INPUT
VCC
NOT
AND2
GND
OUTPU
Se


Name
Value at 0 ps
i0
i_1
i2
i3
Se

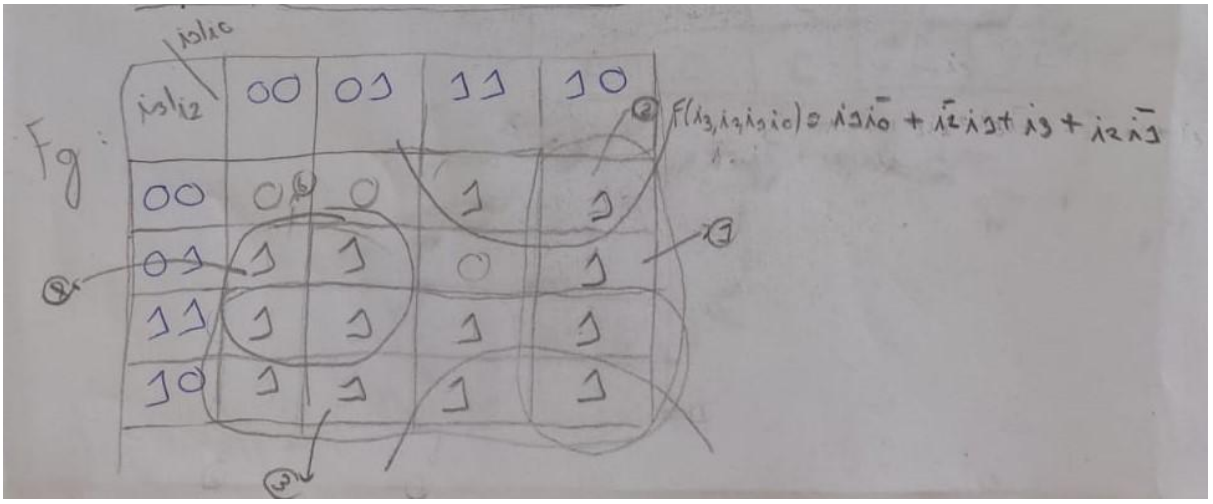
LED F:

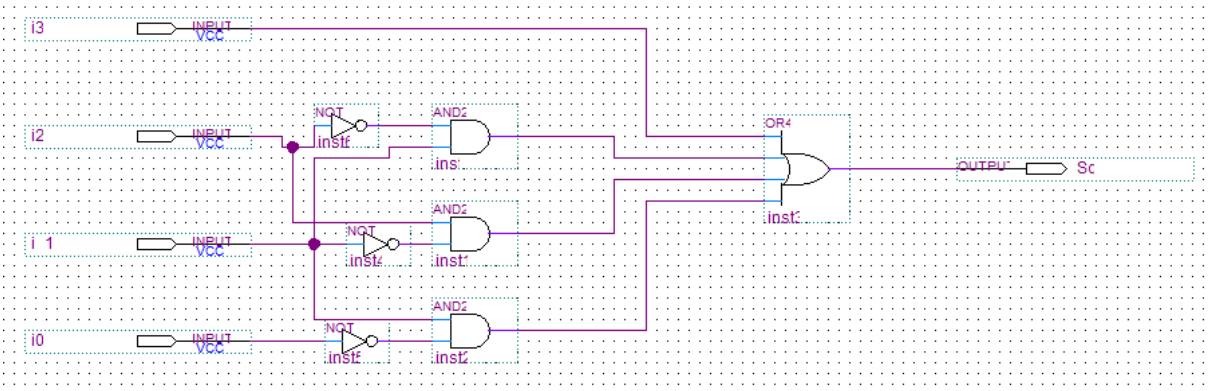


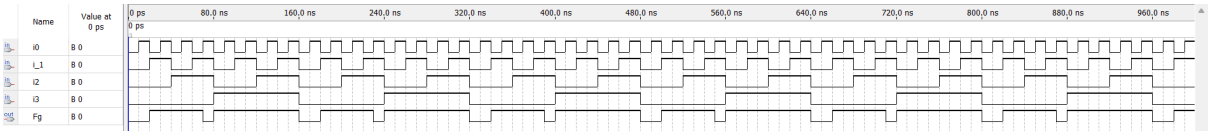

i3
i2
i 1
i0
INPUT
VCC
NOT
AND2
OR
GND
OUTPU
Se


Name
Value at 0 ps
i0
i_1
i2
i3
Fe
0 ps
80,0 ns
160,0 ns
240,0 ns
320,0 ns
400,0 ns
480,0 ns
560,0 ns
640,0 ns
720,0 ns
800,0 ns
880,0 ns
960,0 ns

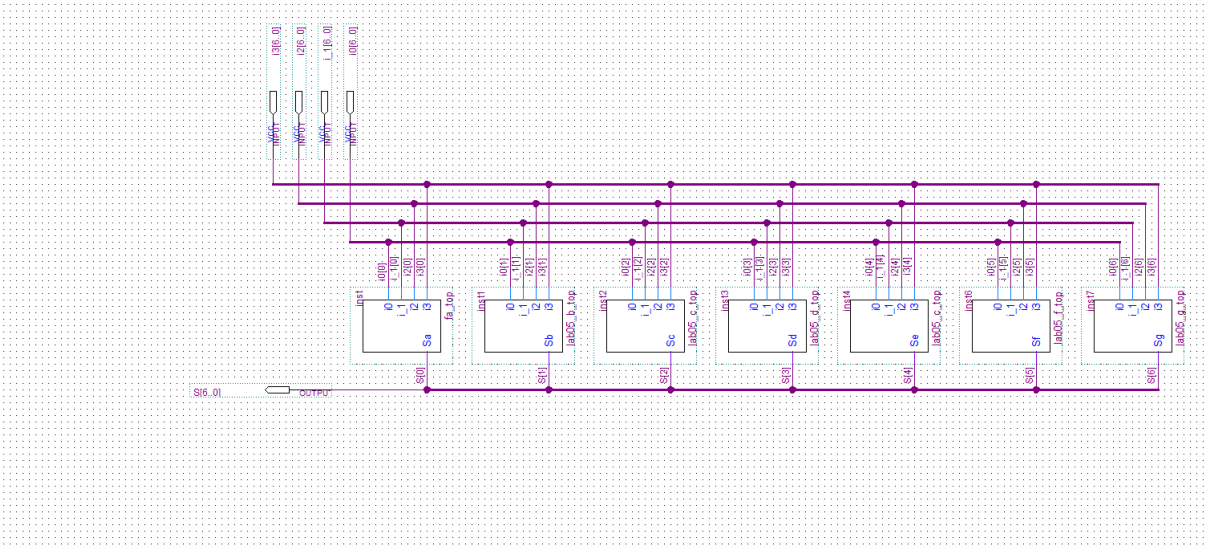
LED G:


Fg :
F(i3,i2,i1,i0) = i3i0 + i2i1 + i1i0 + i2i0


i3
INPUT
VCC
i2
INPUT
VCC
i 1
INPUT
VCC
i0
INPUT
VCC
NOT
AND2
OR4
OUTPU
Sc


Name
Value at 0 ps
i0
i_1
i2
i3
Fg
0 ps
80,0 ns
160,0 ns
240,0 ns
320,0 ns
400,0 ns
480,0 ns
560,0 ns
640,0 ns
720,0 ns
800,0 ns
880,0 ns
960,0 ns

Circuito com todos os LEDs:



Conclusões:

Nesse laboratório, aprendemos uma aplicação um pouco mais prática de decodificadores e como podemos otimizar circuitos com os mapas de karnaught. Apesar de trabalhoso, foi de suma importância para a fixação dos conteúdos aprendidos nas aulas.