SMCxxxAF

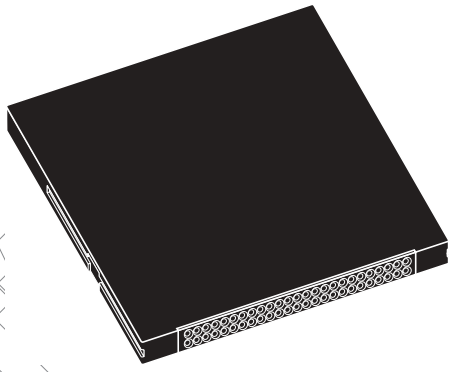
16 MByte, 32 MByte, 64 MByte, 128 MByte, 256 MByte, 512 MByte and 1 GByte, 3.3V/5V Supply CompactFlash™ Card

PRELIMINARY DATA

FEATURES SUMMARY

- CUSTOM-DESIGNED, HIGHLY-INTEGRATED MEMORY CONTROLLER
  - Compliant with CompactFlash™ Specification 2.0
  - Compatible with PCMCIA Specification
  - PC Card ATA Interface supported
  - True IDE Mode compatible
- SMALL FORM FACTOR
  - 36.4mm x 42.8mm x 3.3mm
- LOW-POWER CMOS TECHNOLOGY
- 3.3V / 5.0V POWER SUPPLY
- POWER SAVING MODE (WITH AUTOMATIC WAKE-UP)
- HIGH RELIABILITY
  - MTBF > 3,000,000 hours
  - Data Reliability: < 1 Non-Recoverable Error per 10^{14} Bits Read
  - Endurance: > 600,000 erase/program cycles
  - Number of Card Insertions/Removals: > 10,000
- HIGH PERFORMANCE
  - Up to 22MB/s transfer rate
  - Sustained Write Performance (Host to Flash Memory): 4.5MB/s
- OPERATING SYSTEM SUPPORT
  - Standard Software Drivers operation
- AVAILABLE DENSITIES (FORMATTED)
  - 16 MBytes to 1 GByte

Figure 1. Package



CompactFlash™

Table 1. Product List

Reference	Part Number	Package Form Factor	Operating Voltage Range
SMCxxxAF	SMC016AF	CF Type I	3V to 3.6V or 4.5V to 5.5V
	SMC032AF		
	SMC064AF		
	SMC128AF		
	SMC256AF		
	SMC512AF		
	SMC01GAF		

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SUMMARY DESCRIPTION

The CompactFlash is a small form factor non-volatile memory card which provides high capacity data storage. Its aim is to capture, retain and transport data, audio and images, facilitating the transfer of all types of digital information between a large variety of digital systems.

The Card operates in three basic modes,

- PCMCIA I/O mode
- PCMCIA memory mode
- True IDE mode

It conforms to the PC Card Specification when operating in the PCMCIA I/O mode and PCMCIA memory mode (Personal Computer Memory Card International Association standard, JEIDA in Japan) and to the ATA specification when operating in True IDE Mode. CompactFlash Cards can be used with passive adapters in a PC-Card Type II or Type III socket.

The Card has an internal intelligent controller which manages interface protocols, data storage and retrieval as well as Error Correcting Code (ECC), defect handling, diagnostics and clock control. Once the Card has been configured by the host, it behaves as a standard ATA (IDE) disk drive.

The specification has been realized and approved by the CompactFlash Association (CFA). This non-proprietary specification enables users to develop CF products that function correctly and are compatible with future CF design.

The system highlights are shown in Tables 2, 3, 4, 5 and 6.

Related Documentation

- PCMCIA PC Card Standard, 1995
- PCMCIA PC Card ATA Specification, 1995
- AT Attachment Interface Document, American National Standards Institute, X3.221-1994
- CF+ and CompactFlash Specification Revision 2.0

Table 2. System Performance

System Performance		Typ.	Max.	Unit
Sleep to write			1.6	ms
Sleep to read			1.8	ms
Power up to Ready		58		ms
Data transfer Rate (burst)			22 (150X)(1)	MB/s
Sustained Read			6.2 (42X)(1)	MB/s
Sustained Write			4.5 (30X)(1)	MB/s
Command to DRQ	Read		150	µs
	Write		30	

Note: 1. 150X, 42X and 18X, speed grade markings where 1X = 150 KBytes/s. These values refer to the 256 MByte Compact Flash Card.

Table 3. Current Consumption

Current Consumption (max)	3.3V±10%	5V±10%	Unit
Read	56	60	mA
Write	65	69	mA
Standby	2	5	mA
Sleep Mode	2	5	mA

Table 4. Environmental Specifications

Environmental Specifications	Operating	Non-Operating
Temperature	–40 to 85°C	–50 to 100°C
Humidity (non-condensing)	N/A	85% RH, at 85°C
Salt Water Spray	N/A	3% NaCl at 35°C(1)
Vibration (peak -to-peak)	N/A	30Gmax.
Shock	N/A	3,000Gmax.

Note: 1. MIL STD METHOD 1009

Table 5. Physical Dimensions

Physical Dimensions		Unit
Width	42.8	mm
Height	36.4	mm
Thickness	3.3	mm
Weight (typ.)	10	g

Table 6. System Reliability and Maintenance

MTBF (at 25°C)	> 3,000,000 hours
Insertions/Removals	> 10,000
Preventive Maintenance	None
Data Reliability	< 1 Non-Recoverable Error per 10^{14} bits Read
Endurance	> 600,000 Erase/Program Cycles(1)

Note: 1. Dependent on final system qualification data.

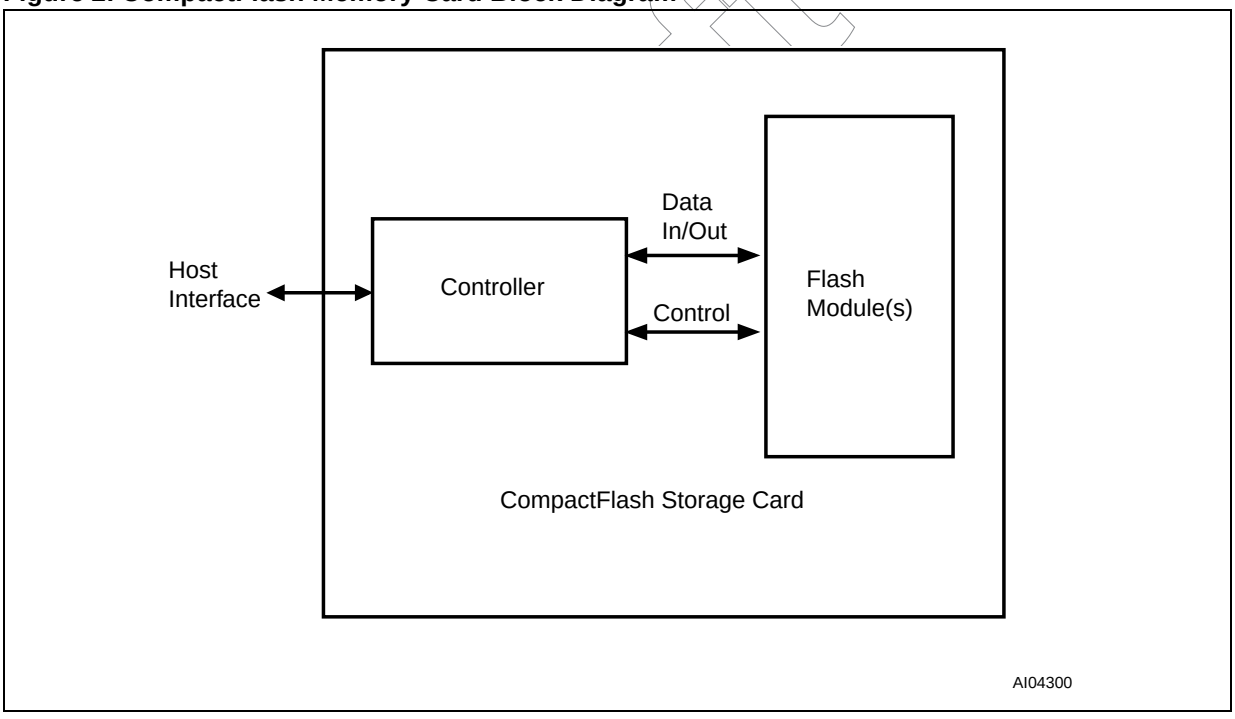
CARD PHYSICAL

Physical Description

The CompactFlash Memory Card contains a single chip controller and Flash memory module(s). The controller interfaces with a host system allowing data to be written to and read from the Flash memory module(s). Figure 2. shows the Block Diagram of the CompactFlash Memory Card.

The Card is offered in a Type I package with a 50-pin connector consisting of two rows of 25 female contacts on 50 mil (1.27mm) centers. Figure 10. shows Type I Card Dimensions.

Figure 2. CompactFlash Memory Card Block Diagram



ELECTRICAL INTERFACE

Electrical Description

The CompactFlash Memory Card operates in three basic modes:

- PC Card ATA using I/O Mode,
- PC Card ATA using Memory Mode,
- True IDE Mode, which is compatible with most disk drives.

The signal/pin assignments are listed in Table 7. Low active signals have a '–' prefix. Pin types are Input, Output or Input/Output.

The configuration of the Card is controlled using the standard PCMCIA configuration registers starting at address 200h in the Attribute Memory space of the memory card. For True IDE Mode, pin 9 is grounded.

Table 8. describes the I/O signals. Inputs are signals sourced from the host while Outputs are signals sourced from the Card. The signals are described for each of the three operating modes.

All outputs from the card are totem pole except the data bus signals that are bi-directional tri-state. Refer to the section titled "Electrical Specifications" for definitions of Input and Output type.

Table 7. Pin Assignment and Pin Type

	PC Card Memory Mode			PC Card I/O Mode			True IDE Mode		
Pin Num	**Signal Name**	**Pin Type**	**In, Out Type**	**Signal Name**	**Pin Type**	**In, Out Type**	**Signal Name**	**Pin Type**	**In, Out Type**
1	GND		Ground	GND		Ground	GND		Ground
2	D03	I/O	I1Z,OZ3	D03	I/O	I1Z,OZ3	D03	I/O	I1Z,OZ3
3	D04	I/O	I1Z,OZ3	D04	I/O	I1Z,OZ3	D04	I/O	I1Z,OZ3
4	D05	I/O	I1Z,OZ3	D05	I/O	I1Z,OZ3	D05	I/O	I1Z,OZ3
5	D06	I/O	I1Z,OZ3	D06	I/O	I1Z,OZ3	D06	I/O	I1Z,OZ3
6	D07	I/O	I1Z,OZ3	D07	I/O	I1Z,OZ3	D07	I/O	I1Z,OZ3
7	–CE1	I	I3U	–CE1	I	I3U	–CS0	I	I3Z
8	A10	I	I1Z	A10	I	I1Z	A10(2)	I	I1Z
9	–OE	I	I3U	–OE	I	I3U	–ATASEL	I	I3U
10	A09	I	I1Z	A09	I	I1Z	A09(2)	I	I1Z
11	A08	I	I1Z	A08	I	I1Z	A08(2)	I	I1Z
12	A07	I	I1Z	A07	I	I1Z	A07(2)	I	I1Z
13	V_{CC}		Power	V_{CC}		Power	V_{CC}		Power
14	A06	I	I1Z	A06	I	I1Z	A06(2)	I	I1Z
15	A05	I	I1Z	A05	I	I1Z	A05(2)	I	I1Z
16	A04	I	I1Z	A04	I	I1Z	A04(2)	I	I1Z
17	A03	I	I1Z	A03	I	I1Z	A03(2)	I	I1Z
18	A02	I	I1Z	A02	I	I1Z	A02	I	I1Z
19	A01	I	I1Z	A01	I	I1Z	A01	I	I1Z
20	A00	I	I1Z	A00	I	I1Z	A00	I	I1Z
21	D00	I/O	I1Z,OZ3	D00	I/O	I1Z,OZ3	D00	I/O	I1Z,OZ3
22	D01	I/O	I1Z,OZ3	D01	I/O	I1Z,OZ3	D01	I/O	I1Z,OZ3

	PC Card Memory Mode			PC Card I/O Mode			True IDE Mode		
Pin Num	**Signal Name**	**Pin Type**	**In, Out Type**	**Signal Name**	**Pin Type**	**In, Out Type**	**Signal Name**	**Pin Type**	**In, Out Type**
23	D02	I/O	I1Z,OZ3	D02	I/O	I1Z,OZ3	D02	I/O	I1Z,OZ3
24	WP	O	OT3	–IOIS16	O	OT3	–IOIS16	O	ON3
25	–CD2	O	Ground	–CD2	O	Ground	–CD2	O	Ground
26	–CD1	O	Ground	–CD1	O	Ground	–CD1	O	Ground
27	D11(1)	I/O	I1Z,OZ3	D11(1)	I/O	I1Z,OZ3	D11(1)	I/O	I1Z,OZ3
28	D12(1)	I/O	I1Z,OZ3	D12(1)	I/O	I1Z,OZ3	D12(1)	I/O	I1Z,OZ3
29	D13(1)	I/O	I1Z,OZ3	D13(1)	I/O	I1Z,OZ3	D13(1)	I/O	I1Z,OZ3
30	D14(1)	I/O	I1Z,OZ3	D14(1)	I/O	I1Z,OZ3	D14(1)	I/O	I1Z,OZ3
31	D15(1)	I/O	I1Z,OZ3	D15(1)	I/O	I1Z,OZ3	D15(1)	I/O	I1Z,OZ3
32	–CE2(1)	I	I3U	–CE2(1)	I	I3U	–CS1(1)	I	I3Z
33	–VS1	O	Ground	–VS1	O	Ground	–VS1	O	Ground
34	–IORD	I	I3U	–IORD	I	I3U	–IORD	I	I3Z
35	–IOWR	I	I3U	–IOWR	I	I3U	–IOWR	I	I3Z
36	–WE	I	I3U	–WE	I	I3U	–WE(3)	I	I3U
37	READY	O	OT1	IREQ	O	OT1	INTRQ	O	OZ1
38	V_{CC}		Power	V_{CC}		Power	V_{CC}		Power
39	–CSEL	I	I2Z	–CSEL	I	I2Z	–CSEL	I	I2U
40	–VS2	O	OPEN	–VS2	O	OPEN	–VS2	O	OPEN
41	RESET	I	I2Z	RESET	I	I2Z	-RESET	I	I2Z
42	–WAIT	O	OT1	–WAIT	O	OT1	IORDY	O	ON1
43	–INPACK	O	OT1	–INPACK	O	OT1	RFU	O	OZ1
44	–REG	I	I3U	–REG	I	I3U	RFU(6)	I	I3U
45	BVD2	I/O	I1U,OT1	–SPKR	I/O	I1U,OT1	–DASP	I/O	I1U,ON1
46	BVD1	I/O	I1U,OT1	–STSCHG	I/O	I1U,OT1	–PDIAG	I/O	I1U,ON1
47	D08(1)	I/O	I1Z,OZ3	D08(1)	I/O	I1Z,OZ3	D08(1)	I/O	I1Z,OZ3
48	D09(1)	I/O	I1Z,OZ3	D09(1)	I/O	I1Z,OZ3	D09(1)	I/O	I1Z,OZ3
49	D10(1)	I/O	I1Z,OZ3	D10(1)	I/O	I1Z,OZ3	D10(1)	I/O	I1Z,OZ3
50	GND		Ground	GND		Ground	GND		Ground

Note: 1. These signals are required only for 16 bit accesses and not required when installed in 8 bit systems. Devices should allow for 3-state signals not to consume current.
2. The signal should be grounded by the host.
3. The signal should be tied to V_{CC} by the host.
4. The mode is optional for CF+ Cards, but required for CompactFlash Memory Cards.
5. The -CSEL signal is ignored by the card in PC Card modes. However, because it is not pulled up on the card in these modes it should not be left floating by the host in PC Card modes. In these modes, the pin is normally connected by the host to PC Card A25 or grounded by the host.
6. The signal should be held High or tied to V_{CC} by the host
7. RFU is Reserved for Future Use

Table 8. Signal Description

Signal Name	Dir.	Pin	Description
A10 to A0 (PC Card Memory Mode)	I	8,10,11,12, 14,15,16,17, 18,19,20	Used (with –REG) to select: the I/O port address registers, the memory mapped port address registers, a Byte in the card's information structure and its configuration control and status registers.
A10 to A0 (PC Card I/O Mode)			Same as PC Card Memory Mode
A2 to A0 (True IDE Mode)			Only A2 to A0 are used to select the one of eight registers in the Task File, the remaining lines should be grounded.
BVD1 (PC Card Memory Mode)	I/O	46	The battery voltage status of the card, as no battery is required it is asserted High.
–STSCHG (PC Card I/O Mode)			Alerts the host to changes in the READY and Write Protect states. Its use is controlled by the Card Configuration and Status Register.
–PDIAG (True IDE Mode)			The Pass Diagnostic signal in the Master/Slave handshake protocol.
BVD2 (PC Card Memory Mode)	I/O	45	The battery voltage status of the card, as no battery is required it is asserted High.
–SPKR (PC Card I/O Mode)			The Binary Audio output from the Card. It is asserted High as audio functions are not supported.
–DASP (True IDE Mode)			This input/output is the Disk Active/Slave Present signal in the Master/Slave handshake protocol.
D15-D00 (PC Card Memory Mode)	I/O	31,30,29,28, 27,49,48,47, 6,5,4,3,2, 23,22,21	Carry the Data, Commands and Status information between the host and the controller. D00 is the LSB of the Even Byte of the Word. D08 is the LSB of the Odd Byte of the Word.
D15-D00 (PC Card I/O Mode)			Same as PC Card Memory Mode.
D15-D00 (True IDE Mode)			All Task File operations occur in Byte mode on D00 to D07 while all data transfers are 16 bit using D00 to D15.
GND (PC Card Memory Mode)		1,50	Ground.
GND (PC Card I/O Mode)			Same for all modes.
GND (True IDE Mode)			Same for all modes.
–INPACK (PC Card Memory Mode)	O	43	Not used, should not be connected to the host.
–INPACK (PC Card I/O Mode)			The Input Acknowledge is asserted when the Card is selected and responding to an I/O read cycle at the current address on the bus. It is used by the host to control the enable of any input data buffers between the Card and CPU.
Reserved (True IDE Mode)			Not used, should not be connected to the host.

Signal Name	Dir.	Pin	Description
–IORD (PC Card Memory Mode)	I	34	Not used.
–IORD (PC Card I/O Mode)			I/O Read strobe generated by the host. It gates I/O data onto the bus.
–IORD (True IDE Mode)			Same as PC Card I/O Mode.
–CD1, –CD2 (PC Card Memory Mode)	O	26,25	These are connected to ground on the Card. They are used by the host to determine that the Card is fully inserted into its socket.
–CD1, –CD2 (PC Card I/O Mode)			Same for all modes.
–CD1, –CD2 (True IDE Mode)			Same for all modes.
–CE1, –CE2 (PC Card Memory Mode)	I	7,32	Used to select the Card and to indicate whether a Byte or a Word operation is being performed. –CE2 accesses the odd Byte, –CE1 accesses the even Byte or the odd Byte depending on A0 and –CE2. A multiplexing scheme based on A0, –CE1, –CE2 allows 8 bit hosts to access all data on D0 to D7.
–CE1, –CE2 (PC Card I/O Mode)			Same as PC Card Memory Mode.
–CS0, –CS1 (True IDE Mode)			CS0 is the chip select for the task file registers, while CS1 selects the Alternate Status Register and the Device Control Register.
–CSEL (PC Card Memory Mode)			Not used.
–CSEL (PC Card I/O Mode)	I	39	Not used.
–CSEL (True IDE Mode)			This internally pulled up signal is used to configure the Card as a Master or Slave. When grounded it is configured as a Master, when open it is configured as a Slave.
–IOWR (PC Card Memory Mode)	I	35	Not used.
–IOWR (PC Card I/O Mode)			The I/O Write strobe pulse is used to clock I/O data on the bus into the Card controller registers. Clocking occurs on the rising edge.
–IOWR (True IDE Mode)			Same as PC Card I/O Mode.
–OE (PC Card Memory Mode)	I	9	This is an Output Enable strobe generated by the host interface. It reads data and the CIS and configuration registers.
–OE (PC Card I/O Mode)			Reads the CIS and configuration registers.
–ATASEL (True IDE Mode)			Grounded by the host.

Signal Name	Dir.	Pin	Description
READY (PC Card Memory Mode)	O	37	Indicates whether the Card is busy (Low), or ready to accept a new data transfer operation (High). The Host socket must provide a pull-up resistor. At power up and Reset, the READY signal is held Low until the commands are completed. No access should be made during this time. The READY signal is held High whenever the Card has been powered up with RESET continuously disconnected or asserted.
–IREQ (PC Card I/O Mode)			Interrupt Request. It is strobed Low to generate a pulse mode interrupt or held Low for a level mode interrupt.
INTRQ (True IDE Mode)			Active High Interrupt Request to the host.
–REG (PC Card Memory Mode)	I	44	Used to distinguish between Common Memory and Register (Attribute) Memory accesses. High for Common Memory, Low for Attribute Memory.
–REG (PC Card I/O Mode)			Must be Low during I/O Cycles when the I/O address is on the Bus.
Reserved (True IDE Mode)			Not used, should be connected to V_{CC} by the host.
RESET (PC Card Memory Mode)	I	41	Resets the Card (active High). The Card is Reset at power up only if this pin is left High or unconnected.
RESET (PC Card I/O Mode)			Same as PC Card Memory Mode.
–RESET (True IDE Mode)			Hardware Reset from the host (active Low).
V_{CC} (PC Card Memory Mode)		13,38	+5V, +3.3V power.
V_{CC} (PC Card I/O Mode)			Same for all modes.
V_{CC} (True IDE Mode)			Same for all modes.
–VS1, –VS2 (PC Card Memory Mode)	O	33,40	Voltage Sense Signals.–VS1 is grounded so that the CIS can be read at 3.3 volts and –VS2 is reserved by PCMCIA for a secondary voltage.
–VS1, –VS2 (PC Card I/O Mode)			Same for all modes.
–VS1, –VS2 (True IDE Mode)			Same for all modes.
–WAIT (PC Card Memory Mode)	O	42	Signals the host to delay completion of a memory or I/O cycle that is in progress (active Low).
–WAIT (PC Card I/O Mode)			Same as PC Card Memory Mode.
IORDY (True IDE Mode)			Use as IORDY.

Signal Name	Dir.	Pin	Description
–WE (PC Card Memory Mode)	I	36	Driven by the host to strobe memory write data to the registers.
–WE (PC Card I/O Mode)			Used for writing to the configuration registers.
–WE (True IDE Mode)			Not used, should be connected to V_{CC} by the host.
WP (PC Card Memory Mode)	O	24	No write protect switch available. It is held Low after the completion of the reset initialization sequence.
–IOIS16 (PC Card I/O Mode)			Used for the 16 bit Port (–IOIS16) function. Low indicates that a 16 bit or odd Byte only operation can be performed at the addressed port.
–IOCS16 (True IDE Mode)			Asserted Low when the Card is expecting a Word data transfer cycle.

Electrical Specification

Table 9. defines the DC Characteristics for the CompactFlash Memory Card. Unless otherwise stated, conditions are:

- V_{CC} = 5V ± 10%
- V_{CC} = 3.3V ± 10%
- -40 °C to 85 °C

The Card operates correctly in both the voltage ranges shown in Table 9. To comply with this specification, current requirements must not exceed the maximum limit shown in Table 10.

Table 9. Absolute Maximum Conditions

Parameter	Symbol	Conditions
Input Power	V_{CC}	–0.3V to 6.5V
Voltage on any pin except V_{CC} with respect to GND	V	–0.5V to V_{CC} + 0.5V

Table 10. Input Power

Voltage	Maximum Average RMS Current	Measurement Conditions
3.3V ± 10%	65mA	3.3V at 25°C
5V ± 10%	70mA	5.0V at 25°C

Current Measurement

The current is measured by connecting an amp meter in series with the V_{CC} supply. The meter should be set to the 2A scale range, and have a fast current probe with an RC filter with a time constant of 0.1ms. Current measurements are taken while looping on a data transfer command with a sector count of 128. Current consumption values for both read and write commands are not to exceed the Maximum Average RMS Current specified in Table 10. Table 11. shows the Input Leakage Current, Table 12. the Input Characteristics, Table 13. the Output Drive Type and Table 14. the Output Drive Characteristics.

Table 11. Input Leakage Current

Type	Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
IxZ	Input Leakage Current	IL	$V_{IH} = V_{CC}$ $V_{IL} = GND$	–1		1	µA
IxU	Pull Up Resistor	RPU1	$V_{CC} = 5.0V$	50		500	kΩ
IxD	Pull Down Resistor	RPD1	$V_{CC} = 5.0V$	50		500	kΩ

Note: x refers to the characteristics described in Table 12. For example, I1U indicates a pull up resistor with a type 1 input characteristic.

Table 12. Input Characteristics

Type	Parameter	Symbol	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
			$V_{CC} = 3.3V$			$V_{CC} = 5.0V$			
1	Input Voltage CMOS	V_{IH}	2.4			2.4			V
		V_{IL}			0.6			0.8	
2	Input Voltage CMOS	V_{IH}	1.5			2.0			V
		V_{IL}			0.6			0.8	
3	Input Voltage CMOS Schmitt Trigger	V_{TH}		1.8			2.8		V
		V_{TL}		1.0			2.0		

Table 13. Output Drive Type

Type	Output Type	Valid Conditions
OTx	Totempole	I_{OH} & I_{OL}
OZx	Tri-State N-P Channel	I_{OH} & I_{OL}
OPx	P-Channel Only	I_{OH} Only
ONx	N-Channel Only	I_{OL} Only

Note: x refers to the characteristics described in Table 14. For example, OT3 refers to totem pole output with a type 3 output drive characteristic.

Table 14. Output Drive Characteristics

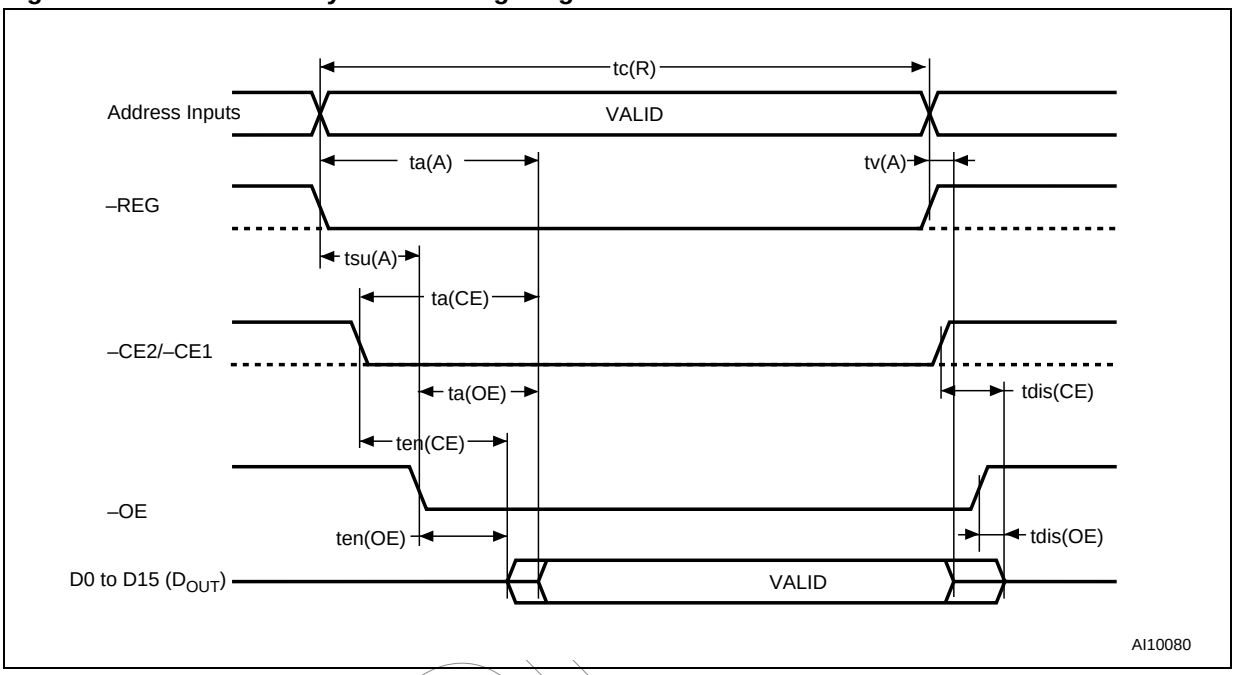
Type	Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
1	Output Voltage	V_{OH}	$I_{OH} = –4mA$	$V_{CC} – 0.8V$			V
		V_{OL}	$I_{OL} = 4mA$			Gnd + 0.4V	
2	Output Voltage	V_{OH}	$I_{OH} = –8mA$	$V_{CC} – 0.8V$			V
		V_{OL}	$I_{OL} = 8mA$			Gnd + 0.4V	
3	Output Voltage	V_{OH}	$I_{OH} = –8mA$	$V_{CC} – 0.8V$			V
		V_{OL}	$I_{OL} = 8mA$			Gnd + 0.4V	
X	Tri-State Leakage Current	I_{OZ}	$V_{OL} = Gnd$	–10		10	µA
			$V_{OH} = V_{CC}$				

Command Interface

There are two types of bus cycles and timing sequences that occur in the PCMCIA type interface, direct mapped I/O transfer and memory access. Tables 15, 16, 17, 18, 19, 20 and 21 show the read and write timing parameters. Figures 3, 4, 5, 6, 7, 8 and 9 show the read and write timing diagrams.

Note, the Wait Width time is intentionally less than the PCMCIA Specification of 12µs. Its maximum value can be determined from the Card Information Structure.

Figure 3. Attribute Memory Read Timing Diagram

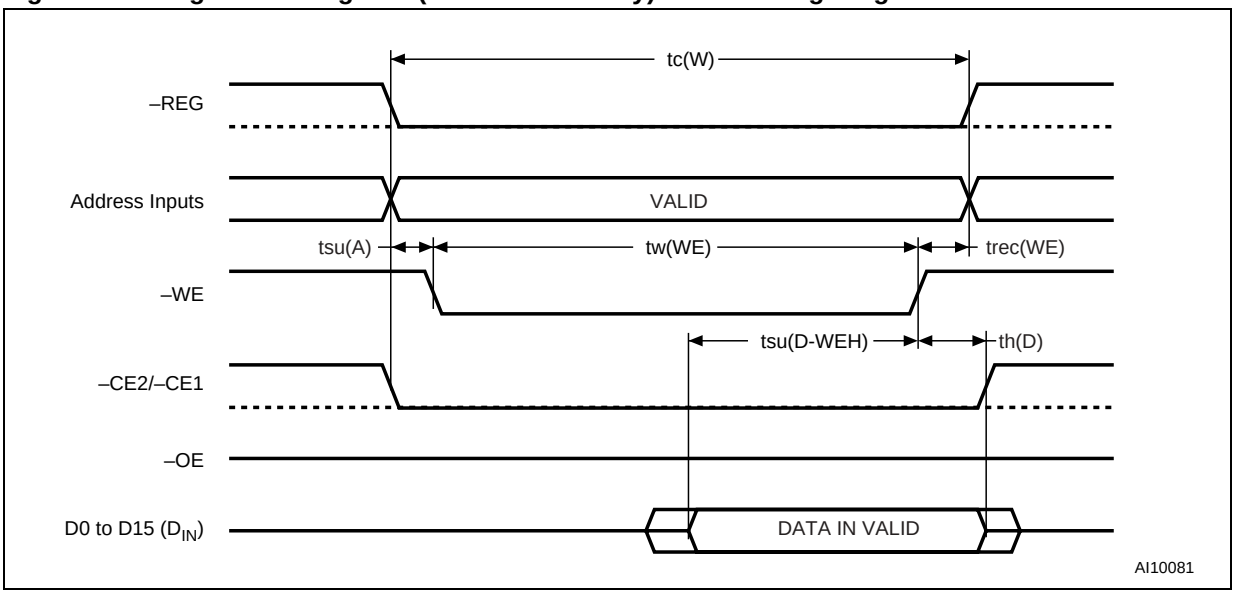


Note: D_{OUT} signifies data provided by the CompactFlash Memory Card or CF+ Card to the system. The -CE signal or both the -OE signal and the -WE signal must be de-asserted between consecutive cycle operations.

Table 15. Attribute Memory Read Timing

Symbol	IEEE Symbol	Parameter	Min	Max	Unit
tc(R)	t_{AVAV}	Read Cycle Time	300		ns
ta(A)	t_{AVQV}	Address Access Time		300	ns
ta(CE)	t_{ELQV}	CE Access Time		300	ns
ta(OE)	t_{GLQV}	OE Access Time		150	ns
tdis(CE)	t_{EHQZ}	Output Disable Time from CE		100	ns
tdis(OE)	t_{GHQZ}	Output Disable Time from OE		100	ns
ten(CE)	t_{ELQNZ}	Output Enable Time from CE	5		ns
ten(OE)	t_{GLQNZ}	Output Enable Time from OE	5		ns
tv(A)	t_{AXQX}	Data Valid from Address Change	0		ns
tsu(A)	t_{AVGL}	Address Setup Time	30		ns

Figure 4. Configuration Register (Attribute Memory) Write Timing Diagram

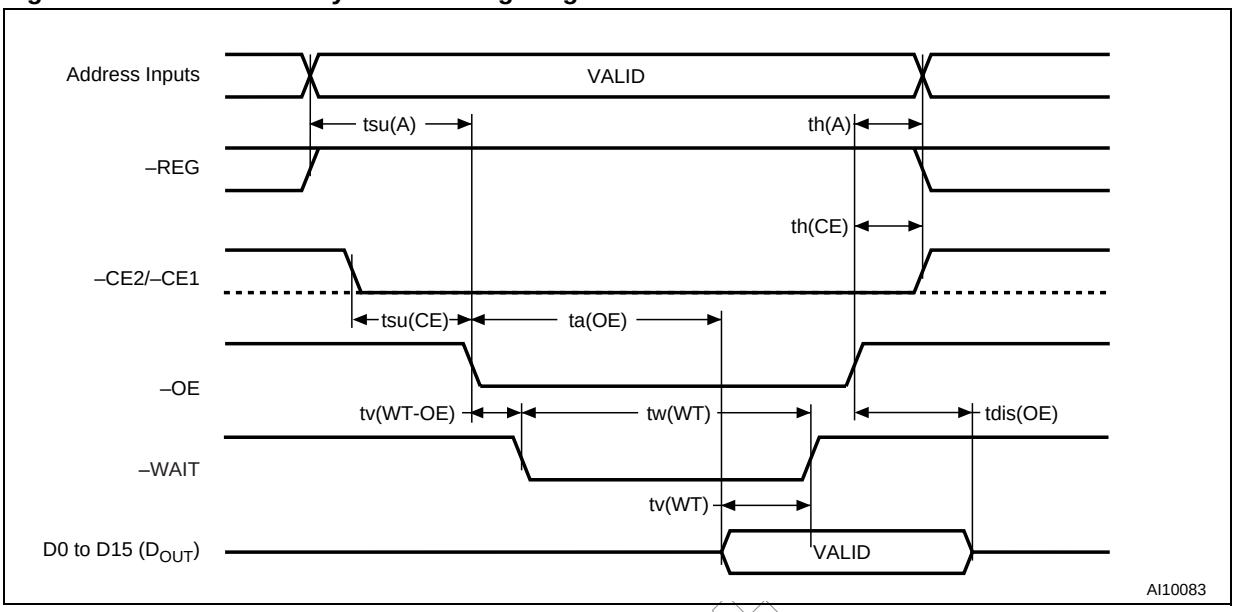


Note: D_{IN} signifies data provided by the system to the CompactFlash Card or CF+ Card.

Table 16. Configuration Register (Attribute Memory) Write Timing

Symbol	IEEE Symbol	Parameter	Min	Max	Unit
tc(W)	t_{AVAV}	Write Cycle Time	250		ns
tw(WE)	t_{WLWH}	Write Pulse Width	150		ns
tsu(A)	t_{AVWL}	Address Setup Time	30		ns
tsu(D-WEH)	t_{DVWH}	Data Setup Time from WE	80		ns
th(D)	t_{WMDX}	Data Hold Time	30		ns
trec(WE)	t_{WMAX}	Write Recovery Time	30		ns

Figure 5. Common Memory Read Timing Diagram



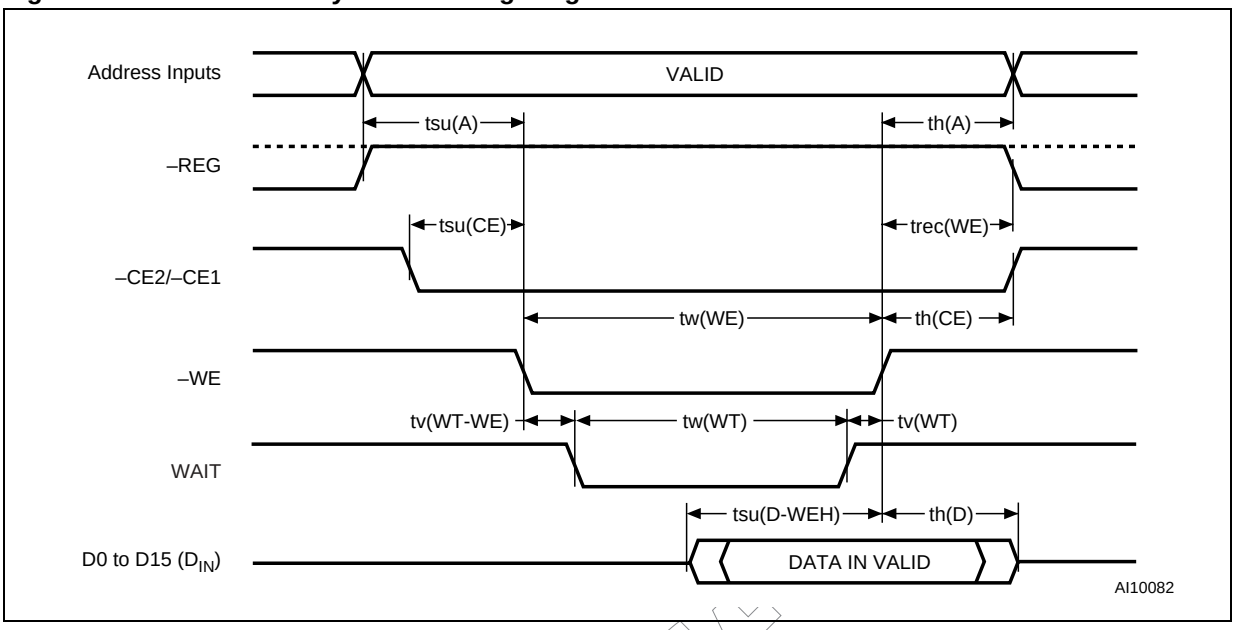
Note: D_{OUT} means data provided by the CompactFlash Memory Card or CF+ Card to the system.

Table 17. Common Memory Read Timing

Symbol	IEEE Symbol	Parameter	Min	Max	Unit
ta(OE)	t_{GLQV}	Output Enable Access Time		125	ns
tdis(OE)	t_{GHQZ}	Output Disable Time from OE		100	ns
tsu(A)	t_{AVGL}	Address Setup Time	30		ns
th(A)	t_{GHAX}	Address Hold Time	20		ns
tsu(CE)	t_{ELGL}	CE Setup Time	0		ns
th(CE)	t_{GHEH}	CE Hold Time	20		ns
tv(WT-OE)	t_{GLWTV}	Wait Delay Falling from OE		35	ns
tv(WT)	t_{QVWTH}	Data Setup for Wait Release		0	ns
tw(WT)	t_{WTLWTH}	Wait Width Time		350 (3000 for CF+)	ns

Note: The maximum load on -WAIT is 1 LSTTL with 50pF total load. The -WAIT signal may be ignored if the -OE cycle to cycle time is greater than the Wait Width time. The Max Wait Width time can be determined from the Card Information Structure. The Wait Width time meets the PCMCIA specification of 12µs but is intentionally less in this specification.

Figure 6. Common Memory Write Timing Diagram



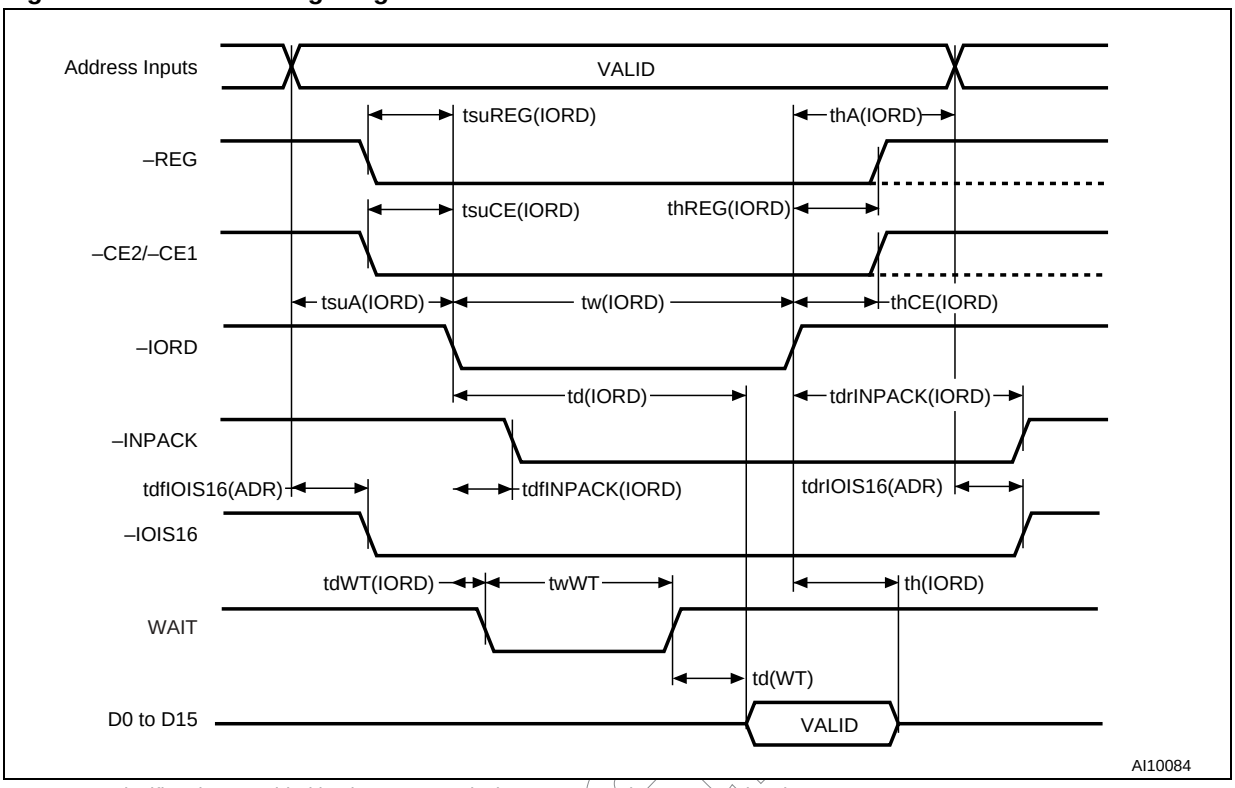
Note: D_{IN} signifies data provided by the system to the CompactFlash Memory Card.

Table 18. Common Memory Write Timing

Symbol	IEEE Symbol	Parameter	Min	Max	Unit
tsu(D-WEH)	t_{DVWH}	Data Setup Time from WE	80		ns
th(D)	t_{WMDX}	Data Hold Time	30		ns
tw(WE)	t_{WLWH}	WE Pulse Width	150		ns
tsu(A)	t_{AVGL}	Address Setup Time	30		ns
tsu(CE)	t_{ELWL}	CE Setup Time before WE	0		ns
trec(WE)	t_{WMAX}	Write Recovery Time	30		ns
th(A)	t_{GHAX}	Address Hold Time	20		ns
th(CE)	t_{GHEH}	CE Hold following WE	20		ns
tv(WT-WE)	t_{WLWTV}	Wait Delay Falling from WE		35	ns
tv(WT)	t_{WTHWH}	WE High from Wait Release	0		ns
tw(WT)	t_{WTLWTH}	Wait Width Time		350	ns

Note: The maximum load on -WAIT is 1 LSTTL with 50 pF total load. The -WAIT signal may be ignored if the -WE cycle to cycle time is greater than the Wait Width time. The Max Wait Width time can be determined from the Card Information Structure. The Wait Width time meets the PCMCIA specification of 12µs but is intentionally less in this specification.

Figure 7. I/O Read Timing Diagram



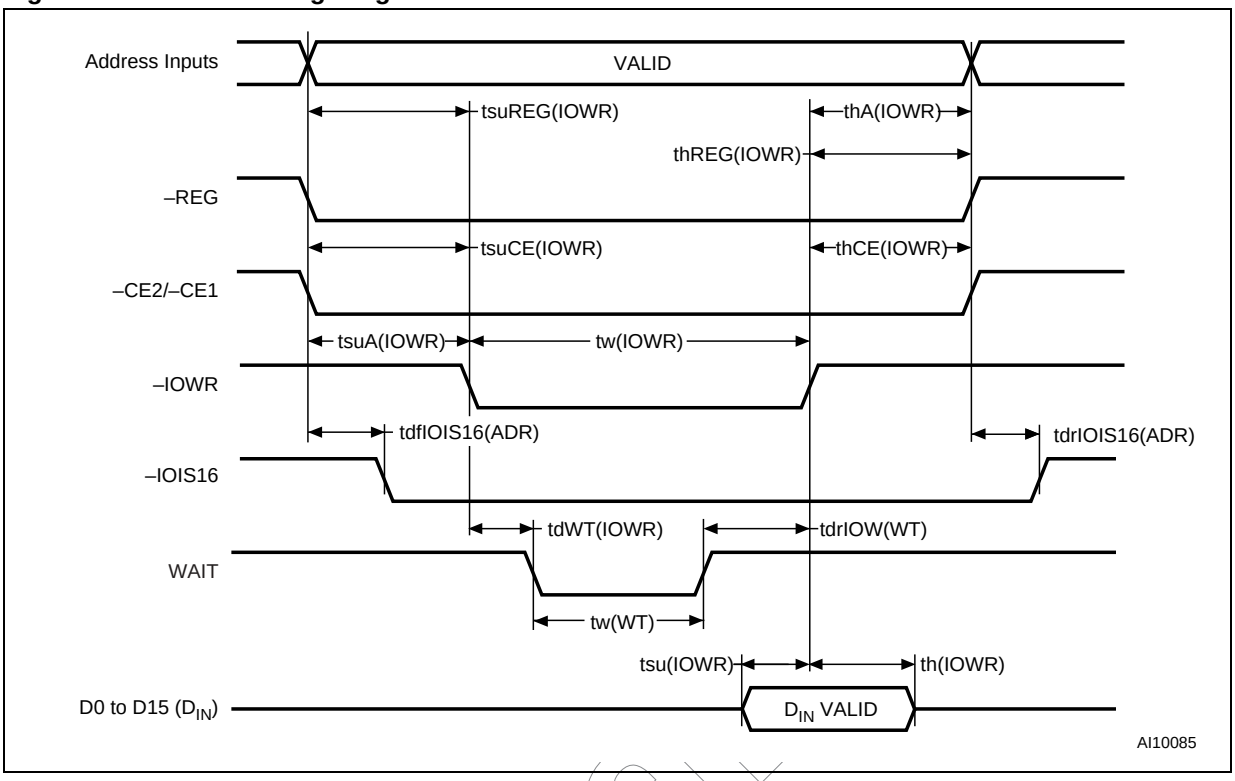
Note: D_{OUT} signifies data provided by the CompactFlash Memory Card or CF+ Card to the system.

Table 19. I/O Read Timing

Symbol	IEEE Symbol	Parameter	Min	Max	Unit
td(IORD)	t_{IGLQV}	Data Delay after IORD		100	ns
th(IORD)	t_{IGHQX}	Data Hold following IORD	0		ns
tw(IORD)	t_{IGLIGH}	IORD Width Time	165		ns
tsuA(IORD)	t_{AVIGL}	Address Setup before IORD	70		ns
thA(IORD)	t_{IGHAX}	Address Hold following IORD	20		ns
tsuCE(IORD)	t_{ELIGL}	CE Setup before IORD	5		ns
thCE(IORD)	t_{IGHEH}	CE Hold following IORD	20		ns
tsuREG(IORD)	t_{RGLIGL}	REG Setup before IORD	5		ns
thREG(IORD)	t_{IGHRGH}	REG Hold following IORD	0		ns
tdfINPACK(IORD)	t_{IGLIAL}	INPACK Delay Falling from IORD	0	45	ns
tdrINPACK(IORD)	t_{IGHIAH}	INPACK Delay Rising from IORD		45	ns
tdfIOIS16(A)	t_{AVISL}	IOIS16 Delay Falling from Address		35	ns
tdrIOIS16(A)	t_{AVISH}	IOIS16 Delay Rising from Address		35	ns
tdWT(IORD)	t_{IGLWTL}	Wait Delay Falling from IORD		35	ns
td(WT)	t_{WTHQV}	Data Delay from Wait Rising		0	ns
tw(WT)	t_{WTLWTH}	Wait Width Time		350 (3000 for CF+)	ns

Note: Maximum load on -WAIT, -INPACK and -IOIS16 is 1 LSTTL with 50 pF total load.Minimum time from -WAIT High to -IORD High is 0ns, but minimum -IORD width must still be met. Wait Width time meets PCMCIA specification of 12µs but is intentionally less in this spec.

Figure 8. I/O Write Timing Diagram



Note: D_{IN} signifies data provided by the system to the CompactFlash Memory Card or CF+ Card.

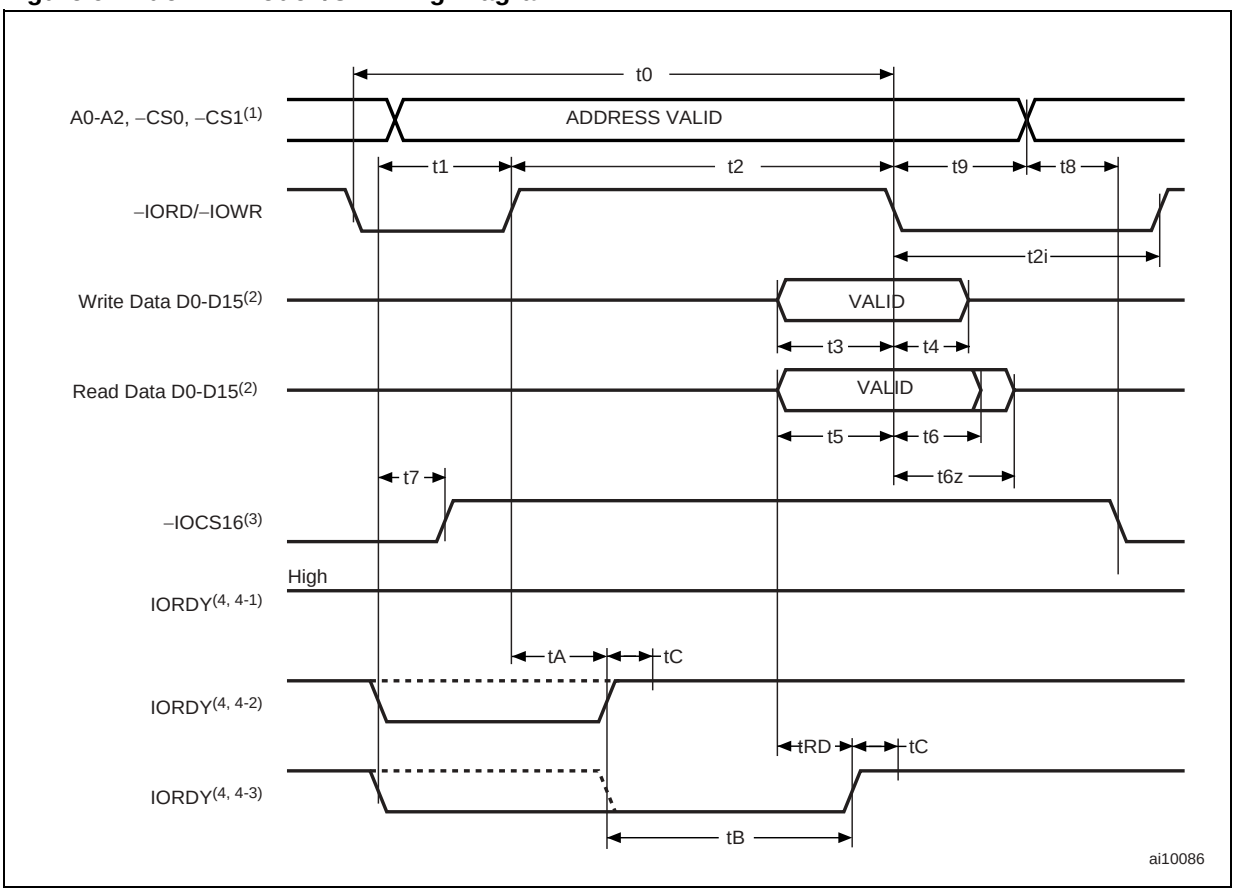
Table 20. I/O Write Timing

Symbol	IEEE Symbol	Parameter	Min. (ns)	Max. (ns)	Unit
tsu(IOWR)	t_{QVIWH}	Data Setup before IOWR	60		ns
th(IOWR)	t_{IWHQX}	Data Hold following IOWR	30		ns
tw(IOWR)	t_{IWLIWH}	IOWR Width Time	165		ns
tsuA(IOWR)	t_{AVIWL}	Address Setup before IOWR	70		ns
thA(IOWR)	t_{IWHAX}	Address Hold following IOWR	20		ns
tsuCE(IOWR)	t_{ELIWL}	CE Setup before IOWR	5		ns
thCE(IOWR)	t_{IWHEH}	CE Hold following IOWR	20		ns
tsuREG(IOWR)	t_{RGLIWL}	REG Setup before IOWR	5		ns
thREG(IOWR)	t_{IWHRGH}	REG Hold following IOWR	0		ns
tdfIOIS16(A)	t_{AVISL}	IOIS16 Delay Falling from Address		35	ns
tdrIOIS16(A)	t_{AVISH}	IOIS16 Delay Rising from Address		35	ns
tdWT(IOWR)	t_{IWLWTL}	Wait Delay Falling from IOWR		35	ns
tdrIOWR(WT)	t_{WTHIWH}	IOWR High from Wait High	0		ns
tw(WT)	t_{WTLWTH}	Wait Width Time		350 (3000 for CF+)	ns

Note: The maximum load on -WAIT, -INPACK, and -IOIS16 is 1 LSTTL with 50pF total load. Minimum time from -WAIT High to -IOWR High is 0 ns, but minimum -IOWR width must still be met. The Wait Width time meets the PCMCIA specification of 12 µs but is intentionally less in this specification.

The timing diagram for True IDE mode of operation in this section is drawn using the conventions in the ATA-4 specification, which are different than the conventions used in the PCMCIA specification and earlier versions of this specification. Signals are shown with their asserted state as High regardless of whether the signal is actually negative or positive true. Consequently, the -IORD, the -IOWR and the -IOCS16 signals are shown in the diagram inverted from their electrical states on the bus.

Figure 9. True IDE Mode I/O Timing Diagram



Note: 1. The device addresses consists of –CS0, –CS1, and A2-A0.
2. The Data I/O consist of D15-D0 (16-bit) or D7-D0 (8 bit).
3. –IOCS16 is shown for PIO modes 0, 1 and 2. For other modes, this signal is ignored.
4. The device drives IORDY Low to extend the PIO cycle. The determination of whether the cycle is to be extended is made by the host t_A after –IORD or –IOWR has been asserted. IORDY can be asserted and de-asserted as described in the following three cases:
(4-1) The device never drives IORDY Low (IORDY remains asserted): No wait is generated.
(4-2) The device starts to drive IORDY Low before/during t_A, but re-asserts IORDY before t_A has elapsed. No wait is generated.
(4-3) The device drives IORDY Low before/during t_A and IORDY remains Low after t_A has elapsed: a wait is generated. The cycle completes after IORDY is re-asserted. For cycles where a wait is generated and –IORD is asserted, the device must place the read data on D15-D0 t_{RD} before re-asserting IORDY.

Table 21. True IDE Mode I/O Read/Write Timing Diagram

Symbol	Parameter(1)	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Unit
t_0(2)	Cycle time (min)	600	383	240	180	120	ns
t_1	Address Valid to -IORD/-IOWR setup (min)	70	50	30	30	25	ns
t_2(2)	-IORD/-IOWR (min)	165	125	100	80	70	ns
t_2(2)	-IORD/-IOWR (min) Register (8 bit)	290	290	290	80	70	ns
t_{2i}(2)	-IORD/-IOWR recovery time (min)	-	-	-	70	25	ns
t_3	-IOWR data setup (min)	60	45	30	30	20	ns
t_4	-IOWR data hold (min)	30	20	15	10	10	ns
t_5	-IORD data setup (min)	50	35	20	20	20	ns
t_6	-IORD data hold (min)	5	5	5	5	5	ns
t_{6Z}(3)	-IORD data tri-state (max)	30	30	30	30	30	ns
t_7(5)	Address valid to -IOCS16 assertion (max)	90	50	40	N/A	N/A	ns
t_8(5)	Address valid to -IOCS16 released (max)	60	45	30	N/A	N/A	ns
t_9	-IORD/-IOWR to address valid hold	20	15	10	10	10	ns
t_{RD}	Read Data Valid to IORDY active (min), if IORDY initially Low after t_A	0	0	0	0	0	ns
t_A(4)	IORDY Setup time	35	35	35	35	35	ns
t_B	IORDY Pulse Width (max)	1250	1250	1250	1250	1250	ns
t_C	IORDY assertion to release (max)	5	5	5	5	5	ns

Note: 1. The maximum load on -IOCS16 is 1 LSTTL with a 50pF total load. Minimum time from -IORDY High to -IORD High is 0ns, but minimum -IORD width must still be met.

2. t_0 is the minimum total cycle time, t_2 is the minimum command active time, and t_{2i} is the minimum command recovery time or command inactive time. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t_0, t_2, and t_{2i} have to be met. The minimum total cycle time requirement is greater than the sum of t_2 and t_{2i}. This means a host implementation can lengthen either or both t_2 or t_{2i} to ensure that t_0 is equal to or greater than the value reported in the device's identify drive data. A CompactFlash Memory Card implementation should support any legal host implementation.
3. This parameter specifies the time from the falling edge of –IORD to the moment when the data bus is no longer driven by the CompactFlash Memory Card (tri-state).
4. The delay from the activation of –IORD or –IOWR to the first time the state of IORDY is sampled. If IORDY is inactive then the host will have to wait until IORDY is active before the PIO cycle can be completed. If the CompactFlash Memory Card is not driving IORDY Low during t_A after the activation of –IORD or –IOWR, then t_5 shall be met and t_{RD} is not applicable. If the CompactFlash Memory Card is driving IORDY Low during t_A after the activation of –IORD or –IOWR, then t_{RD} shall be met and t_5 is not applicable.
5. t_7 and t_8 apply only to modes 0, 1 and 2. This signal is not valid for other modes.

Card Configuration

The CompactFlash Memory Card is identified by information in the Card Information Structure (CIS). The Card has four configuration registers (Tables 22 and 23).

- Configuration Option Register
- Pin Replacement Register
- Card Configuration and Status Register
- Socket and Copy Register

They are used to coordinate the I/O spaces and the Interrupt level of cards that are located in the system. In addition, in I/O card mode these registers provide a method for accessing status information that would normally appear on dedicated pins in memory card mode. The location of the card configuration registers should always be read from the CIS.These registers cannot be used in True IDE mode.

No writes should be performed to the attribute memory except to the configuration register addresses. All other attribute memory locations are reserved. See the section 'Attribute Memory Function'.

Table 22. CompactFlash Memory Card Registers and Memory Space Decoding

–CE2	–CE1	–REG	–OE	–WE	A10	A9	A8-A4	A3	A2	A1	A0	Selected Space
1	1	X	X	X	X	X	XXX	XX	X	X	X	Standby
X	0	0	0	1	0	1	XXX	XX	X	X	0	Configuration Registers Read
1	0	1	0	1	X	X	XXX	XX	X	X	X	Common Memory Read (D7 to D0)
0	1	1	0	1	X	X	XXX	XX	X	X	X	Common Memory Read (D15 to D8)
0	0	1	0	1	X	X	XXX	XX	X	X	0	Common Memory Read (D15 to D0)
X	0	0	1	0	0	1	XXX	XX	X	X	0	Configuration Registers Write
1	0	1	1	0	X	X	XXX	XX	X	X	X	Common Memory Write (D7 to D0)
0	1	1	1	0	X	X	XXX	XX	X	X	X	Common Memory Write (D15 to D8)
0	0	1	1	0	X	X	XXX	XX	X	X	0	Common Memory Write (D15 to D0)
X	0	0	0	1	0	0	XXX	XX	X	X	0	Card Information Structure Read
1	0	0	1	0	0	0	XXX	XX	X	X	0	Invalid Access (CIS Write)
1	0	0	0	1	X	X	XXX	XX	X	X	1	Invalid Access (Odd Attribute Read)
1	0	0	1	0	X	X	XXX	XX	X	X	1	Invalid Access (Odd Attribute Write)
0	1	0	0	1	X	X	XXX	XX	X	X	X	Invalid Access (Odd Attribute Read)
0	1	0	1	0	X	X	XXX	XX	X	X	X	Invalid Access (Odd Attribute Write)

Table 23. CompactFlash Memory Card Configuration Registers Decoding

–CE2	–CE1	–REG	–OE	–WE	A10	A9	A8-A4	A3	A2	A1	A0	Selected Register
X	0	0	0	1	0	1	00	0	0	0	0	Configuration Option Register Read
X	0	0	1	0	0	1	00	0	0	0	0	Configuration Option Register Write
X	0	0	0	1	0	1	00	0	0	1	0	Card Status Register Read
X	0	0	1	0	0	1	00	0	0	1	0	Card Status Register Write
X	0	0	0	1	0	1	00	0	1	0	0	Pin Replacement Register Read
X	0	0	1	0	0	1	00	0	1	0	0	Pin Replacement Register Write
X	0	0	0	1	0	1	00	0	1	1	0	Socket and Copy Register Read
X	0	0	1	0	0	1	00	0	1	1	0	Socket and Copy Register Write

Configuration Option Register (Base + 00h in Attribute Memory)

The Configuration Option Register is used to configure the Card's interface, address decoding and interrupt to the Card (see Table 24.).

Conf5 - Conf0 (Configuration Index). These bits are used to select the operation mode of the Card as shown in Table 25.. This bit is set to '0' by Reset.

Table 24. Configuration Option Register (default value: 00h)

Operation	D7	D6	D5	D4	D3	D2	D1	D0
R/W	X	LevlREQ	Conf5	Conf4	Conf3	Conf2	Conf1	Conf0

Table 25. CompactFlash Memory Card Configurations

Conf5	Conf4	Conf3	Conf2	Conf1	Conf0	Mapping Mode	Card Mode	Task File Register Address
0	0	0	0	0	0	Memory	Memory	0h - Fh, 400h - 7FFh
0	0	0	0	0	1	Contiguous I/O	I/O	xx0h - xxFh
0	0	0	0	1	0	Primary I/O	I/O	1F0h - 1F7h, 3F6h - 3F7h
0	0	0	0	1	1	Secondary I/O	I/O	170h - 177h, 376h - 377h

Card Configuration and Status Register (Base + 02h in Attribute Memory)

The Card Configuration and Status Register contains information about the Card's status (see Table 26.).

Changed. Indicates that one or both of the Pin Replacement register (CRDY, or CWProt) bits are set to '1'. When the Changed bit is set, –STSCHG (Pin 46) is held Low and if the SigChg bit is '1' the Card is configured for the I/O interface.

SigChg. This bit is set and reset by the host to enable and disable a state-change signal from the Status Register (issued on Status Changed pin 46). If no state change signal is desired, this bit should be set '0' and pin 46 (–STSCHG) will be held High while the Card is configured for I/O.

IOis8. The host sets this bit to '1' if the Card is to be configured in 8 bit I/O Mode. The Card is always configured for both 8 and 16 bit I/O, so this bit is ignored.

-XE. This bit is set and reset by the host to disable and enable Power Level 1 commands in CF+ cards. In the Compact Flash Card this bit has value '0' and is not writable.

Audio. This bit is set and reset by the host to enable and disable audio information on -SPKR when the CF+ card is configured. This bit should always be '0' for CompactFlash Memory Cards.

PwrDwn. This bit indicates whether the Card is in the power saving mode or active mode. When the PwrDwn bit is set to '1', the Card enters power down mode. When set to '0', the Card enters active mode. The READY value on Pin Replacement Register becomes BUSY when this bit is changed. READY will not become Ready until the power state requested has been entered. The Card automatically powers down when it is idle and powers back up when it receives a command.

Int. This bit represents the internal state of the interrupt request. It is available whether or not the I/O interface has been configured. It remains valid until the condition which caused the interrupt request has been serviced. If interrupts are disabled by the –IEN bit in the Device Control Register, this bit is '0'.

Table 26. Card Configuration and Status Register (default value: 00h)

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	Changed	SigChg	IOIS8	-XE	Audio	PwrDwn	Int	0
Write	0	SigChg	IOIS8	-XE	Audio	PwrDwn	0	0

Pin Replacement Register (Base + 04h in Attribute Memory)

This register contains information on the state of the READY signal when configured in memory mode and the IREQ signal in I/O mode. See Tables 27 and 28.

CReady. This bit is set to '1' when the bit RReady changes state. This bit can also be written by the host.

CWProt. This bit is set to '1' when the bit RWProt changes state. This bit can also be written by the host.

RReady. This bit is used to determine the internal state of the Ready signal. In I/O mode it is used as an interrupt request. When written, this bit acts as a mask (MReady) for writing the corresponding bit CReady.

WProt. This bit is always '0' since the CompactFlash Memory Card or CF+ Card does not have a Write Protect switch. When written, this bit acts as a mask for writing the corresponding CWProt bit.

MReady. This bit acts as a mask for writing the corresponding CReady bit.

MWProt. This bit when written acts as a mask for writing the corresponding CWProt bit.

Table 27. Pin Replacement Register (default value: 0Ch)

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	0	0	CReady	CWProt	1	1	RReady	WProt
Write	0	0	CReady	CWProt	0	0	RReady	MWProt

Table 28. Pin Replacement Changed Bit/Mask Bit Values

Initial Value of 'C' Status	Written by Host		Final 'C' Bit	Comments
	'C' Bit	'M' Bit		
0	X	0	0	Unchanged
1	X	0	1	Unchanged
X	0	1	0	Cleared by Host
X	1	1	1	Set by Host

Socket and Copy Register (Base + 06h in Attribute Memory)

This register contains additional configuration information which identifies the Card from other cards. This register is always written by the system before writing the Configuration Option Register (see Table 29.).

Drive # This value can be used to address two different cards in the case of twin card configuration.

X. the socket number is ignored by the card.

Table 29. Socket and Copy Register (default value: 00h)

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	Reserved	0	0	Drive #	0	0	0	0
Write	0	0	0	Drive #	X	X	X	X

Attribute Memory Function

Attribute memory is a space where identification and configuration information are stored, and is limited to 8 bit wide accesses at even addresses. The card configuration registers are also located here, the base address of the configuration registers is 200h.

For the Attribute Memory Read function, signals –REG and –OE must be active and –WE inactive during the cycle. As in the Main Memory Read functions, the signals –CE1 and –CE2 control the even and odd Byte address, but only the even Byte data is valid during the Attribute Memory access. Refer to Table 30. for signal states and bus validity.

Table 30. Attribute Memory Function

Function Mode	–REG	–CE2	–CE1	A10	A9	A0	–OE	–WE	D15 to D8	D7 to D0
Standby	X	H	H	X	X	X	X	X	High-Z	High-Z
Read Byte Access CIS (8 bits)	L	H	L	L	L	L	L	H	High-Z	Even Byte
Write Byte Access CIS (8 bits) Invalid	L	H	L	L	L	L	H	L	Don't Care	Even Byte
Read Byte Access Configuration (8 bits)	L	H	L	L	H	L	L	H	High-Z	Even Byte
Write Byte Access Configuration (8 bits)	L	H	L	L	H	L	H	L	Don't Care	Even Byte
Read Byte Access Configuration CF+ (8 bits)	L	H	L	X	X	L	L	H	High-Z	Even Byte
Write Byte Access Configuration CF+ (8 bits)	L	H	L	X	X	L	H	L	Don't Care	Even Byte
Read Word Access CIS (16 bits)	L	L	L	L	L	X	L	H	Not Valid	Even Byte
Write Word Access CIS (16 bits) Invalid	L	L	L	L	L	X	H	L	Don't Care	Even Byte
Read Word Access Configuration (16 bits)	L	L	L	L	H	X	L	H	Not Valid	Even Byte
Write Word Access Configuration (16 bits)	L	L	L	L	H	X	H	L	Don't Care	Even Byte
Read Word Access Configuration CF+ (16 bits)	L	L	L	X	X	X	L	H	Not Valid	Even Byte
Write Word Access Configuration CF+ (16 bits)	L	L	L	X	X	X	H	L	Don't Care	Even Byte

Note: The –CE signal or both the –OE signal and the –WE signal must be de-asserted between consecutive cycle operations.

I/O Transfer Function

The I/O transfer to or from the Card can be either 8 or 16 bits. When a 16 bit accessible port is addressed, the –IOIS16 signal is asserted by the Card, otherwise it is de-asserted. When a 16 bit transfer is attempted, and the –IOIS16 signal is not asserted, the system must generate a pair of 8 bit references to access the Word's even and odd Bytes. The Card permits both 8 and 16 bit accesses to all of its I/O addresses, so –IOIS16 is asserted for all addresses. The Card may request the host to extend the length of an input cycle until data is ready by first asserting –WAIT (see Table 31.).

Table 31. I/O Function

Function Code	–REG	–CE2	–CE1	A0	–IORD	–IOWR	D15 to D8	D7 to D0
Standby Mode	X	H	H	X	X	X	High Z	High Z
Byte Input Access (8 bits)	L L	H H	L L	L H	L L	H H	High Z High Z	Even Byte Odd Byte
Byte Output Access (8 bits)	L L	H H	L L	L H	H H	L L	Don't Care Don't Care	Even Byte Odd Byte
Word Input Access (16 bits)	L	L	L	L	L	H	Odd Byte	Even Byte
Word Output Access (16 bits)	L	L	L	L	H	L	Odd Byte	Even Byte
I/O Read Inhibit	H	X	X	X	L	H	Don't Care	Don't Care
I/O Write Inhibit	H	X	X	X	H	L	High Z	High Z
High Byte Input Only (8 bits)	L	L	H	X	L	H	Odd Byte	High Z
High Byte Output Only (8 bits)	L	L	H	X	H	L	Odd Byte	Don't Care

Common Memory Transfer Function

The Common Memory transfer to or from the Card permits both 8 or 16 bit access to all of the Common Memory addresses. The Card may request the host to extend the length of a memory read or write cycle by first asserting –WAIT (see Table 32.).

Table 32. Common Memory Function

Function Code	–REG	–CE2	–CE1	A0	–OE	–WE	D15 to D8	D7 to D0
Standby Mode	X	H	H	X	X	X	High Z	High Z
Byte Read Access (8 bits)	H H	H H	L L	L H	L L	H H	High Z High Z	Even Byte Odd Byte
Byte Write Access (8 bits)	H H	H H	L L	L H	H H	L L	Don't Care Don't Care	Even Byte Odd Byte
Word Read Access (16 bits)	H	L	L	X	L	H	Odd Byte	Even Byte
Word Write Access (16 bits)	H	L	L	X	H	L	Odd Byte	Even Byte
Odd Byte Read Only (8 bits)	H	L	H	X	L	H	Odd Byte	High Z
Odd Byte Write Only (8 bits)	H	L	H	X	H	L	Odd Byte	Don't Care

True IDE Mode I/O Function

The Card can be configured in a True IDE Mode of operation. It is configured in this mode only when the –OE signal is grounded by the host during the power off to power on cycle. In this True IDE Mode the PCMCIA protocol and configuration are disabled and only I/O operations to the Task File and Data Register are allowed. No Memory or Attribute Registers are accessible to the host. The Set Feature Command can be used to put the device in 8 bit Mode (see Table 33.).

Removing and reinserting the Card while the host computer's power is on will reconfigure the Card to PC Card ATA mode.

Table 33. True IDE Mode I/O Function

Function Code	–CE2	–CE1	A2 to A0	–IORD	–IOWR	D15 to D8	D7 to D0
Invalid Mode	L	L	X	X	X	High Z	High Z
Standby Mode	H	H	X	X	X	High Z	High Z
Task File Write	H	L	1h-7h	H	L	Don't Care	Data In
Task File Read	H	L	1h-7h	L	H	High Z	Data Out
Data Register Write	H	L	L	H	L	Odd-Byte In	Even-Byte In
Data Register Read	H	L	L	L	H	Odd-Byte Out	Even-Byte Out
Control Register Write	L	H	6h	H	L	Don't Care	Control In
Alternate Status Read	L	H	6h	L	H	High Z	Status Out
Drive Address	L	H	7h	L	H	High Z	Data Out

METAFORMAT

Metaformat Overview

The goal of the Metaformat is to describe the requirements and capabilities of the CompactFlash Memory Card and CF+ Card as thoroughly as possible. This includes describing the power requirements, IO requirements, memory requirements, manufacturer information and details about the services provided.

The Metaformat is a hierarchy of layers where each layer is numbered with a number that increases with the level of abstraction.

Layers are also provided to describe the data recording format and data organization, for memory and ATA cards that wish to adhere to the CFA/PCMCIA specification.

Below the Metaformat there is the physical layer, which describes the electrical and physical characteristics of CF+ Cards.

The CF+ Metaformat conforms directly to the PCMCIA Metaformat Specification. Refer to that document for a detailed description of the Metaformat.

Metaformat Requirements

CF+ Cards have the following Card Information Structure (CIS) requirements:

- All CF+ Cards have a CIS that describes the functionality and characteristics of the card.
- It should be possible to read the CIS of a CF+ Card whenever the card is powered, READY is being asserted and the card has been reset by the host after power-up in accordance with the CompactFlash Standard. This includes after the CF+ Card is configured and when the PwrDwn bit is set in the Card Configuration and Status Register. (See the Electrical Specification section.)
- All CF+ Cards should provide at least the mandatory Tuples as described in the PCMCIA Metaformat Specification, Tuple Summary Table.
- All linear memory CF+ Cards should describe how they are partitioned, even if the entire CF+ Card is used as a single partition.

SOFTWARE INTERFACE

CF-ATA Drive Register Set Definition and Protocol

The CompactFlash Memory Card can be configured as a high performance I/O device through:

- Standard PC-AT disk I/O address spaces
  - 1F0h-1F7h, 3F6h-3F7h (primary);
  - 170h-177h, 376h-377h (secondary) with IRQ 14 (or other available IRQ).
- Any system decoded 16 Byte I/O block using any available IRQ.
- Memory space.

Communication to or from the Card is done using the Task File registers which provide all the necessary registers for control and status information. The PCMCIA interface connects peripherals to the host using four-register mapping methods. Table 33. is a detailed description of these methods:

Table 34. I/O Configurations

Standards Configurations			
Config Index	**I/O or Memory**	**Address**	**Description**
0	Memory	0h-Fh, 400h-7FFh	Memory Mapped
1	I/O	xx0h-xxFh	I/O Mapped 16 Continuous Registers
2	I/O	1F0-1F7h, 3F6h-3F7h	Primary I/O Mapped
3	I/O	170-177h, 376h-377h	Secondary I/O Mapped

Memory Mapped Addressing (Conf = 0)

When the Card registers are accessed via memory references, the registers appear in the common memory space window: 0-2KBytes as shown in Table 35. This window accesses the Data Register FIFO. It does not allow random access to the data buffer within the Card.

Register 0 is accessed with –CE1 and –CE2 Low, as a Word register on the combined Odd and Even Data Bus (D15 to D0). It can also be accessed with –CE1 Low and –CE2 High, by a pair of Byte accesses to offset 0. The address space of this Word register overlaps the address space of the Error and Feature Bytewide registers at offset 1. When accessed twice as Byte register with –CE1 Low, the first Byte is the even Byte of the Word and the second is the odd Byte. A Byte access to address 0 with –CE1 High and –CE2 Low accesses the Error (read) or Feature (write) register.

Registers at offset 8, 9 and D are non-overlapping duplicates of the registers at offset 0 and 1. Register 8 is equivalent to register 0, while register 9 accesses the odd Byte. Therefore, if the registers are Byte accessed in the order 9 then 8 the data will be transferred odd Byte then even Byte. Repeated Byte accesses to register 8 or 0 will access consecutive (even then odd) Bytes from the data buffer. Repeated Word accesses to register 8, 9 or 0 will access consecutive Words from the data buffer, however repeated Byte accesses to register 9 are not supported. Repeated alternating Byte accesses to registers 8 then 9 will access consecutive (even then odd) Bytes from the data buffer.

Accesses to even addresses between 400h and 7FFh access register 8. Accesses to odd addresses between 400h and 7FFh access register 9. This 1 KByte memory window to the data register is provided so that hosts can perform memory-to-memory block moves to the data register when the register lies in memory space. Some hosts, such as the X86 processors, must increment both the source and destination addresses when executing the memory-to-memory block move instruction. Some PCMCIA socket adapters also have an embedded auto incrementing address logic.

A Word access to address at offset 8 will provide even data on the least significant Byte of the data bus, along with odd data at offset 9 on the most significant Byte of the data bus.

Table 35. Memory Mapped Decoding

–REG	A10	A9 to A4	A3	A2	A1	A0	Offset	–OE=0	–WE=0
1	0	X	0	0	0	0	0h	Even Data Register	Even Data Register
1	0	X	0	0	0	1	1h	Error Register	Feature Register
1	0	X	0	0	1	0	2h	Sector Count Register	Sector Count Register
1	0	X	0	0	1	1	3h	Sector Number Register	Sector Number Register
1	0	X	0	1	0	0	4h	Cylinder Low Register	Cylinder Low Register
1	0	X	0	1	0	1	5h	Cylinder High Register	Cylinder High Register
1	0	X	0	1	1	0	6h	Select Card/Head Register	Select Card/Head Register
1	0	X	0	1	1	1	7h	Status Register	Command Register
1	0	X	1	0	0	0	8h	Dup. Even Data Register	Dup. Even Data Register
1	0	X	1	0	0	1	9h	Dup. Odd Data Register	Dup. Odd Data Register
1	0	X	1	1	0	1	Dh	Dup. Error Register	Dup. Feature Register
1	0	X	1	1	1	0	Eh	Alternate Status Register	Device Control Register
1	0	X	1	1	1	1	Fh	Drive Address Register	Reserved
1	1	X	X	X	X	0	8h	Even Data Register	Even Data Register
1	1	X	X	X	X	1	9h	Odd Data Register	Odd Data Register

Contiguous I/O Mapped Addressing (Conf = 1)

When the system decodes a contiguous block of I/O registers to select the Card, the registers are accessed in the block of I/O space decoded by the system as shown in Table 36.

As for the Memory Mapped Addressing, register 0 is accessed with –CE1 Low and –CE2 Low (and A0 don't Care) as a Word register on the combined Odd and Even Data Bus (D15 to D0). This register may also be accessed with –CE1 Low and –CE2 High, by a pair of Byte accesses to offset 0. The address space of this Word register overlaps the address space of the Error and Feature Bytewide registers at offset 1. When accessed twice as Byte register with –CE1 Low, the first Byte is the even Byte of the Word and the second is the odd Byte. A Byte access to register 0 with –CE1 High and –CE2 Low accesses the error (read) or feature (write) register.

Registers at offset 8, 9 and D are non-overlapping duplicates of the registers at offset 0 and 1. Register 8 is equivalent to register 0, while register 9 accesses the odd Byte. Therefore, if the registers are Byte accessed in the order 9 then 8 the data will be transferred odd Byte then even Byte. Repeated Byte accesses to register 8 or 0 will access consecutive (even than odd) Bytes from the data buffer. Repeated Word accesses to register 8, 9 or 0 will access consecutive Words from the data buffer, however repeated Byte accesses to register 9 are not supported. Repeated alternating Byte accesses to registers 8 then 9 will access consecutive (even then odd) Bytes from the data buffer.

Table 36. Contiguous I/O Decoding

–REG	A10 to A4	A3	A2	A1	A0	Offset	–IORD=0	–IOWR=0
0	X	0	0	0	0	0h	Even Data Register	Even Data Register
0	X	0	0	0	1	1h	Error Register	Feature Register
0	X	0	0	1	0	2h	Sector Count Register	Sector Count Register
0	X	0	0	1	1	3h	Sector Number Register	Sector Number Register
0	X	0	1	0	0	4h	Cylinder Low Register	Cylinder Low Register
0	X	0	1	0	1	5h	Cylinder High Register	Cylinder High Register
0	X	0	1	1	0	6h	Select Card/Head Register	Select Card/Head Register
0	X	0	1	1	1	7h	Status Register	Command Register
0	X	1	0	0	0	8h	Dup. Even Data Register	Dup. Even Data Register
0	X	1	0	0	1	9h	Dup. Odd Data Register	Dup. Odd Data Register
0	X	1	1	0	1	Dh	Dup. Error Register	Dup. Feature Register
0	X	1	1	1	0	Eh	Alternate Status Register	Device Control Register
0	X	1	1	1	1	Fh	Drive Address Register	Reserved

I/O Primary and Secondary Address Configurations (Conf = 2,3)

When the system decodes the Primary and Secondary Address Configurations, the registers are accessed in the block of I/O space as shown in Table 37.

As for the Memory Mapped Addressing, register 0 is accessed with –CE1 Low and –CE2 Low (and A0 don't Care) as a Word register on the combined Odd and Even Data Bus (D15 to D0). This register may also be accessed with –CE1 Low and –CE2 High, by a pair of Byte accesses to offset 0. The address space of this Word register overlaps the address space of the Error and Feature Bytewide registers at offset 1. When accessed twice as Byte register with –CE1 Low, the first Byte is the even Byte of the Word and the second is the odd Byte. A Byte access to register 0 with –CE1 High and –CE2 Low accesses the error (read) or feature (write) register.

Table 37. Primary and Secondary I/O Decoding

–REG	A9 to A4	A3	A2	A1	A0	–IORD=0	–IOWR=0
0	1F(17)h	0	0	0	0	Even Data Register	Even Data Register
0	1F(17)h	0	0	0	1	Error Register	Feature Register
0	1F(17)h	0	0	1	0	Sector Count Register	Sector Count Register
0	1F(17)h	0	0	1	1	Sector Number Register	Sector Number Register
0	1F(17)h	0	1	0	0	Cylinder Low Register	Cylinder Low Register
0	1F(17)h	0	1	0	1	Cylinder High Register	Cylinder High Register
0	1F(17)h	0	1	1	0	Select Card/Head Register	Select Card/Head Register
0	1F(17)h	0	1	1	1	Status Register	Command Register
0	3F(37)h	0	1	1	0	Alternate Status Register	Device Control Register
0	3F(37)h	0	1	1	1	Drive Address Register	Reserved

True IDE Mode Addressing

When the Card is configured in the True IDE Mode, the I/O decoding is as shown in Table 38.

Table 38. True IDE Mode I/O Decoding

–CE2	–CE1	A2	A1	A0	–IORD=0	–IOWR=0
1	0	0	0	0	Data Register	Data Register
1	0	0	0	1	Error Register	Feature Register
1	0	0	1	0	Sector Count Register	Sector Count Register
1	0	0	1	1	Sector Number Register	Sector Number Register
1	0	1	0	0	Cylinder Low Register	Cylinder Low Register
1	0	1	0	1	Cylinder High Register	Cylinder High Register
1	0	1	1	0	Select Card/Head Register	Select Card/Head Register
1	0	1	1	1	Status Register	Command Register
0	1	1	1	0	Alternate Status Register	Device Control Register
0	1	1	1	1	Drive Address	Reserved

CF-ATA REGISTERS

The following section describes the hardware registers used by the host software to issue commands to the Card. These registers are collectively referred to as the 'task file'.

Data Register (Address 1F0h [170h]; Offset 0, 8, 9)

The Data Register is a 16 bit register used to transfer data blocks between the Card data buffer and the Host. This register overlaps the Error Register. Table 39. describes the combinations of Data register access and explains the overlapped Data and Error/Feature Registers. Because of the overlapped registers, access to the 1F1h, 171h or offset 1 are not defined for Word (–CE2 and –CE1 set to '0') operations, and are treated as accesses to the Word Data Register. The duplicated registers at offsets 8, 9 and Dh have no restrictions on the operations that can be performed.

Table 39. Data Register Access

Data Register	–CE2	–CE1	A0	Offset	Data Bus
Word Data Register	0	0	X	0, 8, 9	D15 to D0
Even Data Register	1	0	0	0, 8	D7 to D0
Odd Data Register	1	0	1	9	D7 to D0
Odd Data Register	0	1	X	8, 9	D15 to D8
Error/Feature Register	1	0	1	1, Dh	D7 to D0
Error/Feature Register	0	1	X	1	D15 to D8
Error/Feature Register	0	0	X	Dh	D15 to D8

Error Register (Address 1F1h [171h]; Offset 1, 0Dh Read Only)

This read only register contains additional information about the source of an error when an error is indicated in bit 0 of the Status register. The bits are defined in Table 40. This register is accessed on data bits D15 to D8 during a write operation to offset 0 with –CE2 Low and –CE1 High.

Bit 7 (BBK). This bit is set when a Bad Block is detected.

Bit 6 (UNC). This bit is set when an Uncorrectable Error is encountered.

Bit 5. This bit is '0'.

Bit 4 (IDNF). This bit is set if the requested sector ID is in error or cannot be found.

Bit 3. This bit is '0'.

Bit 2 (Abort). This bit is set if the command has been aborted because of a Card status condition (Not Ready, Write Fault, etc.) or when an invalid command has been issued.

Bit 1. This bit is '0'.

Bit 0 (AMNF). This bit is set when there is a general error.

Table 40. Error Register

D7	D6	D5	D4	D3	D2	D1	D0
BBK	UNC	0	IDNF	0	ABRT	0	AMNF

Feature Register (Address 1F1h [171h]; Offset 1, 0Dh Write Only)

This write-only register provides information on features that the host can utilize. It is accessed on data bits D15 to D8 during a write operation to Offset 0 with –CE2 Low and –CE1 High.

Sector Count Register (Address 1F2h [172h]; Offset 2)

This register contains the number of sectors of data to be transferred on a read or write operation between the host and Card. If the value in this register is zero, a count of 256 sectors is specified. If the command was successful, this register is zero at completion. If not successfully completed, the register contains the number of sectors that need to be transferred in order to complete the request. The default value is 01h.

Sector Number (LBA 7-0) Register (Address 1F3h [173h]; Offset 3)

This register contains the starting sector number or bits 7 to 0 of the Logical Block Address (LBA), for any data access for the subsequent sector transfer command.

Cylinder Low (LBA 15-8) Register (Address 1F4h [174h]; Offset 4)

This register contains the least significant 8 bits of the starting cylinder address or bits 15 to 8 of the Logical Block Address.

Cylinder High (LBA 23-16) Register (Address 1F5h [175h]; Offset 5)

This register contains the most significant bits of the starting cylinder address or bits 23 to 16 of the Logical Block Address.

Drive/Head (LBA 27-24) Register (Address 1F6h [176h]; Offset 6)

The Drive/Head register is used to select the drive and head. It is also used to select LBA addressing instead of cylinder/head/sector addressing. The bits are defined in Table 41.

Bit 7. This bit is set to '1'.

Bit 6 (LBA). LBA is a flag to select either Cylinder/Head/Sector (CHS) or Logical Block Address Mode (LBA). When LBA is set to '0', Cylinder/Head/Sector mode is selected. When LBA is set to '1', Logical Block Address is selected. In Logical Block Mode, the Logical Block Address is interpreted as follows:

LBA7-LBA0: Sector Number Register D7 to D0.

LBA15-LBA8: Cylinder Low Register D7 to D0.

LBA23-LBA16: Cylinder High Register D7 to D0.

LBA27-LBA24: Drive/Head Register bits HS3 to HS0.

Bit 5. This bit is set to '1'.

Bit 4 (DRV). DRV is the drive number. When DRV is '0', drive/card 0 is selected (Master). When DRV is '1', drive/card 1 is selected (Slave). The Card is set to Card 0 or 1 using the copy field (Drive #) of the PCMCIA Socket & Copy configuration register.

Bit 3 (HS3). When operating in the Cylinder, Head, Sector mode, this is bit 3 of the head number. It is bit 27 in the Logical Block Address mode.

Bit 2 (HS2). When operating in the Cylinder, Head, Sector mode, this is bit 2 of the head number. It is bit 26 in the Logical Block Address mode.

Bit 1 (HS1). When operating in the Cylinder, Head, Sector mode, this is bit 1 of the head number. It is Bit 25 in the Logical Block Address mode.

Bit 0 (HS0). When operating in the Cylinder, Head, Sector mode, this is bit 0 of the head number. It is Bit 24 in the Logical Block Address mode.

Table 41. Drive/Head Register

D7	D6	D5	D4	D3	D2	D1	D0
1	LBA	1	DRV	HS3	HS2	HS1	HS0

Status & Alternate Status Registers (Address 1F7h [177h] & 3F6h [376h]; Offsets 7 & Eh)

These registers return the Card status when read by the host.

Reading the Status Register clears a pending interrupt. Reading the Auxiliary Status Register does not clear a pending interrupt.

The Status Register should be accessed in Byte mode; in Word mode it is recommended that Alternate Status Register is used. The status bits are described as follows

Bit 7 (BUSY). The busy bit is set when only the Card can access the command register and buffer, The host is denied access. No other bits in this register are valid when this bit is set to '1'.

Bit 6 (RDY). This bit indicates whether the device is capable of performing CompactFlash Memory Card operations. This bit is cleared at power up and remains cleared until the Card is ready to accept a command.

Bit 5 (DWF). When set this bit indicates a Write Fault has occurred.

Bit 4 (DSC). This bit is set when the Card is ready.

Bit 3 (DRQ). The Data Request is set when the Card requires information be transferred either to or from the host through the Data register. The bit is cleared by the next command.

Bit 2 (CORR). This bit is set when a Correctable data error has been encountered and the data has been corrected. This condition does not terminate a multi-sector read operation.

Bit 1 (IDX). This bit is always set to '0'.

Bit 0 (ERR). This bit is set when the previous command has ended in some type of error. The bits in the Error register contain additional information describing the error. In case of read or write access commands that end with an error, the address of the first sector with an error is in the command block registers. This bit is cleared by the next command.

Table 42. Status & Alternate Status Register

D7	D6	D5	D4	D3	D2	D1	D0
BUSY	RDY	DWF	DSC	DRQ	CORR	0	ERR

Device Control Register (Address 3F6h [376h]; Offset Eh)

This write-only register is used to control the CompactFlash Memory Card interrupt request This register can be written even if the device is BUSY. The bits are defined as follows:

Bit 7 to 2. Don't care. The host should reset this bit to '0'.

Bit 1 (–IEn). When the Interrupt Enable bit is set to '0', –IREQ interrupts are enabled. When the bit is set to '1', interrupts from the Card are disabled. This bit also controls the Int bit in the and Status Register. It is set to '0' at power on and Reset.

Bit 0. This bit is set to '0'.

Table 43. Device Control Register

D7	D6	D5	D4	D3	D2	D1	D0
X(0)	X(0)	X(0)	X(0)	X(0)	X(0)	–IEn	0

Card (Drive) Address Register (Address 3F7h [377h]; Offset Fh)

This read-only register is provided for compatibility with the AT disk drive interface and can be used for confirming the drive status. It is recommended that this register is not mapped into the host's I/O space because of potential conflicts on Bit 7. The bits are defined as follows:

Bit 7. This bit is don't care.

Bit 6 (–WTG). This bit is '0' when a write operation is in progress, otherwise, it is '1'.

Bit 5 (–HS3). This bit is the negation of bit 3 in the Drive/Head register.

Bit 4 (–HS2). This bit is the negation of bit 2 in the Drive/Head register.

Bit 3 (–HS1). This bit is the negation of bit 1 in the Drive/Head register.

Bit 2 (–HS0). This bit is the negation of bit 0 in the Drive/Head register.

Bit 1 (–nDS1). This bit is '0' when drive 1 is active and selected.

Bit 0 (–nDS0). This bit is '0' when the drive 0 is active and selected.

Table 44. Card (Drive) Address Register

D7	D6	D5	D4	D3	D2	D1	D0
X	–WTG	–HS3	–HS2	–HS1	–HS0	–nDS1	–nDS0

CF-ATA COMMAND DESCRIPTION

This section defines the software requirements and the format of the commands the Host sends to the Card. Commands are issued to the Card by loading the required registers in the command block with the supplied parameters, and then writing the command code to the Command Register. There are three classes of command acceptance, all dependent on the host not issuing commands unless the Card is not busy (BSY is '0').

- **Class 1.** Upon receipt of a Class 1 command, the Card sets BSY within 400ns.
- **Class 2 .** Upon receipt of a Class 2 command, the Card sets BSY within 400ns, sets up the sector buffer for a write operation, sets DRQ within 700µs, and clears BSY within 400ns of setting DRQ.
- **Class 3.** Upon receipt of a Class 3 command, the Card sets BSY within 400ns, sets up the sector buffer for a write operation, sets DRQ within 20ms (assuming no re-assignments), and clears BSY within 400ns of setting DRQ.

For reasons of backward compatibility some commands are implemented as 'no operation' NOP.

Table 45. summarizes the CF-ATA command set with the paragraphs that follow describing the individual commands and the task file for each.

Table 45. CF-ATA Command Set

Class	Command	Code	FR	SC	SN	CY	DH	LBA
1	Check Power Mode	E5h or 98h					D	
1	Execute Drive Diagnostic	90h					YD	
1	Erase Sector(s)	C0h		Y	Y	Y	Y	Y
1	Identify Drive	ECh					D	
1	Idle	E3h or 97h		Y			D	
1	Idle Immediate	E1h or 95h					D	
1	Initialize Drive Parameters	91h		Y			Y	
1	NOP	00h					D	
1	Read Buffer	E4h					D	
1	Read Multiple	C4h		Y	Y	Y	Y	Y
1	Read Sector(s)	20h or 21h		Y	Y	Y	Y	Y
1	Read Verify Sector(s)	40h or 41h		Y	Y	Y	Y	Y
1	Recalibrate	1Xh					D	
1	Request Sense	03h					D	
1	Seek	7Xh			Y	Y	Y	Y
1	Set Features	EFh	Y				D	
1	Set Multiple Mode	C6h		Y			D	
1	Set Sleep Mode	E6h or 99h					D	
1	Stand By	E2h or 96h					D	
1	Stand By Immediate	E0h or 94h					D	
1	Translate Sector	87h		Y	Y	Y	Y	Y
1	Wear Level	F5h					Y	
2	Write Buffer	E8h					D	
3	Write Multiple	C5h		Y	Y	Y	Y	Y
3	Write Multiple w/o Erase	CDh		Y	Y	Y	Y	Y
2	Write Sector(s)	30h or 31h		Y	Y	Y	Y	Y
2	Write Sector(s) w/o Erase	38h		Y	Y	Y	Y	Y
3	Write Verify	3Ch		Y	Y	Y	Y	Y

Note: FR = Features Register, SC = Sector Count Register, SN = Sector Number Register, CY = Cylinder Registers, DH = Card/Drive/Head Head Register, LBA = Logical Block Address Mode Supported (see command descriptions for use),
Y - The register contains a valid parameter for this command. For the Drive/Head Register Y means both the Compact Flash Memory Card and head parameters are used.
D - only the Compact Flash Memory Card parameter is valid and not the head parameter
C - the register contains command specific data (see command descriptors for use).

Check Power Mode (98h or E5h)

This command checks the power mode.

Issuing the command while the Card is in Standby mode, is about to enter Standby, or is exiting Standby, the command will set BSY, set the Sector Count Register to 00h, clear BSY and generate an interrupt.

Issuing the command when the Card is in Idle mode will set BSY, set the Sector Count Register to FFh, clear BSY and generate an interrupt.

Table 46. defines the Byte sequence of the Check Power Mode command.

Table 46. Check Power Mode

Bit	7	6	5	4	3	2	1	0
Command (7)	98h or E5h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sect Num (3)	X							
Sect Cnt (2)	X							
Feature (1)	X							

Execute Drive Diagnostic (90h)

This command performs the internal diagnostic tests implemented by the Card.

In PCMCIA configuration, this command only runs on the Card which is addressed by the Drive/Head register when the command is issued. This is because PCMCIA card interface does not allow for direct inter-drive communication.

In True IDE Mode, the Drive bit is ignored and the diagnostic command is executed by both the Master and the Slave with the Master responding with the status for both devices.

Table 47. defines the Execute Drive Diagnostic command Byte sequence. The Diagnostic codes shown in Table 48. are returned in the Error Register at the end of the command.

Table 47. Execute Drive Diagnostic

Bit	7	6	5	4	3	2	1	0
Command (7)	90h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sect Num (3)	X							
Sect Cnt (2)	X							
Feature (1)	X							

Table 48. Diagnostic Codes

Code	Error Type
01h	No Error Detected
02h	Formatter Device Error
03h	Sector Buffer Error
04h	ECC Circuitry Error
05h	Controlling Microprocessor Error
8Xh	Slave Error in True IDE Mode

Erase Sector(s) (C0h)

This command is used to pre-erase and condition data sectors prior to a Write Sector Without Erase command or a Write Multiple Without Erase command. There is no data transfer associated with this command but a Write Fault error status can occur. Table 49. defines the Byte sequence of the Erase Sector command.

Table 49. Erase Sector(s)

Bit	7	6	5	4	3	2	1	0
Command (7)	C0h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sect Num (3)	Sector Number (LBA 7-0)							
Sect Cnt (2)	Sector Count							
Feature (1)	X							

Identify Drive (ECh)

The Identify Drive command enables the host to receive parameter information from the Card. This command has the same protocol as the Read Sector(s) command. Table 50. defines the Identify Drive command Byte sequence. All reserved bits or Words are zero. Table 51. shows the definition of each field in the Identify Drive Information.

Word 0: General Configuration. This field indicates that the device is a CompactFlash Memory Card.

Word 1: Default Number of Cylinders. This field contains the number of translated cylinders in the default translation mode. This value will be the same as the number of cylinders.

Word 3: Default Number of Heads. This field contains the number of translated heads in the default translation mode.

Word 6: Default Number of Sectors per Track. This field contains the number of sectors per track in the default translation mode.

Word 7-8: Number of Sectors per Card. This field contains the number of sectors per Card. This double Word value is also the first invalid address in LBA translation mode.

Word 10-19: Memory Card Serial Number. The contents of this field are right justified and padded with spaces (20h).

Word 23-26: Firmware Revision. This field contains the revision of the firmware for this product.

Word 27-46: Model Number. This field contains the model number for this product and is left justified and padded with spaces (20h).

Word 47: Read/Write Multiple Sector Count. This field contains the maximum number of sectors that can be read or written per interrupt using the Read Multiple or Write Multiple commands.

Word 49: Capabilities.

- Bit 13 Standby Timer

  is set to '0' to indicate that the Standby timer operation is defined by the manufacturer.

- Bit 11 IORDY Support

  is set to '0' to indicate that the Card may support IORDY operation.

- Bit 10 IORDY may be disabled

  Is set to ‘0’ to indicate that IORDY may not be disabled.
- Bit 9 LBA support

  CompactFlash Memory Cards support LBA mode addressing.
- Bit 8 DMA Support

  DMA mode is not supported.

Word 51: PIO Data Transfer Cycle Timing Mode. This field defines the mode for PIO data transfer. For backward compatibility with BIOSs written before Word 64 was defined for advanced modes, a device reports in Word 51, the highest original PIO mode it can support (PIO mode 0, 1 or 2).

Bits 15-8: are set to 02H.

Word 53: Translation Parameter Valid.

- Bit 1: is set to '1' to indicate that Words 64 to 70 are valid
- Bit 0: is set to '1' to indicate that Words 54 to 58 are valid

Word 54-56: Current Number of Cylinders, Heads, Sectors/Track. These fields contains the current number of user addressable Cylinders, Heads, and Sectors/Track in the current translation mode.

Word 57-58: Current Capacity. This field contains the product of the current cylinders, heads and sectors.

Word 59: Multiple Sector Setting.

- Bits 15-9 are reserved and must be set to ‘0’.
- Bit 8 is set to ‘1’, to indicate that the Multiple Sector Setting is valid.
- Bits 7-0 are the current setting for the number of sectors to be transferred for every interrupt, on Read/Write Multiple commands; the only values returned are 00h or 01h.

Word 60-61: Total Sectors Addressable in LBA Mode. This field contains the number of sectors addressable for the Card in LBA mode only.

Word 64: Advanced PIO transfer modes supported. This field is bit significant. Any number of bits may be set to ‘1’ in this field by the CompactFlash Memory Card to indicate the advanced PIO modes it is capable of supporting.

- Bits 7-2 are reserved for future advanced PIO modes.
- Bit 1 is set to ‘1’, indicates that the CompactFlash Memory Card supports PIO mode 4.
- Bit 0 is set to ‘1’ to indicate that the CompactFlash Memory Card supports PIO mode 3.

Word 67: Minimum PIO transfer cycle time without flow control. This field gives the minimum cycle time (in ns) that the host should use for the CompactFlash Memory Card to provide data integrity during transfer when flow control is not used. The value returned is 78h (for Cycle time values refer to Table 21.)

Word 68: Minimum PIO transfer cycle time with IORDY. This field gives the minimum cycle time (in ns) supported by the CompactFlash Memory Card to perform data transfers using IORDY flow control. The value returned is 78h (for Cycle time values refer to Table 21.)

Table 50. Identify Drive

Bit	7	6	5	4	3	2	1	0
Command (7)	ECh							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sect Num (3)	X							
Sect Cnt (2)	X							
Feature (1)	X							

Table 51. Identify Drive Information

Word Address	Default Value	Total Bytes	Data Field Type Information
0	848Ah	2	General Configuration (signature for the CompactFlash Memory Card)
1	XXXXh	2	Default number of cylinders
2	0000h	2	Reserved
3	00XXh	2	Default number of heads
4	0000h	2	Obsolete
5	0000h	2	Obsolete
6	XXXXh	2	Default number of sectors per track
7-8	XXXXh	4	Number of sectors per card (Word 7 = MSW, Word 8 = LSW)
9	0000h	2	Obsolete
10-19	aaaa	20	Serial number in ASCII (right justified)
20	0000h	2	Obsolete
21	0000h	2	Obsolete
22	0004h	2	Reserved
23-26	aaaa	8	Firmware revision in ASCII. Big Endian Byte Order in Word
27-46	aaaa	40	Model number in ASCII (right justified) Big Endian Byte Order in Word
47	0001h	2	Maximum number of sectors on Read/Write Multiple command
48	0000h	2	Reserved
49	0200h	2	Capabilities
50	0000h	2	Reserved
51	0200h	2	PIO data transfer cycle timing mode
52	0000h	2	Obsolete
53	0003h	2	Field validity
54	XXXXh	2	Current numbers of cylinders
55	XXXXh	2	Current numbers of heads
56	XXXXh	2	Current sectors per track
57-58	XXXXh	4	Current capacity in sectors (LBAs)(Word 57 = LSW, Word 58 = MSW)
59	01XXh	2	Multiple sector setting
60-61	XXXXh	4	Total number of sectors addressable in LBA Mode
62-63	0000h	4	Reserved
64	0003h	2	Advanced PIO modes supported
65-66	0000h	4	Reserved
67	0078h	2	Minimum PIO transfer cycle time without flow control
68	0078h	2	Minimum PIO transfer cycle time with IORDY flow control
69-128	0000h	120	Reserved
129-159	0000h	62	manufacturer unique Bytes
160-255	0000h	192	Reserved

Idle (97h or E3h)

This command causes the Card to set BSY, enter the Idle mode, clear BSY and generate an interrupt. If the sector count is non-zero, it is interpreted as a timer count (each count is 5ms) and the automatic power down mode is enabled. If the sector count is zero, the automatic power down mode is disabled. Note that this time base (5ms) is different from the ATA specification. Table 52. defines the Byte sequence of the Idle command.

Table 52. Idle

Bit	7	6	5	4	3	2	1	0
Command (7)	97h or E3h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sect Num (3)	X							
Sect Cnt (2)	Timer Count (5ms increments)							
Feature (1)	X							

Idle Immediate (95h or E1h)

This command causes the Card to set BSY, enter the Idle mode, clear BSY and generate an interrupt. Table 53. defines the Idle Immediate command Byte sequence.

Table 53. Idle Immediate

Bit	7	6	5	4	3	2	1	0
Command (7)	95h or E1h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sect Num (3)	X							
Sect Cnt (2)	X							
Feature (1)	X							

Initialize Drive Parameters (91h).

This command enables the host to set the number of sectors per track and the number of heads per cylinder. Only the Sector Count and the Card/Drive/Head registers are used by this command. Table 54. defines the Initialize Drive Parameters command Byte sequence.

Table 54. Initialize Drive Parameters

Bit	7	6	5	4	3	2	1	0
Command (7)	91h							
C/D/H (6)	X	0	X	Drive	Max Head (no. of heads 1)			
Cyl High (5)	X							
Cyl Low (4)	X							
Sect Num (3)	X							
Sect Cnt (2)	Number of Sectors							
Feature (1)	X							

NOP (00h)

This command always fails with the CompactFlash Memory Card returning command aborted. Table 55. defines the Byte sequence of the NOP command.

Table 55. NOP

Bit	7	6	5	4	3	2	1	0
Command (7)	00h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sect Num (3)	X							
Sect Cnt (2)	X							
Feature (1)	X							

Read Buffer (E4h)

The Read Buffer command enables the host to read the current contents of the Card's sector buffer. This command has the same protocol as the Read Sector(s) command. Table 56. defines the Read Buffer command Byte sequence.

Table 56. Read Buffer

Bit	7	6	5	4	3	2	1	0
Command (7)	E4h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sect Num (3)	X							
Sect Cnt (2)	X							
Feature (1)	X							

Read Multiple (C4h)

The Read Multiple command performs similarly to the Read Sectors command. Interrupts are not generated on every sector, but on the transfer of a block which contains the number of sectors defined by a Set Multiple command.

Command execution is identical to the Read Sectors operation except that the number of sectors defined by a Set Multiple command are transferred without intervening interrupts. DRQ qualification of the transfer is required only at the start of the data block, not on each sector.

The block count of sectors to be transferred without intervening interrupts is programmed by the Set Multiple Mode command, which must be executed prior to the Read Multiple command. When the Read Multiple command is issued, the Sector Count Register contains the number of sectors (not the number of blocks or the block count) requested. If the number of requested sectors is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n sectors, where:

n = (sector count) module (block count).

If the Read Multiple command is attempted before the Set Multiple Mode command has been executed or when Read Multiple commands are disabled, the Read Multiple operation is rejected with an Aborted Command error. Disk errors encountered during Read Multiple commands are posted at the beginning of the block or partial block transfer, but DRQ is still set and the data transfer will take place as it normally would, including transfer of corrupted data, if any.

Interrupts are generated when DRQ is set at the beginning of each block or partial block. The error reporting is the same as that on a Read Sector(s) Command. This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register.

If an error occurs, the read terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The flawed data is pending in the sector buffer.

Subsequent blocks or partial blocks are transferred only if the error was a correctable data error. All other errors cause the command to stop after transfer of the block which contained the error.

Table 57. defines the Read Multiple command Byte sequence.

Table 57. Read Multiple

Bit	7	6	5	4	3	2	1	0
Command (7)	C4h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sect Num (3)	Sector Number (LBA 7-0)							
Sect Cnt (2)	Sector Count							
Feature (1)	X							

Read Sector(s) (20h or 21h)

This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is issued and after each sector of data (except the last one) has been read by the host, the Card sets BSY, puts the sector of data in the buffer, sets DRQ, clears BSY, and generates an interrupt. The host then reads the 512 Bytes of data from the buffer.

If an error occurs, the read terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head, and sector number of the sector where the error occurred. The flawed data is pending in the sector buffer. Table 58. defines the Read Sector command Byte sequence.

Table 58. Read Sector(s)

Bit	7	6	5	4	3	2	1	0
Command (7)	20h or 21h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sect Num (3)	Sector Number (LBA 7-0)							
Sect Cnt (2)	Sector Count							
Feature (1)	X							

Read Verify Sector(s) (40h or 41h)

This command is identical to the Read Sectors command, except that DRQ is never set and no data is transferred to the host. When the command is accepted, the Card sets BSY. When the requested sectors have been verified, the Card clears BSY and generates an interrupt.

If an error occurs, the verify terminates at the sector where the error occurs. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The Sector Count Register contains the number of sectors not yet verified.

Table 59. defines the Read Verify Sector command Byte sequence.

Table 59. Read Verify Sector(s)

Bit	7	6	5	4	3	2	1	0
Command (7)	40h or 41h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sect Num (3)	Sector Number (LBA 7-0)							
Sect Cnt (2)	Sector Count							
Feature (1)	X							

Recalibrate (1Xh)

This command is effectively a NOP command to the Card and is provided for compatibility purposes. Table 60. defines the Recalibrate command Byte sequence.

Table 60. Recalibrate

Bit	7	6	5	4	3	2	1	0
Command (7)	1Xh							
C/D/H (6)	1	LBA	1	Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sect Num (3)	X							
Sect Cnt (2)	X							
Feature (1)	X							

Request Sense (03h)

This command requests extended error information for the previous command. Table 61. defines the Request Sense command Byte sequence. Table 62. defines the valid extended error codes. The extended error code is returned to the host in the Error Register.

Table 61. Request Sense

Bit	7	6	5	4	3	2	1	0
Command (7)	03h							
C/D/H (6)	1	X	1	Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sect Num (3)	X							
Sect Cnt (2)	X							
Feature (1)	X							

Table 62. Extended Error Codes

Extended Error Code	Description
00h	No Error Detected
01h	Self Test OK (No Error)
09h	Miscellaneous Error
21h	Invalid Address (Requested Head or Sector Invalid)
2Fh	Address Overflow (Address Too Large)
35h, 36h	Supply or generated Voltage Out of Tolerance
11h	Uncorrectable ECC Error
18h	Corrected ECC Error
05h, 30-34h, 37h, 3Eh	Self Test or Diagnostic Failed
10h, 14h	ID Not Found
3Ah	Spare Sectors Exhausted
1Fh	Data Transfer Error / Aborted Command
0Ch, 38h, 3Bh, 3Ch, 3Fh	Corrupted Media Format
03h	Write / Erase Failed

Seek (7Xh)

This command is effectively a NOP command to the Card although it does perform a range check of cylinder and head or LBA address and returns an error if the address is out of range. Table 63. shows the Seek command Byte sequence.

Table 63. Seek

Bit	7	6	5	4	3	2	1	0
Command (7)	7Xh							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sect Num (3)	X (LBA 7-0)							
Sect Cnt (2)	X							
Feature (1)	X							

Set Features (EFh)

This command is used by the host to establish or select certain features. Table 64. shows the Set Features command Byte sequence. Table 65. defines all features that are supported.

Features 01h and 81h are used to enable and clear 8 bit data transfer modes in True IDE Mode. If the 01h feature command is issued all data transfers will occur on the low order D7D0 data bus and the –IOIS16 signal will not be asserted for data register accesses.

Feature 03h allows the host to select the PIO transfer mode by specifying a value in the Sector Count register (see Table 66. for values). The upper 5 bits define the type of transfer and the low order 3 bits encode the mode value. One PIO mode should be selected at all times. The host may change the selected mode by issuing the Set Features command.

Feature code 9Ah enables the host to configure the card to best meet the host system's power requirements. The host sets a value in the Sector Count register that is equal to one-fourth of the desired maximum average current (in mA) that the card should consume. For example, if the Sector Count register were set to 6, the card would be configured to provide the best possible performance without exceeding 24 mA. Upon completion of the command, the card responds to the host with the range of values supported by the card. The minimum value is set in the Cylinder Low Register, and the maximum value is set in the Cylinder Hi register. The default value, after a power on reset, is to operate at the highest performance and therefore the highest current mode.

The card will accept values outside this programmable range, but will operate at either the lowest power or highest performance as appropriate.

Table 64. Set Features

Bit	7	6	5	4	3	2	1	0
Command (7)	EFh							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sect Num (3)	X							
Sect Cnt (2)	Config							
Feature (1)	Feature							

Table 65. Features Supported

Feature	Operation
01h	Enable 8 bit data transfers.
03h	Set transfer mode based on value in Sector Count register.
55h	Disable Read Look Ahead.
69h	NOP Accepted for backward compatibility.
81h	Disable 8 bit data transfer.
96h	NOP Accepted for backward compatibility.
97h	Accepted for backward compatibility. Use of this Feature is not recommended.
9Ah	Set the host current source capability. Allows trade-off between current drawn and read/write speed.

Table 66. Transfer Mode Values

Mode	Bits (7:3)	Bits (2:0)
PIO default mode	00000b	000b
PIO default mode, disable IORDY	00000b	001b
PIO flow control transfer mode	00001b	Mode(1)

Note: 1. Mode = transfer mode number

Set Multiple Mode (C6h)

This command enables the Card to perform Read and Write Multiple operations and establishes the block count for these commands. The Sector Count Register is loaded with the number of sectors per block. Upon receipt of the command, the Card sets BSY and checks the Sector Count Register.

If the Sector Count Register contains a valid value and the block count is supported, the value is loaded for all subsequent Read Multiple and Write Multiple commands and execution is enabled. If a block count is not supported, an Aborted Command error is posted, and Read Multiple and Write Multiple commands are disabled. If the Sector Count Register contains '0' when the command is issued, Read and Write Multiple commands are disabled. At power on, or after a hardware reset (unless disabled by a Set Feature command), the default mode is Read and Write Multiple disabled. Table 67. defines the Set Multiple Mode command Byte sequence.

Table 67. Set Multiple Mode

Bit	7	6	5	4	3	2	1	0
Command (7)	C6h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sect Num (3)	X							
Sect Cnt (2)	Sector Count							
Feature (1)	X							

Set Sleep Mode (99h or E6h)

This command causes the CompactFlash Memory Card to set BSY, enter the Sleep mode, clear BSY and generate an interrupt. Recovery from sleep mode is accomplished by simply issuing another command (a reset is permitted but not required). Sleep mode is also entered when internal timers expire so the host does not need to issue this command except when it wishes to enter Sleep mode immediately. The default value for the timer is 5 milliseconds. Note that this time base (5ms) is different from the ATA Specification. Table 68. defines the Set Sleep Mode command Byte sequence.

Table 68. Set Sleep Mode

Bit	7	6	5	4	3	2	1	0
Command (7)	99h or E6h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sect Num (3)	X							
Sect Cnt (2)	X							
Feature (1)	X							

Standby (96h or E2)

This command causes the Card to set BSY, enter the Sleep mode (which corresponds to the ATA 'Standby' Mode), clear BSY and return the interrupt immediately. Recovery from Sleep mode is accomplished by issuing another command (a reset is not required). Table 69. defines the Standby command Byte sequence.

Table 69. Standby

Bit	7	6	5	4	3	2	1	0
Command (7)	96h or E2h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sect Num (3)	X							
Sect Cnt (2)	X							
Feature (1)	X							

Standby Immediate (94h or E0h)

This command causes the Card to set BSY, enter the Sleep mode (which corresponds to the ATA Standby Mode), clear BSY and return the interrupt immediately.

Recovery from Sleep mode is accomplished by issuing another command (a reset is not required). Table 70. defines the Standby Immediate Byte sequence.

Table 70. Standby Immediate

Bit	7	6	5	4	3	2	1	0
Command (7)	94h or E0h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sect Num (3)	X							
Sect Cnt (2)	X							
Feature (1)	X							

Translate Sector (87h)

This command allows the host a method of determining the exact number of times a user sector has been erased and programmed. The controller responds with a 512 Byte buffer of information containing the desired cylinder, head and sector, including its Logical Address, and the Hot Count, if available, for that sector. Table 71. defines the Translate Sector command Byte sequence. Table 72. represents the information in the buffer.

Table 71. Translate Sector

Bit	7	6	5	4	3	2	1	0
Command (7)	87h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sect Num (3)	Sector Number (LBA 7-0)							
Sect Cnt (2)	X							
Feature (1)	X							

Table 72. Translate Sector Information

Address	Information
00h-01h	Cylinder MSB (00), Cylinder LSB (01)
02h	Head
03h	Sector
04-06h	LBA MSB (04) - LSB (06)
07-12h	Reserved
13h	Erased Flag (FFh) = Erased; 00h = Not Erased
14h-17h	Reserved
18h-1Ah	Hot Count MSB (18) - LSB (1A); 0 = Hot Count not supported
1Bh-1FFh	Reserved

Wear Level (F5h)

This command is effectively a NOP command and only implemented for backward compatibility. The Sector Count Register will always be returned with a 00h indicating Wear Level is not needed.

Table 73. defines the Wear Level command Byte sequence.

Table 73. Wear Level

Bit	7	6	5	4	3	2	1	0
Command (7)	F5h							
C/D/H (6)	X			Drive	Flag			
Cyl High (5)	X							
Cyl Low (4)	X							
Sect Num (3)	X							
Sect Cnt (2)	Completion Status							
Feature (1)	X							

Write Buffer (E8h)

The Write Buffer command enables the host to overwrite contents of the Card's sector buffer with any data pattern desired. This command has the same protocol as the Write Sector(s) command and transfers 512 Bytes.

Table 74. defines the Write Buffer command Byte sequence.

Table 74. Write Buffer

Bit	7	6	5	4	3	2	1	0
Command (7)	E8h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sect Num (3)	X							
Sect Cnt (2)	X							
Feature (1)	X							

Write Multiple Command (C5h)

This command is similar to the Write Sectors command. The Card sets BSY within 400ns of accepting the command. Interrupts are not presented on each sector but on the transfer of a block which contains the number of sectors defined by Set Multiple. Command execution is identical to the Write Sectors operation except that the number of sectors defined by the Set Multiple command is transferred without intervening interrupts.

DRQ qualification of the transfer is required only at the start of the data block, not on each sector. The block count of sectors to be transferred without intervening interrupts is programmed by the Set Multiple Mode command, which must be executed prior to the Write Multiple command.

When the Write Multiple command is issued, the Sector Count Register contains the number of sectors (not the number of blocks or the block count) requested. If the number of requested sectors is not evenly divisible by the sector/block, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n sectors, where:

n = (sector count) module (block count).

If the Write Multiple command is attempted before the Set Multiple Mode command has been executed or when Write Multiple commands are disabled, the Write Multiple operation will be rejected with an aborted command error.

Errors encountered during Write Multiple commands are posted after the attempted writes of the block or partial block transferred. The Write command ends with the sector in error, even if it is in the middle of a block. Subsequent blocks are not transferred in the event of an error. Interrupts are generated when DRQ is set at the beginning of each block or partial block.

The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred and the Sector Count Register contains the residual number of sectors that need to be transferred for successful completion of the command. For example, each block has 4 sectors, a request for 8 sectors is issued and an error occurs on the third sector. The Sector Count Register contains 6 and the address is that of the third sector.

Note: The current revision of the CompactFlash Memory Card only supports a block count of 1 as indicated in the Identify Drive Command information. The Write Multiple command is provided for compatibility with future products which may support a larger block count.

Table 75. defines the Write Multiple command Byte sequence.

Table 75. Write Multiple

Bit	7	6	5	4	3	2	1	0
Command (7)	C5h							
C/D/H (6)	1	LBA	1	Drive	Head			
Cyl High (5)	Cylinder High							
Cyl Low (4)	Cylinder Low							
Sect Num (3)	Sector Number							
Sect Cnt (2)	Sector Count							
Feature (1)	X							

Write Multiple without Erase (CDh)

This command is similar to the Write Multiple command with the exception that an implied erase before write operation is not performed. The sectors should be pre-erased with the Erase Sector(s) command before this command is issued. Table 76. defines the Write Multiple without Erase command Byte sequence.

Table 76. Write Multiple without Erase

Bit	7	6	5	4	3	2	1	0
Command (7)	CDh							
C/D/H (6)	X	LBA	1	Drive	Head			
Cyl High (5)	Cylinder High							
Cyl Low (4)	Cylinder Low							
Sect Num (3)	Sector Number							
Sect Cnt (2)	Sector Count							
Feature (1)	X							

Write Sector(s) (30h or 31h)

This command writes from 1 to 256 sectors as specified in the Sector Count Register. A sector count of zero requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is accepted, the Card sets BSY, sets DRQ and clears BSY, then waits for the host to fill the sector buffer with the data to be written. No interrupt is generated to start the first host transfer operation. No data should be transferred by the host until BSY has been cleared by the host.

For multiple sectors, after the first sector of data is in the buffer, BSY will be set and DRQ will be cleared. After the next buffer is ready for data, BSY is cleared, DRQ is set and an interrupt is generated. When the final sector of data is transferred, BSY is set and DRQ is cleared. It will remain in this state until the command is completed at which time BSY is cleared and an interrupt is generated. If an error occurs during a write of more than one sector, writing terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The host may then read the command block to determine what error has occurred, and on which sector. Table 77. defines the Write Sector(s) command Byte sequence.

Table 77. Write Sector(s)

Bit	7	6	5	4	3	2	1	0
Command (7)	30h or 31h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sect Num (3)	Sector Number (LBA 7-0)							
Sect Cnt (2)	Sector Count							
Feature (1)	X							

Write Sector(s) without Erase (38h)

This command is similar to the Write Sector(s) command with the exception that an implied erase before write operation is not performed. This command has the same protocol as the Write Sector(s) command. The sectors should be pre-erased with the Erase Sector(s) command before this command is issued. If the sector is not pre-erased a normal write sector operation will occur. Table 78. defines the Write Sector(s) without Erase command Byte sequence.

Table 78. Write Sector(s) without Erase

Bit	7	6	5	4	3	2	1	0
Command (7)	38h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sect Num (3)	Sector Number (LBA 7-0)							
Sect Cnt (2)	Sector Count							
Feature (1)	X							

Write Verify (3Ch)

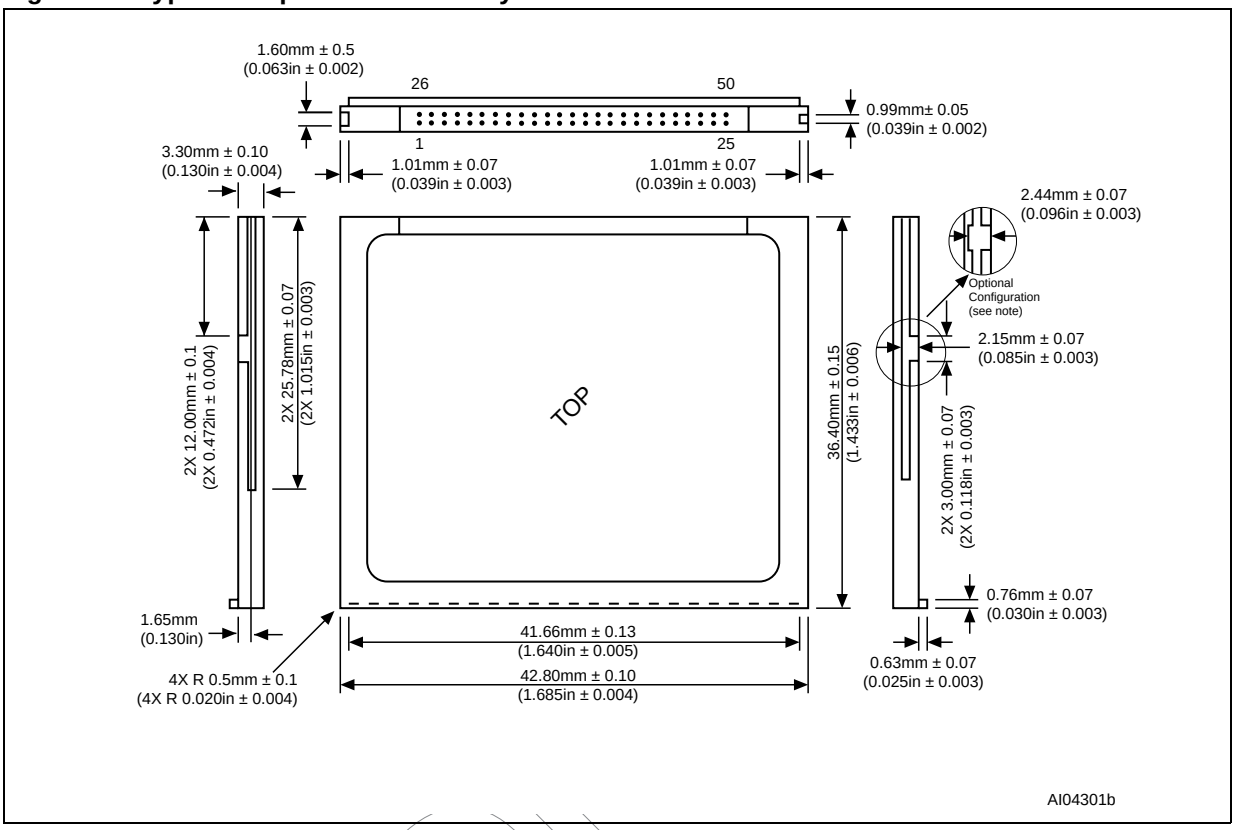
This command is similar to the Write Sector(s) command, except each sector is verified immediately after being written. This command has the same protocol as the Write Sector(s) command. Table 79. defines the Write Verify command Byte sequence.

Table 79. Write Verify

Bit	7	6	5	4	3	2	1	0
Command (7)	3Ch							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sect Num (3)	Sector Number (LBA 7-0)							
Sect Cnt (2)	Sector Count							
Feature (1)	X							

PACKAGE MECHANICAL

Figure 10. Type I CompactFlash Memory Card Dimensions



PART NUMBERING

Table 80. Ordering Information Scheme

Example: SMC 256 A F A 6 E

Memory Card Standard

SMC = Storage Medium, CompactFlash

Density

016 = 16 MBytes
032 = 32 MBytes
064 = 64 MBytes
128 = 128 MBytes
256 = 256 MBytes
512 = 512 MBytes
01G = 1 GByte

Options of the Standard

A = CF Type I

Memory Type

F = Flash Memory

Card Version

A = Version depending on device mix

Temperature Range

6 = -40 to 85°C

Packing

Blank = Standard Packing (tray)
E = Lead-Free Package, Standard Packing (tray)

Note: Other digits may be added to the ordering code for preprogrammed parts or other options.
Devices are shipped from the factory with the memory content bits erased to ’1’.
For further information on any aspect of the device, please contact your nearest ST Sales Office.

REVISION HISTORY

Table 81. Document Revision History

Date	Version	Revision Details
30-Jun-2004	0.1	First Issue
04-Aug-2004	0.2	Operating and Non-Operating voltage ranges modified (see Table 4., Environmental Specifications and Table 80., Ordering Information Scheme). Conditions for Voltage on any pin except V_{CC} with respect to GND modified in Table 9., Absolute Maximum Conditions. Unit for IxD modified in Table 11., Input Leakage Current. Small text changes. In Table 2., System Performance, Sustained Write and Command to DRQ Max values changed, Reset to Ready parameter changed to Power-up to Ready and equivalent speed grades given in multiples of X (see Note: 1.). CompactFlash Storage Card renamed as CompactFlash Memory Card.
29-Sep-2004	0.3	Code for “Standard Packing (tray)” Packing option corrected in Table 80., Ordering Information Scheme.
17-Dec-2004	0.4	Sustained Write Performance updated in FEATURES SUMMARY and Table 2., System Performance. Table 6., System Reliability and Maintenance added in SUMMARY DESCRIPTION section. Weight updated in Figure 5., Common Memory Read Timing Diagram. Figure 10., Type I CompactFlash Memory Card Dimensions updated.
18-Feb-2005	0.5	All text, tables and figures relating to the Security features of the SMCxxxAF from removed. All text, tables and figures related to *Soft Reset* features, removed. *Flush Cache (E7h)* and *Format Track (50h)* sections removed. *Read Long Sector (22h to 23h)* and *Write Long Sector (32h to 33h)* removed. All text, tables and figures relating to three sections on *Key Management*, removed. *Word 82-84*, *Word 85-87*, *Word 91* and *Word 162* sections removed from Identify Drive (ECh). Table 70., *Power Management Levels*, removed. Added Table 66. to Set Features (EFh) section. Text altered in Configuration Option Register (Base + 00h in Attribute Memory), Read Sector(s) (20h or 21h), Read Verify Sector(s) (40h or 41h), Set Multiple Mode (C6h). and Set Features (EFh). Modified Word 49: Capabilities section. Modified Table 2., Table 4., Table 6., Table 10., Table 12., Table 24., Table 43., Table 45., Table 51., Table 62. and Table 65. Modifications to Electrical Specification and PART NUMBERING sections. Minor modifications to headings in the ELECTRICAL INTERFACE section.