

# Juan Pablo Duarte Sepúlveda

Current Position	<b>Graduate Student Researcher</b> Department of Electrical Engineering & Computer Sciences, University of California, Berkeley 550 Sutardja Dai Hall, MC1764, Berkeley, CA 94720.
Mobile	+1-510-506-0311
Email	jpduarte@berkeley.edu
Homepage	<a href="http://eecs.berkeley.edu/~jpduarte">http://eecs.berkeley.edu/~jpduarte</a>

## Education

Sept. 2012 - May 2018	<b>Ph.D. Electrical Engineering &amp; Computer Sciences</b> University of California, Berkeley Thesis: <i>Mathematical Compact Models of Advanced Transistors for Numerical Simulation and Hardware Design</i> Advisor: Professor Chenming Hu
Sept. 2010 - Feb. 2012	<b>M.S. Electrical Engineering</b> Korea Advanced Institute of Science and Technology Thesis: <i>Core Compact Models for Multiple-Gate Field-Effect-Transistors</i> Advisor: Professor Yang-Kyu Choi
Mar. 2007 - Aug. 2010	<b>B.S. Electrical Engineering</b> Korea Advanced Institute of Science and Technology
Mar. 2005 - Dec. 2006	<b>Electronic Engineering Student</b> Universidad Técnica Federico Santa María, Chile

## Publications

Over 56 publications, including journals, conferences, and book chapters. Over 1200 citations (Publication list: <http://tinyurl.com/juanpublications>). Industry standard spice model releases for BSIM6, BSIM-CMG, and BSIM-IMG (<http://bsim.berkeley.edu/>).

## Experience

2018 - Present	<b>University of California, Berkeley</b> <i>Technology aware hardware design for AI</i> : Modeling, simulation and design of new hardware architectures for AI applications using advanced memory and logic devices.
2016 - 2017	<b>University of California, Berkeley</b> <i>Negative-Capacitance Transistors</i> : Numerical simulation, compact modeling, and circuit evaluation.
2015 - 2017	<b>University of California, Berkeley</b> <i>Mathematical Compact Model for Independent Gate Transistors (BSIM-IMG)</i> : A new core model for UTBSOI transistors including back-gate inversion was developed considering good speed and convergence capabilities.
2012 - 2015	<b>University of California, Berkeley</b> <i>Unified Compact Model of Advanced CMOS (BSIM-CMG)</i> : A comprehensive mathematical model was developed for FinFET transistors with

complex fin structures and new materials was developed for industrial applications.

- 2017 **University of California, Berkeley**  
*Main Lecturer*  
*DeCal Course: Hardware Makers:* Students learned how to create hardware with wifi/bluetooth connections of several prototyping boards, sensors, actuators, and additional electronics components.
- 2016 **University of California, Berkeley**  
*Graduate Student Instructor*  
 Designing Information Devices and Systems II (Fall/Spring): I was a Lab Instructor where students focused on the fundamentals of designing and building modern information devices and systems that interface with the real world.
- 2015 **Thomas J. Watson Research Center, IBM, Yorktown, NY**  
*Summer Research Intern*  
 Complementary Metal-Oxide Semiconductor (CMOS) Device intern: Measurement and characterization of III-V transistors.
- 2012 **Universidad Técnica Federico Santa María, Valparaíso, Chile**  
*Lecturer*  
*Digital System Lab (Laboratorio de Sistemas Digitales), Advanced Design of Digital Systems (Diseño Avanzado de Sistemas Digitales), Physical Electronics (Física Electrónica)*
- 2010 – 2012 **Korea Advanced Institute of Science and Technology, Daejeon, Korea**  
*Graduate Research Assistant with Prof. Yang-Kyu Choi*  
*Exploration of Nano-Fusion Memory Technology. Development of novel 3D stacked devices and core materials for the next generation flash memory. Terabit Nonvolatile Memory Development. Trans-scale convergence technology for nano devices.*
- 2009 – 2010 **Korea Advanced Institute of Science and Technology, Daejeon, Korea**  
*Undergraduate Research Assistant with Prof. Yang-Kyu Choi*  
 Project: *Underlap field effect transistor modeling for biosensor applications*
- 2009 **Korea Advanced Institute of Science and Technology, Daejeon, Korea**  
*Research internship with Prof. Hyun Myung*  
 Project: *Mobile Harbor Control Design*
- 2006 **Universidad Técnica Federico Santa María, Departamento de Física, Valparaíso, Chile**  
*Teacher Assistant with Prof. Pedro del Canto*  
 Course: *Introducción a la Física*

## Honors and Awards

- 2013 Best Student Paper Award at the 2013 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD) for the paper “Unified FinFET Compact Model: Modelling Trapezoidal Triple-Gate FinFETs”
- 2010 – 2011 International graduate student scholarship, Korea Advanced Institute of Science and Technology
- 2007 – 2010 International undergraduate student scholarship, Korea Advanced Institute of Science and Technology
- 2006 First prize, *Academic Merit Award*, Universidad Técnica Federico Santa María, Chile

2005 – 2006	Honor student, Departamento de Electrónica, Universidad Técnica Federico Santa María, Chile
2005 – 2006	Undergraduate scholarship, Universidad Técnica Federico Santa María, Chile

## Skills

Programming and Scientific Languages	Python, Verilog, MATLAB, Mathematica, Origin, C, Java, Arduino, Processing, HTML, $\text{\LaTeX}$
Circuit and System Tools	Hspice, Cadence Spectre, Cadence Schematic, Cadence Virtuoso Layout, Synopsys VCA, Synopsys IC Compiler, Synopsys Primetime, NGSpice, Pspice, HFSS, ModelSim, Xilinx ISE Design Suite, CST Microwave Studio, CoventorWare
Process and Device Simulation	ATLAS, ATHENA, Synopsys TCAD tools
Operating system	Linux, Windows
CMOS Device Fabrication	Experience with different types of equipment such as contact aligner, tube furnaces, wet etching and cleaning equipment, etc.
CMOS Device Characterization	Experience with different types of equipment such as probe stations, microscopes, LCR meter, in-line test equipment, etc.
Product Design	Laser Cutter, 3D Printing, Fusion 360, Eagle
Sensor Technology	CMOS based bio-sensors, accelerometers, gyroscopes, magnetometers, force-sensitive resistors, ribbon sensors, photo cells, long flex sensors

## Languages

Spanish	Native speaker
English	Fluent
Korean	Basic
Indonesian	Intermediate

## Extracurricular Activities

2017	USA Cycling Collegiate Road National Championships, Sixth place Team Qualification/Sixteenth place Individual Qualification, Grand Junction, CO.
2016	Founder of Cyclists Green Initiative
2016	USA Cycling Collegiate Road National Championships, Fifth place Team Pursuit, Asheville, NC.
2015	Community Service, The Berkeley Project
2010 – 2012	Member of International Food Committee, KAIST
2009 – 2012	Representative of Latin America in KISA, KAIST International Student Association
2009	Cofounder Association of Chilean Students in Korea
2009 – 2010	Member of KAPEX, the SoC design group in KAIST
2007	KAIST Swimming Competition, Third prize 200m
2004 – Present	Surfing and Longboard Skating
2003	National Cycling Championship, Second place, Chile
2003	National Velodrome Championship, Third place, Team Pursuit, Chile

## References

### **Prof. Chenming Hu**

Telephone

E-mail

Website

Advisor during graduate study at University of California, Berkeley

+1-510-642-3393

hu@eecs.berkeley.edu

bsim.berkeley.edu

### **Prof. Yang-Kyu Choi**

Telephone

E-mail

Website

Advisor during graduate study at KAIST, South Korea

+82-42-350-3477

ykchoi@ee.kaist.ac.kr

nobelab.kaist.ac.kr