Lab 2: FPGA Emulation

Objective

- ✓ Introduce Xilinx demo board emulation flow.

Prerequisite

- ✓ Fundamentals of logic gates.
- ✓ Verilog HDL representation of Logic components.

Experiments

1 Emulate exp1 in lab1 (a full adder ***s***+***cout***=***x***+***y***+***cin***) with the following parameters.

I/O	***x***	***y***	***cin***	***s***	***cout***
LOC	T1	P2	P1	H5	H6

2 Derive a BCD (***i***[3:0]) to 14-segment display decoder (***D_ssd***[14:0]), and also use four LEDs (***d***[3:0]) to monitor the 4-bit BCD number. (Other values of ***i*** outside the range will show F).

3 (Bonus) Design a single digit decimal adder and use the result of exp2 to display the two inputs on the first two digits of the seven-segment display and the results on the rest two digits.

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