Lab 3: Counters

Objective

- ✓ Review synchronous sequential circuits.
- ✓ Review counter logics.

Prerequisite

- ✓ Fundamentals of logic gates.
- ✓ Clocking concepts
- ✓ Logic modeling in Verilog HDL.

Pre-labs

1 Consider a 4-bit synchronous binary up counter.
  1.1 Draw the logic diagram
  1.2 Construct Verilog RTL representation for the logics with verification.

Experiments

1 Frequency Divider: Construct a 25-bit synchronous binary counter. Use the MSB of the counter, we can get a frequency divider which provides a $1/2^{25}$ frequency output (f_{out}) of the original clock ($f_{crystal}$, 40MHz). Construct a frequency divider of this kind.
  1.1 Write the specification of the frequency divider.
  1.2 Draw the block diagram of the frequency divider.
  1.3 Implement the frequency divider with the following parameters.

I/O	$f_{crystal}$	f_{out}
Site	R10	H5

2 Construct a single digit BCD up counter with the divided clock as the clock frequency and display on the seven-segment display.
  2.1 Construct a BCD up counter.
  2.2 Construct a BCD-to-seven-segment display decoder.
  2.3 Combine the above two together.

3 Construct a 2-digit BCD up counter (from 00 to 99) using exp2 as a building block. Use the divided clock as the clock frequency and display on the seven-segment display.

4 (Bonus) Construct a 30 seconds count down timer (stop at 00).

TA: _____

