Demo 4: External Clock and Phase-Locked Loop

ECE3056 Fall 2016

October 3, 2016

1 Overview

The behavior of this demo is exactly the same as Demo 3, but it runs 3 times faster, as the system clock is now from the internal phase-locked loop clock multiplier, guided by the external (to the microcontroller chip) 8MHz crystal, instead of the internal 8MHz RC oscillator.

2 Operation

Switching the clock source to the PLL is a somewhat involved process:

1. Enable the HSE (high speed external) oscillator.
2. Set PLL source to HSE predivider output.
3. Set PLL multiplication factor.
4. Turn on PLL.
5. Set clock source to PLL.

This can be done in four writes to the RCC (reset and clock control) register space; steps 2 and 3 can be combined into a single write to the RCC `cfgr` register.

3 Further Reading

The source is thoroughly annotated with comments, pointing to the pages in the ST Microelectronics manuals where further information can be found on each system used.

4 Exercises

The following exercises can be completed by modifying the demo code.

1. Modify the code to run only the EXTI interrupt service routine at the faster clock rate, switching back to the 8MHz rate when this routine is exited.