# JASON PIEN

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## Education

- **Brown University** — Providence, RI
  *Bachelor of Science in Computer Engineering; GPA: 3.97* — *Expected May 2025*
  - **Relevant Coursework**: Deep Learning, Computer Vision, Digital Electronics Syst Design, Data Structure & Alg, Linear Algebra, Digital Computing Systems, Statistical Inference I

## Experience

- **Ernst & Young** — New York City, NY
  *Incoming Software Engineering Intern* — *Summer 2024*
  - **Artificial Intelligence**: Learning and implementing next-generation technologies within leading investment banks, insurers, and investment managers
- **Freedays Venture** — Providence, RI
  *Co-founder, Software Engineer* — *Jun 2023 - Present*
  - **Hardware**: Developed an initial proof of concept breadboard prototype using C and ESP32, before transitioning to software
  - **Large Language Models**: Implemented OpenAI API to gpt-3.5-turbo, developed scripts for data cleansing and fine-tuned the application model
  - **Watch the pich**: https://youtu.be/jiVpAeGX-Dk?si=mXDfZeWbAeLYsC66&t=2060
- **Linkr** — Remote
  *UI/UX Designer* — *Mar 2023 - Sept 2023*
  - **Figma**: Led two separate UX redesigns using Balsamiq & Figma at Linkr, an all-in-one monetization platform serving 15M+ creators & brands
- **Brown School of Engineering** — Remote
  *Teaching Assistant & Mentor* — *Aug 2022 - Jan 2023*
  - **Mentorship**: Mentored and led 10 students in Intro to Engineering by holding weekly meetings and preparing section material
  - **Project Execution**: Assisted with the design and project execution of labs within the Brown Design Workshop

## Projects

- **jasonpien.com**: Self-taught HTML5/CSS and JavaScript for Personal Website featuring SVG path animations
- **Small Single Cycle CPU**: Developed to support 32 bit ARM instruction featuring ALU, decode logic support for MOV, Branch, Memory, and data processing instructions. Connected the data memory RAM to support simple LDR and STR instructions. Outputs to a small 16x16 display attached to the CPU
- **FPGA Stopwatch**: Altera Cyclone V DE0-CV FPGA w/ Verilog HDL within Intel Quartus Prime 20.1, I developed a FSM hardware stopwatch with logic support to a full binary to BCD converter outputting to 6 7-segment HEX displays.

## Programming Skills

- **Languages**: Python 3.9.18, Verilog HDL, RISC-V, Java, Javascript, MATLAB, HTML5/CSS
- **Technologies**: TensorFlow 2.15.0, Git, Google CoLab, Quartus Prime 20.1, LTSpice, Altera Cyclone V FPGA, ESP32, ARM Cortex-M boards

## Awards

- **Tau Beta Pi**: Initiated in 2023 as top 1/8th of the junior class for academic excellence in engineering
- **Brown Entrepreneurship Scholarly Award**: Awarded $4000 as a recognition and grant for being accepted into Brown's elite startup accelerator program
- **National Collegiate Taekwondo Bronze Medalist**: National Collegiate Taekwondo Championship, Bantam Weight black belt sparring