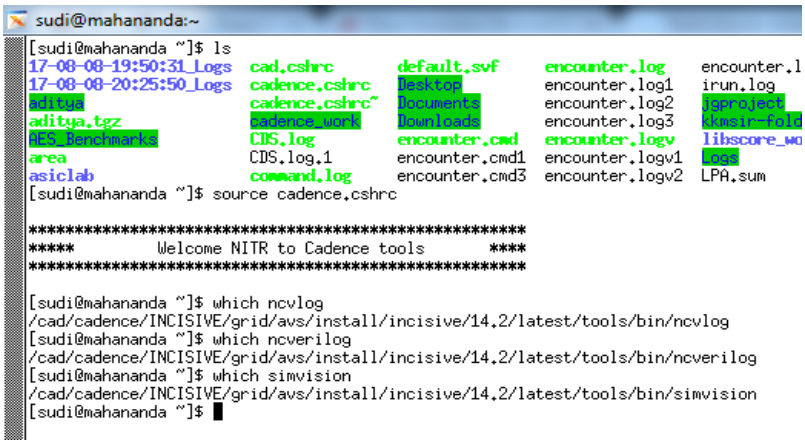
ASIC Design Lab (EC-664)

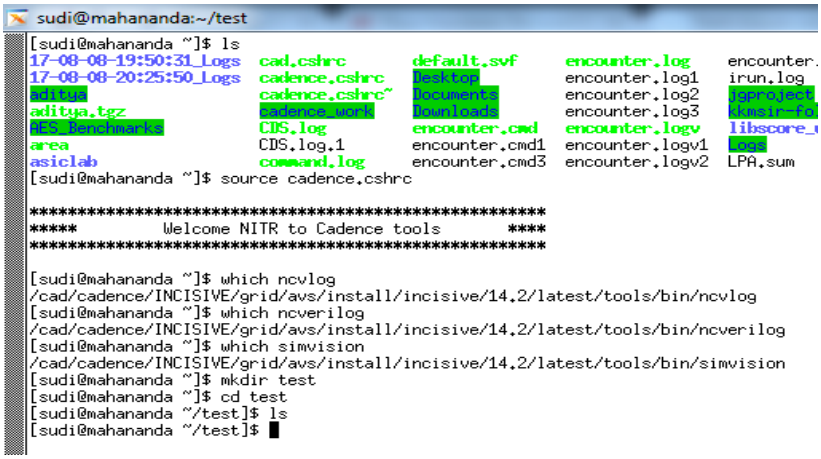
Experiment – I

Simulation of Finite State Machine (FSM) based Designs in Verilog HDL.

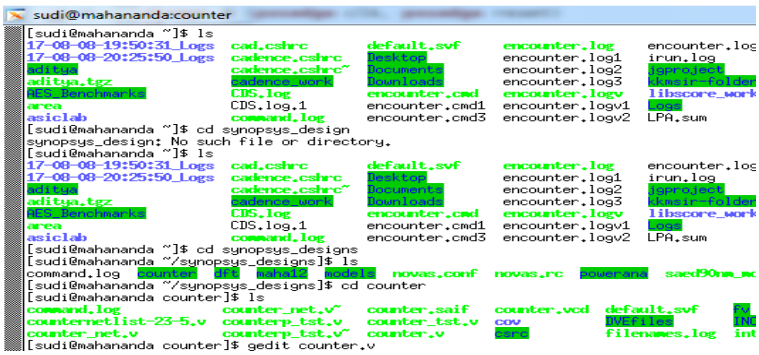
1. Open the terminal
2. Source the cadence.cshrc
3. Check whether the commands are working as below: -

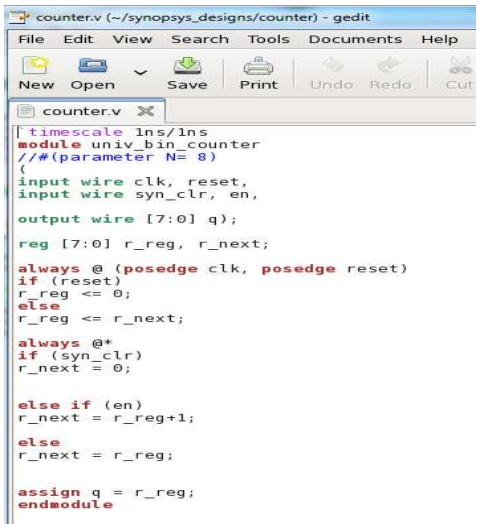


4. Create a directory for saving files as below: -

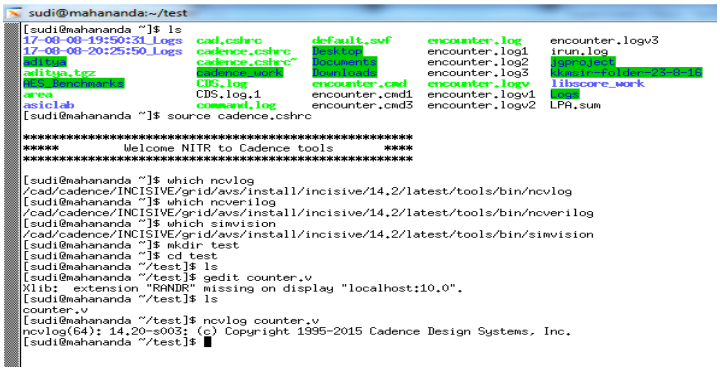


5. Create design_file.v as shown below: - (gedit counter.v)

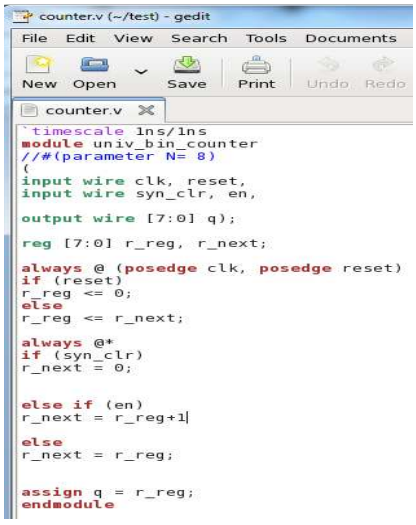




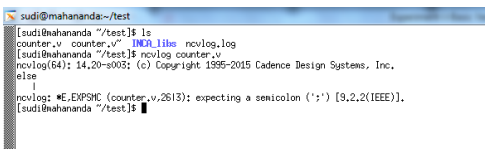
6. Check the syntax of design.v (in this example: counter.v) (no syntax errors found)



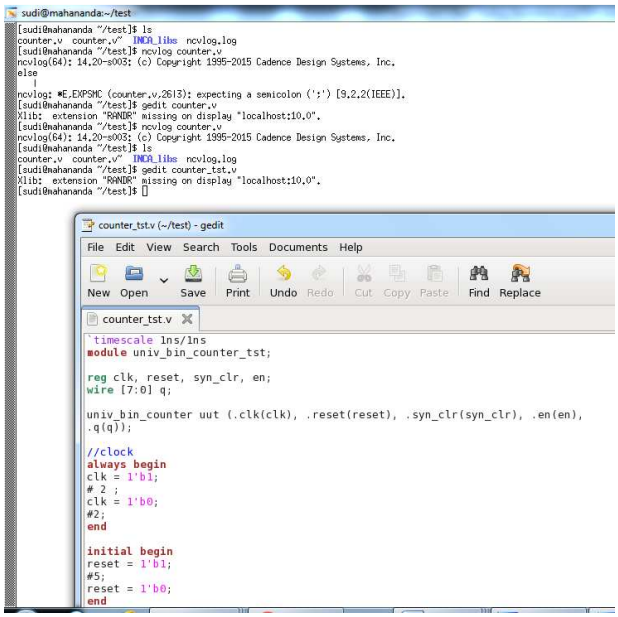
7. Induce syntax error in line 24 by removing semicolon



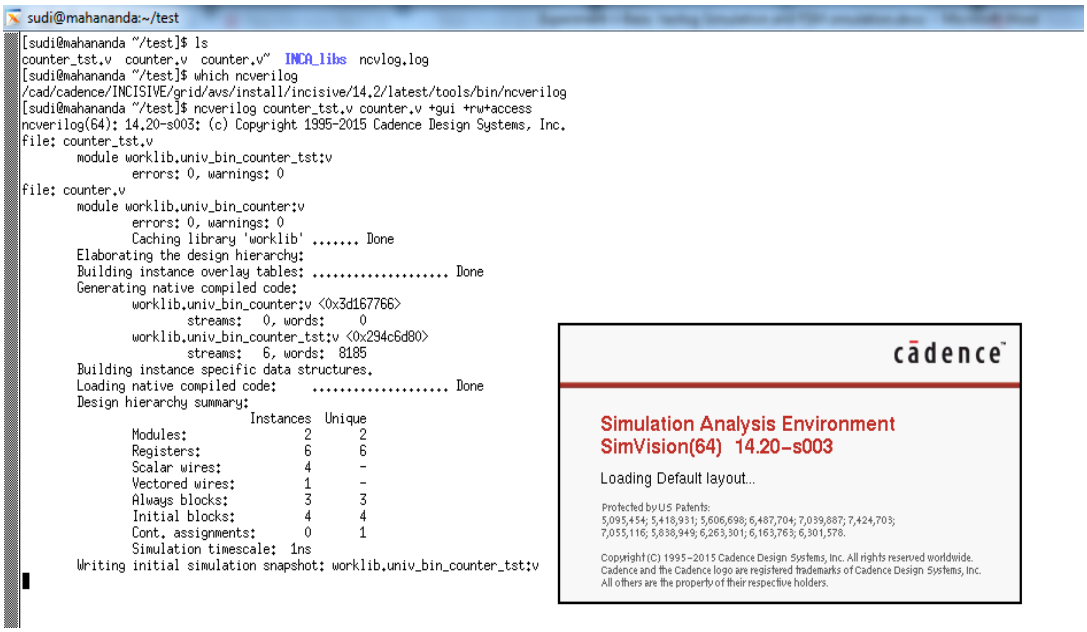
8. Perform syntax check: - (shows syntax near 26|3)



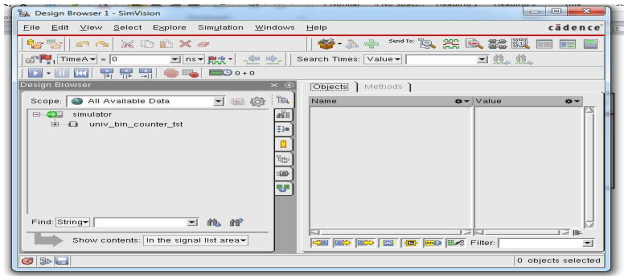
9. Correct the syntax check and save the file.
10. Similarly create the testbench file for design, check syntax and save the file. (Shown below)



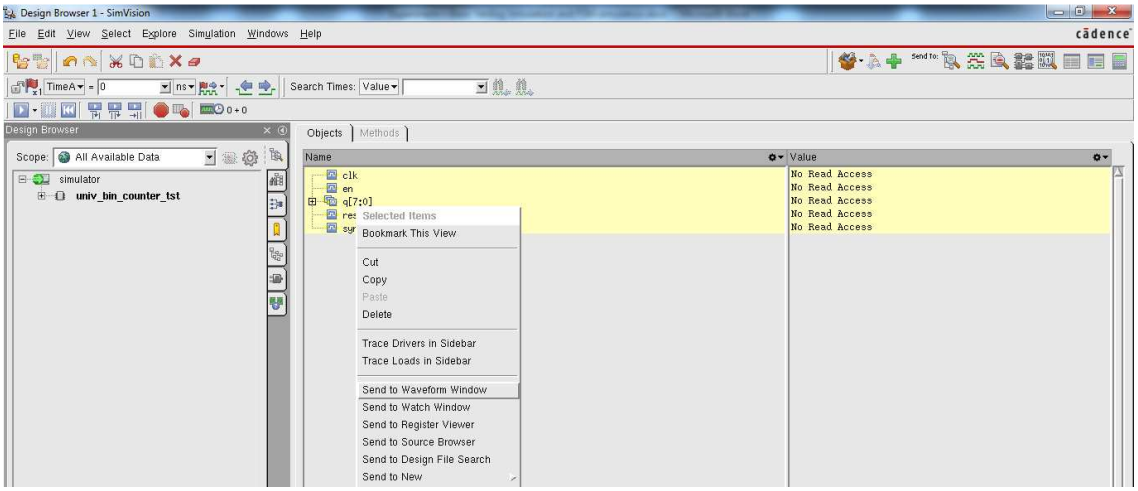
11. Execute the command as below: - ncverilog counter_tst.v counter.v +gui +access+rw



12. Simvision gui will open: -



13. Right click on signals as shown below and send to Waveform Window: -



14. Run the simulation: -

15. Observe the waveforms: -