ASIC Design Lab

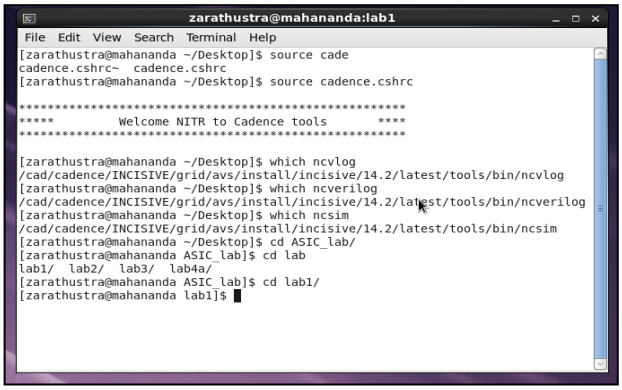
EC 6272, Spring 2019-2020

VLSI Laboratory, ECE Department, NIT Rourkela, India

This tutorial will discuss the various views that make-up an effective RTL design model and then illustrate how to use a Cadence ASIC tools to check an RTL design with simulation, and synthesizing RTL model.
This tutorial requires entering commands manually for each of the tools to enable students to gain a better understanding of the detailed steps involved in this process.

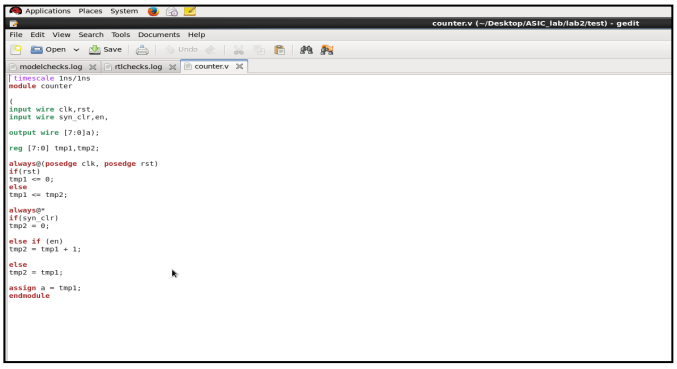
Simulation of Finite State Machine (FSM) based Designs in Verilog HDL.

1. Open the terminal
2. Source the cadence.cshrc
3. Check whether the commands are working as below: -



4. Create a directory for saving files

5. Create design_file.v as shown below: - (gedit counter.v)

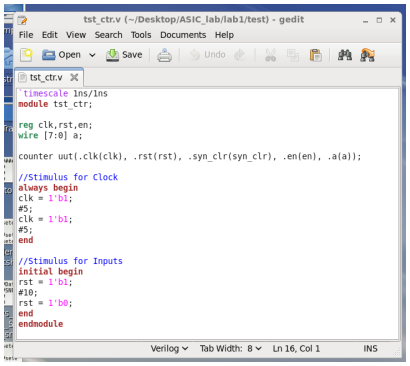


6. Check the syntax of design.v (in this example: counter.v) (no syntax errors found)

7. Induce syntax error in random deliberately and perform syntax check

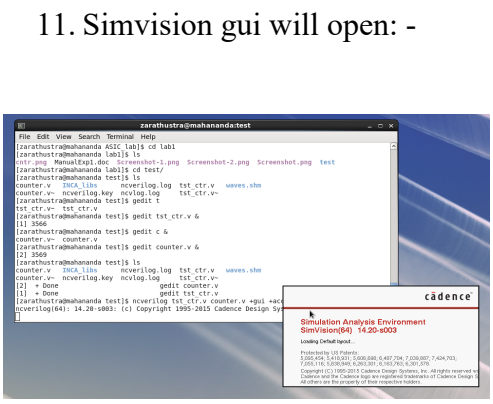
8. Correct the syntax check and save the file.

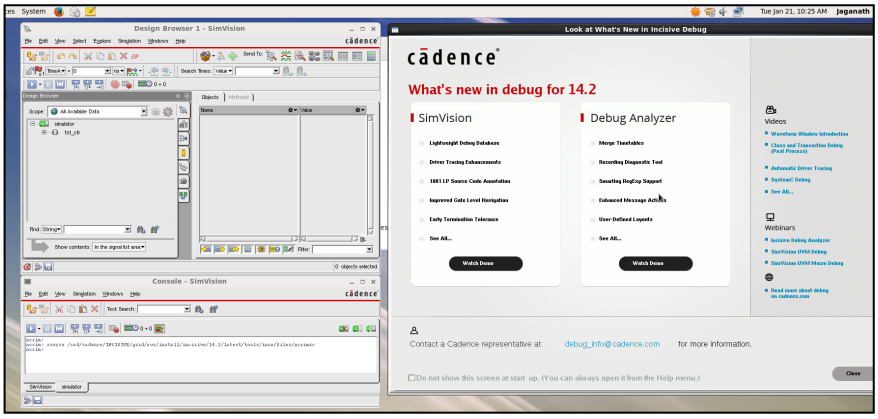
9. Similarly create the testbench file for design, check syntax and save the file. (Shown below)



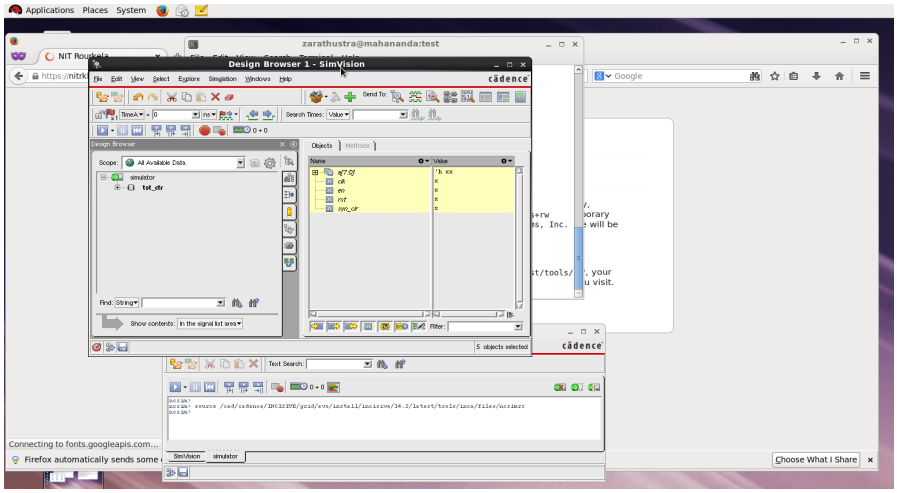
10. Execute the command as below: - ncverilog counter_tst.v counter.v +gui +access+rw

11. Simvision gui will open: -

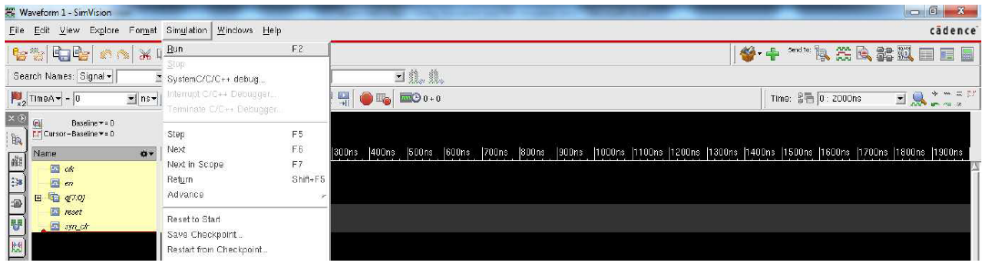




12. Right click on signals as shown below and send to Waveform Window: -



13. Run the simulation: -



14. Observe the waveforms: -