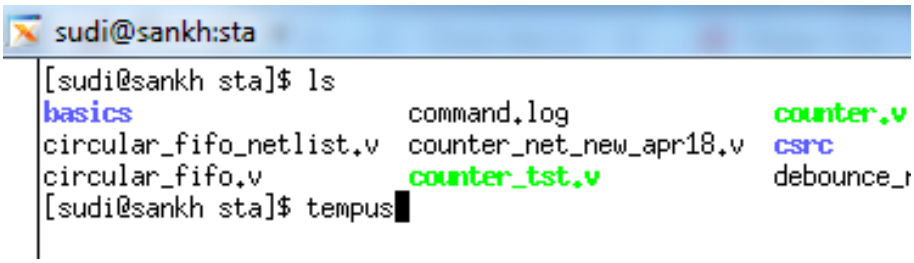
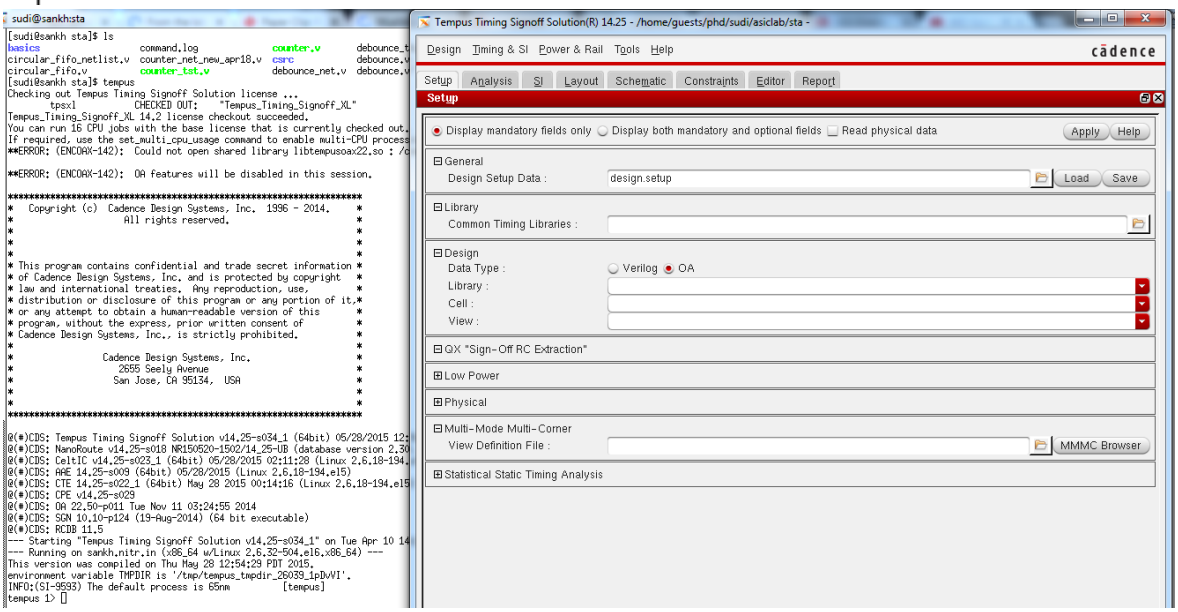
ASIC Design Lab (EC-6272)

Experiment – IX

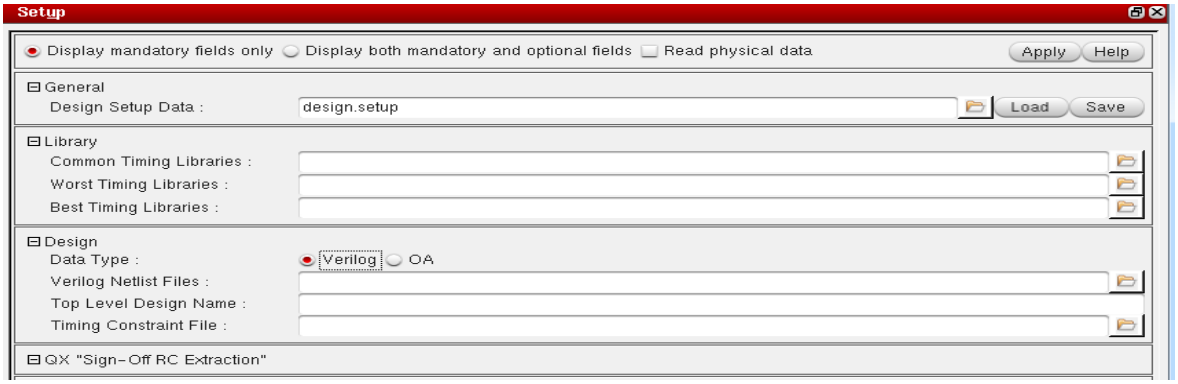
Static Timing Analysis

1. Open the terminal
2. Source the cadence.cshrc
3. In this experiment, we are performing static timing analysis (STA). STA can be performed on both pre-layout and post-layout netlist. In this experiment we perform pre-layout STA. The files required for this experiment is: -
    a. Synthesized netlist (from synthesis tool : Design compiler or RTL compiler)
    b. Timing library files (.lib file used in synthesis in RTL compiler)
4. In a ASIC lab directory, create design_netlist.v using synthesis with constraints.
5. Open the tempus (Cadence STA tool) using command as below: -

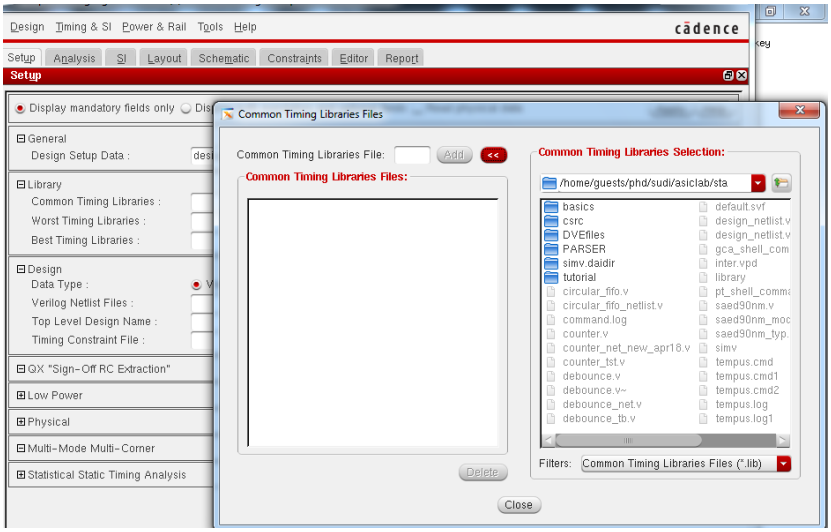


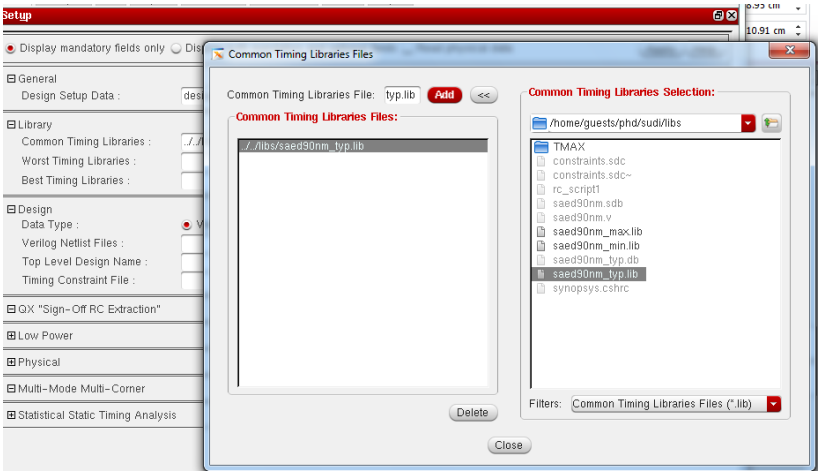


6. Select the: - Display mandatory fields only and Data type to Verilog as below: -

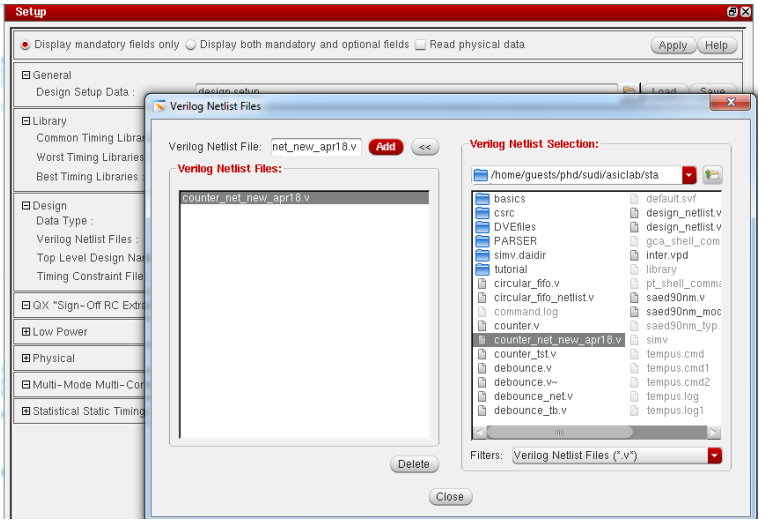


7. Click on common timing libraries, browse and select .lib file used for synthesis from libs folder or where ever you have saved .lib file as below: -

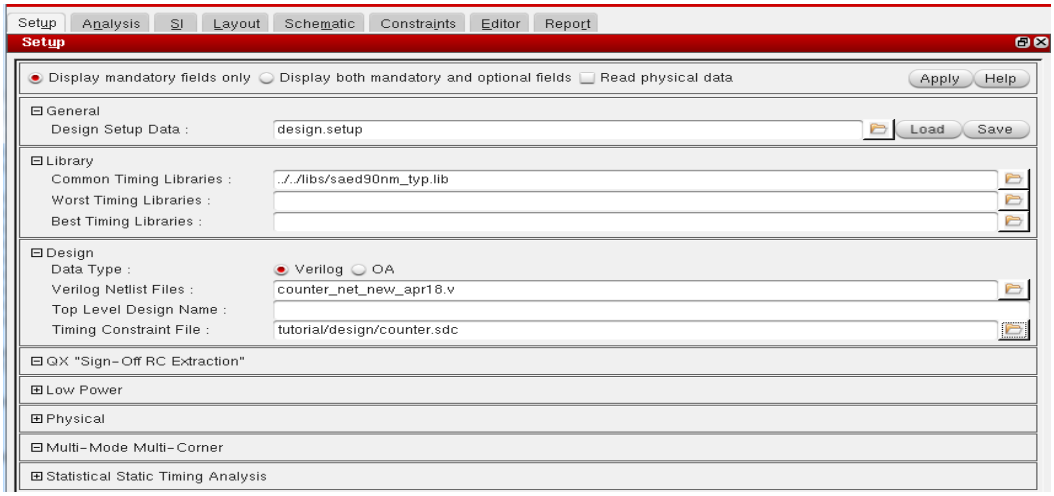




8. Select the gate level netlist as below: -

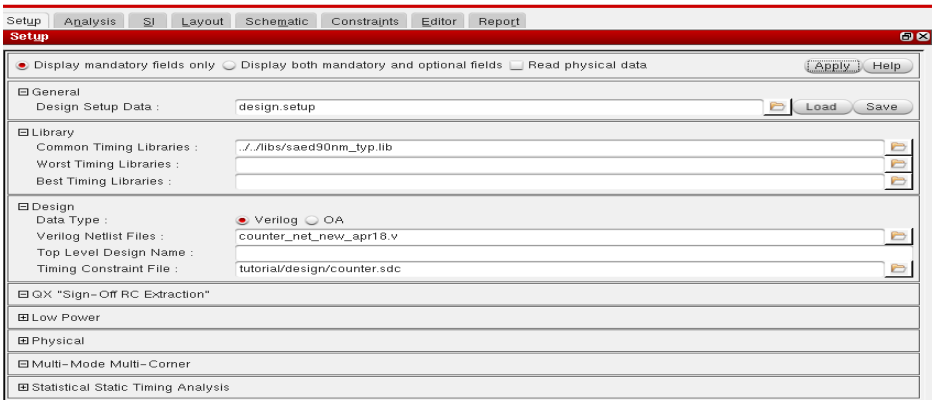


9. Read the timing constraints file as below (constraints are designed for gate level netlist, understand netlist by opening netlist in gedit): -




```
create_clock [get_port clk]  -name clk  -period 20  -waveform {0 10}
set_clock_uncertainty -setup 0.45  [get_clocks clk]
set_input_transition 0.100 [all_inputs]
set_load 0.23 [all_outputs]

set_max_delay 12 -from [get_clocks clk]
set_max_delay 0.05 -from [get_port reset] -to [get_pin r_reg_reg[0]/RSTB]
set_max_delay 0.05 -from [get_port reset] -to [get_pin r_reg_reg[1]/RSTB]
set_max_delay 0.05 -from [get_port reset] -to [get_pin r_reg_reg[2]/RSTB]
set_max_delay 0.05 -from [get_port reset] -to [get_pin r_reg_reg[3]/RSTB]
set_max_delay 0.05 -from [get_port reset] -to [get_pin r_reg_reg[4]/RSTB]
set_max_delay 0.05 -from [get_port reset] -to [get_pin r_reg_reg[5]/RSTB]
set_max_delay 0.05 -from [get_port reset] -to [get_pin r_reg_reg[6]/RSTB]
set_max_delay 0.05 -from [get_port reset] -to [get_pin r_reg_reg[7]/RSTB]

set_max_delay 0.05 -from [get_port en] -to [get_pin U3/IN4]
set_max_delay 0.05 -from [get_port en] -to [get_pin U4/IN4]
set_max_delay 0.05 -from [get_port en] -to [get_pin U5/IN4]
set_max_delay 0.05 -from [get_port en] -to [get_pin U6/IN4]
set_max_delay 0.05 -from [get_port en] -to [get_pin U7/IN4]
set_max_delay 0.05 -from [get_port en] -to [get_pin U8/IN4]
set_max_delay 0.05 -from [get_port en] -to [get_pin U9/IN4]
set_max_delay 0.05 -from [get_port en] -to [get_pin U10/IN4]

set_max_delay 0.05 -from [get_port syn_clr] -to [get_pin U3/IN2]
set_max_delay 0.05 -from [get_port clk] -to [get_pin r_reg_reg[0]/D]
set_max_delay 0.05 -from [get_port clk] -to [get_pin r_reg_reg[1]/D]
set_max_delay 0.05 -from [get_port clk] -to [get_pin r_reg_reg[2]/D]
set_max_delay 0.05 -from [get_port clk] -to [get_pin r_reg_reg[3]/D]
set_max_delay 0.05 -from [get_port clk] -to [get_pin r_reg_reg[4]/D]
set_max_delay 0.05 -from [get_port clk] -to [get_pin r_reg_reg[5]/D]
set_max_delay 0.05 -from [get_port clk] -to [get_pin r_reg_reg[6]/D]
set_max_delay 0.05 -from [get_port clk] -to [get_pin r_reg_reg[7]/D]

set_output_delay 3.5 [list [get_ports {q[0]}] [get_ports {q[1]}] [get_ports {q[2]}] [get_ports {q[3]}] [get_ports {q[4]}] [get_ports {q[5]}] [get_ports {q[6]}]
[get_ports {q[7]}]]
```

10. Click on Apply: -



11. Go to terminal and type report_timing as below: -

```
tempus 1>
tempus 1>
tempus 1> report_timing
################################################################
#   Generated by:         Cadence Tempus 14.25-s034_1
#   OS:                   Linux x86_64(Host ID sankh.nitr.in)
#   Generated on:         Tue Apr 10 14:53:11 2018
#   Design:               univ_bin_counter
#   Command:              report_timing
################################################################
################################################################################
# Design Mode: 65nm
# Analysis Mode: MMMC OCV
# Extraction Mode: default
# Delay Calculation Options: engine=aae SIAware=false(signoff)
# Switching Delay Calculation Engine to AAE
################################################################################
Topological Sorting (CPU = 0:00:00.0, MEM = 525.9M, InitMEM = 525.9M)
AAE_MTTC: End Timing Check Calculation. (CPU Time=0:00:00.0, Real Time=0:00:00.0)
AAE_THRD: End delay calculation. (MEM=651.039 CPU=0:00:00.0 REAL=0:00:00.0)
*** CDM Built up (cpu=0:00:00.3  real=0:00:00.0  mem= 651.0M) ***
Path 1: VIOLATED Recovery Check with Pin r_reg_reg[0]/CLK
Endpoint:   r_reg_reg[0]/RSTB (^) checked with  leading edge of 'clk'
Beginpoint: reset             (v) triggered by  leading edge of '@'
Path Groups: {async_default}
Other End Arrival Time          0.000
- Recovery                     -0.115
+ Path Delay                    0.050
- Uncertainty                   0.450
= Required Time                -0.285
- Arrival Time                  0.109
= Slack Time                   -0.394
     Clock Rise Edge                      0.000
     + Input Delay                        0.000
     = Beginpoint Arrival Time            0.000
     ---------------------------------------------------------------------------------------
      Instance             Arc              Cell              Delay    Arrival    Required
                                                                       Time       Time
     ---------------------------------------------------------------------------------------
                           reset v                                     0.000      -0.394
     U18                   INP v -> ZN ^    INVX0             0.109    0.109      -0.285
     r_reg_reg[0]          RSTB ^           DFFARX1           0.000    0.109      -0.285
     ---------------------------------------------------------------------------------------

tempus 2>
```

12. Observe that slack is negative. So open the timing cosntraints file. Increase the clk period to 40 in the constraints file as : -

```
create_clock [get_port clk]  -name clk  -period 40  -waveform {0 10}
set_clock_uncertainty -setup 0.45  [get_clocks clk]
set_input_transition 0.100 [all_inputs]
```

Save the constraints file. Click on browse to timing constraints file and delete the constraints file and reselect the saved file (updated with clk period 40 or 80). Just remove all set_max and other constraints and just keep the only two statements related to clk as below :-

```
create_clock [get_port clk]  -name clk  -period 80  -waveform {0 10}
set_clock_uncertainty -setup 0.45  [get_clocks clk]
```

13. Report_timing in tempus and find positive slack: -

```
tempus 1>
tempus 1> report_timing
################################################################
#   Generated by:         Cadence Tempus 14.25-s034_1
#   OS:                   Linux x86_64(Host ID sankh.nitr.in)
#   Generated on:         Tue Apr 10 15:16:36 2018
#   Design:               univ_bin_counter
#   Command:              report_timing
################################################################
################################################################################
# Design Mode: 65nm
# Analysis Mode: MMMC OCV
# Extraction Mode: default
# Delay Calculation Options: engine=aae SIAware=false(signoff)
# Switching Delay Calculation Engine to AAE
################################################################################
Topological Sorting (CPU = 0:00:00.0, MEM = 496.5M, InitMEM = 495.5M)
AAE_MTTC: End Timing Check Calculation. (CPU Time=0:00:00.0, Real Time=0:00:00.0)
AAE_THRD: End delay calculation. (MEM=636.672 CPU=0:00:00.0 REAL=0:00:00.0)
*** CDM Built up (cpu=0:00:00.2  real=0:00:01.0  mem= 636.7M) ***
Path 1: MET Setup Check with Pin r_reg_reg[7]/CLK
Endpoint:   r_reg_reg[7]/D (^) checked with  leading edge of 'clk'
Beginpoint: r_reg_reg[1]/Q (v) triggered by  leading edge of 'clk'
Path Groups: {clk}
Other End Arrival Time          0.000
- Setup                         0.086
+ Phase Shift                  80.000
- Uncertainty                   0.450
= Required Time                79.464
- Arrival Time                  0.876
= Slack Time                   78.589
     Clock Rise Edge                      0.000
     + Clock Network Latency (Ideal)      0.000
     = Beginpoint Arrival Time            0.000
     --------------------------------------------------------------------------
      Instance             Arc              Cell              Delay    Arri
                                                                       Time
     --------------------------------------------------------------------------
     r_reg_reg[1]          CLK ^                                       0.000
     r_reg_reg[1]          CLK ^ -> Q v     DFFARX1           0.196    0.196
     add_24/U1_1_1         A0 v -> C1 v     HADDX1            0.094    0.289
     add_24/U1_1_2         B0 v -> C1 v     HADDX1            0.089    0.378
     add_24/U1_1_3         B0 v -> C1 v     HADDX1            0.089    0.467
     add_24/U1_1_4         B0 v -> C1 v     HADDX1            0.089    0.556
     add_24/U1_1_5         B0 v -> C1 v     HADDX1            0.089    0.645
     add_24/U1_1_6         B0 v -> C1 v     HADDX1            0.091    0.736
     add_24/U2             IN1 v -> Q ^     XOR2X1            0.062    0.798
     U3                    IN1 ^ -> Q ^     AO22X1            0.078    0.876
     r_reg_reg[7]          D ^              DFFARX1           0.000    0.876
     --------------------------------------------------------------------------

tempus 2>
```

14. Keep experiment with adding set_max constraints and work out a optimal postive slack.