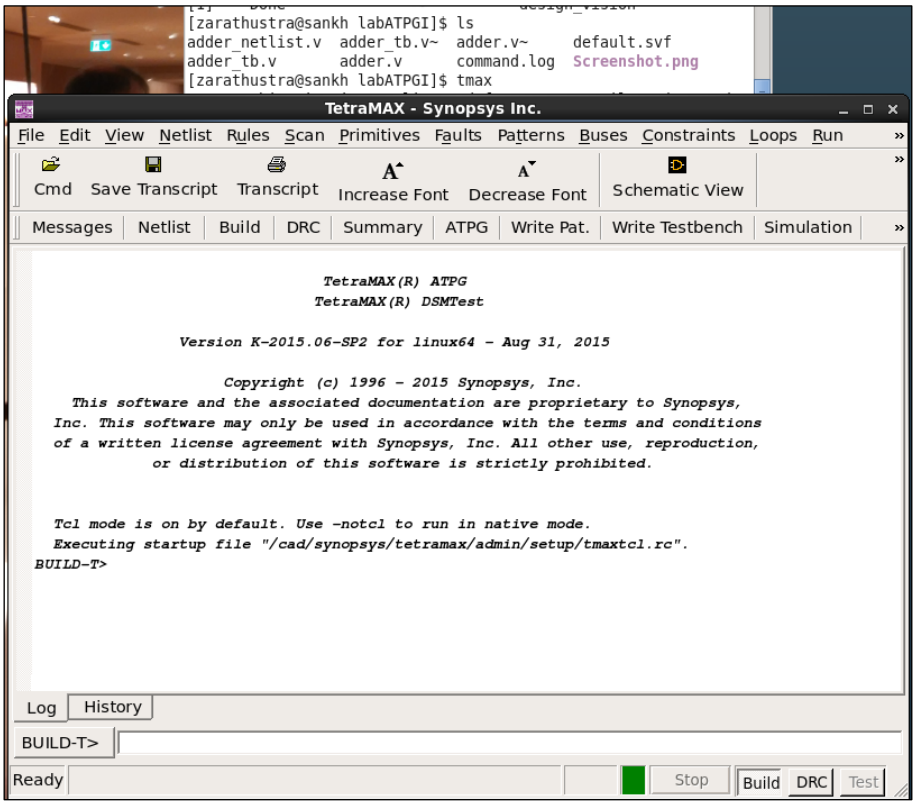
ASIC Design Lab (EC-6272)
Experiment – VII A
Synopsys ATPG Tools

In this laboratory session, we will perform ATPG (Automatic Test Pattern Generation) tool training and explore the tool for a combinational circuit design.

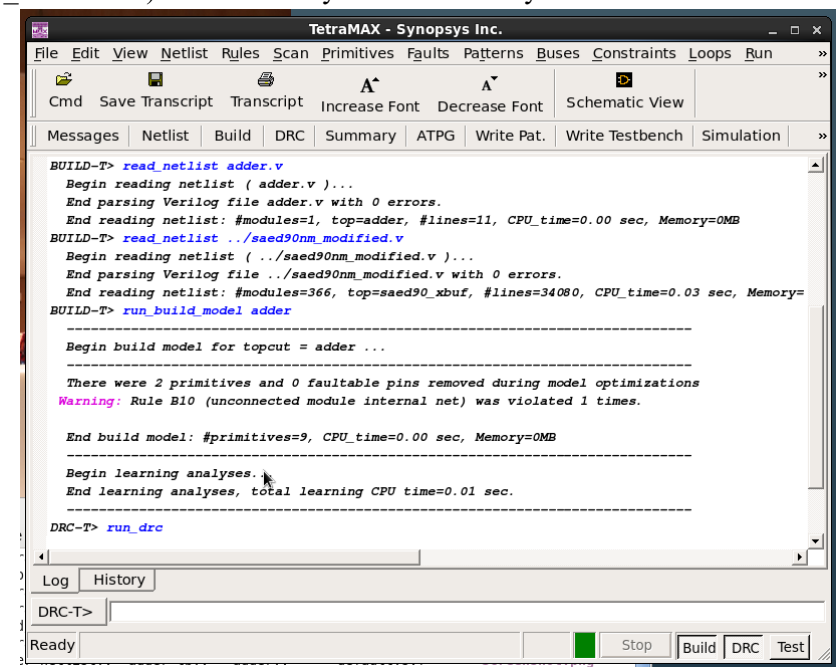
1. Open the terminal
2. Source the synopsys.cshrc
3. Check whether the commands are working as below. Terminal will echo the installation path of tools

```
File  Edit  View  Search  Terminal  Help
[zarathustra@sankh labATPGI]$ source ~/synopsys.cshrc
[zarathustra@sankh labATPGI]$ which tmax
/cad/synopsys/tetramax/bin/tmax
[zarathustra@sankh labATPGI]$ ls
adder_tb.v  adder_tb.v~  adder.v  adder.v~
[zarathustra@sankh labATPGI]$
```

4. In a ASIC lab directory, make design.v (any combinational circuit)
5. Synthesize the combinational circuit in design_vision (without constraints and/or you can do with constraints also). Follow the steps described in synthesis experiment. Save the netlist in verilog format.
6. Open Tetramax tool (Synopsys ATPG tool).



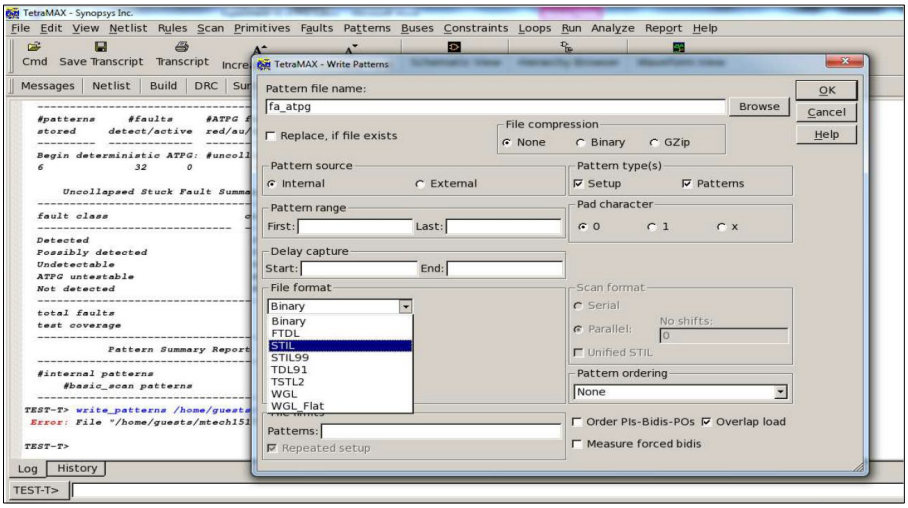
7. Read design_netlist.v (combinational circuit synthesized in design_vision) and library.v (saed90nm_modified.v). Available in your libs directory.



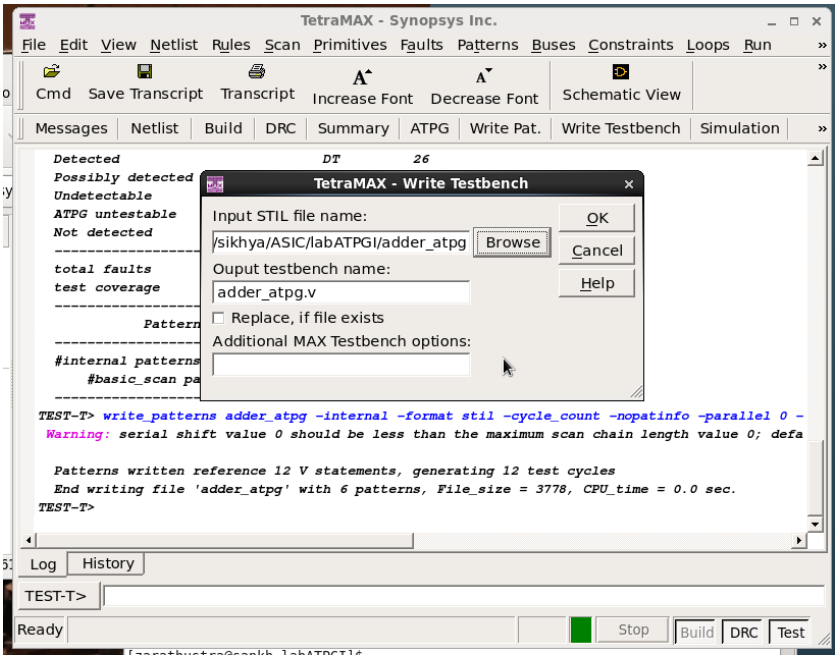
8. Execute the following commands in Tmax command line: -

```
1  read_netlist /home/zarathustra/sikhya/ASIC/labATPGI/adder_netlist.v
2  read_netlist /home/zarathustra/sikhya/ASIC/saed90nm_modified.v
3  run_build_model adder
4  run_drc
5  add_faults -all
6  run_atpg -ndetects 1
```

9. Select and Save the patterns in the form of STIL format. (as shown below): - (click on write_patterns to get below window)



10. Click on the Write Testbench on browse on point to fa_atpg file and give a output file name as adder_atpg.v .



11. Exit Tetramax and simulate the atpg with the command shown in figure below

12. Observe the executable file “simv” created as before and execute simv (./simv –gui) to verify the simulation.