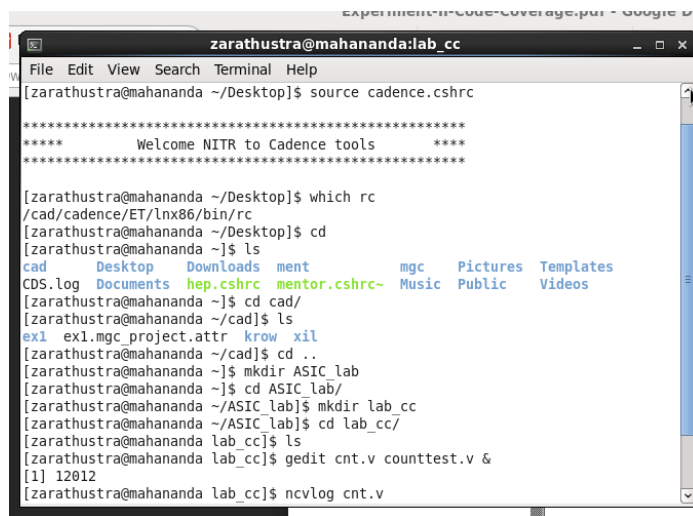


ASIC Design Lab (EC-6272)

Experiment – III

Code Coverage

1. Open the terminal
2. Source the cadence.cshrc
3. Check whether the commands are working as below. Make a working folder, script the verilog RTL and testbench, as below. Check for syntax errors and carry ahead with simulation following the next step.



```

zarathustra@mahananda:lab_cc
File Edit View Search Terminal Help
[zarathustra@mahananda ~/Desktop]$ source cadence.cshrc
*****
***** Welcome NITR to Cadence tools *****
*****

[zarathustra@mahananda ~/Desktop]$ which rc
/cad/cadence/ET/lnx86/bin/rc
[zarathustra@mahananda ~/Desktop]$ cd
[zarathustra@mahananda ~]$ ls
cad Desktop Downloads ment mgc Pictures Templates
CDS.log Documents hep.cshrc mentor.cshrc- Music Public Videos
[zarathustra@mahananda ~]$ cd cad/
[zarathustra@mahananda ~/cad]$ ls
exl exl.mgc_project.attr krow xil
[zarathustra@mahananda ~/cad]$ cd ..
[zarathustra@mahananda ~]$ mkdir ASIC_lab
[zarathustra@mahananda ~]$ cd ASIC_lab/
[zarathustra@mahananda ~/ASIC_lab]$ mkdir lab_cc
[zarathustra@mahananda ~/ASIC_lab]$ cd lab_cc/
[zarathustra@mahananda lab_cc]$ ls
[zarathustra@mahananda lab_cc]$ gedit cnt.v counttest.v &
[1] 12012
[zarathustra@mahananda lab_cc]$ ncvlog cnt.v

```

4. Execute the following commands for coverage in the terminal
ncverilog design_file.v testbench_file.v +gui +access+rw +nccoverage+all



```

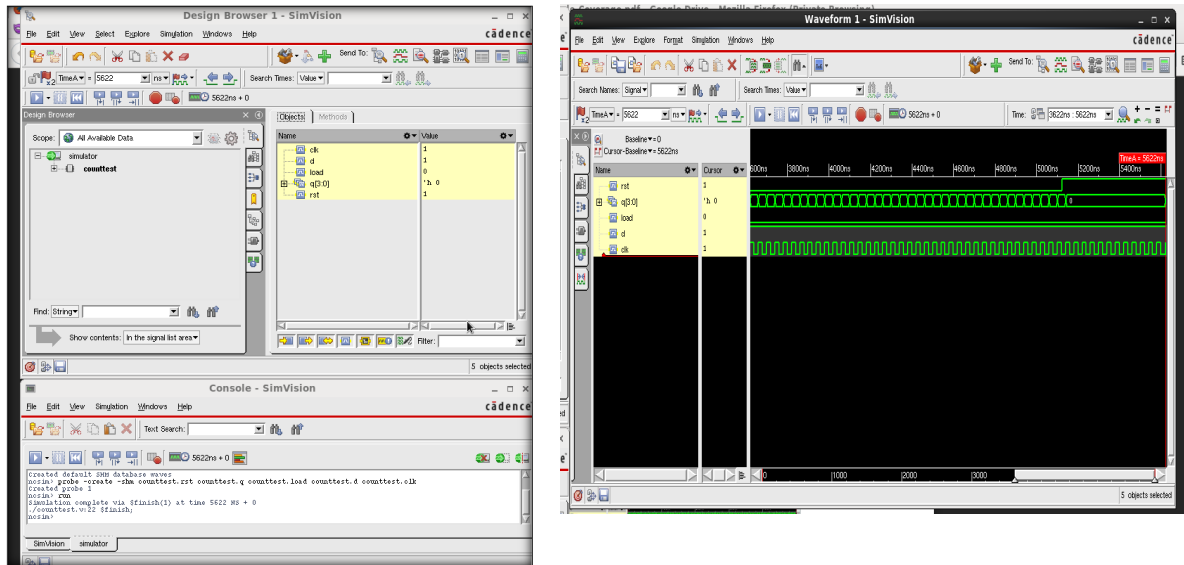
Experiment-II-Code-Coverage.pat - Google Drive - Mozilla Firefox
zarathustra@mahananda:lab_cc
File Edit View Search Terminal Help
ncvlog(64): 14.20-s003: (c) Copyright 1995-2015 Cadence Design Systems, Inc.
[zarathustra@mahananda lab_cc]$ ncverilog counttest.v cnt.v +gui +access+rw +nccoverage+all
ncvlog(64): 14.20-s003: (c) Copyright 1995-2015 Cadence Design Systems, Inc.
file: counttest.v
  module worklib.counttest:v
    errors: 0, warnings: 0
file: cnt.v
  module worklib.cnt:v
    errors: 0, warnings: 0
    Caching library 'worklib' ..... Done
  Elaborating the design hierarchy:

  Extracting FSMs for coverage:
    worklib.cnt
    worklib.counttest
  Total FSMs extracted = 0
cnt al(clk, rst, d,q,load);
nclab: *W,CUVMPW (./counttest.v,5[17]: port sizes differ in port connection (1/4).
Building instance overlay tables: ..... Done
Enabling instrumentation for coverage types: block expression FSM toggle functional
Generating native compiled code:
  worklib.cnt:v <0x3e481147>
    streams: 4, words: 2058
  worklib.counttest:v <0x2bf0637b>
    streams: 7, words: 4651
Building instance specific data structures.
Loading native compiled code: ..... Done
Design hierarchy summary:

      Instances Unique
Modules:      2      2
Registers:    6      6

```

5. Simulate completely



6. Observe the “cov_work” folder in the directory

```

zarathustra@mahananda:lab_cc
File Edit View Search Terminal Help

Scalar wires:      3      -
Vectored wires:   2      -
Always blocks:    2      2
Initial blocks:   1      1
Pseudo assignments: 4      4
Simulation timescale: 1ns
Writing initial simulation snapshot: worklib.counttest.v

-----
Relinquished control to SimVision...
ncsim> source /cad/cadence/INCISIVE/grid/avs/install/incisive/14.2/latest/tools/inca/files/ncs
imrc
ncsim> ...Regained control from SimVision

coverage setup:
workdir : ./cov_work
dutinst : counttest(counttest)
scope : scope
testname : test

coverage files:
model(design data) : ./cov_work/scope/icc_4a8a4bdb_00000000.ucm
data : ./cov_work/scope/test/icc_4a8a4bdb_00000000.ucd
[zarathustra@mahananda lab_cc]$ ls
cnt.v      INCA_libs  ncverilog.log  Screenshot02.png  waves.shm
counttest.v  ncverilog.key  Screenshot00.png  Screenshot03.png
cov_work    ncverilog.log  Screenshot01.png  Screenshot0.png
[zarathustra@mahananda lab_cc]$

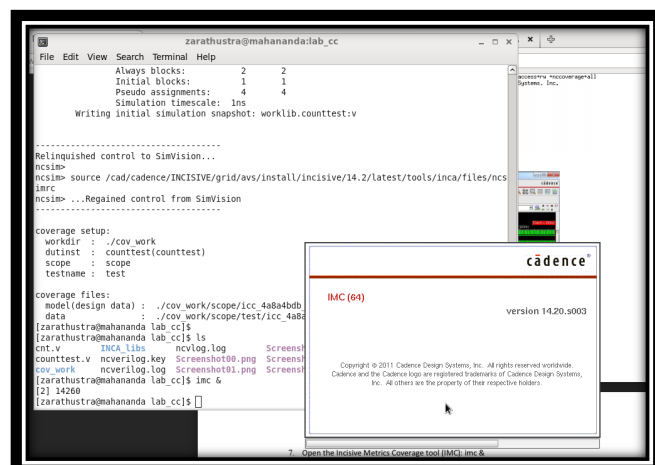
```

7. Open the Incisive Metrics Coverage tool (IMC) in the terminal
imc &

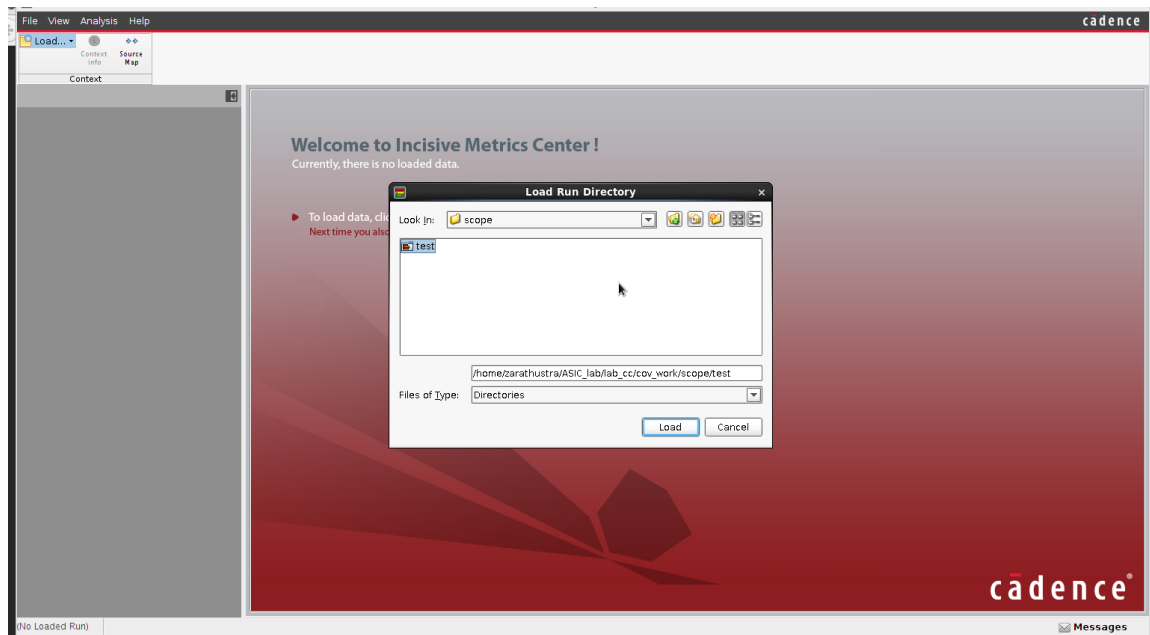
```

model(design data) : ./cov_work/scope/icc_4a8a4bdb
data : ./cov_work/scope/test/icc_4a8a4bdb
[zarathustra@mahananda lab_cc]$ ls
cnt.v      INCA_libs  ncverilog.log  Screenshot02.png  waves.shm
counttest.v  ncverilog.key  Screenshot00.png  Screenshot03.png
cov_work    ncverilog.log  Screenshot01.png  Screenshot0.png
[zarathustra@mahananda lab_cc]$ imc &
[2] 14260
[zarathustra@mahananda lab_cc]$

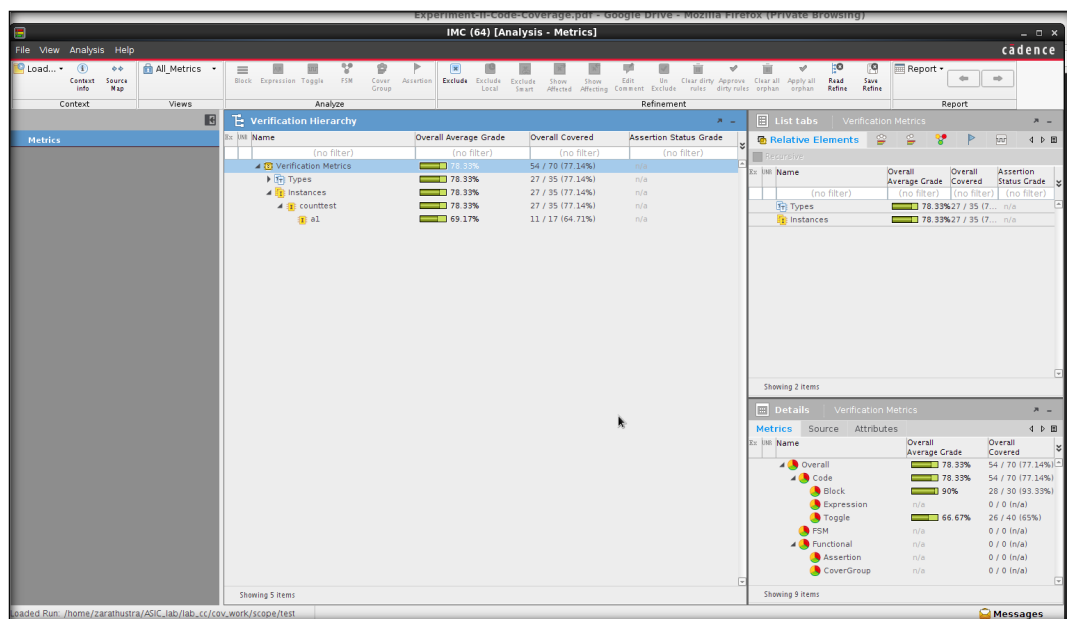
```



8. Load the test file from the folder “cov_work”



9. IMC opens the coverage metrics analysis



10. Write better testbenches for all the designs : - Counter, FIFO, Debouncing circuit, Edge detector to get 96% coverage in all categories: - FSM, toggle, block and expression.