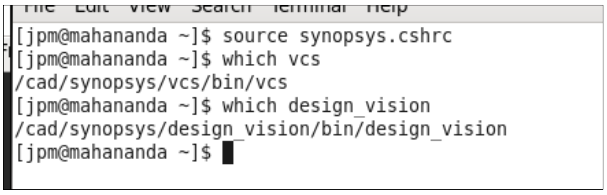
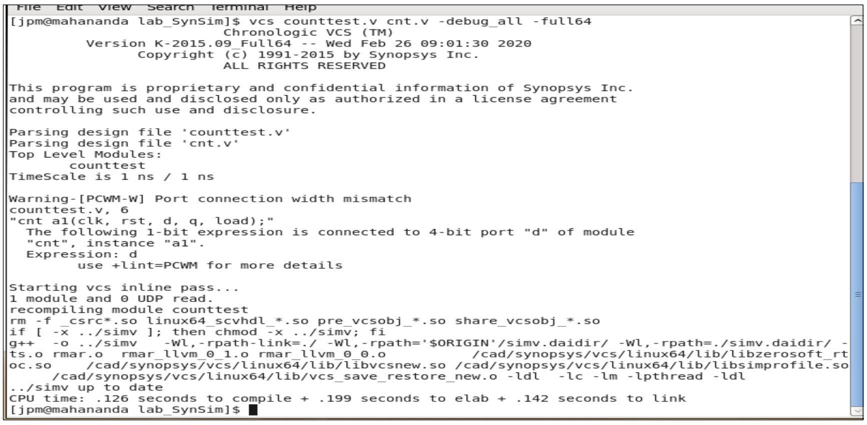
ASIC Design Lab (EC-6272)
Experiment – VI
Synopsys Simulation and Synthesis Tools

1. Open the terminal
2. Source the synopsys.cshrc
3. Check whether the commands are working as below. Terminal will echo the installation path of tools as below.



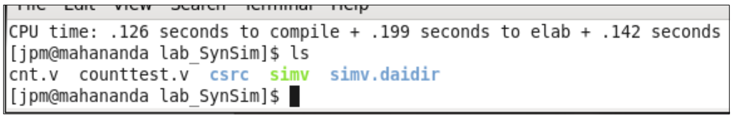
```
[jpm@mahananda ~]$ source synopsys.cshrc
[jpm@mahananda ~]$ which vcs
/cad/synopsys/vcs/bin/vcs
[jpm@mahananda ~]$ which design_vision
/cad/synopsys/design_vision/bin/design_vision
[jpm@mahananda ~]$ █
```

4. Create a directory for saving files as below and simulate using VCS (VCS is simulation tool from synopsys similar to cadence ncverilog (ncsim) . The command line is shown below: -



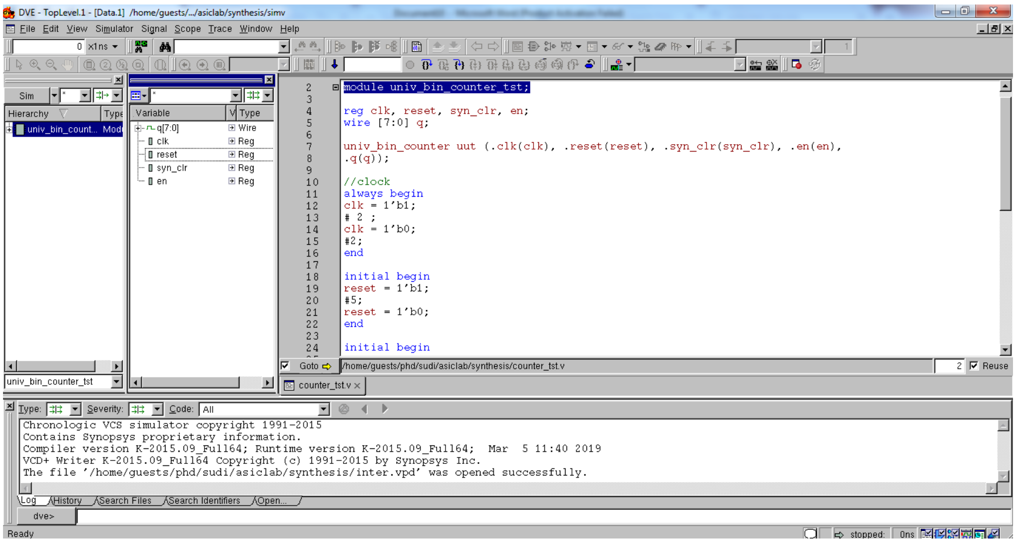
```
[jpm@mahananda lab_SynSim]$ vcs counttest.v cnt.v -debug_all -full64
                         Chronologic VCS (TM)
         Version K-2015.09_Full64 -- Wed Feb 26 09:01:30 2020
               Copyright (c) 1991-2015 by Synopsys Inc.
                         ALL RIGHTS RESERVED

This program is proprietary and confidential information of Synopsys Inc.
and may be used and disclosed only as authorized in a license agreement
controlling such use and disclosure.

Parsing design file 'counttest.v'
Parsing design file 'cnt.v'
Top Level Modules:
       counttest
TimeScale is 1 ns / 1 ns

Warning-[PCWM-W] Port connection width mismatch
counttest.v, 6
"cnt a1(clk, rst, d, q, load);"
  The following 1-bit expression is connected to 4-bit port "d" of module
  "cnt", instance "a1".
  Expression: d
        use +lint=PCWM for more details

Starting vcs inline pass...
1 module and 0 UDP read.
recompiling module counttest
rm -f _csrc*.so linux64_scvhdl_*.so pre_vcsobj_*.so share_vcsobj_*.so
if [ -x ../simv ]; then chmod -x ../simv; fi
g++  -o ../simv   -Wl,-rpath-link=./ -Wl,-rpath='$ORIGIN'/simv.daidir/ -Wl,-rpath=./simv.daidir/ -
ts.o rmar.o  rmar_llvm_0_1.o rmar_llvm_0_0.o          /cad/synopsys/vcs/linux64/lib/libzerosoft_rt
oc.so    /cad/synopsys/vcs/linux64/lib/libvcsnew.so /cad/synopsys/vcs/linux64/lib/libsimprofile.so
    /cad/synopsys/vcs/linux64/lib/vcs_save_restore_new.o -ldl  -lc -lm -lpthread -ldl
../simv up to date
CPU time: .126 seconds to compile + .199 seconds to elab + .142 seconds to link
[jpm@mahananda lab_SynSim]$ █
```

5. Observe the executable file "simv" is created as shown below and execute simv. (./simv –gui)



```
CPU time: .126 seconds to compile + .199 seconds to elab + .142 seconds
[jpm@mahananda lab_SynSim]$ ls
cnt.v  counttest.v  csrc  simv  simv.daidir
[jpm@mahananda lab_SynSim]$ █
```

6. Execution will open a simulation tool as below: -

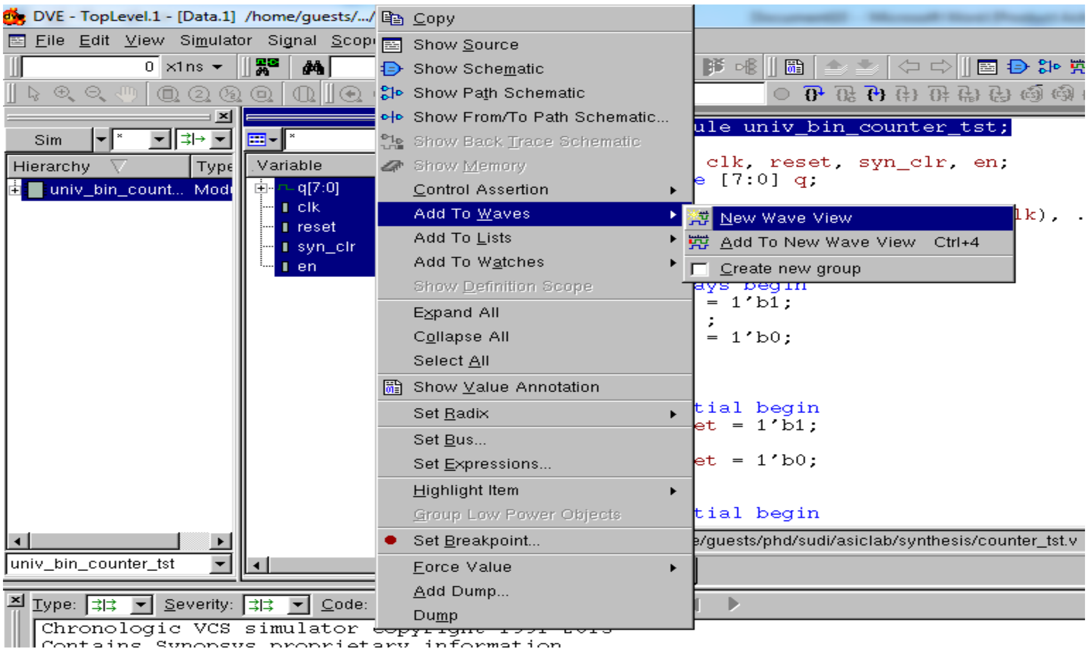


```
module univ_bin_counter_tst;

reg clk, reset, syn_clr, en;
wire [7:0] q;

univ_bin_counter uut (.clk(clk), .reset(reset), .syn_clr(syn_clr), .en(en),
.q(q));

//clock
always begin
clk = 1'b1;
# 2 ;
clk = 1'b0;
#2;
end

initial begin
reset = 1'b1;
#5;
reset = 1'b0;
end

initial begin
```

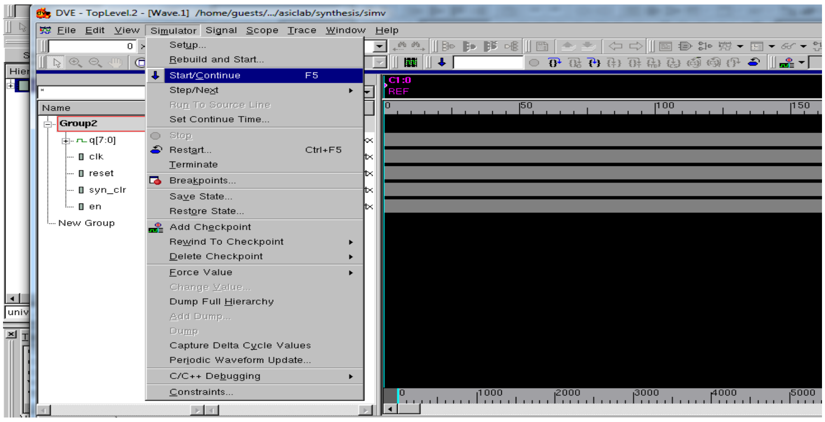
/home/guests/phd/sudi/asiclab/synthesis/counter_tst.v

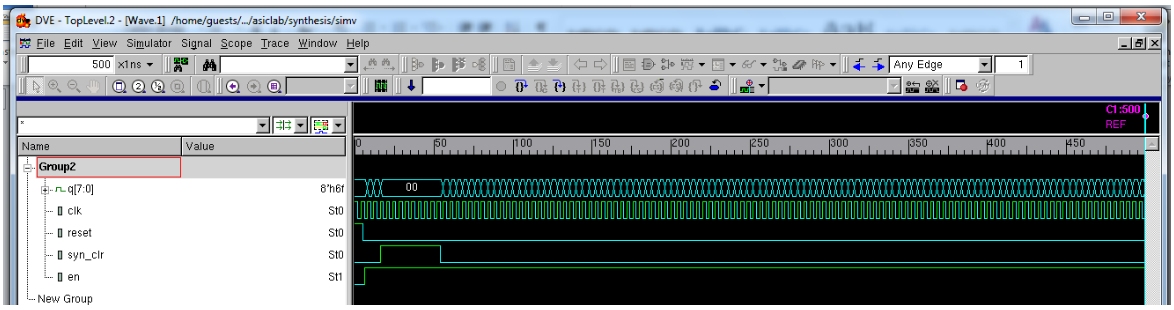
```
Chronologic VCS simulator copyright 1991-2015
Contains Synopsys proprietary information.
Compiler version K-2015.09_Full64; Runtime version K-2015.09_Full64;  Mar  5 11:40 2019
VCD+ Writer K-2015.09_Full64 Copyright (c) 1991-2015 by Synopsys Inc.
The file '/home/guests/phd/sudi/asiclab/synthesis/inter.vpd' was opened successfully.
```

7. Select the signals and send them to waveform window as below: -



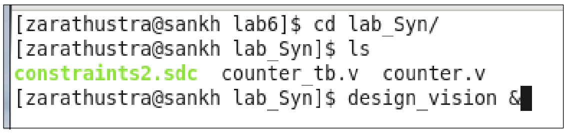
8. Run the simulation as below: -




DVE - TopLevel.2 - [Wave.1] /home/guests/.../asiclab/synthesis/simv
File Edit View Simulator Signal Scope Trace Window Help
500 x1ns
Any Edge
Name
Value
Group2
q[7:0] 8'h6f
clk St0
reset St0
syn_clr St0
en St1
New Group
C1:500
REF
00

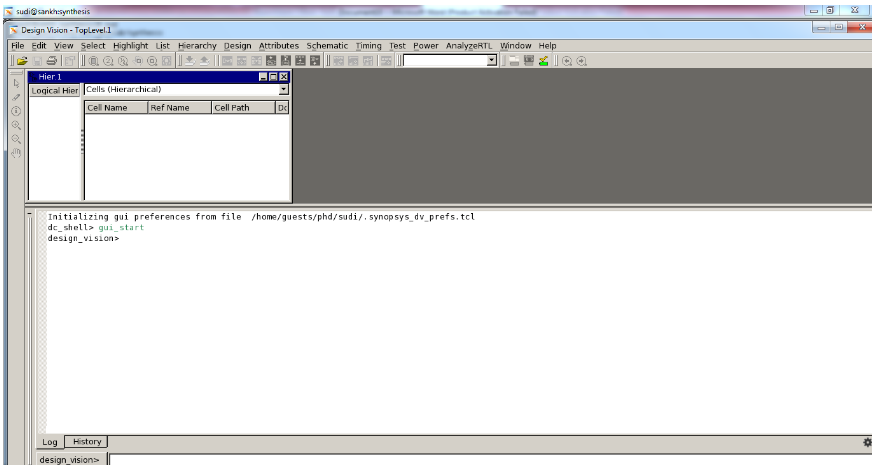
9. Similarly we can simulate all the designs using Synopsys VCS and perform coverge anlaysis using cmView.

10. Synthesis: - Create a directory for saving files as below and Invoke the design_vision tool as below: -



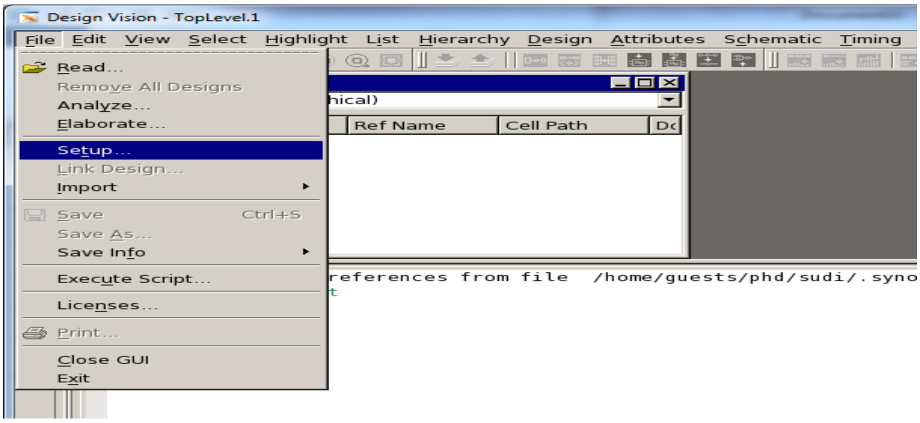
```
[zarathustra@sankh lab6]$ cd lab_Syn/
[zarathustra@sankh lab_Syn]$ ls
constraints2.sdc  counter_tb.v  counter.v
[zarathustra@sankh lab_Syn]$ design_vision &
```

Synopsys_Design_Vision_Tool

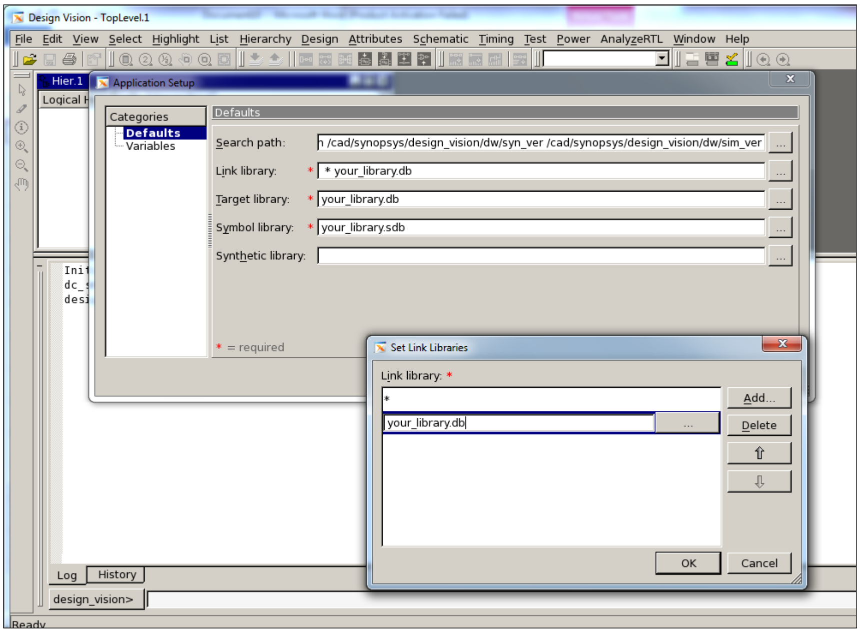

sudi@sankh:synthesis
Design Vision - TopLevel.1
File Edit View Select Highlight List Hierarchy Design Attributes Schematic Timing Test Power AnalyzeRTL Window Help
Hier.1
Logical Hier
Cells (Hierarchical)
Cell Name
Ref Name
Cell Path
Dc
Log
History
design_vision>

```
Initializing gui preferences from file  /home/guests/phd/sudi/.synopsys_dv_prefs.tcl
dc_shell> gui_start
design_vision>
```

11. Add the libraries, (similar to .lib files used in Cadence genus). Here we add .db and .sdb files as below: -



```
references from file  /home/guests/phd/sudi/.syno
```


Design Vision - TopLevel.1
File Edit View Select Highlight List Hierarchy Design Attributes Schematic Timing Test Power AnalyzeRTL Window Help
Hier.1
Logical H
Application Setup
Categories
Defaults
Variables
Defaults
Set Link Libraries
Add...
Delete
OK
Cancel
Log
History
design_vision>
Ready

Search path: h /cad/synopsys/design_vision/dw/syn_ver /cad/synopsys/design_vision/dw/sim_ver

Link library: * * your_library.db

Target library: * your_library.db

Symbol library: * your_library.sdb

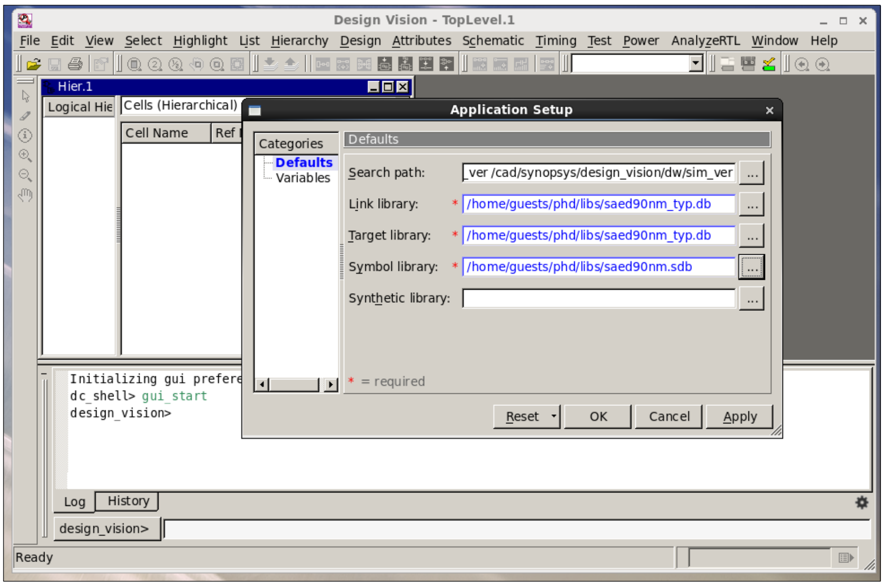
Synthetic library:

* = required

Link library: *

*

your_library.db


Design Vision - TopLevel.1
File Edit View Select Highlight List Hierarchy Design Attributes Schematic Timing Test Power AnalyzeRTL Window Help
Hier.1
Logical Hie
Cells (Hierarchical)
Cell Name
Ref
Application Setup
Categories
Defaults
Variables
Log
History
Reset
OK
Cancel
Apply
Ready

Defaults

Search path: ver /cad/synopsys/design_vision/dw/sim_ver

Link library: * /home/guests/phd/libs/saed90nm_typ.db

Target library: * /home/guests/phd/libs/saed90nm_typ.db

Symbol library: * /home/guests/phd/libs/saed90nm.sdb

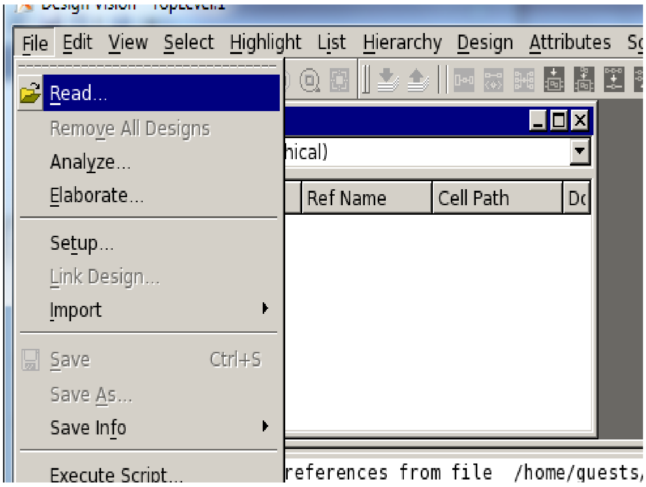
Synthetic library:

* = required

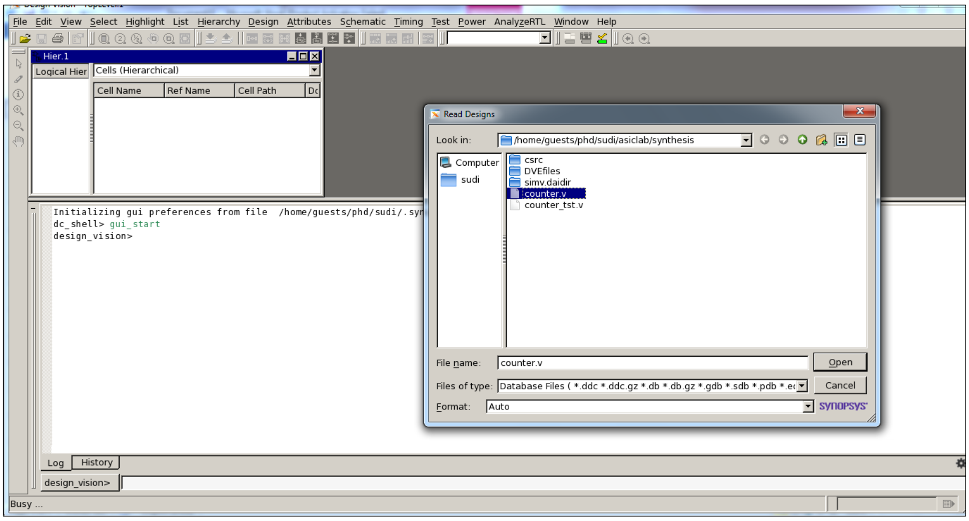
```
Initializing gui prefere
dc_shell> gui_start
design_vision>
```

(Click on Ok)

12. Read the design (design.v):-



```
references from file  /home/guests/
```



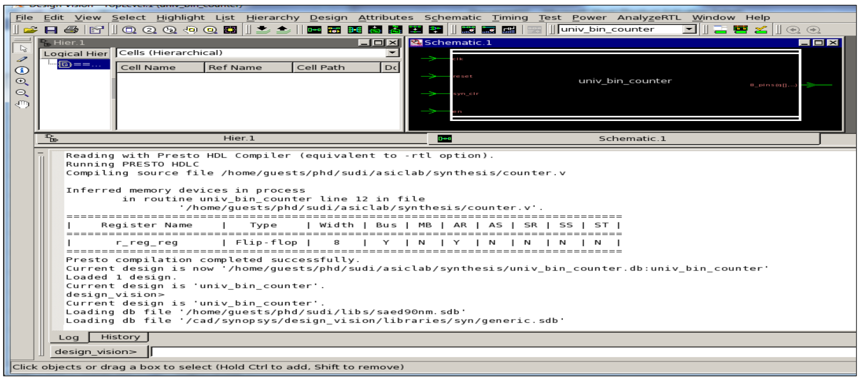
Look in: /home/guests/phd/sudi/asiclab/synthesis

File name: counter.v

Files of type: Database Files (*.ddc *.ddc.gz *.db *.db.gz *.gdb *.sdb *.pdb *.e

Format: Auto

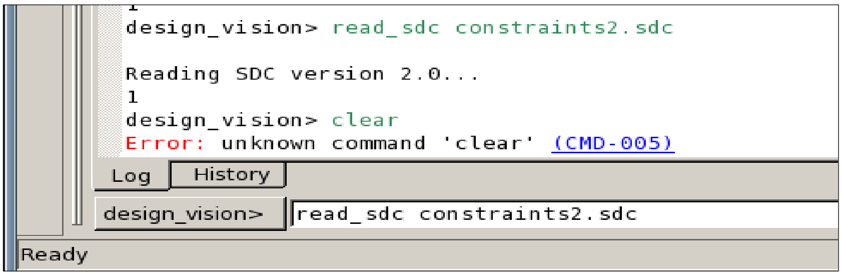
```
Initializing gui preferences from file  /home/guests/phd/sudi/.syn
dc_shell> gui_start
design_vision>
```



```
Reading with Presto HDL Compiler (equivalent to -rtl option).
Running PRESTO HDLC
Compiling source file /home/guests/phd/sudi/asiclab/synthesis/counter.v

Inferred memory devices in process
        in routine univ_bin_counter line 12 in file
                '/home/guests/phd/sudi/asiclab/synthesis/counter.v'.
===============================================================================
|     Register Name      |    Type     | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|       r_reg_reg        | Flip-flop |    8    |  Y  | N  | Y  | N  | N  | N  | N  |
===============================================================================
Presto compilation completed successfully.
Current design is now '/home/guests/phd/sudi/asiclab/synthesis/univ_bin_counter.db:univ_bin_counter'
Loaded 1 design.
Current design is 'univ_bin_counter'.
design_vision>
Current design is 'univ_bin_counter'.
Loading db file '/home/guests/phd/sudi/libs/saed90nm.sdb'
Loading db file '/cad/synopsys/design_vision/libraries/syn/generic.sdb'
```

Click objects or drag a box to select (Hold Ctrl to add, Shift to remove)

13. Constraints are optional and we can synthesize the design with or without constraints. In this case, we synthesize the design using constraints.
14. Read the constraints using the command: - read_sdc constraints2.sdc (constraints are desiged for counter design).

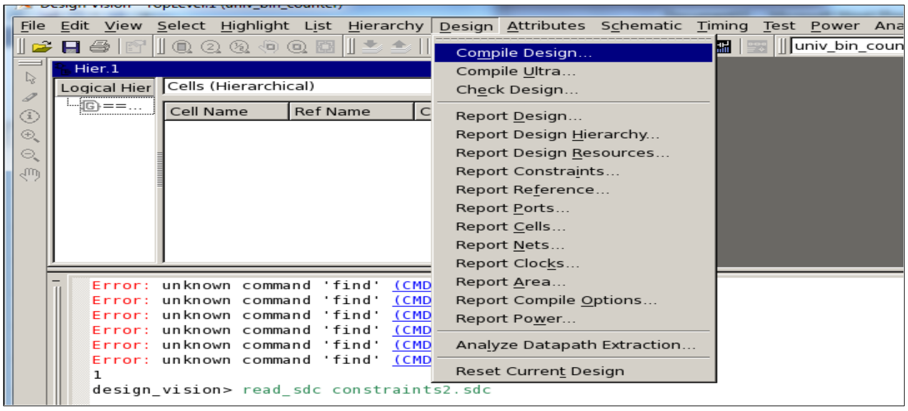


```
design_vision> read_sdc constraints2.sdc

Reading SDC version 2.0...
1
design_vision> clear
Error: unknown command 'clear' (CMD-005)
```

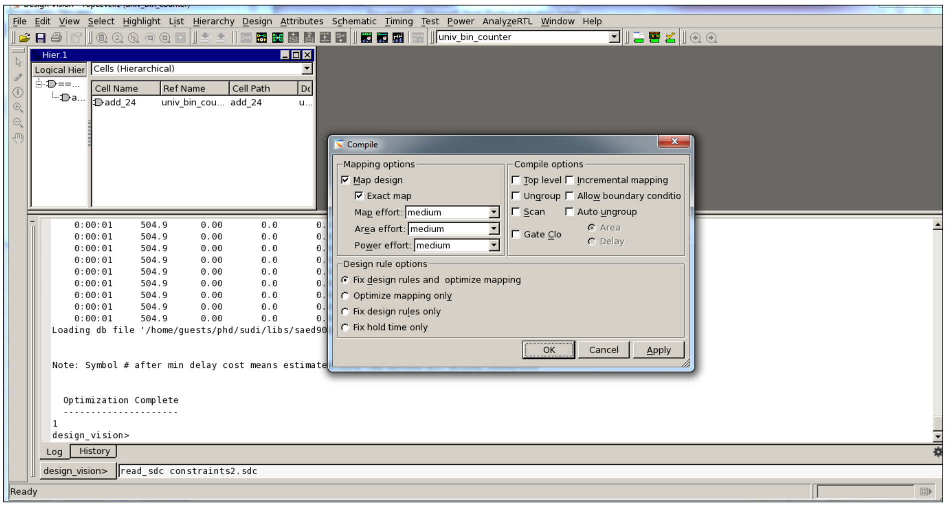
design_vision> read_sdc constraints2.sdc

Ready

15. Compile design: -



```
Error: unknown command 'find' (CMD
Error: unknown command 'find' (CMD
Error: unknown command 'find' (CMD
Error: unknown command 'find' (CMD
Error: unknown command 'find' (CMD
Error: unknown command 'find' (CMD
1
design_vision> read_sdc constraints2.sdc
```



Cell Name	Ref Name	Cell Path	Dc
add_24	univ_bin_cou...	add_24	u...

```
    0:00:01      504.9      0.00       0.0       0.
    0:00:01      504.9      0.00       0.0       0.
    0:00:01      504.9      0.00       0.0       0.
    0:00:01      504.9      0.00       0.0       0.
    0:00:01      504.9      0.00       0.0       0.
    0:00:01      504.9      0.00       0.0       0.
    0:00:01      504.9      0.00       0.0       0.
    0:00:01      504.9      0.00       0.0       0.
    0:00:01      504.9      0.00       0.0       0.
Loading db file '/home/guests/phd/sudi/libs/saed90


Note: Symbol # after min delay cost means estimate


  Optimization Complete
  ---------------------
1
design_vision>
```

design_vision> read_sdc constraints2.sdc

Ready

Compile

Mapping options
- ☑ Map design
- ☑ Exact map
- Map effort: medium
- Area effort: medium
- Power effort: medium

Compile options
- ☐ Top level ☐ Incremental mapping
- ☐ Ungroup ☐ Allow boundary conditio
- ☐ Scan ☐ Auto ungroup
- ☐ Gate Clo ● Area ○ Delay

Design rule options
- ● Fix design rules and optimize mapping
- ○ Optimize mapping only
- ○ Fix design rules only
- ○ Fix hold time only

File Edit View Select Highlight List Hierarchy Design Attributes Schematic Timing Test Power AnalyzeRTL Window Help
univ_bin_counter
Hier.1
Logical Hier
Cells (Hierarchical)
Log
History
OK
Cancel
Apply

16. Click on OK to compile the design.

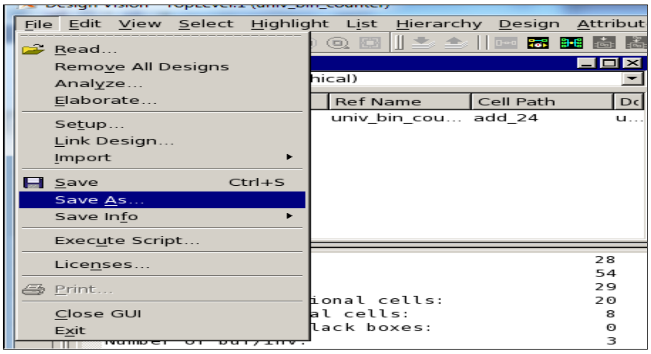
17. Execute the following commands and note the results: -

    report_area

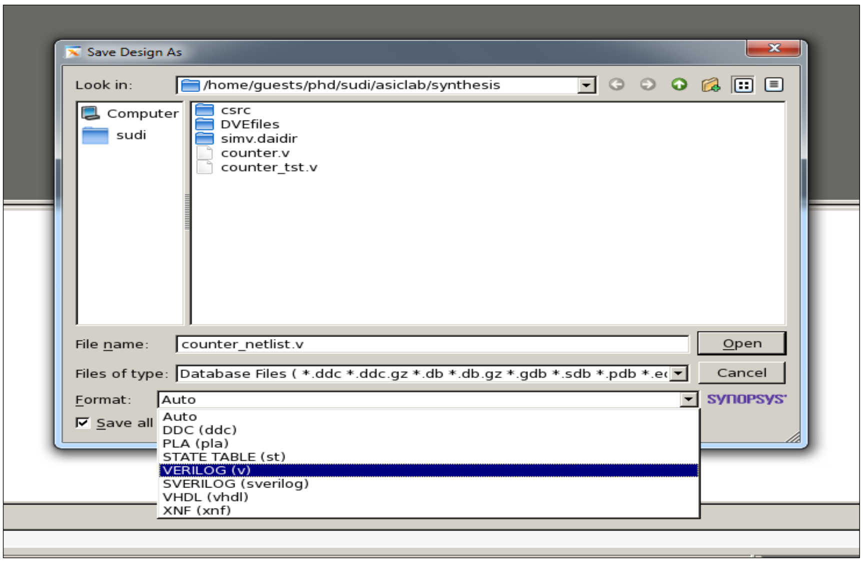
    report_power

    report_timing

18. Save the gate level netlist for the design (in this case, design is counter.v)



    Save the gate level netlist as below: (file name:- counter_netlist.v and format: - change to Verilog): -



Look in: /home/guests/phd/sudi/asiclab/synthesis

csrc
DVEfiles
simv.daidir
counter.v
counter_tst.v

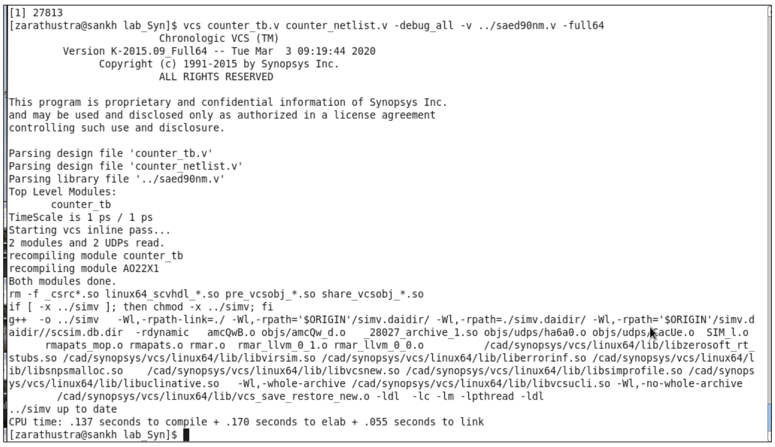
File name: counter_netlist.v

Files of type: Database Files (*.ddc *.ddc.gz *.db *.db.gz *.gdb *.sdb *.pdb *.e(

Format: Auto

☑ Save all

19. File -> exit the design_vision and view the gate level netlist (using gedit command)
20. Simulate the gate level netlist using Synopsys VCS tool as below: -



```
[1] 27813
[zarathustra@sankh lab_Syn]$ vcs counter_tb.v counter_netlist.v -debug_all -v ../saed90nm.v -full64
                         Chronologic VCS (TM)
         Version K-2015.09_Full64 -- Tue Mar  3 09:19:44 2020
               Copyright (c) 1991-2015 by Synopsys Inc.
                         ALL RIGHTS RESERVED

This program is proprietary and confidential information of Synopsys Inc.
and may be used and disclosed only as authorized in a license agreement
controlling such use and disclosure.

Parsing design file 'counter_tb.v'
Parsing design file 'counter_netlist.v'
Parsing library file '../saed90nm.v'
Top Level Modules:
       counter_tb
TimeScale is 1 ps / 1 ps
Starting vcs inline pass...
2 modules and 2 UDPs read.
recompiling module counter_tb
recompiling module AO22X1
Both modules done.
rm -f _csrc*.so linux64_scvhdl_*.so pre_vcsobj_*.so share_vcsobj_*.so
if [ -x ../simv ]; then chmod -x ../simv; fi
g++  -o ../simv   -Wl,-rpath-link=./ -Wl,-rpath='$ORIGIN'/simv.daidir/ -Wl,-rpath=./simv.daidir/ -Wl,-rpath='$ORIGIN'/simv.d
aidir//scsim.db.dir  -rdynamic   amcQwB.o objs/amcQw_d.o   _28027_archive_1.so objs/udps/ha6a0.o objs/udps/cacUe.o  SIM_l.o
      rmapats_mop.o rmapats.o rmar.o  rmar_llvm_0_1.o rmar_llvm_0_0.o          /cad/synopsys/vcs/linux64/lib/libzerosoft_rt_
stubs.so /cad/synopsys/vcs/linux64/lib/libvirsim.so /cad/synopsys/vcs/linux64/lib/liberrorinf.so /cad/synopsys/vcs/linux64/l
ib/libsnpsmalloc.so    /cad/synopsys/vcs/linux64/lib/libvcsnew.so /cad/synopsys/vcs/linux64/lib/libsimprofile.so /cad/synops
ys/vcs/linux64/lib/libuclinative.so   -Wl,-whole-archive /cad/synopsys/vcs/linux64/lib/libvcsucli.so -Wl,-no-whole-archive
        /cad/synopsys/vcs/linux64/lib/vcs_save_restore_new.o -ldl  -lc -lm -lpthread -ldl
../simv up to date
CPU time: .137 seconds to compile + .170 seconds to elab + .055 seconds to link
[zarathustra@sankh lab_Syn]$ 
```

21. Observe the executable file “simv” created as before and execute simv. (./simv –gui) to verify the simulation.