

# ASIC Design Lab

EC 6272, Spring 2019-2020

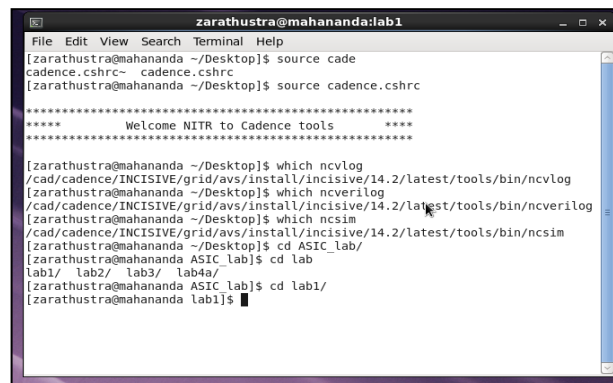
VLSI Laboratory, ECE Department, NIT Rourkela, India

This tutorial will discuss the various views that make-up an effective RTL design model and then illustrate how to use a Cadence ASIC tools to check an RTL design with simulation, and synthesizing RTL model.

This tutorial requires entering commands manually for each of the tools to enable students to gain a better understanding of the detailed steps involved in this process.

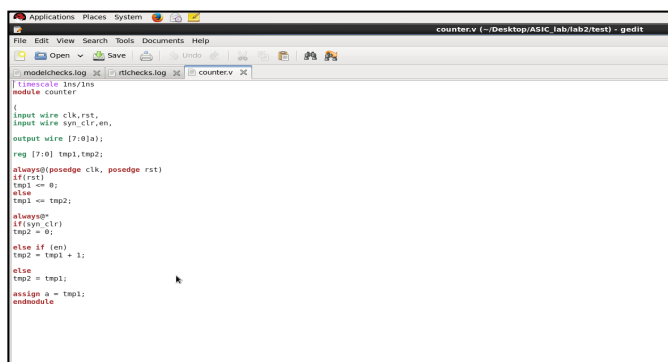
Simulation of Finite State Machine (FSM) based Designs in Verilog HDL.

1. Open the terminal
2. Source the cadence.cshrc
3. Check whether the commands are working as below: -



```
zarathustra@mahananda:lab1
File Edit View Search Terminal Help
[zarathustra@mahananda ~/Desktop]$ source cade
cadence.cshrc~ cadence.cshrc
[zarathustra@mahananda ~/Desktop]$ source cadence.cshrc
***** Welcome NITR to cadence tools *****
[zarathustra@mahananda ~/Desktop]$ which ncvclog
/cad/cadence/INCISIVE/grid/avs/install/incisive/14.2/latest/tools/bin/ncvclog
[zarathustra@mahananda ~/Desktop]$ which ncverilog
/cad/cadence/INCISIVE/grid/avs/install/incisive/14.2/latest/tools/bin/ncverilog
[zarathustra@mahananda ~/Desktop]$ which ncsim
/cad/cadence/INCISIVE/grid/avs/install/incisive/14.2/latest/tools/bin/ncsim
[zarathustra@mahananda ~/Desktop]$ cd ASIC_lab/
[zarathustra@mahananda ASIC_lab]$ cd lab
lab1/ lab2/ lab3/ lab4a/
[zarathustra@mahananda ASIC_lab]$ cd lab1/
[zarathustra@mahananda lab1]$
```

4. Create a directory for saving files
5. Create design\_file.v as shown below: - (gedit counter.v)

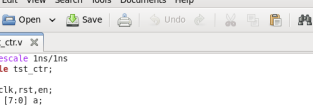


```
counter.v (~Desktop/ASIC_lab/lab2/test) - gedit
// counter.v
module counter
(
    input wire clk, rst,
    input wire sym_clr_en,
    output wire [7:0]a;
    reg [7:0] tmp1, tmp2;

    always@(posedge clk, posedge rst)
        if(rst)
            tmp1 <= 0;
        else
            tmp1 <= tmp2;

    always@(*)
        if(sym_clr)
            tmp2 = 0;
        else if(en)
            tmp2 = tmp1 + 1;
        else
            tmp2 = tmp1;

    assign a = tmp1;
endmodule
```

- 
- ```

tst_ctr.v (~Desktop/ASIC_lab/lab1/test) - gedit
File Edit View Search Tools Documents Help
[Icons] Open Save Undo Redo Find Replace
tst_ctr.v
timescale 1ns/1ns
module tst_ctr;

    reg clk,rst,en;
    wire {7:0} a;

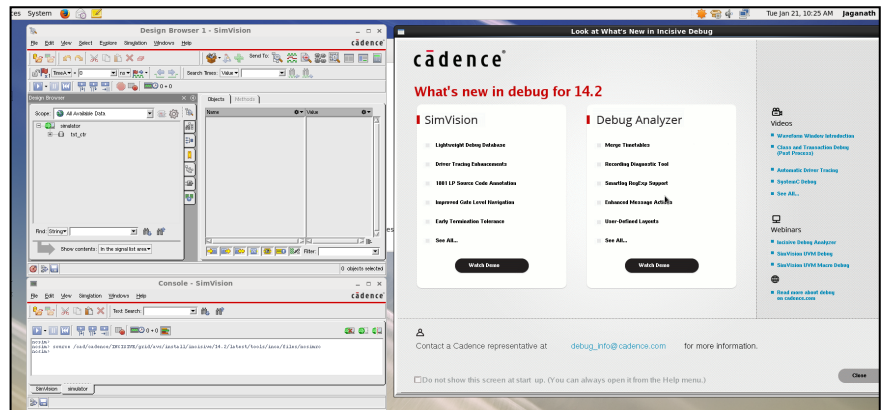
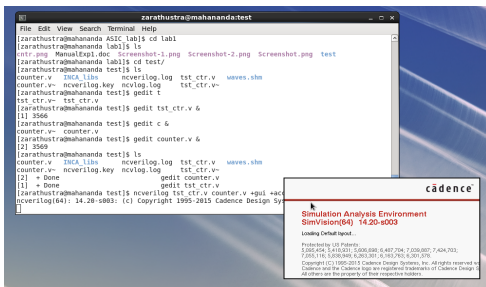
    counter uut(.clk(clk), .rst(rst), .syn_clr(syn_clr), .en(en), .a(a));

    //Stimulus for Clock
    always begin
        clk = 1'b0;
        #5;
        clk = 1'b1;
        #5;
    end

    //Stimulus for Inputs
    initial begin
        rst = 1'b1;
        #10;
        rst = 1'b0;
        end
endmodule

```
- Verilog Tab Width: 8 v L16, Col 1 INS

11. Simvision gui will open: -

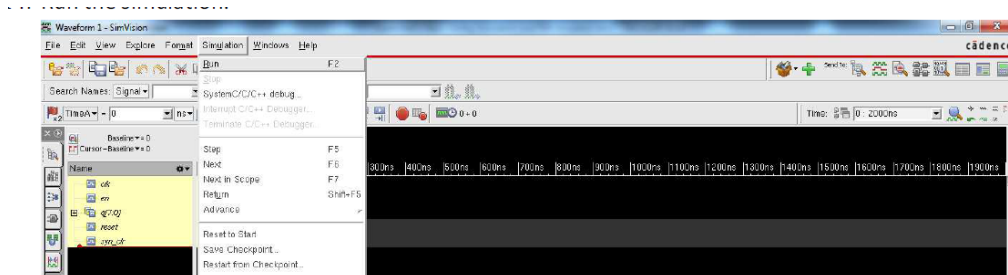


The screenshot displays a web browser window titled "Design Browser 1 - SimVision". The browser's address bar shows "https://nbs4...". The main content area features a table with two columns: "Name" and "Value". The table lists several variables and their corresponding values:

| Name | Value  |
|------|--------|
| a77  | 10.000 |
| ch   | 0.000  |
| f    | 0.000  |
| f1   | 0.000  |
| f2   | 0.000  |

The browser also includes a search bar and various navigation buttons. The background of the screen shows a desktop environment with a taskbar and other application windows, including a "Test Search" window and a "Connecting to fonts.googleapis.com..." window.

13. Run the simulation: -



14. Observe the waveforms: -

