ASIC Design Lab (EC-6272)

Experiment – VIII

Power Analysis (Dynamic power)

1. Open the terminal
2. Source the synopsys.cshrc
3. In this experiment, we perform power analysis (dynamic power) of the design using power compiler.
4. In a ASIC lab directory, create design.v. Create the testbench.v for design.v and simulate the design in VCS.

```
sudi@sankh:powerana
[sudi@sankh powerana]$ ls
counter_tst.v  counter.v
[sudi@sankh powerana]$ vcs counter_tst.v counter.v -debug_all -full64
                         Chronologic VCS (TM)
         Version K-2015.09_Full64 -- Mon Mar 26 11:07:37 2018
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                         ALL RIGHTS RESERVED

This program is proprietary and confidential information of Synopsys Inc.
and may be used and disclosed only as authorized in a license agreement
controlling such use and disclosure.

Parsing design file 'counter_tst.v'
Parsing design file 'counter.v'
Top Level Modules:
       univ_bin_counter_tst
TimeScale is 1 ns / 1 ns
Starting vcs inline pass...
1 module and 0 UDP read.
recompiling module univ_bin_counter_tst
rm -f _csrc*.so linux64_scvhdl_*.so pre_vcsobj_*.so share_vcsobj_*.so
if [ -x ../simv ]; then chmod -x ../simv; fi
g++  -o ../simv    -Wl,-rpath-link=./ -Wl,-rpath='$ORIGIN'/simv.daidir/ -Wl,-rpath=./simv.daidir/ -l
_mop.o rmapats.o rmar.o  rmar_llvm_0_1.o rmar_llvm_0_0.o          /cad/synopsys/vcs/linux64/lib/lib
s/linux64/lib/libsnpsmalloc.so    /cad/synopsys/vcs/linux64/lib/libvcsnew.so /cad/synopsys/vcs/linu
bvcsucli.so -Wl,-no-whole-archive          /cad/synopsys/vcs/linux64/lib/vcs_save_restore_new.o -l
../simv up to date
CPU time: .137 seconds to compile + .196 seconds to elab + .113 seconds to link
[sudi@sankh powerana]$ ls
counter_tst.v  counter.v  csrc  simv  simv.daidir
[sudi@sankh powerana]$ ./simv -gui
[sudi@sankh powerana]$ ls
counter_tst.v  counter.v  csrc  DVEfiles  inter.vpd  simv  simv.daidir  ucli.key
[sudi@sankh powerana]$
```
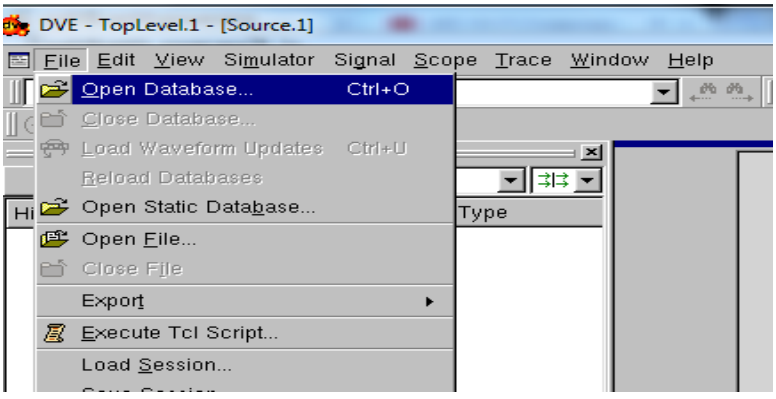
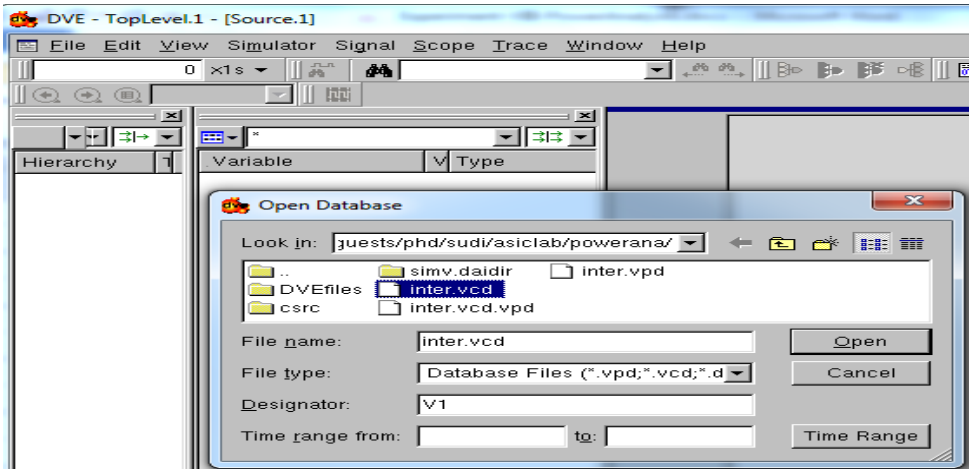
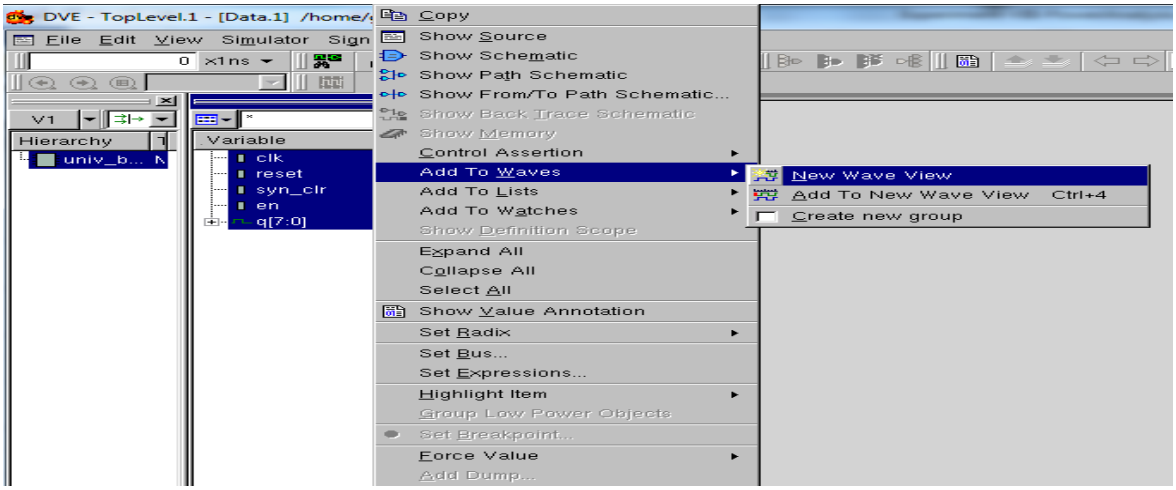
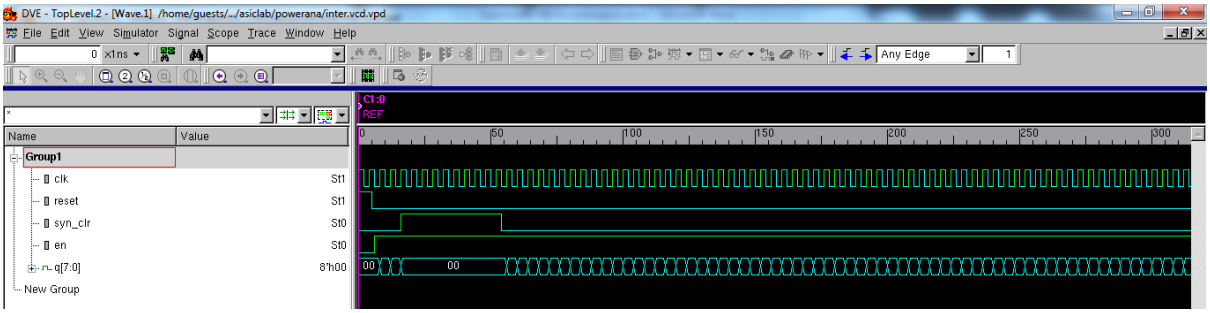

5. After simulation of design, it creates inter.vpd. Convert the vpd to vcd and vcd to saif format.
   [sudi@sankh powerana]$ vpd2vcd inter.vpd inter.vcd
6. (VCD: Value Change Dump and SAIF : Swithcing Activity Interchange format)
7. Once the simulation snapshot is stored in VCD or VPD format, we can open it using any waveform viewer. (dve or simvision). Commands are below: -

```
[sudi@sankh powerana]$ ls
counter_tst.v  counter.v  csrc  DVEfiles  inter.vcd  inter.vpd  simv  simv.daidir  ucli.key
[sudi@sankh powerana]$ dve
ERROR - /cad/synopsys/vcs/gui/dve/linux/bin is not valid directory.  Check if DVE variable is valid.  If you wan
[sudi@sankh powerana]$ dve -full64
[sudi@sankh powerana]$
```





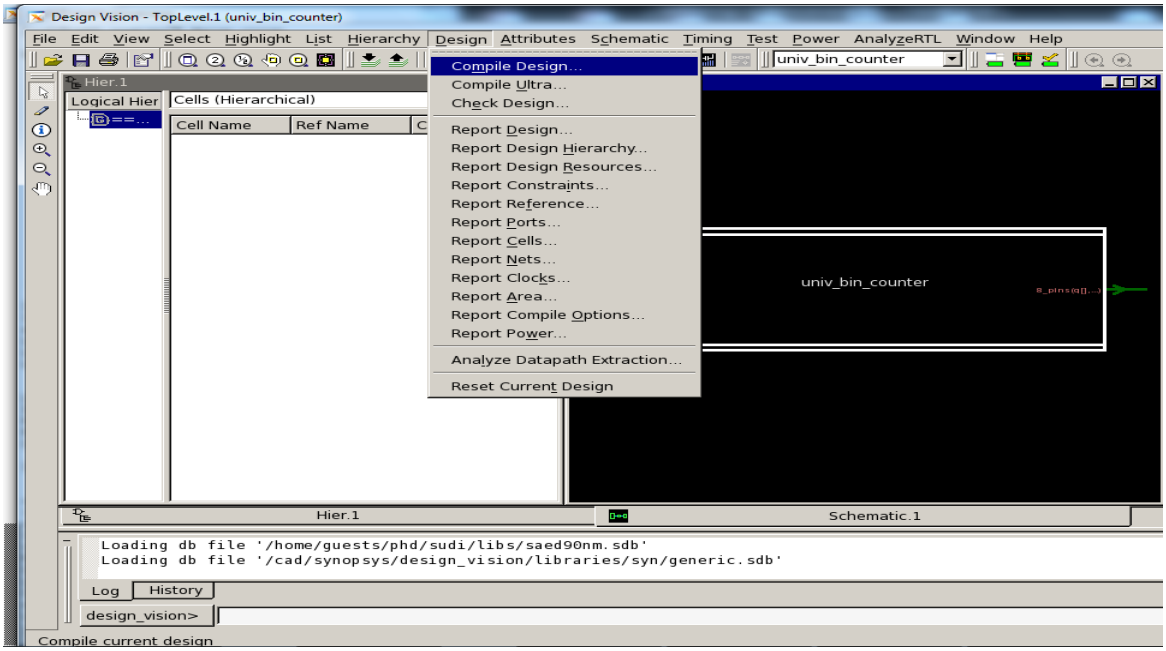


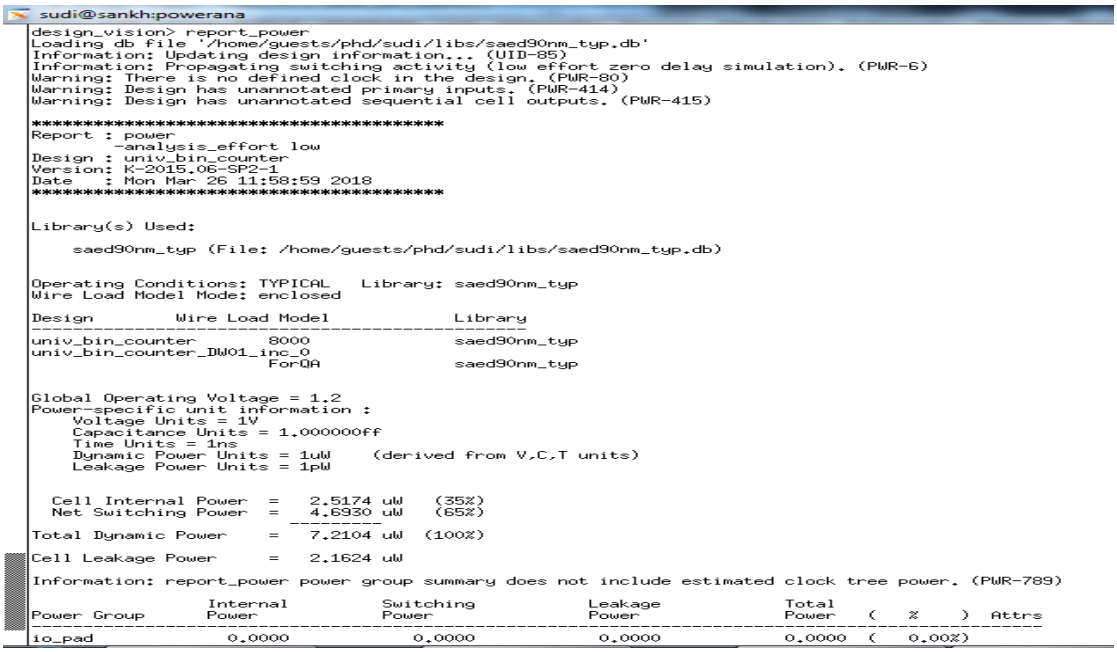


8. Power compiler is a integral part of Design Vision and accepts only SAIF files. So convert VCD to SAIF as below: -

```
[sudi@sankh powerana]$ vcd2saif -input inter.vcd -output inter.saif
VCD to SAIF translator version K-2015.06-SP2 Synopsys, Inc.
direct mapping all VCD instances
processing header of VCD file: inter.vcd
processing value changes of VCD file: inter.vcd
generating backward SAIF file: inter.saif
[sudi@sankh powerana]$ ls
counter_tst.v  counter.v  csrc  DVEfiles  inter.saif  inter.vcd  inter.vcd.vpd  inter.vpd  opendatabase.log  simv  simv.daidir  ucli.key
[sudi@sankh powerana]$
```

9. Open design_vision. Read the library and design into design vision. Compile the design and report power.





10. To save the power report into a separte text file use the following command: -

11. Open the new terminal. Go to the power analysis folder and open the Power1 file in gedit.

```
Global Operating Voltage = 1.2
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =   2.5174 uW   (35%)
  Net Switching Power  =   4.6930 uW   (65%)
                         ---------
Total Dynamic Power    =   7.2104 uW  (100%)

Cell Leakage Power     =   2.1624 uW

Information: report_power power group summary does not include estimated clock tree power. (PWR-789)

                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000              0.0000            0.0000  (   0.00%)
memory             0.0000           0.0000              0.0000            0.0000  (   0.00%)
black_box          0.0000           0.0000              0.0000            0.0000  (   0.00%)
clock_network      0.0000           0.0000              0.0000            0.0000  (   0.00%)
register           0.0000           0.0000              0.0000            0.0000  (   0.00%)
sequential     -6.8914e-02         5.8188e-02         8.9700e+05            0.8863 (   9.46%)
combinational      2.5863           4.6349          1.2654e+06            8.4865  (  90.54%)
--------------------------------------------------------------------------------------------------
Total              2.5174 uW        4.6930 uW     2.1624e+06 pW         9.3728 uW
1
```

12. Now read the saif file into design_vision as below, and do compile design again (re-synthesize). And execute report_power.

```
design_vision> read_saif -input inter.saif -instance_name univ_bin_counter_tst/uut
Error: No switching activity has been annotated. (PWR-362)
0
design_vision> read_saif -input inter.saif -instance_name uut
Error: No switching activity has been annotated. (PWR-362)
0
design_vision> read_saif -input inter.saif -instance_name univ_bin_counter_tst/uut
Error: No switching activity has been annotated. (PWR-362)
0
design_vision> read_saif -input inter.saif -instance_name univ_bin_counter_tst
1
design_vision> compile -exact_map
```

13. report_power again. Compare the dynamic power in Power1 and Power2 reports.

```
sudi@sankh:powerana

  Optimization Complete
  ---------------------
1
design_vision> report_power > power2
design_vision> report_power
****************************************************
Report : power
        -analysis_effort low
Design : univ_bin_counter
Version: K-2015.06-SP2-1
Date   : Mon Mar 26 14:22:38 2018
****************************************************

Library(s) Used:

    saed90nm_typ (File: /home/guests/phd/sudi/libs/saed90nm_typ.db)

Operating Conditions: TYPICAL   Library: saed90nm_typ
Wire Load Model Mode: enclosed

Design          Wire Load Model               Library
------------------------------------------------------
univ_bin_counter       8000                   saed90nm_typ
univ_bin_counter_DW01_inc_0
                       ForQA                  saed90nm_typ

Global Operating Voltage = 1.2
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =  24.6532 uW   (83%)
  Net Switching Power  =   4.9317 uW   (17%)
                         ---------
Total Dynamic Power    =  29.5849 uW  (100%)

Cell Leakage Power     =   2.2664 uW
```

14. Change the stimulus (input patterns) in the testbench.v and analyze the dynamic power for different stimulus.
15. Do the power analysis for all designs.