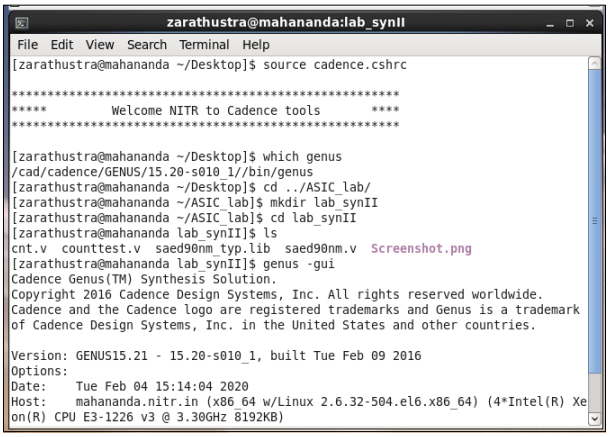
ASIC Design Lab (EC-6272)
Experiment – IV
Synthesis II

1. Open a terminal in the workstation and source cadence.cshrc in the terminal
2. In this lab session, Synthesis of RTL models **with constraints** will be carried out, for which a few library files and a constraint file will be shared in the lab session. The necessary files can be downloaded from links provided during class.
3. Make a working folder, script the verilog RTL and testbench (Follow the instructions in the previous experiment Synthesis Part-I).
4. We use Cadence synthesis tool : GENUS Synthesis Solution. Type the command as below and check path of genus is echoed or not in the workstation.



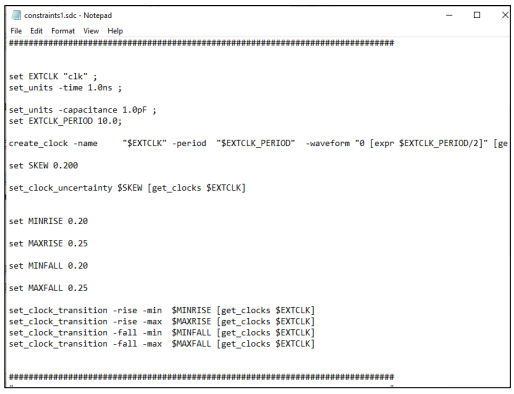
5. In the terminal, execute genus –gui for invoking the EDA Synthesis tool

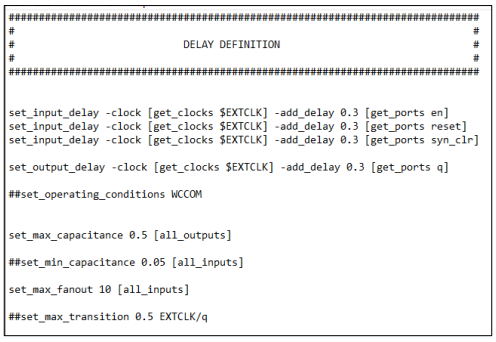
   ]$ **genus –gui**

6. Minimize the gui and follow below instructions, mentioning the proper path for linking the saed90nm library files

   genus@root:> read_libs saed90nm_typ.lib
   genus@root:> read_hdl -v2001 counter.v
   genus@root:> elaborate

7. A constraint file is sourced to insert constraints as shown below, and Change the constraints accordingly for your designs (input, output and clock).





genus@root:> read_sdc constraints1.sdc

genus@root:> synthesize -to_mapped

8. Save the gate level netlist

   genus@root:> write_hdl > d_with_cnstr_netlist.v

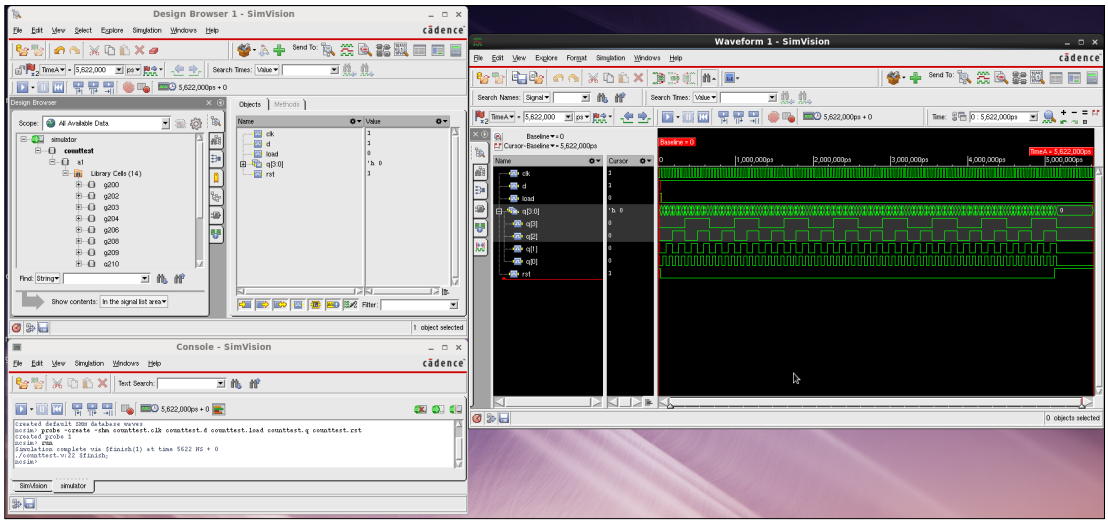
9. Find the d_with_cnstr_netlist.v file created in the working directory.

10. Record and save the area, timing and power by following the below commands

    genus@root:> report_units
    genus@root:> report_timing > timing
    genus@root:> report_area > area
    genus@root:> report_power > power
    genus@root:> report_utilization
    genus@root:> report_sequential

11. Do the synthesis and report timing. Change the constraints and check for the slack. And compare the area, timing, power for unconstrained and constrained synthesized designs (while varying the constraints).
12. Simulate the design as done in earlier experiment. Check the simulation using this netlist file with constraints. (Blindly don't follow the manual. Give the correct path based on where you have the libs folder copied. Use the command "pwd" to get path)

    ]$ ncverilog counter_tst.v d_with_cnstr_netlist.v +access+rw -v saed90nm.v +gui



For more details check the Genus_gui document in the installed folder