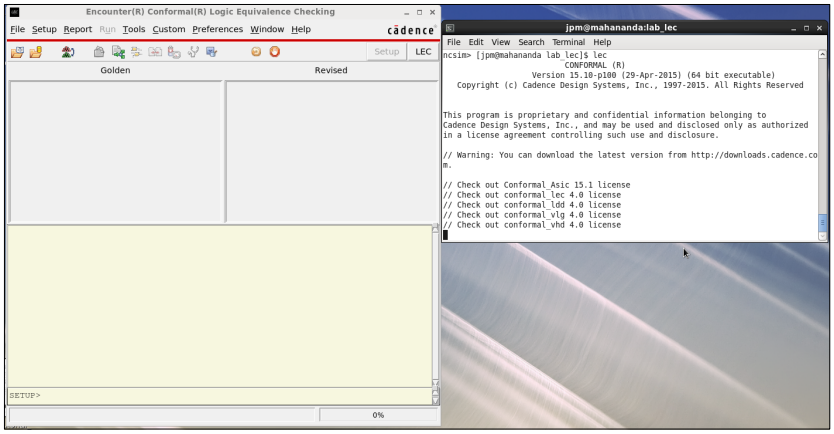
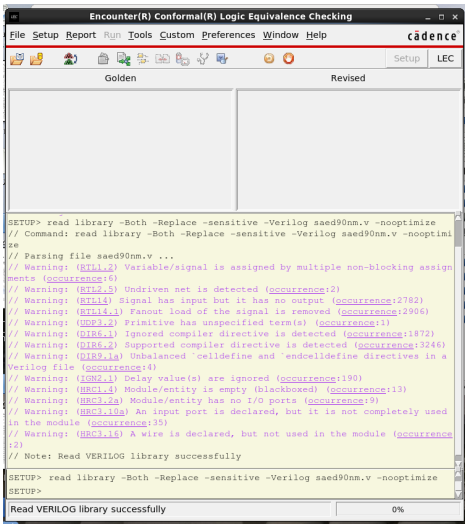
# ASIC Design Lab (EC-6272)
# Experiment – V
# Logic Equivalence Checking

1. Open the terminal
2. Source the cadence.cshrc
3. In this experiment, we are performing equivalence checking. RTL code and synthesized gate-level netlist are compared structurally using LEC (Logical Equivalence Checking) tool. We use Cadence Conformal tool in this experiment.
4. In an ASIC lab directory, create design.v. Create the testbench.v and verify the design. And synthesize the design in GENUS (with or without constraints) and save the netlist. Perform gate-level simulations and verify for functionality. In LEC, we are comparing design (RTL code) and gate level netlist statically.
5. Open the conformal using command lec as below: - (execute the following commands in the setup command line)

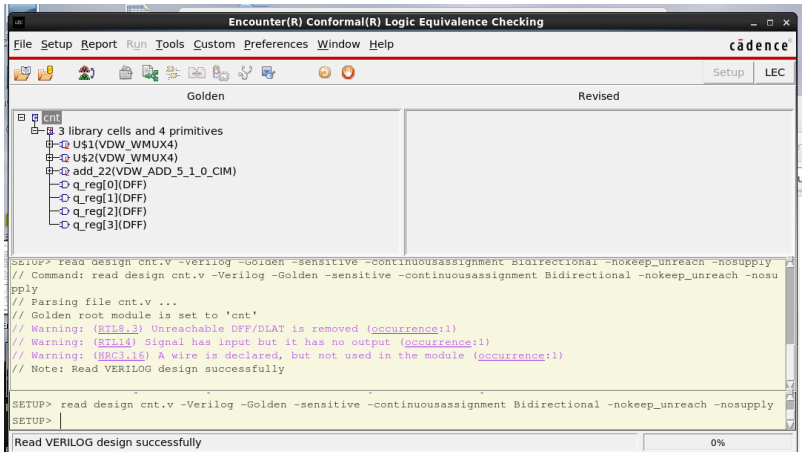



```
SETUP> read library -Both -Replace -sensitive -Verilog saed90nm.v -nooptimize
SETUP> read design cnt.v -Verilog -Golden -sensitive -continuousassignment Bidirectional -nokeep_unreach -nosupply
SETUP> read design des_net.v -Verilog -Revised -sensitive -continuousassignment Bidirectional -nokeep_unreach -nosupply
SETUP> set system mode lec
LEC> add compare points -all
LEC> compare
LEC>
```

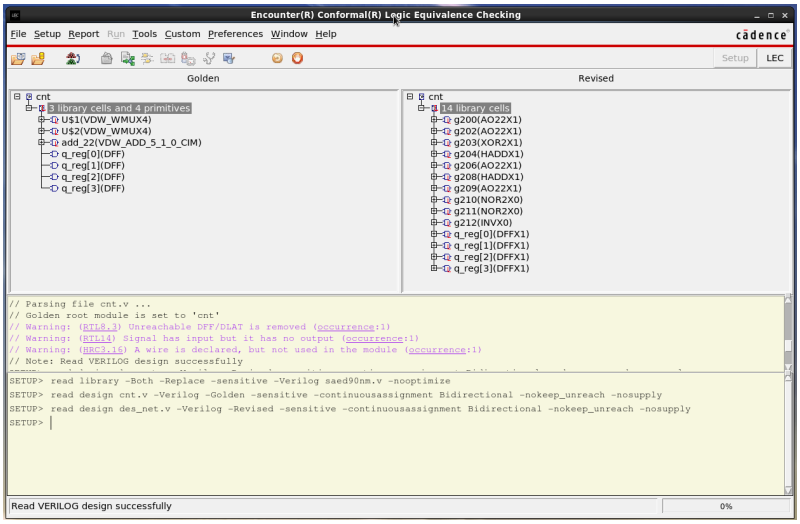



6. Read Library: -

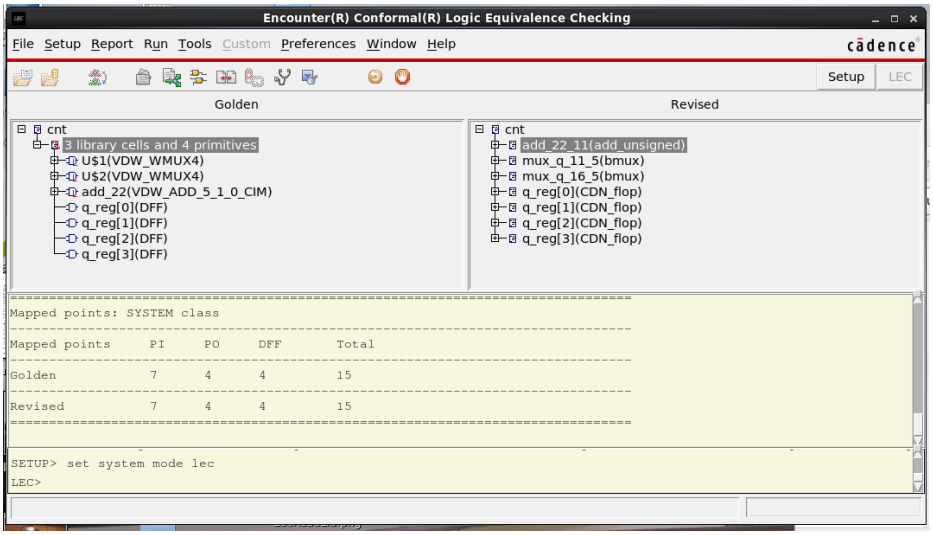
7. Read Golden design file (RTL code): -



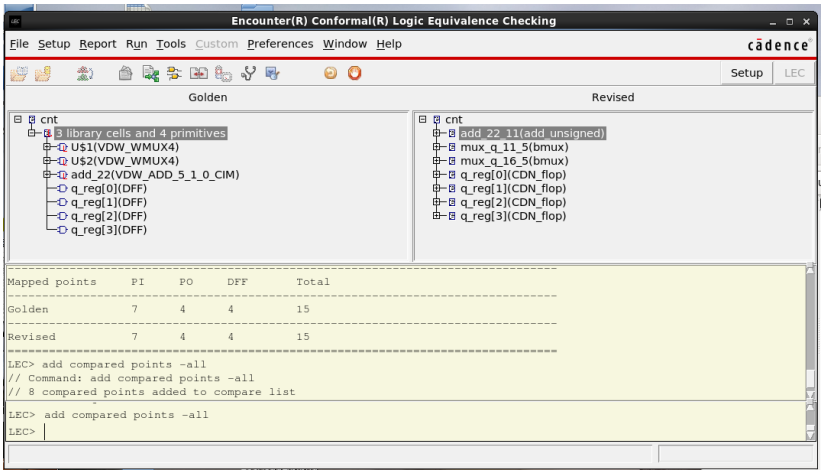

8. Read revised design (gate_level_netlist): -



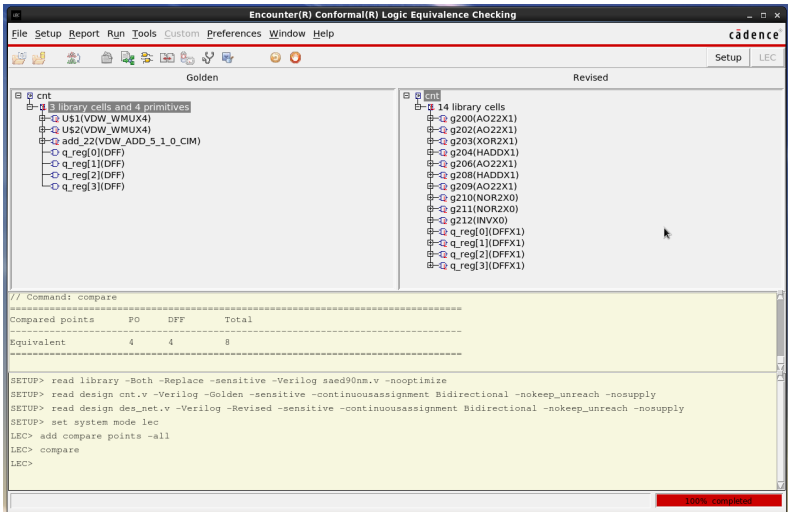

9. Change the mode from “SETUP to “LEC”



10. Add all compare points:-




11. Compare the golden (RTL) and revised (gate level netlist or synthesized netlist): -




12. Compare done. Generally successful comparison is not easy. For large and medium scale designs, we get unsuccessful comparisons. Right click on design name (both golden and revised) and by looking at schematic we can debug the mismatches present, if any.

13. Perform the equivalence checking for all the designs you have done in lab (FIFO etc).