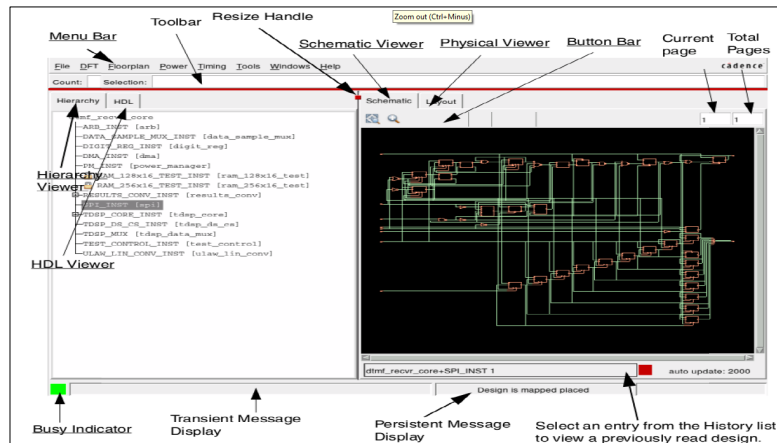


# ASIC Design Lab (EC-6272)

## Experiment – IV

### Synthesis I

1. Open a terminal in the workstations
2. Source cadence.cshrc in the terminal
3. In this lab session, Synthesis of RTL models will be carried out, for which a few library files will be needed. The library files can be downloaded from links provided during class.



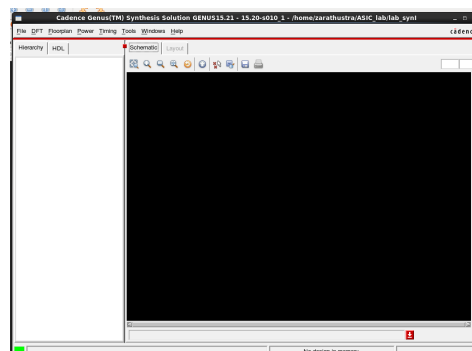
4. Check whether the commands are working as shown in figure below. Make a working folder, script the verilog RTL and testbench. Clear the errors, simulate and confirm the functionality through simvision simulations (Follow the instructions in the experiment-I).
5. We use Cadence synthesis tool : GENUS Synthesis Solution. Type the command as below and check path of genus is echoed or not in the workstation.

```

*****
zarathustra@mahandanda:lab_syn1
File Edit View Search Terminal Help
[zarathustra@mahandanda ~/ASIC_lab]$ which genus
/cad/cadence/GENUS/15.20-s010_1/bin/genus
[zarathustra@mahandanda ~/ASIC_lab]$ mkdir lab_syn1
[zarathustra@mahandanda ~/ASIC_lab]$ cd lab
lab.cc/ lab_syn1/
[zarathustra@mahandanda ~/ASIC_lab]$ cd lab_syn1/
[zarathustra@mahandanda lab_syn1]$ ls
cnt.v counttest.v
[zarathustra@mahandanda lab_syn1]$ ls
cnt.v counttest.v saed90nm.typ.lib saed90nm.v
[zarathustra@mahandanda lab_syn1]$ genus -gui
Cadence Genus(TM) Synthesis Solution
Copyright 2016 Cadence Design Systems, Inc. All rights reserved worldwide.
Cadence and the Cadence logo are registered trademarks and Genus is a trademark
of Cadence Design Systems, Inc. in the United States and other countries.

Version: GENUS15.21 - 15.20-s010_1, built Tue Feb 09 2016
Options:
Date: Thu Jan 30 15:08:43 2020
Host: mahandanda.nitr.in (x86_64 w/Linux 2.6.32-504.el6.x86_64) (4*Intel(R) Xe
on(R) CPU E3-1226 v3 @ 3.30GHz 8192KB)
OS: Red Hat Enterprise Linux Workstation release 6.6 (Santiago)
  
```

6. In the terminal, execute genus –gui for invoking the EDA Synthesis tool  
]\$ genus –gui



- Minimize the gui and follow below instructions, mentioning the proper path for linking the saed90nm library files

```
genus@root:> read_libs saed90nm_typ.lib
genus@root:> read_hdl -v2001 counter.v
genus@root:> elaborate
genus@root:> synthesize -to_mapped
```

- Save the gate level netlist

```
genus@root:> write_hdl > design_netlist.v
```

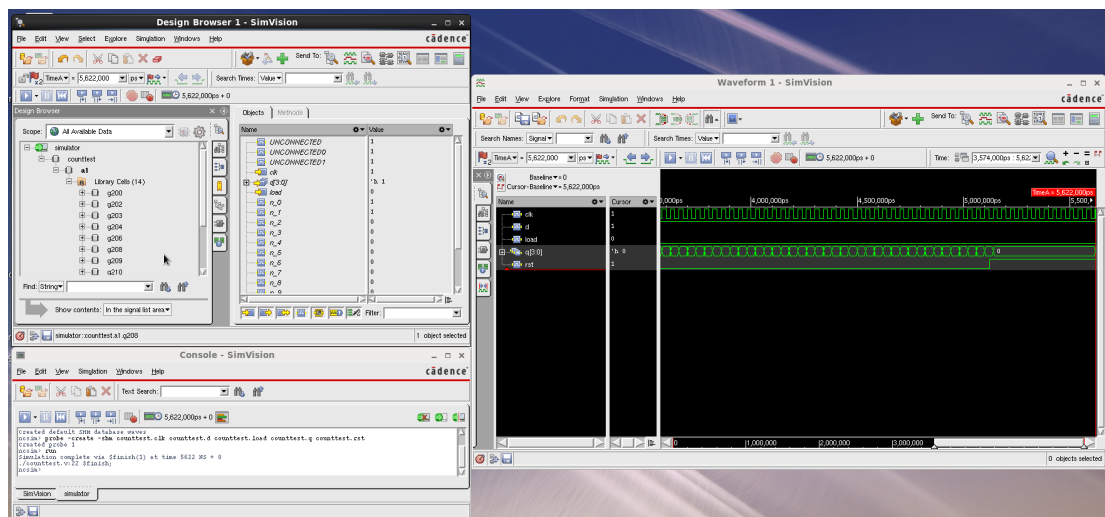
- Find the design\_netlist.v file created in the working directory. A cmd and a log file will also be generated that stores the current activities along with a fv verification file.

- Record the area, timing and power by following the below commands

```
genus@root:> report_units
genus@root:> report_gates
genus@root:> report_utilization
genus@root:> report_sequential
genus@root:> report_power
```

- Simulate the design as you did in earlier experiment. Check the simulation using this netlist file. (Blindly don't follow the manual. Give the correct path based on where you have the libs folder copied. Use the command "pwd" to get path)

```
ljs neverilog counter_tst.v design_netlist.v +access+rw -v saed90nm.v +gui
```



**For more details check the Genus\_gui document in the installed folder**