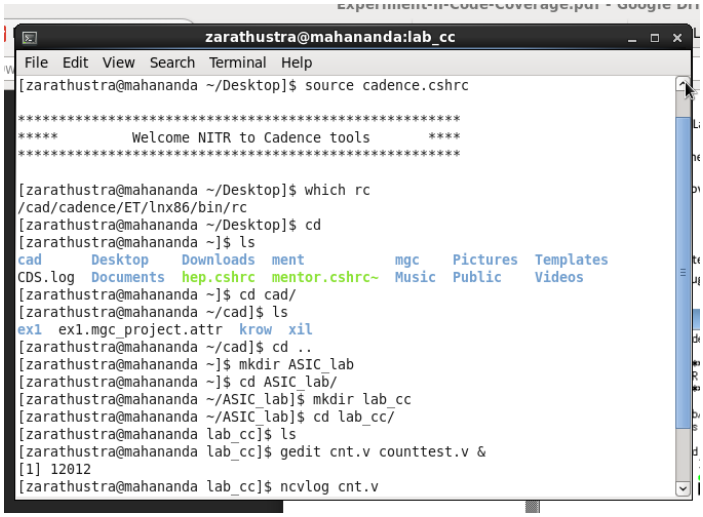
ASIC Design Lab (EC-6272)

Experiment – III

Code Coverage

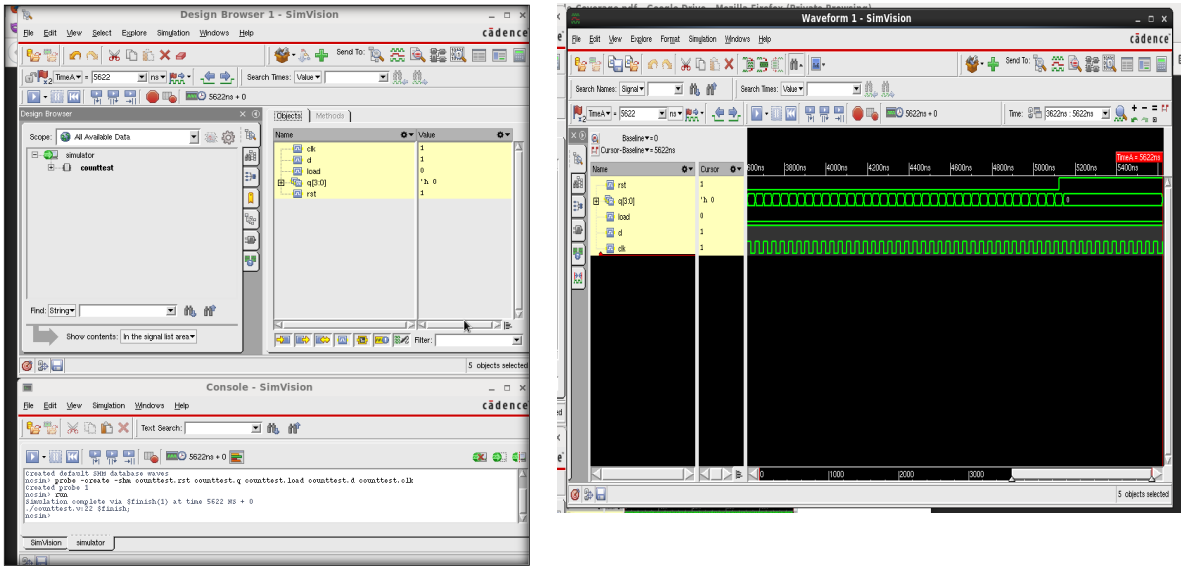
1. Open the terminal
2. Source the cadence.cshrc
3. Check whether the commands are working as below. Make a working folder, script the verilog RTL and testbench, as below. Check for synatx errors and carry ahead with simulation following the next step.



4. Execute the following commands for coverage in the terminal

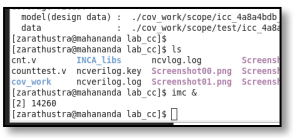
ncverilog design_file.v testbench_file.v +gui +access+rw +nccoverage+all

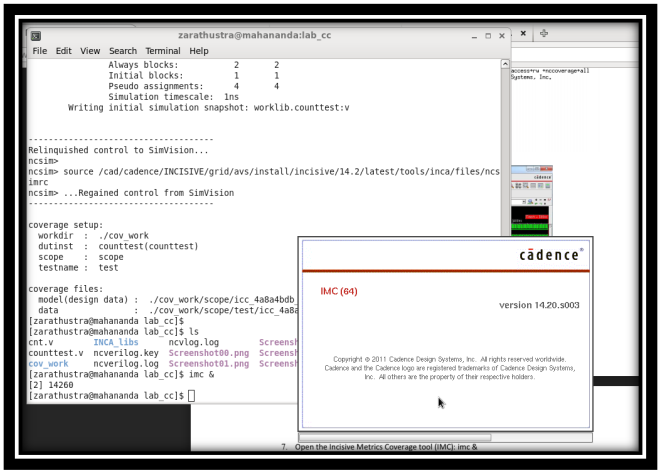
5. Simulate completely



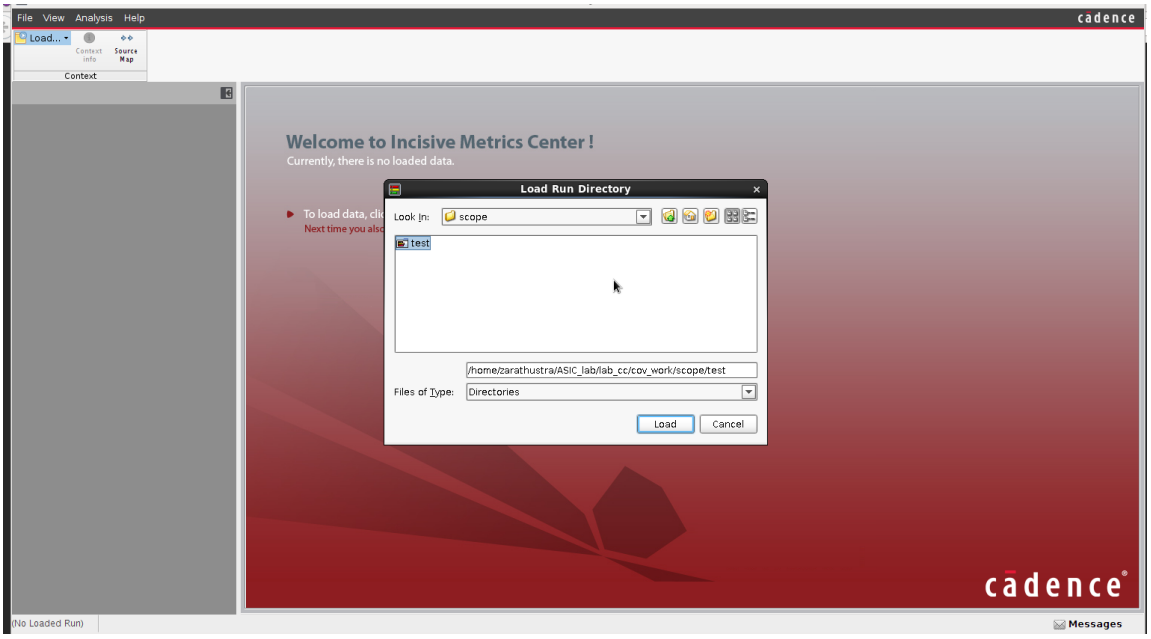
6. Observe the “cov_work” folder in the directory

7. Open the Incisive Metrics Coverage tool (IMC) in the terminal
imc &

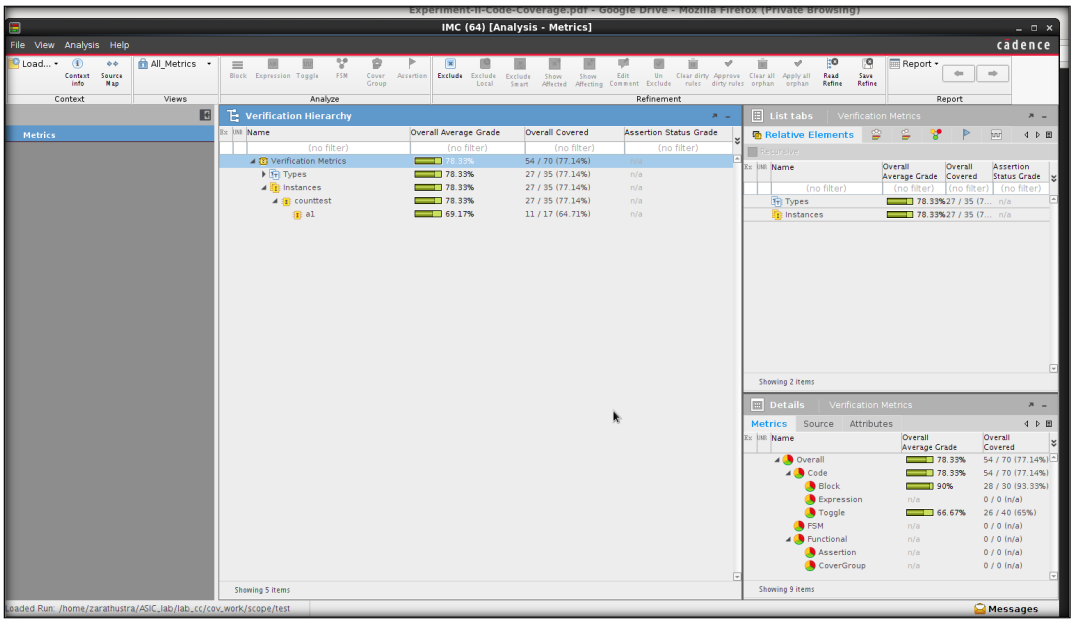




8. Load the test file from the folder “cov_work”



9. IMC opens the coverage metrics analysis



10. Write better testbenches for all the designs : - Counter, FIFO, Debouncing circuit, Edge detector to get 96% coverage in all categories: - FSM, toggle, block and expression.