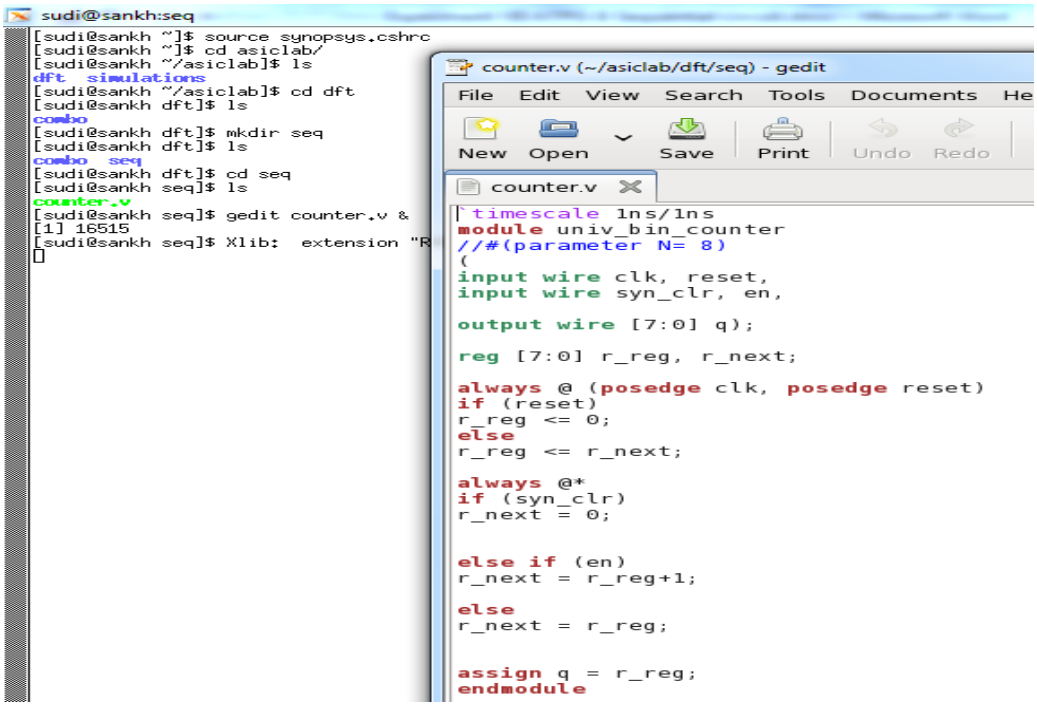
ASIC Design Lab (EC-6272)

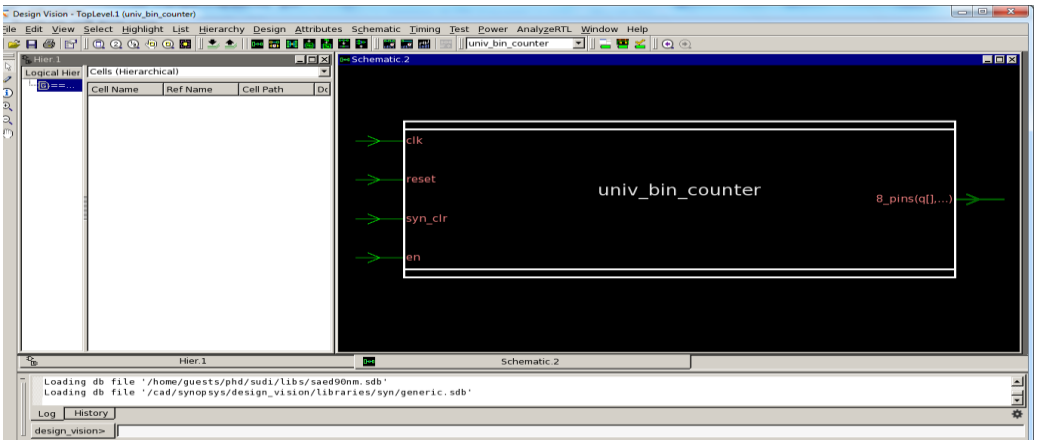
Experiment – VII (ATPG-II)

ATPG for Sequential circuits

1. Open the terminal
2. Source the synopsys.cshrc
3. In a ASIC lab directory, make design.v (any sequential circuit). In this experiment, we perform ATPG (Automatic Test Pattern Generation) for Sequential circuit. In our previous experiment we have peformed ATPG for combinational circuits. Scan insertion is not required for combinational circuits, but it is required for sequential circuits. Scan insertion can be done in DFT compiler which is a integral part of design vision.
4. Open the design vision and execute the following commands. We generate scan inserted synthesized netlist at the end. We also extract spf (STIL procedure file) , which is a input to the Tetramax used for ATPG. (Note: STIL: - Standard Test Interface Language).
5. Make your design ready.



6. Open design_vision. Read the library and design into design vision.



7. Go the terminal as below and execute the following commands to insert dft (scan chain) and spf file.

```
sudi@sankh:seq
Warning:  Site Information is not available ... Have you run install_site?

                              Design Compiler Graphical
                                    DC Ultra (TM)
                                     DFTMAX (TM)
                                Power Compiler (TM)
                                   DesignWare (R)
                                   DC Expert (TM)
                                Design Vision (TM)
                                HDL Compiler (TM)
                                VHDL Compiler (TM)
                                   DFT Compiler
                                Design Compiler(R)

                Version K-2015.06-SP2-1 for linux64 - Sep 09, 2015

                        Copyright (c) 1988 - 2015 Synopsys, Inc.
   This software and the associated documentation are proprietary to Synopsys,
 Inc. This software may only be used in accordance with the terms and conditions
 of a written license agreement with Synopsys, Inc. All other use, reproduction,
              or distribution of this software is strictly prohibited.
Initializing...
Initializing gui preferences from file  /home/guests/phd/sudi/.synopsys_dv_prefs.tcl
design_vision> design_vision> read_file -format verilog {/home/guests/phd/sudi/asiclab/dft/seq/counter.v}
Loading db file '/home/guests/phd/sudi/libs/saed90nm_typ.db'
Loading db file '/cad/synopsys/design_vision/libraries/syn/gtech.db'
Loading db file '/cad/synopsys/design_vision/libraries/syn/standard.sldb'
  Loading link library 'saed90nm_typ'
  Loading link library 'gtech'
Loading verilog file '/home/guests/phd/sudi/asiclab/dft/seq/counter.v'
Detecting input file type automatically (-rtl or -netlist).
Reading with Presto HDL Compiler (equivalent to -rtl option).
Running PRESTO HDLC
Compiling source file /home/guests/phd/sudi/asiclab/dft/seq/counter.v

Inferred memory devices in process
        in routine univ_bin_counter line 12 in file
                '/home/guests/phd/sudi/asiclab/dft/seq/counter.v'.
===============================================================================
|    Register Name     |    Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|      r_reg_reg       | Flip-flop |   8   |  Y  | N  | Y  | N  | N  | N  | N  |
===============================================================================
Presto compilation completed successfully.
Current design is now '/home/guests/phd/sudi/asiclab/dft/seq/univ_bin_counter.db:univ_bin_counter'
Loaded 1 design.
Current design is 'univ_bin_counter'.
design_vision> Current design is 'univ_bin_counter'.
Loading db file '/home/guests/phd/sudi/libs/saed90nm.sdb'
Loading db file '/cad/synopsys/design_vision/libraries/syn/generic.sdb'

design_vision>
```

8. Execute the following commands :-

```
check_design

set_scan_configuration -style multiplexed_flip_flop

link

create_port -direction in [list test_si]
create_port -direction out [list test_so]
create_port -direction in test_en

set_dft_signal -view existing_dft -type reset -port reset -active_state 1
set_dft_signal -view existing_dft -type ScanClock -timing {45 55} -port clk
set_dft_signal -view spec -type scanDataIn -port  [list test_si]
set_dft_signal -view spec -type scanDataOut -port  [list test_so]
set_dft_signal -view spec -type scanEnable -port test_en -active_state 1



create_test_protocol
dft_drc -verbose

set_scan_configuration -chain_count 1
compile -scan
preview_dft
insert_dft
write_test_protocol -output counter.spf
```

```
        in routine univ_bin_counter line 12 in file
                '/home/guests/phd/sudi/asiclab/dft/seq/counter.v'.
=========================================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
=========================================================================================
|     r_reg_reg       | Flip-flop |   8   |  Y  | N  | Y  | N  | N  | N  | N  |
=========================================================================================
Presto compilation completed successfully.
Current design is now '/home/guests/phd/sudi/asiclab/dft/seq/univ_bin_counter.db:univ_bin_counter'
Loaded 1 design.
Current design is 'univ_bin_counter'.
design_vision> Current design is 'univ_bin_counter'.
Loading db file '/home/guests/phd/sudi/libs/saed90nm.sdb'
Loading db file '/cad/synopsys/design_vision/libraries/syn/generic.sdb'

design_vision> check_design

****************************************
check_design summary:
Version:     K-2015.06-SP2-1
Date:        Fri Mar 16 15:08:43 2018
****************************************

                  Name                                                    Total
--------------------------------------------------------------------------------
Cells                                                                      1
    Cells do not drive (LINT-1)                                            1
--------------------------------------------------------------------------------

Warning: In design 'univ_bin_counter', cell 'C73' does not drive any nets. (LINT-1)
1
design_vision>
```

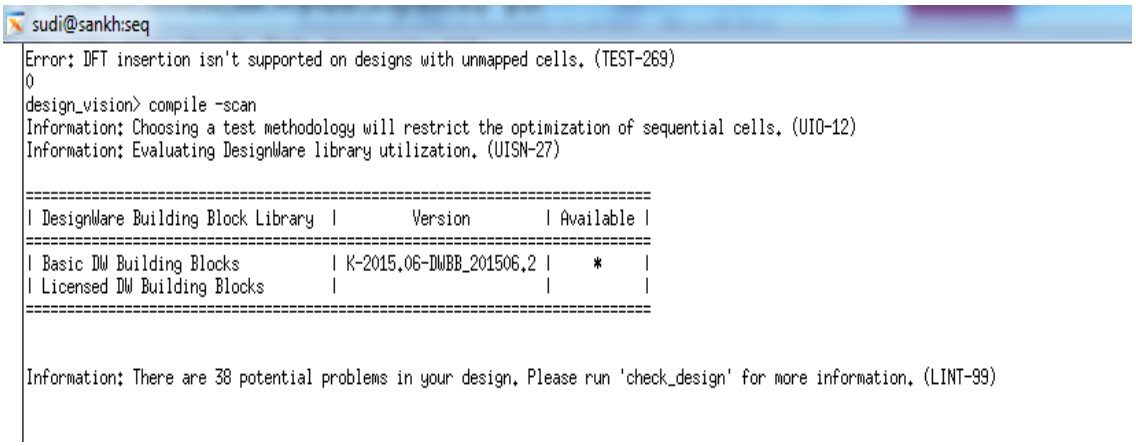
9. Execute all DFT related commands as below: -

```
sudi@sankh:seq
Loading db file '/cad/synopsys/design_vision/libraries/syn/generic.sdb'

design_vision> check_design

****************************************
check_design summary:
Version:     K-2015.06-SP2-1
Date:        Fri Mar 16 15:08:43 2018
****************************************

                  Name                                                    Total
--------------------------------------------------------------------------------
Cells                                                                      1
    Cells do not drive (LINT-1)                                            1
--------------------------------------------------------------------------------

Warning: In design 'univ_bin_counter', cell 'C73' does not drive any nets. (LINT-1)
1
design_vision> set_scan_configuration -style multiplexed_flip_flop
Accepted scan configuration for modes: all_dft
1
design_vision> link

  Linking design 'univ_bin_counter'
  Using the following designs and libraries:
  --------------------------------------------------------------------------
  saed90nm_typ (library)      /home/guests/phd/sudi/libs/saed90nm_typ.db

1
design_vision> create_port -direction in [list test_si]
Creating port 'test_si' in design 'univ_bin_counter'.
1
design_vision> create_port -direction out [list test_so]
Creating port 'test_so' in design 'univ_bin_counter'.
1
design_vision> create_port -direction in test_en
Creating port 'test_en' in design 'univ_bin_counter'.
1
design_vision> set_dft_signal -view existing_dft -type reset -port reset -active_state 1
Accepted dft signal specification for modes: all_dft
1
design_vision> set_dft_signal -view existing_dft -type ScanClock -timing {45 55} -port clk
Accepted dft signal specification for modes: all_dft
1
design_vision> set_dft_signal -view spec -type scanDataIn -port  [list test_si]
Accepted dft signal specification for modes: all_dft
1
design_vision> set_dft_signal -view spec -type scanDataOut -port  [list test_so]
Accepted dft signal specification for modes: all_dft
1
design_vision> set_dft_signal -view spec -type scanEnable -port test_en -active_state 1
Accepted dft signal specification for modes: all_dft
1
design_vision>
```

10. Continue

```
Accepted dft signal specification for modes: all_dft
1
design_vision> create_test_protocol
In mode: all_dft...

Information: Starting test protocol creation. (TEST-219)
  ...reading user specified clock signals...
Information: Identified system/test clock port clk (45.0,55.0). (TEST-265)
  ...reading user specified asynchronous signals...
Information: Identified active high asynchronous control port reset. (TEST-266)
1
design_vision> dft_drc -verbose
In mode: all_dft...
  Pre-DFT DRC enabled

Information: Starting test design rule checking. (TEST-222)
  Loading test protocol
  ...checking vector rules...
  ...checking pre-dft rules...

------------------------------------------------------------
  DRC Report

  Total violations: 0

------------------------------------------------------------


Test Design rule checking did not find violations
Information: Test design rule checking completed. (TEST-123)
Current design is 'univ_bin_counter'.
Current design is 'univ_bin_counter'.
Warning: The current design contains unmapped components. The output netlist might not be read back into the system. (TEST-268)
1
design_vision> set_scan_configuration -chain_count 1
Accepted scan configuration for modes: all_dft
1
design_vision>
```

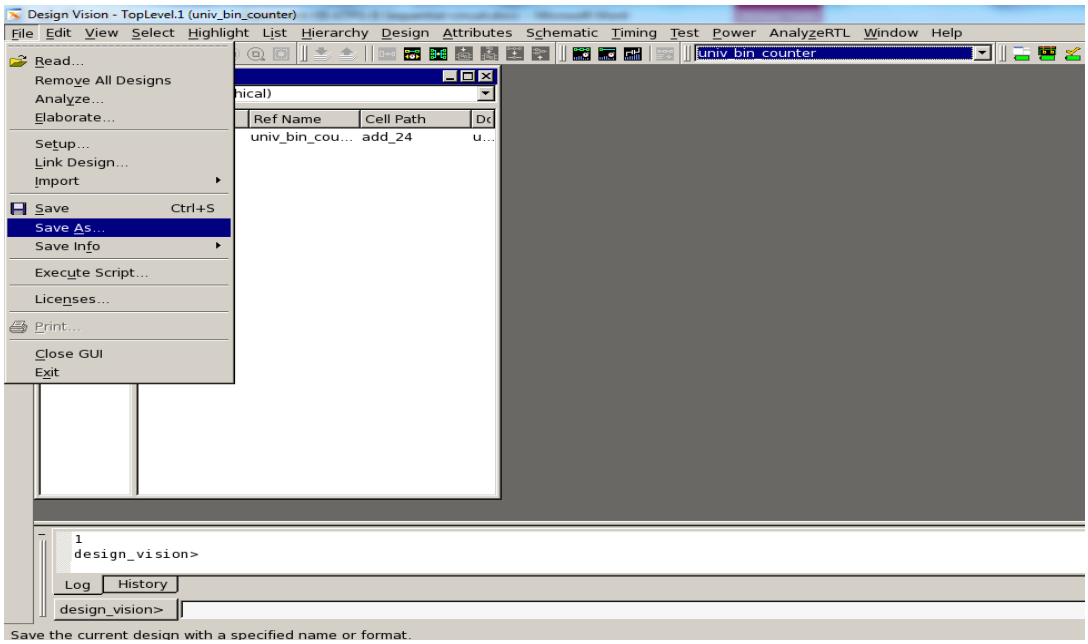
11. Continue: -



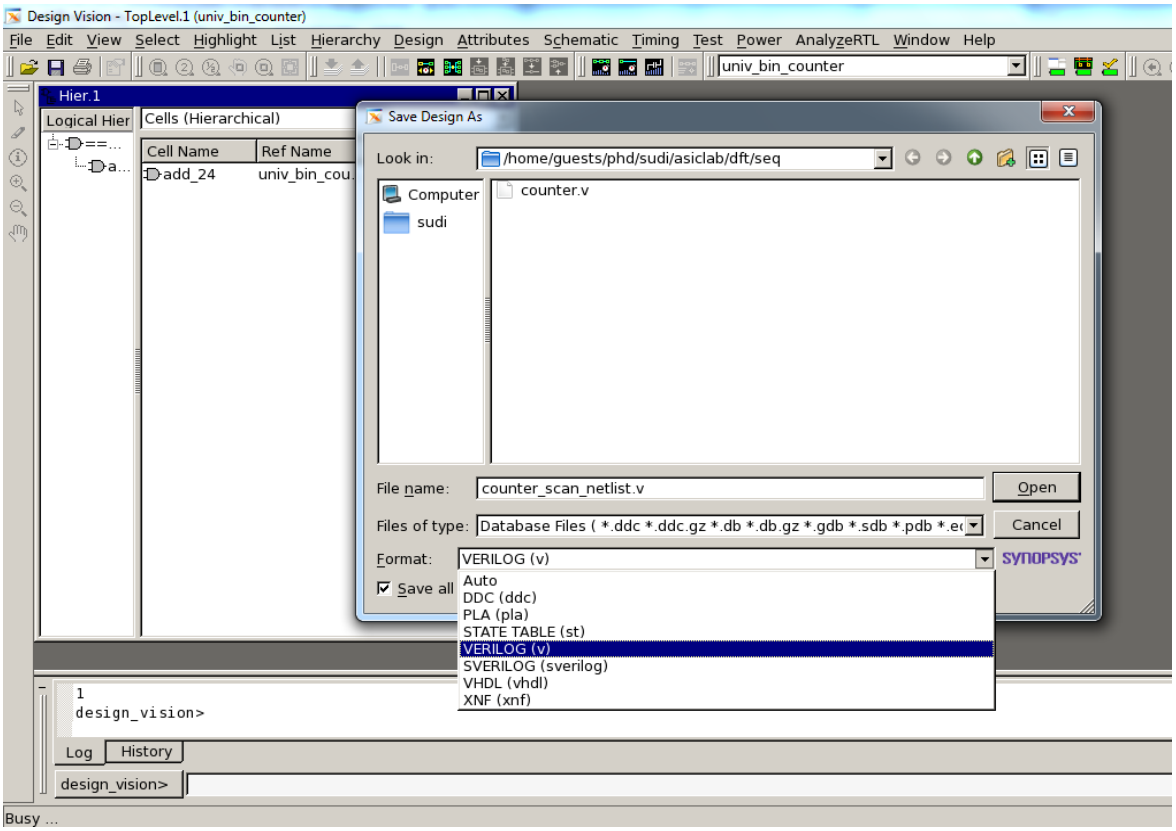
12. Continue: -

```
sudi@sankh:seq
design_vision> preview_dft

Information: Starting test design rule checking. (TEST-222)
Test Design rule checking did not find violations
Information: Test design rule checking completed. (TEST-123)
  Architecting Scan Chains

****************************************
Preview_dft report
For     : 'Insert_dft' command
Design : univ_bin_counter
Version: K-2015.06-SP2-1
Date    : Fri Mar 16 15:19:47 2018
****************************************

Number of chains: 1
Scan methodology: full_scan
Scan style: multiplexed_flip_flop
Clock domain: no_mix
Scan enable: test_en (no hookup pin)


Scan chain '1' (test_si --> test_so) contains 8 cells



************ Test Point Plan Report ************
Total number of test points  : 0
Number of Autofix test points: 0
Number of Wrapper test points: 0
Number of test modes         : 0
Number of test point enables : 0
Number of data sources       : 0
Number of data sinks         : 0
************************************************

1
design_vision> insert_dft
Loading db file '/home/guests/phd/sudi/libs/saed90nm_typ.db'

Information: Starting test design rule checking. (TEST-222)
Test Design rule checking did not find violations
Information: Test design rule checking completed. (TEST-123)
  Architecting Scan Chains
  Routing Scan Chains
  Routing Global Signals
  Mapping New Logic
Resetting current test mode

1
design_vision> write_test_protocol -output counter.spf
Writing test protocol file '/home/guests/phd/sudi/asiclab/dft/seq/counter.spf' for mode 'Internal_scan'...
1
design_vision>
```

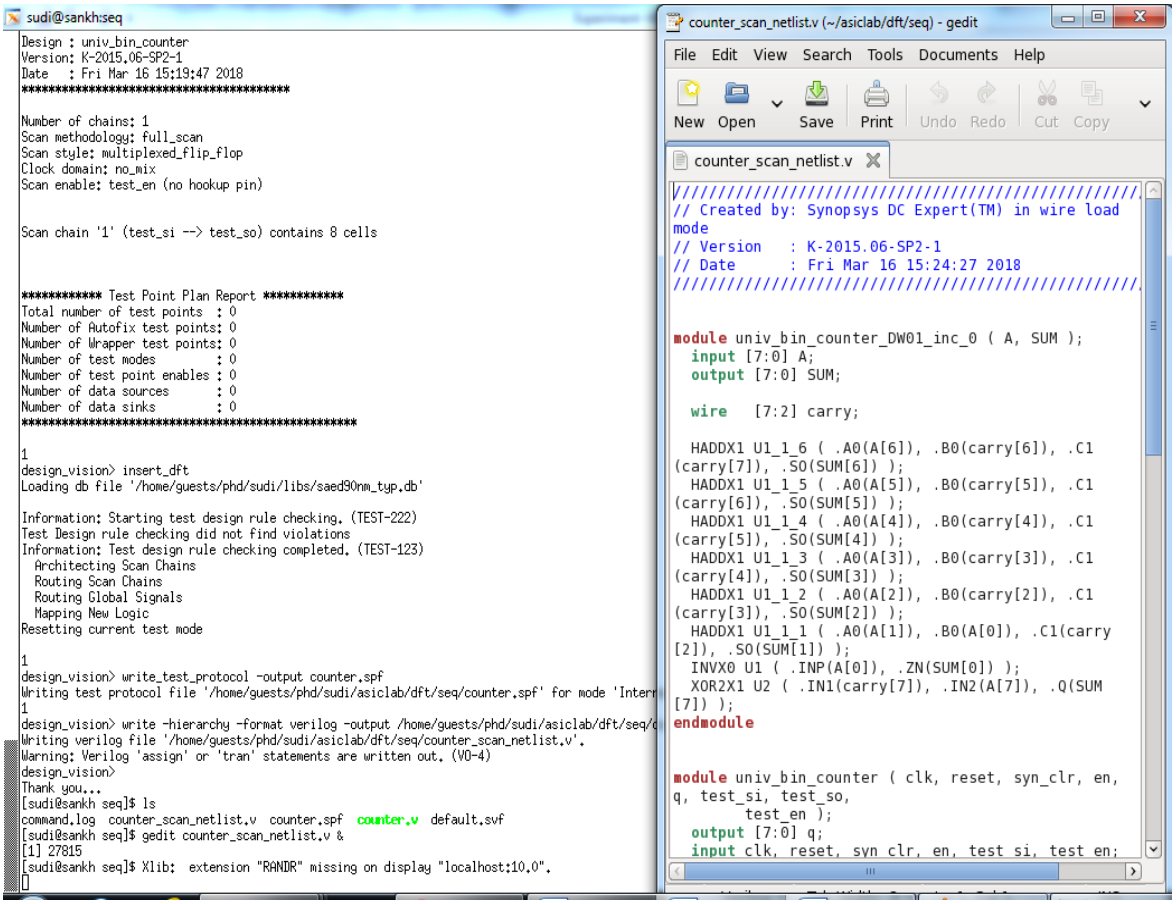
13. Save the scan inserted netlist as below: -



14. Continue: -



15. File- Exit- Design _Vision.
16. Open the counter_scan_netlist.v and observe the difference between your earlier counter_net.v and scan inserted counter_scan_netlist.v



17. Open the Tetramax and generate ATPG

```
 BUILD-T> read_netlist /home/guests/phd/sudi/libs/saed90nm.v

BUILD-T> read_netlist /home/guests/phd/sudi/asiclab/dft/seq/counter_scan_netlist.v


BUILD-T> run_build_model univ_bin_counter


DRC-T> set_drc /home/guests/phd/sudi/asiclab/dft/seq/counter.spf
DRC-T> run_drc


TEST-T> add_faults -all
  280 faults were added to fault list.
TEST-T> run_atpg -ndetects 1


TEST-T> write_patterns /home/guests/phd/sudi/asiclab/dft/seq/counter_scan_netlist -internal -format binary
  End writing file 'counter_scan_netlist' with 16 patterns, File_size = 2488, CPU_time = 0.0 sec.
TEST-T> write_testbench -input /home/guests/phd/sudi/asiclab/dft/seq/counter_scan_netlist -output /home/guests/phd/sudi/asiclab/dft/seq/counter_scan_netlist_atpg
  Executing 'stil2verilog'...
TEST-T> pwd
 /home/guests/phd/sudi/asiclab/dft/seq
TEST-T> write_testbench -input /home/guests/phd/sudi/asiclab/dft/seq/counter_scan_netlist -output counter_aptg.v
  Executing 'stil2verilog'...
TEST-T>
```

18. Simulate the ATPG using VCS as before.