

ASIC Design Lab (EC-6272)

Experiment – IV

Synthesis II

1. Open a terminal in the workstation and source cadence.cshrc in the terminal
2. In this lab session, Synthesis of RTL models **with constraints** will be carried out, for which a few library files and a constraint file will be shared in the lab session. The necessary files can be downloaded from links provided during class.
3. Make a working folder, script the verilog RTL and testbench (Follow the instructions in the previous experiment Synthesis Part-I).
4. We use Cadence synthesis tool : GENUS Synthesis Solution. Type the command as below and check path of genus is echoed or not in the workstation.

```

zarathustra@mahananda:lab_synII
File Edit View Search Terminal Help
[zarathustra@mahananda ~/Desktop]$ source cadence.cshrc

*****
***** Welcome NITR to Cadence tools *****
*****

[zarathustra@mahananda ~/Desktop]$ which genus
/cad/cadence/GENUS/15.20-s010_1/bin/genus
[zarathustra@mahananda ~/Desktop]$ cd ../ASIC_lab/
[zarathustra@mahananda ~/ASIC_lab]$ mkdir lab_synII
[zarathustra@mahananda ~/ASIC_lab]$ cd lab_synII
[zarathustra@mahananda lab_synII]$ ls
cnt.v counttest.v saed90nm.typ.lib saed90nm.v Screenshot.png
[zarathustra@mahananda lab_synII]$ genus -gui
Cadence Genus(TM) Synthesis Solution.
Copyright 2016 Cadence Design Systems, Inc. All rights reserved worldwide.
Cadence and the Cadence logo are registered trademarks and Genus is a trademark
of Cadence Design Systems, Inc. in the United States and other countries.

Version: GENUS15.21 - 15.20-s010_1, built Tue Feb 09 2016
Options:
Date: Tue Feb 04 15:14:04 2020
Host: mahananda.nitr.in (x86_64 w/Linux 2.6.32-504.el6.x86_64) (4*Intel(R) Xe
on(R) CPU E3-1226 v3 @ 3.30GHz 8192KB)

```

5. In the terminal, execute genus –gui for invoking the EDA Synthesis tool

]\$ genus –gui

6. Minimize the gui and follow below instructions, mentioning the proper path for linking the saed90nm library files

```

genus@root:> read_libs saed90nm_typ.lib
genus@root:> read_hdl -v2001 counter.v
genus@root:> elaborate

```

7. A constraint file is sourced to insert constraints as shown below, and Change the constraints accordingly for your designs (input, output and clock).

```

constraints1.sdc - Notepad
File Edit Format View Help
*****
*****
set_EXTCLK "clk" ;
set_units -time 1.0ns ;
set_units -capacitance 1.0pF ;
set_EXTCLK_PERIOD 10.0;

create_clock -name "EXTCLK" -period "EXTCLK_PERIOD" -waveform "0 [expr EXTCLK_PERIOD/2]" {ge
set_SKEW 0.200
set_clock_uncertainty $SKEW [get_clocks EXTCLK]

set_MINRISE 0.20
set_MAXRISE 0.25
set_MINFALL 0.20
set_MAXFALL 0.25

set_clock_transition -rise -min $MINRISE [get_clocks EXTCLK]
set_clock_transition -rise -max $MAXRISE [get_clocks EXTCLK]
set_clock_transition -fall -min $MINFALL [get_clocks EXTCLK]
set_clock_transition -fall -max $MAXFALL [get_clocks EXTCLK]
*****

```

```

*****
#
# DELAY DEFINITION
#
*****
set_input_delay -clock [get_clocks EXTCLK] -add_delay 0.3 [get_ports en]
set_input_delay -clock [get_clocks EXTCLK] -add_delay 0.3 [get_ports reset]
set_input_delay -clock [get_clocks EXTCLK] -add_delay 0.3 [get_ports syn_clr]

set_output_delay -clock [get_clocks EXTCLK] -add_delay 0.3 [get_ports q]

##set_operating_conditions WCCOM

set_max_capacitance 0.5 [all_outputs]

##set_min_capacitance 0.05 [all_inputs]

set_max_fanout 10 [all_inputs]

##set_max_transition 0.5 EXTCLK/q

```

```
genus@root:> read_sdc constraints1.sdc
```

```
genus@root:> synthesize -to_mapped
```

8. Save the gate level netlist

```
genus@root:> write_hdl > d_with_cnstr_netlist.v
```

9. Find the d_with_cnstr_netlist.v file created in the working directory.

10. Record and save the area, timing and power by following the below commands

```
genus@root:> report_units
```

```
genus@root:> report_timing > timing
```

```
genus@root:> report_area > area
```

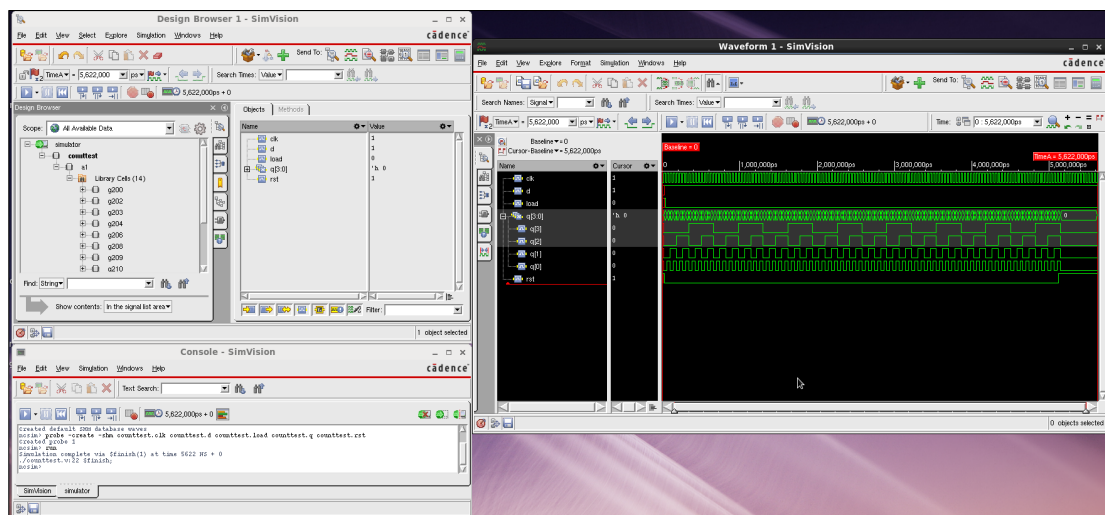
```
genus@root:> report_power > power
```

```
genus@root:> report_utilization
```

```
genus@root:> report_sequential
```

11. Do the synthesis and report timing. Change the constraints and check for the slack. And compare the area, timing, power for unconstrained and constrained synthesized designs (while varying the constraints).
12. Simulate the design as done in earlier experiment. Check the simulation using this netlist file with constraints. (Blindly don't follow the manual. Give the correct path based on where you have the libs folder copied. Use the command "pwd" to get path)

```
[$ neverilog counter_tst.v d_with_cnstr_netlist.v +access+rw -v saed90nm.v +gui
```



For more details check the Genus_gui document in the installed folder