

## ASIC Design Lab (EC-664)

### Experiment – I

#### Simulation of Finite State Machine (FSM) based Designs in Verilog HDL.

1. Open the terminal
2. Source the cadence.cshrc
3. Check whether the commands are working as below: -

```
sudi@mahananda:~  
[sudi@mahananda ~]$ ls  
17-08-08-19:50:31_Logs  cad.cshrc  default.svf  encounter.log  encounter.1  
17-08-08-20:25:50_Logs  cadence.cshrc  default.svf  encounter.log1  irun.log  
aditya  cadence.cshrc  default.svf  encounter.log2  libscore_wd  
aditya.tgz  cadence.cshrc  default.svf  encounter.log3  libscore_wd  
area  CDS.log  encounter.cmd  encounter.logv  libscore_wd  
asiclab  CDS.log.1  encounter.cmd1  encounter.logv1  libscore_wd  
command.log  command.log  encounter.cmd3  encounter.logv2  LPA.sum  
[sudi@mahananda ~]$ source cadence.cshrc  
*****  
***** Welcome NITR to Cadence tools *****  
*****  
[sudi@mahananda ~]$ which ncvlog  
/cad/cadence/INCISIVE/grid/avs/install/incisive/14.2/latest/tools/bin/ncvlog  
[sudi@mahananda ~]$ which ncverilog  
/cad/cadence/INCISIVE/grid/avs/install/incisive/14.2/latest/tools/bin/ncverilog  
[sudi@mahananda ~]$ which simvision  
/cad/cadence/INCISIVE/grid/avs/install/incisive/14.2/latest/tools/bin/simvision  
[sudi@mahananda ~]$
```

4. Create a directory for saving files as below: -

```
sudi@mahananda:~/test  
[sudi@mahananda ~]$ ls  
17-08-08-19:50:31_Logs  cad.cshrc  default.svf  encounter.log  encounter.1  
17-08-08-20:25:50_Logs  cadence.cshrc  default.svf  encounter.log1  irun.log  
aditya  cadence.cshrc  default.svf  encounter.log2  libscore_wd  
aditya.tgz  cadence.cshrc  default.svf  encounter.log3  libscore_wd  
area  CDS.log  encounter.cmd  encounter.logv  libscore_wd  
asiclab  CDS.log.1  encounter.cmd1  encounter.logv1  libscore_wd  
command.log  command.log  encounter.cmd3  encounter.logv2  LPA.sum  
[sudi@mahananda ~]$ source cadence.cshrc  
*****  
***** Welcome NITR to Cadence tools *****  
*****  
[sudi@mahananda ~]$ which ncvlog  
/cad/cadence/INCISIVE/grid/avs/install/incisive/14.2/latest/tools/bin/ncvlog  
[sudi@mahananda ~]$ which ncverilog  
/cad/cadence/INCISIVE/grid/avs/install/incisive/14.2/latest/tools/bin/ncverilog  
[sudi@mahananda ~]$ which simvision  
/cad/cadence/INCISIVE/grid/avs/install/incisive/14.2/latest/tools/bin/simvision  
[sudi@mahananda ~]$ mkdir test  
[sudi@mahananda ~]$ cd test  
[sudi@mahananda ~]$ cd test  
[sudi@mahananda ~]$ ls  
[sudi@mahananda ~]$ cd test  
[sudi@mahananda ~]$ ls  
[sudi@mahananda ~]$
```

5. Create design\_file.v as shown below: - (gedit counter.v)

```
sudi@mahananda:counter  
[sudi@mahananda ~]$ ls  
17-08-08-19:50:31_Logs  cad.cshrc  default.svf  encounter.log  encounter.1  
17-08-08-20:25:50_Logs  cadence.cshrc  default.svf  encounter.log1  irun.log  
aditya  cadence.cshrc  default.svf  encounter.log2  libscore_wd  
aditya.tgz  cadence.cshrc  default.svf  encounter.log3  libscore_wd  
area  CDS.log  encounter.cmd  encounter.logv  libscore_wd  
asiclab  CDS.log.1  encounter.cmd1  encounter.logv1  libscore_wd  
command.log  command.log  encounter.cmd3  encounter.logv2  LPA.sum  
[sudi@mahananda ~]$ cd synopsys_design  
synopsys_design: No such file or directory.  
[sudi@mahananda ~]$ ls  
17-08-08-19:50:31_Logs  cad.cshrc  default.svf  encounter.log  encounter.1  
17-08-08-20:25:50_Logs  cadence.cshrc  default.svf  encounter.log1  irun.log  
aditya  cadence.cshrc  default.svf  encounter.log2  libscore_wd  
aditya.tgz  cadence.cshrc  default.svf  encounter.log3  libscore_wd  
area  CDS.log  encounter.cmd  encounter.logv  libscore_wd  
asiclab  CDS.log.1  encounter.cmd1  encounter.logv1  libscore_wd  
command.log  command.log  encounter.cmd3  encounter.logv2  LPA.sum  
[sudi@mahananda ~]$ cd synopsys_designs  
[sudi@mahananda ~/synopsys_designs]$ ls  
command.log  novas.conf  novas.rc  saad30na_rc  
[sudi@mahananda ~/synopsys_designs]$ cd counter  
[sudi@mahananda counter]$ ls  
command.log  counter_net.v  counter_saif  counter.vcd  default.svf  libscore_wd  
counter_net.v  counter_tst.v  counter_tst.v  counter.v  filesnames.log  int  
[sudi@mahananda counter]$ gedit counter.v
```

```

counter.v (~synopsys_designs/counter) - gedit
File Edit View Search Tools Documents Help
New Open Save Print Undo Redo Cut

counter.v
[
timescale 1ns/1ns
module univ_bin_counter
  /*(parameter N= 8)
  (
    input wire clk, reset,
    input wire syn_clr, en,
    output wire [7:0] q);

    reg [7:0] r_reg, r_next;

    always @ (posedge clk, posedge reset)
    if (reset)
      r_reg <= 0;
    else
      r_reg <= r_next;

    always @*
    if (syn_clr)
      r_next = 0;

    else if (en)
      r_next = r_reg+1;
    else
      r_next = r_reg;

    assign q = r_reg;
  endmodule

```

6. Check the syntax of design.v (in this example: counter.v) (no syntax errors found)

```

sudi@mahananda:~/test
[sudi@mahananda ~]$ ls
17-06-06-19:50:31_Logs  cad.cshrc  default.svf  encounter.log  encounter.logv3
17-06-06-20:25:50_Logs  cadence.cshrc  encounter.log1  encounter.log2  irun.log
editval.tgz             CIS.log     encounter.cad  encounter.log5  libscore_work
area                    CIS.log.1   encounter.cmd1 encounter.logv1  LPA.sum
csiclab                 csocash.log encounter.cmd5 encounter.logv2

[sudi@mahananda ~]$ source cadence.cshrc
*****
***** Welcome NITR to Cadence tools *****
*****

[sudi@mahananda ~]$ which nclog
/cad/cadence/INCISIVE/grid/avs/install/incisive/14.2/latest/tools/bin/nclog
[sudi@mahananda ~]$ which ncverilog
/cad/cadence/INCISIVE/grid/avs/install/incisive/14.2/latest/tools/bin/ncverilog
[sudi@mahananda ~]$ which simvision
/cad/cadence/INCISIVE/grid/avs/install/incisive/14.2/latest/tools/bin/simvision
[sudi@mahananda ~]$ mkdir test
[sudi@mahananda ~]$ cd test
[sudi@mahananda ~/test]$ ls
[sudi@mahananda ~/test]$ gedit counter.v
Xlib: extension "RANDR" missing on display "localhost:10.0".
[sudi@mahananda ~/test]$ ls
counter.v
[sudi@mahananda ~/test]$ nclog counter.v
nclog(64): 14.20-s003; (c) Copyright 1995-2015 Cadence Design Systems, Inc.
[sudi@mahananda ~/test]$

```

7. Induce syntax error in line 24 by removing semicolon

```

counter.v (~test) - gedit
File Edit View Search Tools Documents
New Open Save Print Undo Redo

counter.v
[
timescale 1ns/1ns
module univ_bin_counter
  /*(parameter N= 8)
  (
    input wire clk, reset,
    input wire syn_clr, en,
    output wire [7:0] q);

    reg [7:0] r_reg, r_next;

    always @ (posedge clk, posedge reset)
    if (reset)
      r_reg <= 0;
    else
      r_reg <= r_next;

    always @*
    if (syn_clr)
      r_next = 0;

    else if (en)
      r_next = r_reg+1
    else
      r_next = r_reg;

    assign q = r_reg;
  endmodule

```

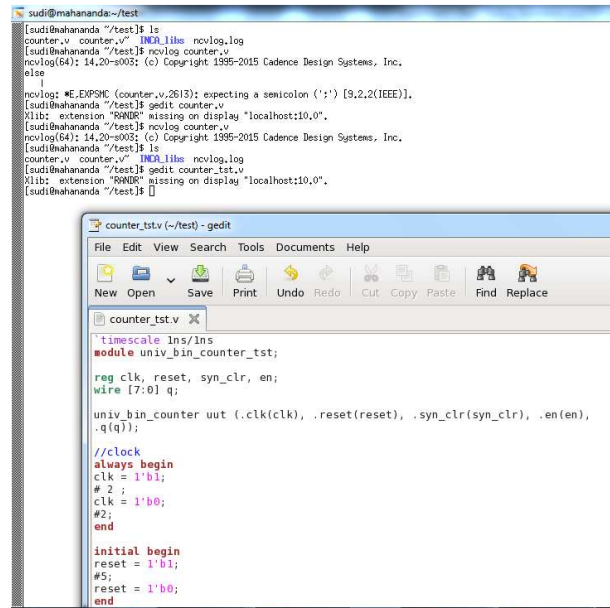
8. Perform syntax check: - (shows syntax near 26|3)

```

sudi@mahananda:~/test
[sudi@mahananda ~/test]$ ls
counter.v  counter.v  INCISIVE  nclog.log
[sudi@mahananda ~/test]$ nclog counter.v
nclog(64): 14.20-s003; (c) Copyright 1995-2015 Cadence Design Systems, Inc.
else
|
nclog: #E:PSNC (counter.v,26|3): expecting a semicolon (';') [9,2,2(IEEE)].
[sudi@mahananda ~/test]$

```

9. Correct the syntax check and save the file.
10. Similarly create the testbench file for design, check syntax and save the file. (Shown below)



```

sudi@mahananda:~/test
[sudi@mahananda ~/test]$ ls
counter.v  counter.v~  INCALike  ncverilog.log
[sudi@mahananda ~/test]$ ncverilog counter.v
ncverilog(64): 14.20-s003: (c) Copyright 1995-2015 Cadence Design Systems, Inc.
else
|
ncverilog: *E:EXPSMC (counter.v.2613): expecting a semicolon (;) [9,2,2(IEEE)].
[sudi@mahananda ~/test]$ gedit counter.v
Xlib: extension "RANDR" missing on display "localhost:10.0".
[sudi@mahananda ~/test]$ ncverilog counter.v
ncverilog(64): 14.20-s003: (c) Copyright 1995-2015 Cadence Design Systems, Inc.
[sudi@mahananda ~/test]$ ls
counter.v  counter.v~  INCALike  ncverilog.log
[sudi@mahananda ~/test]$ gedit counter_tst.v
Xlib: extension "RANDR" missing on display "localhost:10.0".
[sudi@mahananda ~/test]$

```

```

counter_tst.v - gedit
File Edit View Search Tools Documents Help
New Open Save Print Undo Redo Cut Copy Paste Find Replace
counter_tst.v
timescale 1ns/1ns
module univ_bin_counter_tst;

reg clk, reset, syn_clr, en;
wire [7:0] q;

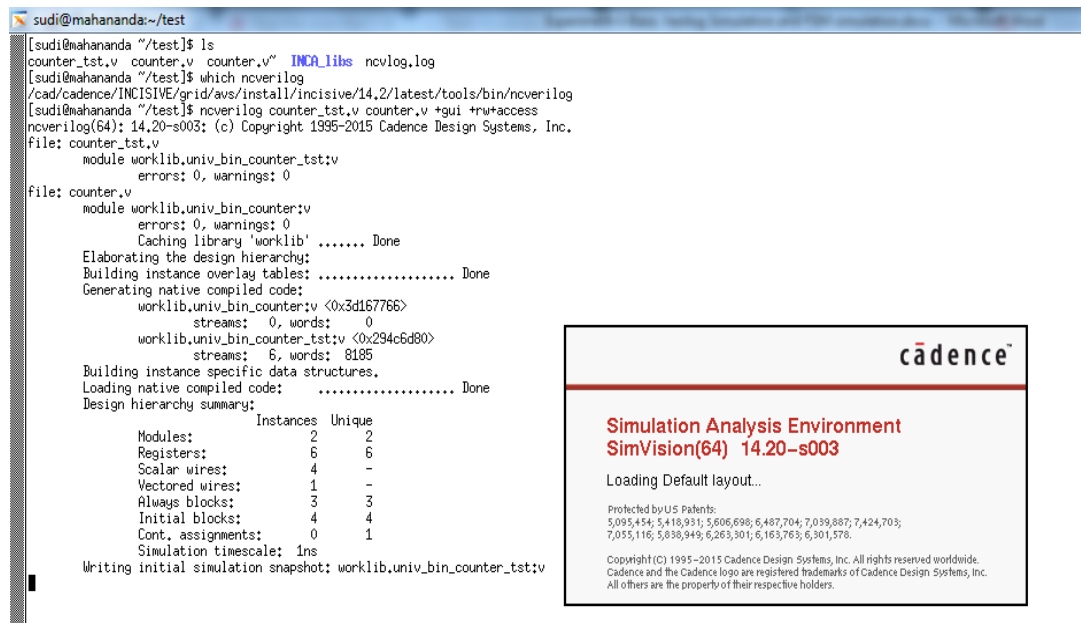
univ_bin_counter uut (.clk(clk), .reset(reset), .syn_clr(syn_clr), .en(en),
.q(q));

//clock
always begin
clk = 1'b1;
# 2;
clk = 1'b0;
#2;
end

initial begin
reset = 1'b1;
#5;
reset = 1'b0;
end

```


11. Execute the command as below: - ncverilog counter\_tst.v counter.v +gui +access+rw



```

sudi@mahananda:~/test
[sudi@mahananda ~/test]$ ls
counter.v  counter.v~  INCALike  ncverilog.log
[sudi@mahananda ~/test]$ which ncverilog
/cad/cadence/INCISIVE/grid/aus/install/incisive/14.2/latest/tools/bin/ncverilog
[sudi@mahananda ~/test]$ ncverilog counter_tst.v counter.v +gui +rw+access
ncverilog(64): 14.20-s003: (c) Copyright 1995-2015 Cadence Design Systems, Inc.
file: counter_tst.v
    module worklib.univ_bin_counter_tst:v
        errors: 0, warnings: 0
file: counter.v
    module worklib.univ_bin_counter:v
        errors: 0, warnings: 0
        Caching library 'worklib' ..... Done
        Elaborating the design hierarchy:
        Building instance overlay tables: ..... Done
        Generating native compiled code:
            worklib.univ_bin_counter:v <0x3d167766>
                streams: 0, words: 0
            worklib.univ_bin_counter_tst:v <0x234c6d80>
                streams: 6, words: 8185
        Building instance specific data structures.
        Loading native compiled code: ..... Done
        Design hierarchy summary:
            Instances Unique
            Modules:    2      2
            Registers:  6      6
            Scalar wires: 4      -
            Vectored wires: 1      -
            Always blocks: 3      3
            Initial blocks: 4      4
            Cont. assignments: 0      1
            Simulation timescale: 1ns
        Writing initial simulation snapshot: worklib.univ_bin_counter_tst:v

```



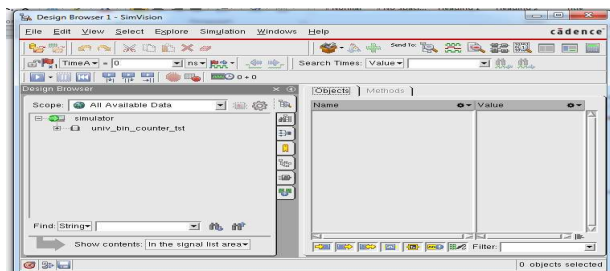
**Simulation Analysis Environment**  
**SimVision(64) 14.20-s003**

Loading Default layout..

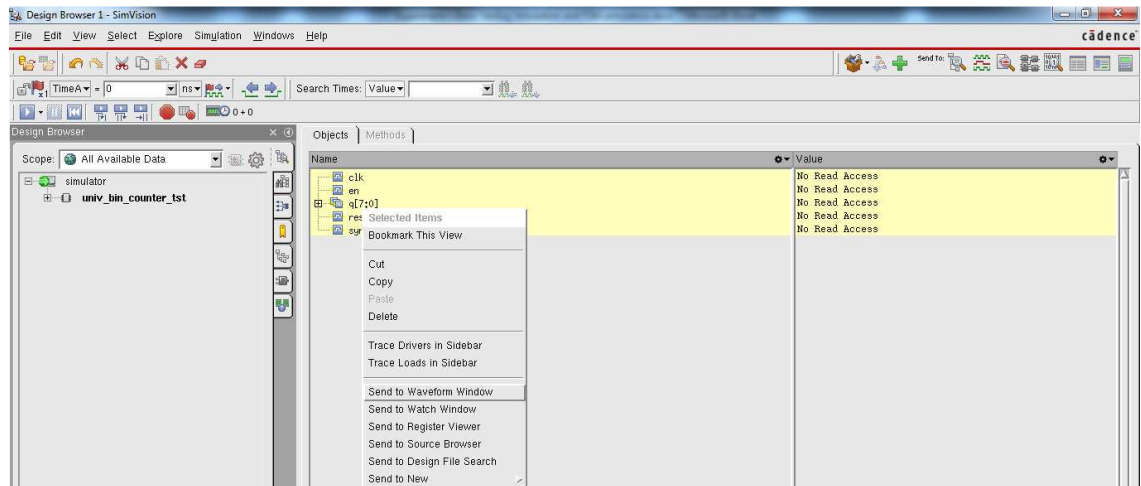
Protected by US Patents:  
5,095,454; 5,418,931; 5,606,698; 6,487,704; 7,039,887; 7,424,703;  
7,055,116; 5,838,949; 6,263,301; 6,163,763; 6,301,578.

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All others are the property of their respective holders.

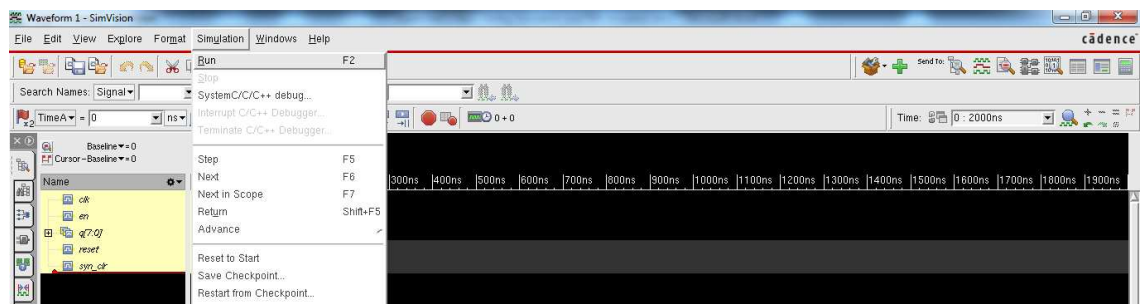
12. Simvision gui will open: -



13. Right click on signals as shown below and send to Waveform Window: -



14. Run the simulation: -



15. Observe the waveforms: -

