swissbit®

Product Data Sheet

Industrial eMMC Memory

EM-10 Series

JEDEC e MMC 4.41 compliant,
BGA 153 ball, MLC

Industrial Temperature Grade
(Automotive on request)

Date: August 27, 2019
Revision: 1.00

made in germany

Contents

Embedded MMC 4.41
EM-10 Automotive e·MMC Memory 4GB to 16GB

1. Product Summary

- Fully compliant with JEDEC e·MMC 4.41 Standard (JESD84-A441)
- 153-ball BGA, 0.5mm pitch
  11.5 x 13mm, RoHS compliant
- AEC-Q100 Grade 2 qualified
- MLC NAND base technology
- Instant-Up function for fast boot, optimal to replace NOR Flash
- e·MMC 4.41 specification, with extended diagnostic features
- Power Supply: (Low-power CMOS technology)
  - VCCQ 1.65V...1.95V or 2.7V...3.6V e·MMC supply
  - VCC 2.7V...3.6V NAND Flash supply
- Optimized FW algorithms
  - Instant-Up function for fast boot
    Proprietary controller function which allows the host to start booting from the e·MMC in DDR mode within less than 10 ms after first command. Highly improved latency compared to standard e·MMC solutions. Targeting fast boot applications, e.g. fast loading of system-critical or safety-relevant data
  - Power loss protection incl. redundancy features and voltage detection to write protect the NAND flash
  - Firmware Protection Features (redundant anchor block & power-up check)
  - Diagnostic features with Life Time Monitoring tool support exceeding e·MMC standard
  - Advanced Wear Leveling technology
    Equal wear leveling of static and dynamic data.
    The wear leveling assures that dynamic data as well as static data is balanced evenly across the memory, maximizing the write endurance of the device
  - Page Based Flash Management: by using a page related flash management the write amplification for random write operations is minimized, allowing for an extended life time and high write performance
  - Read Disturb Management technology
    Read activity is monitored and the content is refreshed before critical levels occur
  - Dynamic Auto Refresh for data retention enhancement
    The interruptible background process maintains the user data for read disturb effects or retention degradation due to high temperature effects
  - Near Miss ECC technology
    Minimize the risk of uncorrectable bit failure over the product life time. Each read command analyzes ECC margin levels and refresh data if necessary
- High reliability
  - Designed for automotive market and especially read intensive application like instrument cluster, navigation and general boot medium use cases, NOR Flash replacement
  - Longevity, long life cycle, high data retention together with high temperature profile
  - Industrial temperature from -40° up to 85°C (automotive grade up to 105°C on request)
  - In-field firmware update without user data loss
  - Controlled BOM & PCN process

2. Ordering Information

Table 1: Standard Product List

Capacity	Part Number
4GBytes	SFEM4096BxEM1T0-t-GE-1y1-STD
8GBytes	SFEM008GBxEM1T0-t-LF-1y1-STD
16GBytes	SFEM016GBxEM1T0-t-HG-1y1-STD

x = product generation; t = temperature; y = firmware revision

Table 2: Available Part Numbers

	Automotive Temperature
Capacity	Part Number
4GBytes	SFEM4096B1EM1T0-I-GE-111-STD
8GBytes	SFEM008GB1EM1T0-I-LF-111-STD
16GBytes	SFEM016GB1EM1T0-I-HG-111-STD

3. Product Description

The Swissbit e·MMC is a managed non-volatile storage consisting of a single chip MMC controller and a NAND flash memory chip inside a JEDEC defined standard BGA package. It is specially designed as a small form factor memory product for storage of data and as a boot media. The performance is optimized for low power consumption. The utilization of MLC NAND technology targets higher demanding automotive and industrial applications, which is supported by the automotive temperature grade specification.

The e·MMC controller directly manages NAND flash, including ECC, wear-leveling, IOPS optimization and read retry. The EM-10 firmware supports fast boot up and short response time as well as optimized data care management for increased retention under elevated temperature conditions. A very detailed life time status information allows for exact lifetime prediction in the real application environment.

e·MMC communication is based on an advanced 10-signal bus. The communication protocol is defined as a part of the JEDEC e·MMC standard and referred to as the e·MMC mode.

3.1 Performance Specification

Table 3: Performance

System Performance		Instant-Up[1]	Typical Sustained[2]	Unit
Burst Data transfer Rate (max clock 52MHz)				MB/s
Sequential Read operation DDR	4GB	86.3	n/a	MB/s
	8GB	85.2	n/a	
	16GB	90.5	n/a	
Sequential Write operation DDR	4GB	n/a	n/a	
	8GB	n/a	n/a	
	16GB	n/a	n/a	
Sequential Read operation SDR	4GB	n/a	49.4	MB/s
	8GB	n/a	49.4	
	16GB	n/a	49.4	
Sequential Write operation SDR	4GB	n/a	14.3	
	8GB	n/a	14.0	
	16GB	n/a	13.9	
Random Read 4kB operation DDR	4GB	n/a	n/a	IOPS
	8GB	n/a	n/a	
	16GB	n/a	n/a	
Random Write 4kB operation DDR	4GB	n/a	n/a	
	8GB	n/a	n/a	
	16GB	n/a	n/a	
Random Read 4kB operation SDR	4GB	n/a	2946	IOPS
	8GB	n/a	3056	
	16GB	n/a	3096	
Random Write 4kB operation SDR	4GB	n/a	1105	
	8GB	n/a	1097	
	16GB	n/a	1091	

Table 4: Device Power Consumption

Capacity[3] [4] [5]	Typ. Read Current		Typ. Write Current		Typ. Standby Current[6]		Autoread	Unit
	VCCQ 1.8V	VCC 3.3V	VCCQ 1.8V	VCC 3.3V	VCCQ 1.8V	VCC 3.3V		
4GB	57	14	37	19	2.5/46/0.6	0.02(14)	20 seconds	mA
8GB	57	14	37	19	2.5/46/0.6	0.04(14)	40 seconds	mA
16GB	57	14	37	19	2.5/46/0.6	0.06(14)	60 seconds	mA

[1] Instant-up function, DDR read mode only, device cache read on, Testmetrix measurement

[2] Typical sustained performance of dirty drives, MLC, 52MHz SDR mode, UP² board Windows 10, low level sequential write/read or Crystal Disk Mark 6.0.0 (random 4k)

[3] Values given for an 8-bit bus width, a clock frequency of 52MHz SDR mode, VCC= 3.3V±5%, VCCQ=1.8V±5%

[4] Standby current is measured at VCC=3.3V±5%,8-bit bus width without clock frequency

[5] Target values

[6] After each power on the eMMC waits ~5minutes with standby current of 2.5mA and then perform the full memory scan for bit errors (VCCQ=46mA, VCC=28mA). After this scan the current is 0.6mA. The autoread settings can be modified on request.

3.2 Environmental Specifications

3.2.1 Recommended Operating Conditions

Table 5: e·MMC Recommended Operating Conditions

Parameter	min	typ	max	unit
Operating Temperature	-40	25	105[7]	°C

3.2.2 Recommended Storage Conditions

Table 6: e·MMC Recommended Storage Conditions

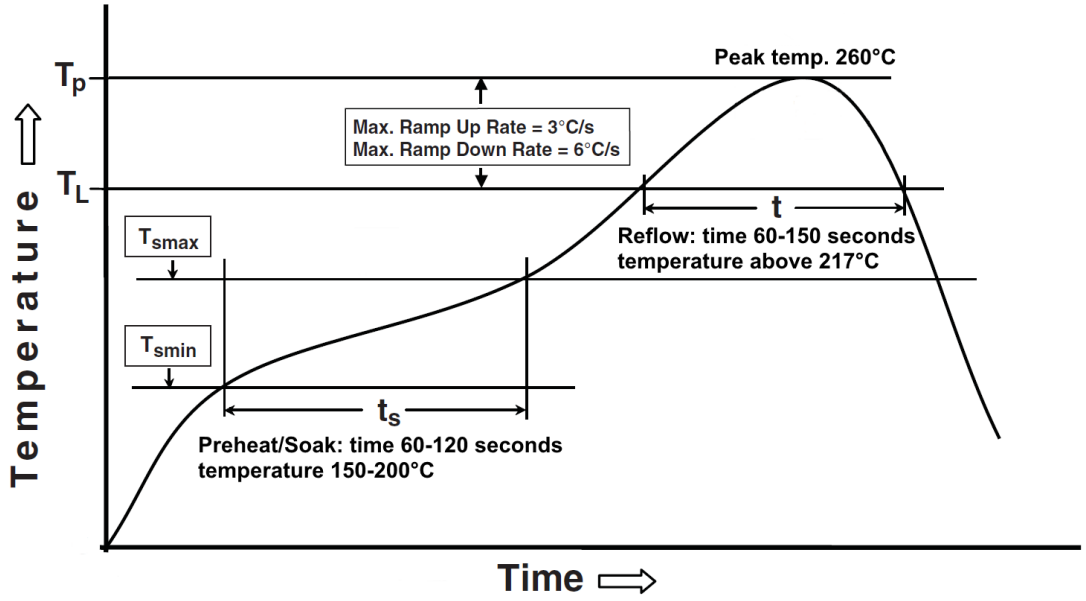
Parameter	min	typ	max	unit
Storage Temperature	-40	25	105[7]	°C

3.2.3 Reflow Profile and MSL

Table 7: Reflow and MSL conditions

Parameter	Condition
MSL	Level 3 (storage condition 168 hours, ≦30°C/ 60% RH)
Reflow	According to IPC/JEDEC J-STD-020D.1: Peak temp 260°C, 217°C endurance 60~150 seconds, up to 3 times reflow

Figure 1: Reflow profile



3.2.4 EMC

Table 8: EMC

Parameter	Condition	
EMC / EMI	**Human Body Model:** up to 2kV, Class 2 or better according to AEC-Q100-002	**Charged Device Model:** up to 750V corner balls, 500V other balls according to AEC-Q100-011

[7] High temperature storage reduces the data retention time

3.3 Physical Dimensions

Table 9: Physical Dimensions

Physical Dimensions	Value	Unit
Length	13±0.1	mm
Width	11.5±0.1	
Thickness	1.1 max.	
Weight (typ.)	< 1	g

3.4 Reliability

Table 10: Reliability

Parameter	Value
Data Retention at beginning @ 40°C	10 years
Data Retention at life end (3k PE cycles) @ 40°C	1 year

4. Capacity specification

Table 11: e·MMC capacity specification

Capacity	Sectors	Total addressable User Data Area (Byte)
4GB	7,634,944	3,909,091,328
8GB	15,269,888	7,818,182,656
16GB	30,539,776	15,636,365,312

Table 12: Partition capacity specification

Capacity	Boot partition 1	Boot partition 2	RPMB
4GB	16,384kB	16,384kB	4,096kB
8GB to 16GB	32,640kB	32,640kB	4,096kB

5. Card Mechanical

5.1 Physical description

The e·MMC contains a single chip controller and Flash memory module(s). The controller interfaces with a host system allowing data to be written to and read from the Flash memory module(s). Figure 2and Figure 3 show card dimensions.

Figure 2: Mechanical Dimensions e·MMC

Package Mechanical (11.5 x 13.0 x 1.1mm)

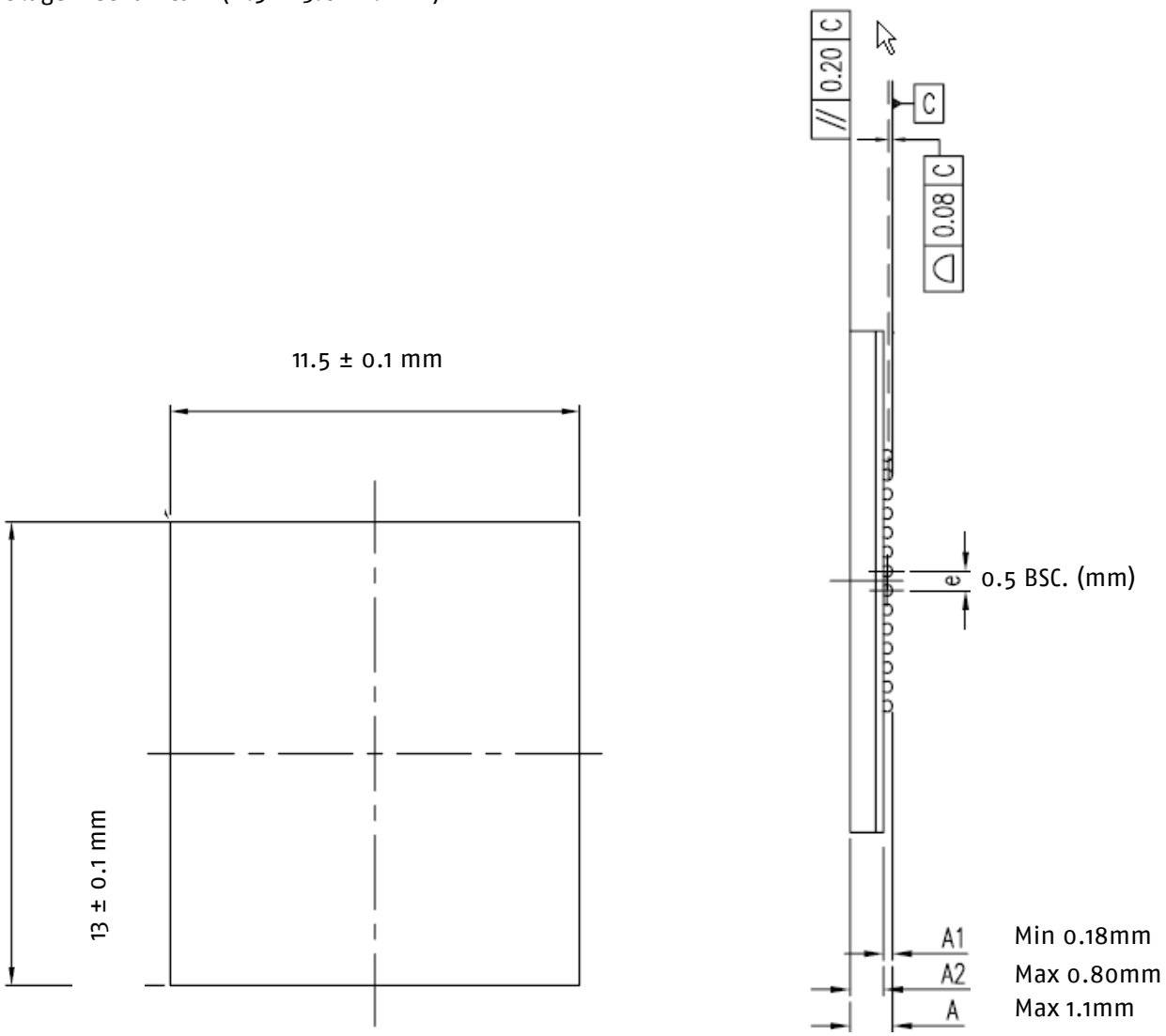
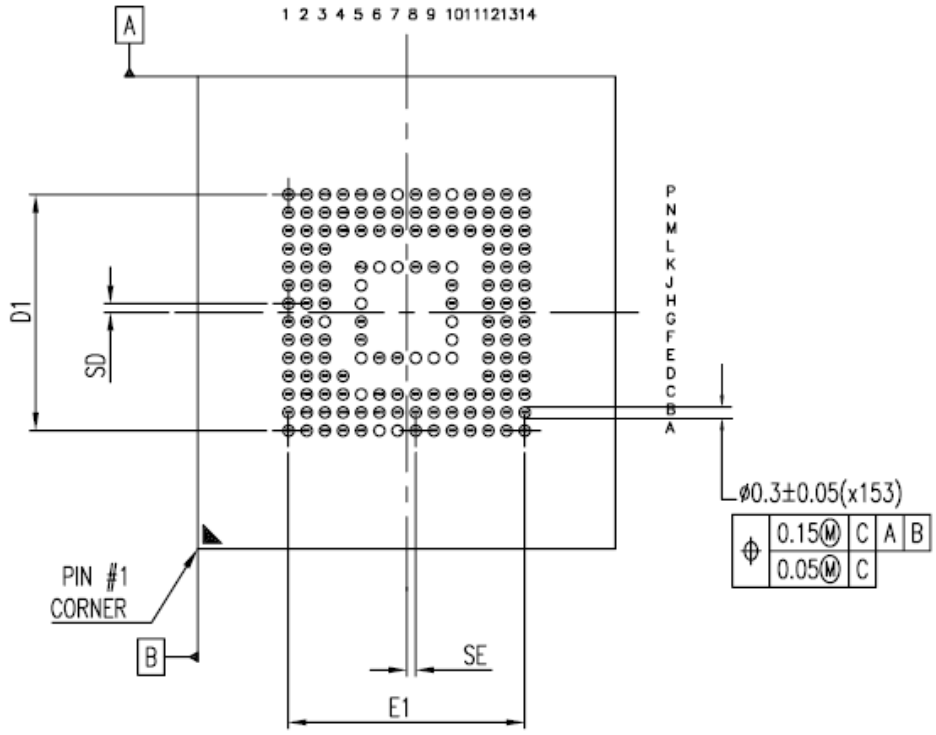


Figure 3: Mechanical Dimensions e·MMC (continued)



BOTTOM VIEW

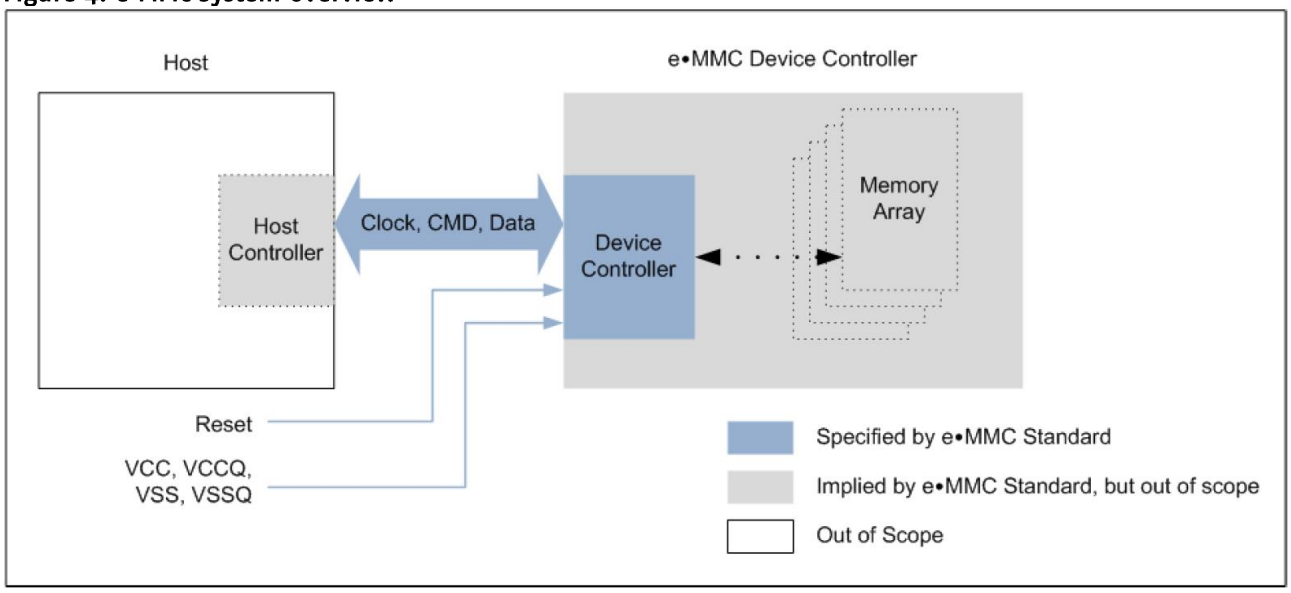
N	SE (MM)	SD (MM)	E1(MM)	D1(MM)	JEDEC(REF)
153	0.25 BSC.	0.25 BSC.	6.50 BSC.	6.50 BSC.	MO-276 BA

6. e·MMC Device and System

6.1 e·MMC System Overview

The e·MMC specification covers the behavior of the interface and the Device controller. As part of this specification the existence of a host controller and a memory storage array are implied but the operation of these pieces is not fully specified.

Figure 4: e·MMC System Overview



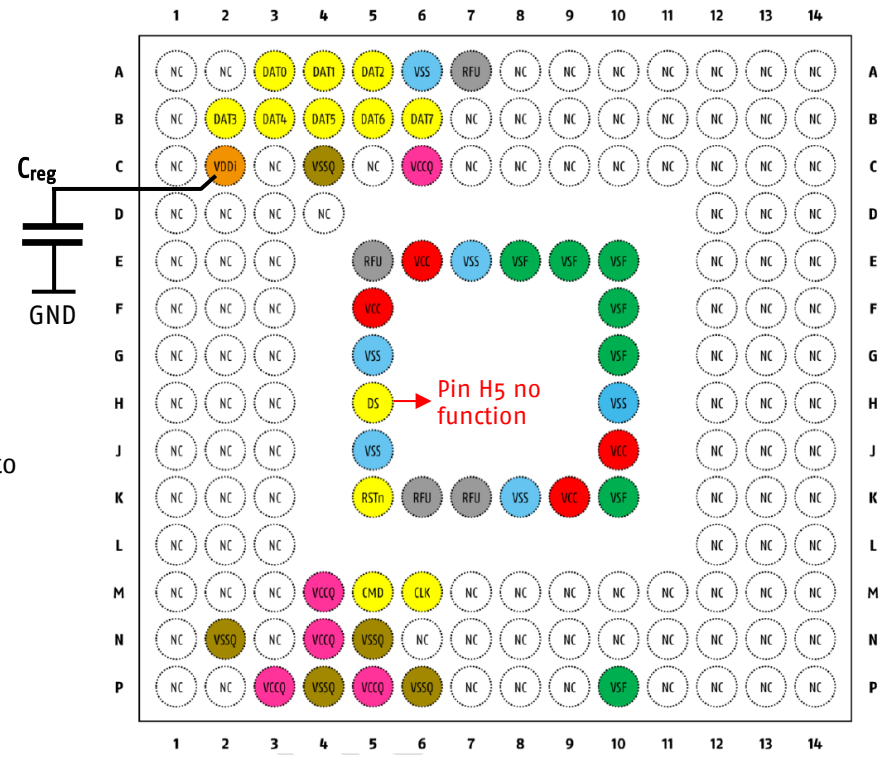
6.2 Pinout

Figure 5: Ball assignment (top view, ball down)

Minimum capacity requirement for C_{reg} (at V_{DDi} pin):

C_{reg} min = 2.2µF

Recommendations:
- Type: 6.3V, X5R
- Placement close to e·MMC BGA



RFU pins: Reserved for Future Use, must be left floating on host (do not connect)
VSF pins: Vendor Specific Function, must generally be left floating on host (do not connect), further functionality options below

Table 13: Pinout

Name	Type[8]	Ball No.	Description
CLK	I	M6	Clock: Each cycle directs a 1-bit transfer on the command and DAT lines.
CMD	I/O/PP/OD	M5	Command: A bidirectional channel used for device initialization and command transfer. Command has two operating modes: 1) Open-drain for initialization. 2) Push-pull for fast command transfer.
DAT0	I/O/PP	A3	Data I/O0: Bidirectional channel used for data transfer.
DAT1	I/O/PP	A4	Data I/O1: Bidirectional channel used for data transfer.
DAT2	I/O/PP	A5	Data I/O2: Bidirectional channel used for data transfer.
DAT3	I/O/PP	B2	Data I/O3: Bidirectional channel used for data transfer.
DAT4	I/O/PP	B3	Data I/O4: Bidirectional channel used for data transfer.
DAT5	I/O/PP	B4	Data I/O5: Bidirectional channel used for data transfer.
DAT6	I/O/PP	B5	Data I/O6: Bidirectional channel used for data transfer.
DAT7	I/O/PP	B6	Data I/O7: Bidirectional channel used for data transfer.
RST_n	I	K5	Reset signal pin
VCC	S	E6, F5, J10, K9	VCC: Flash memory I/F and Flash memory power supply.
VCCQ	S	C6, M4, N4, P3, P5	VCCQ : Memory controller core and MMC interface I/O power supply.
VSS	S	A6, E7, G5, H10, J5, K8	VSS: Flash memory I/F and Flash memory ground connection.
VSSQ	S	C4, N2, N5, P4, P6	VSSQ: Memory controller core and MMC I/F ground connection.
VDDi		C2	VDDi : Connect capacitor Creg from VDDi to GND.
DS	O/PP	H5	Data Strobe: no function, only for HS400 mode (not supported)
NC			Not connected
Vendor specific pins			
ISO_CLK	O/PP	E8	CLK for optional Security Chip interface
ISO_RSTN	O/PP	E9	Reset for optional Security Chip interface
ISO_DATA	O/PP	E10	Data for optional Security Chip interface
UART_TX	O/U	F10	Debugging UART Transmit Data Input.
UART_RX	I/U	G10	Debugging UART Receive Data Input.
UART_CLK	I/U	K10	Debugging UART Clock Input.
ROM_Boot	I/O/U	P10	ROM-Boot

[8] I: input; O: output; PP: push-pull; OD: open-drain; NC: Not connected; S: power supply, U Pull up.

6.3 e·MMC Communication Interface

The e·MMC device transfers data via a configurable number of data bus signals. The communication signals are:

- Clock (CLK)
  Each cycle of this signal directs a one bit transfer on the command and either a one bit (1x) or a two bits transfer (2x) on all the data lines. The frequency may vary between zero and the maximum clock frequency.

- Command (CMD)
  This signal is a bidirectional command channel used for Device initialization and transfer of commands. The CMD signal has two operation modes: open-drain for initialization mode, and push-pull for fast command transfer. Commands are sent from the e·MMC host controller to the e·MMC Device and responses are sent from the Device to the host.

- Input/Outputs (DAT0-DAT7)
  These are bidirectional data channels. The DAT signals operate in push-pull mode. Only the Device or the host is driving these signals at a time. By default, after power up or reset, only DAT0 is used for data transfer. A wider data bus can be configured for data transfer, using either DAT0-DAT3 or DAT0-DAT7, by the e·MMC host controller. The e·MMC Device includes internal pull-ups for data lines DAT1-DAT7. Immediately after entering the 4-bit mode, the Device disconnects the internal pull ups of lines DAT1, DAT2, and DAT3. Correspondingly, immediately after entering to the 8-bit mode the Device disconnects the internal pull-ups of lines DAT1–DAT7.

6.4 Bus Protocol

After a power-on reset, the host must initialize the device by a special message-based MultiMediaCard bus protocol. For more details, refer to section 6.4.2 of the JEDEC Standard JESD84-A441.

6.5 Bus Speed Modes

e·MMC defines several bus speed modes as shown in Table 14.

Table 14: Bus Speed Mode

Mode Name	Data Rate	IO Voltage	Bus Width	Frequency	Max Data Transfer (implies x8 bus width)
Backwards Compatibility with legacy MMC card	Single	3.3/1.8V	1, 4, 8	0-26MHz	26MB/s
High Speed SDR	Single	3.3/1.8V	4, 8	0-52MHz	52MB/s
High Speed DDR[9]	Dual	3.3/1.8V	4, 8	0-52MHz	104MB/s

[9] For EM-10 the DDR mode is only applicable in Instant-up

7. e·MMC Functional Description

7.1 e·MMC Overview

All communication between host and device are controlled by the host (master). The host sends a command, which results in a device response. For more details, refer to section 7 of the JEDEC Standard JESD84-A441.
Five operation modes are defined for the e·MMC system:

- Boot operation mode
- Card identification mode
- Interrupt mode
- Data transfer mode
- Inactive mode

7.2 Boot Operation Mode

In boot operation mode, the master (e·MMC host) can read boot data from the slave (e·MMC device) by keeping CMD line low or sending CMD0 with argument + 0xFFFFFFFA, before issuing CMD1. The data can be read from either boot area or user area depending on register setting. For more details, refer to section 7.3 of the JEDEC Standard JESD84-A441.

7.3 Card Identification Mode

While in device identification mode the host resets the device, validates operation voltage range and access mode, identifies the device and assigns a Relative device Address (RCA) to the device on the bus. All data communication in the Device Identification Mode uses the command line (CMD) only. For more details, refer to section 7.4 of the JEDEC Standard JESD84-A441.

7.4 Interrupt Mode

The interrupt mode on the e·MMC system enables the master (e·MMC host) to grant the transmission allowance to the slaves (Device) simultaneously. This mode reduces the polling load for the host and hence, the power consumption of the system, while maintaining adequate responsiveness of the host to a Device request for service. Supporting e·MMC interrupt mode is an option, both for the host and the Device. For more details, refer to section 7.5 of the JEDEC Standard JESD84-A441.

7.5 Data Transfer Mode

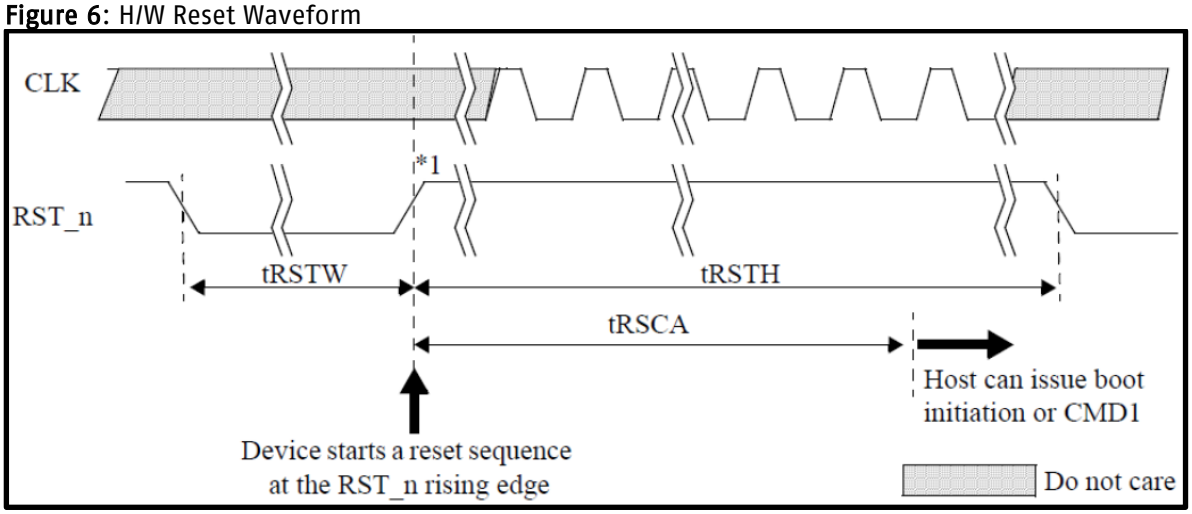
When the Device is in *Stand-by* State, communication over the CMD and DAT lines will be performed in push-pull mode. For more details, refer to section 7.6 of the JEDEC Standard JESD84-A441.

7.6 Inactive Mode

The device will enter inactive mode if either the device operating voltage range or access mode is not valid. The device can also enter inactive mode with GO_INACTIVE_STATE command (CMD15). The device will reset to *Pre-idle* state with power cycle. For more details, refer to section 7.1 of the JEDEC Standard JESD84-A441.

7.7 H/W Reset Operation

Figure 6: H/W Reset Waveform



Device will detect the rising edge of RST_n signal to trigger internal reset sequence

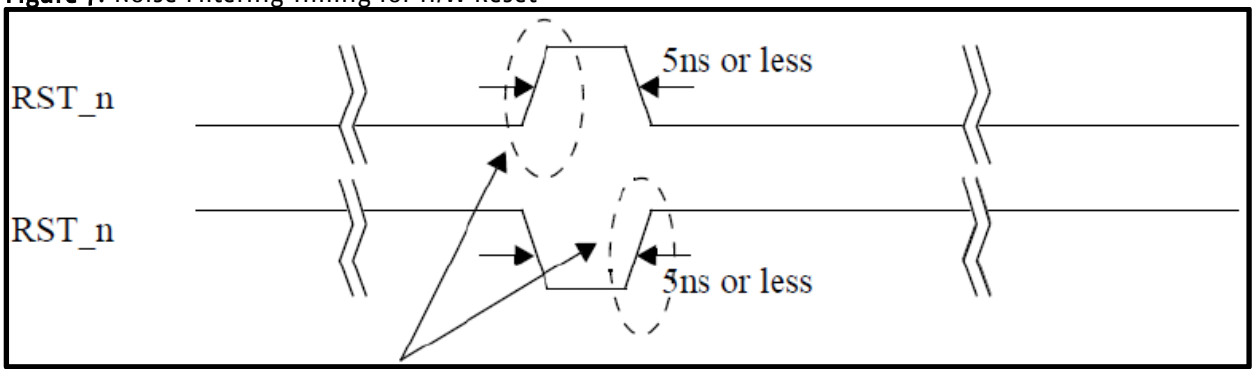
Table 15: H/W Reset Timing Parameters

Symbol	Comment	Min	Max	Unit
tRSTW	RST_n pulse width	1		[us]
tRSCA	RST_n to Command time	200[10]		[us]
tRSTH	RST_n high period (interval time)	1		[us]

7.8 Noise Filtering Timing for H/W Reset

Device must filter out 5ns or less pulse width for noise immunity

Figure 7: Noise Filtering Timing for H/W Reset



Device must not detect these rising edge.
Device must not detect 5ns or less of positive or negative RST_n pulse. Device must detect more than or equal to 1us of positive or negative RST_n pulse width.

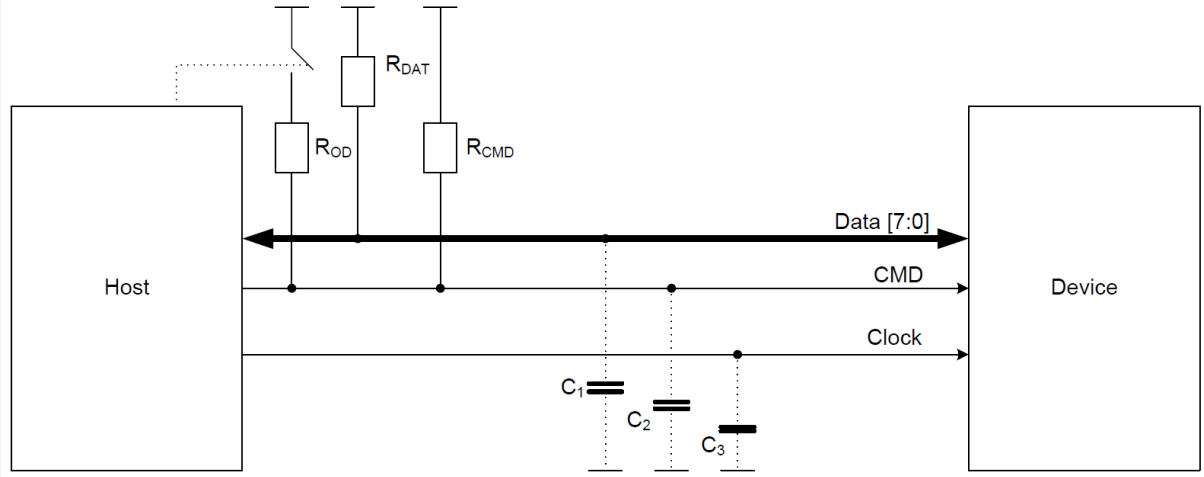
[10] 74 cycles of clock signal required before issuing CMD1 or CMD0 with argument 0xFFFFFFFA

8. The e·MMC bus

The e·MMC bus has ten communication lines and three supply lines:

- CMD: Command is a bidirectional signal. The host and Device drivers are operating in two modes, open drain and push/pull.
- DAT0-7: Data lines are bidirectional signals. Host and Device drivers are operating in push-pull mode.
- CLK: Clock is a host to Device signal. CLK operates in push-pull mode.

Figure 8: Bus Circuitry Diagram



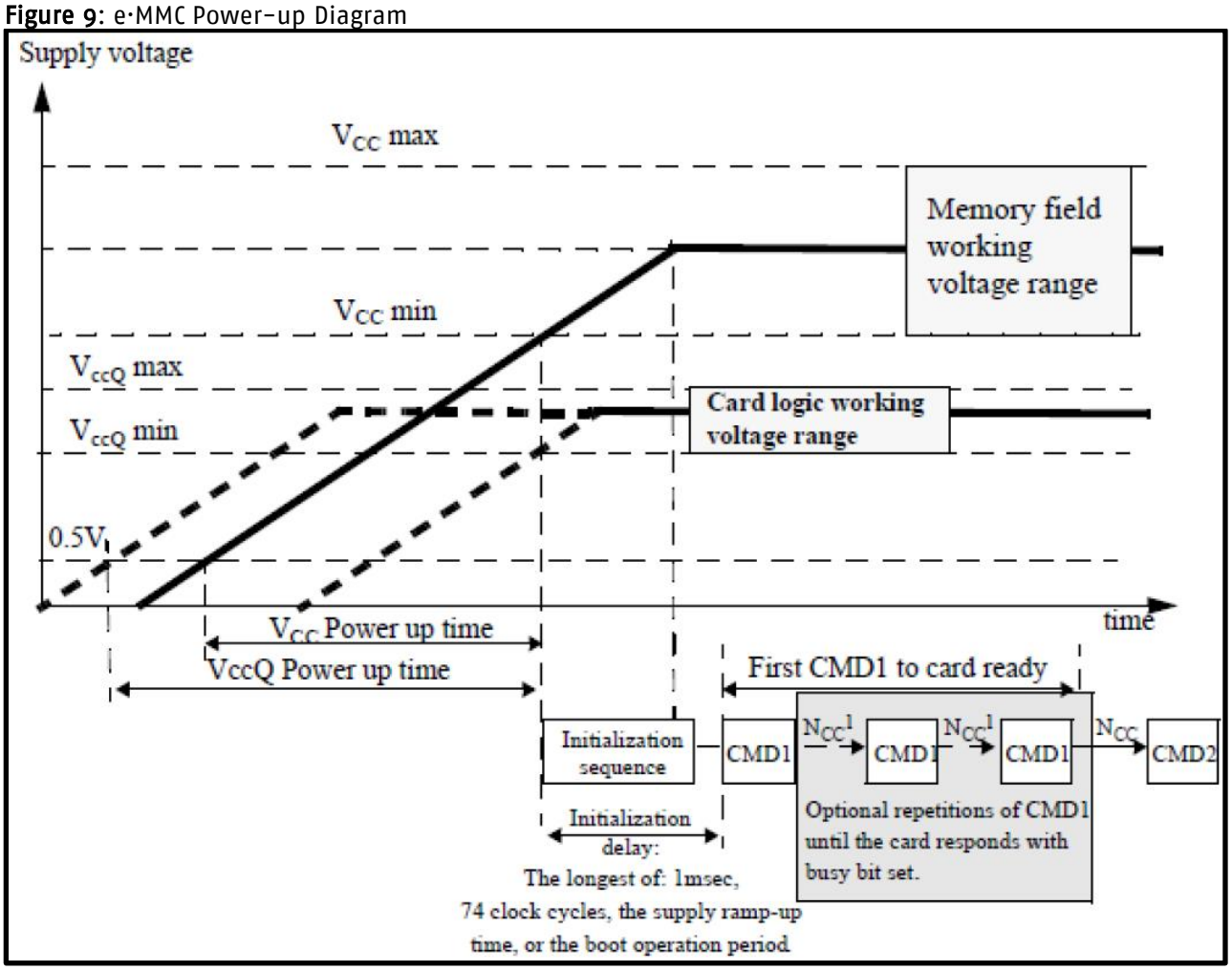
The R_{OD} is switched on and off by the host synchronously to the open-drain and push-pull mode transitions. The host does not have to have open drain drivers, but must recognize this mode to switch on the R_{OD}. R_{DAT} and R_{CMD} are pull-up resistors protecting the CMD and the DAT lines against bus floating device when all device drivers are in a high-impedance mode.
A constant current source can replace the R_{OD} by achieving a better performance (constant slopes for the signal rising and falling edges). If the host does not allow the switchable R_{OD} implementation, a fixed R_{CMD} can be used. Consequently the maximum operating frequency in the open drain mode has to be reduced if the used R_{CMD} value is higher than the minimal one given in Table 19.

8.1 Power-up

8.1.1 e·MMC power-up

An e·MMC bus power-up is handled locally in each device and in the bus master. Figure 9 shows the power-up sequence and is followed by specific instructions regarding the power-up sequence. Refer to section 12.3.1 of the JEDEC Standard JESD84-A441.

Figure 9: e·MMC Power-up Diagram

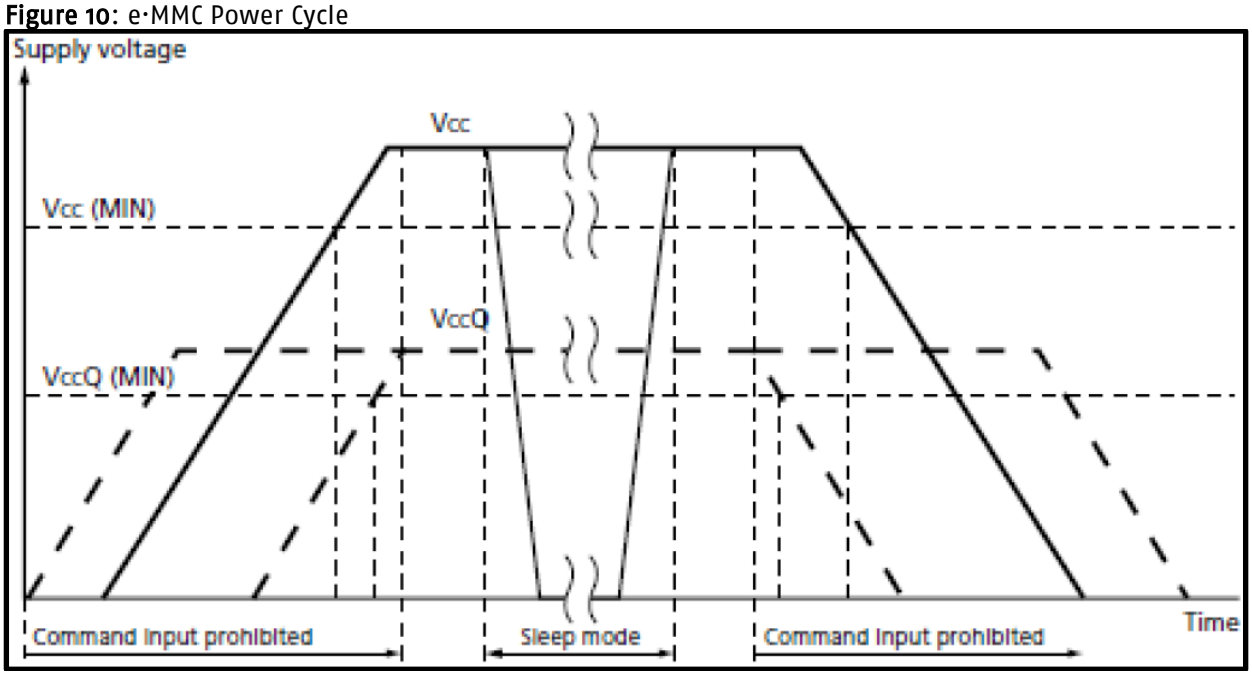


Both voltages VCC and VCCQ should be applied within 80ms.

8.1.2 e·MMC Power Cycling

The master can execute any sequence of V_{CC} and V_{CCQ} power-up/power-down. However, the master must not issue any commands until V_{CC} and V_{CCQ} are stable within each operating voltage range. After the slave enters sleep mode, the master can power-down V_{CC} to reduce power consumption. It is necessary for the slave to be ramped up to V_{CC} before the host issues CMD5 (SLEEP_AWAKE) to wake the slave unit. For more information about power cycling refer to Section 12.3.3 of the JEDEC Standard JESD84-A441.

Figure 10: e·MMC Power Cycle



At power on both voltages VCC and VCCQ should be applied within 80ms.

8.2 Bus Operating Conditions

Table 16: General Operating Conditions

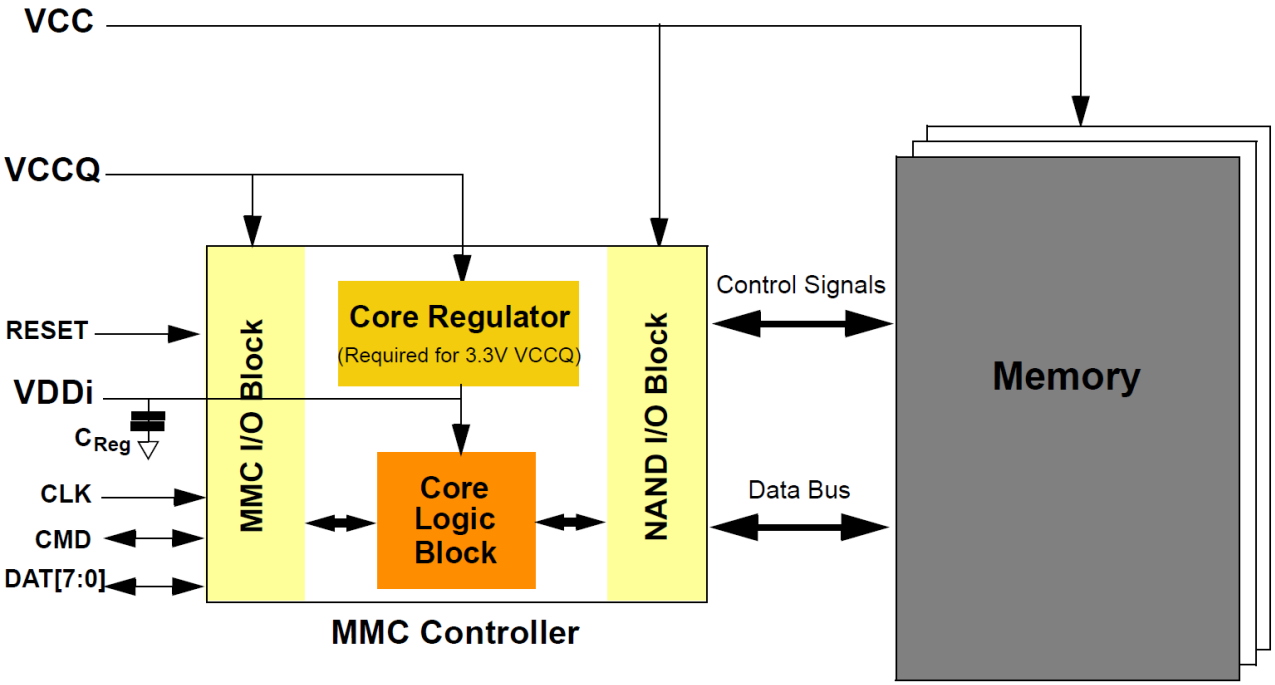
Parameter	Symbol	Min	Max.	Unit	Remark
Peak voltage on all lines		-0.5	VCCQ + 0.5	V	
All Inputs					
Input Leakage Current (before initialization sequence and/or the internal pull up resistors connected)		-100	100	µA	
Input Leakage Current (after initialization sequence and the internal pull up resistors disconnected)		-2	2	µA	
All Outputs					
Output Leakage Current (before initialization sequence)		-100	100	µA	
Output Leakage Current (after initialization sequence)		-2	2	µA	

8.2.1 Power supply e·MMC

In the e·MMC, V_{CC} is used for the NAND flash device and its interface voltage; V_{CCQ} is for the controller and the MMC interface voltage as shown in Figure 11. The core regulator is optional and only required when internal core logic voltage is regulated from V_{CCQ}.
A C_{Reg} capacitor must be connected to the V_{DDi} terminal to stabilize regulator output on the system.

It is recommended to use a C_{Reg}=2.2µF capacitor X5R or better.

Figure 11: e·MMC Internal Power Diagram



8.2.2 e·MMC Power Supply Voltages

The e·MMC supports one or more combinations of VCC and VCCQ as shown in Table 17. The VCCQ must be defined at equal to or less than VCC.

Table 17: e·MMC Operating Voltage

Parameter	Symbol	MIN	MAX	Unit	Remarks
Supply voltage (NAND)	V_{CC}	2.7	3.6	V	
Supply voltage (I/O)	VCCQ	2.7	3.6	V	
		1.7	1.95	V	
Supply power-up for 3.3V	t_{PRUH}		35	ms	
Supply power-up for 1.8V	t_{PRUL}		25	ms	

The e·MMC must support at least one of the valid voltage configurations, and can optionally support all valid voltage configurations (see Table 18).

Table 18: e·MMC Voltage Combinations

		VCCQ	
		1.7V–1.95V	**2.7V–3.6V**
VCC	**2.7V–3.6V**	Valid	Valid

8.2.3 Bus Signal Line Load

The total capacitance C_L of each line of the e·MMC bus is the sum of the bus master capacitance C_{HOST}, the bus capacitance C_{BUS} itself and the capacitance C_{DEVICE} of e·MMC connected to this line:

$C_L = C_{HOST} + C_{BUS} + C_{DEVICE}$

The sum of the host and bus capacitances must be under 20pF.

Table 19: Signal Line Load

Parameter	Symbol	Min	Max	Unit	Remark
Pull-up resistance for CMD	R_{CMD}	4.7	100[11]	Kohm	to prevent bus floating
Pull-up resistance for DAT0–7	R_{DAT}	10	100[11]	Kohm	to prevent bus floating
Pull-up resistance for RST_n	R_{RST_n}	4.7	50	Kohm	It is not necessary to put pull-up resistance on RST_n (H/W rest) line if host does not use H/W reset. (Extended CSD register [162] = 0 b)
Bus signal line capacitance	CL		30	pF	Single Device
Single Device capacitance	C_{BGA}		6	pF	
Maximum signal line inductance			16	nH	
Impedance on CLK / CMD / DAT0~7		45	55	ohm	Impedance match
V_{CCQ} decoupling capacitor	$C_{...}$	1		µF	It should be located as close as possible to the balls defined in order to minimize connection parasitic
VCC capacitor value	$C_{...}$	2.2+0.1		µF	It should be located as close as possible to the balls defined in order to minimize connection parasitic
V_{DDi} capacitor value	$C_{...}$	1[12]		µF	To stabilize regulator output to controller core logics. It should be located as close as possible to the balls defined in order to minimize connection parasitic

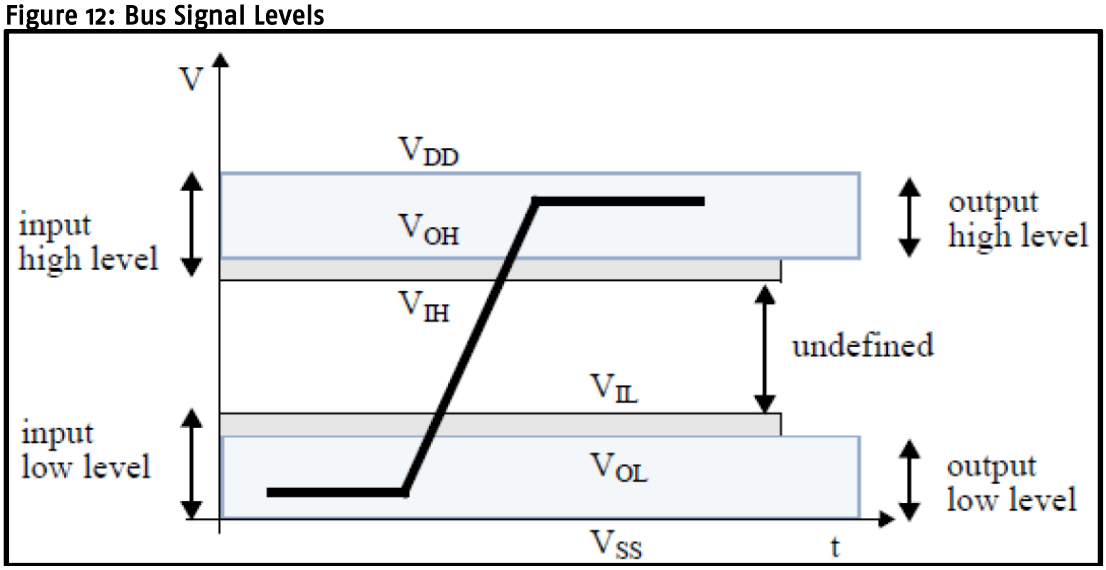
[11] Recommended max 50k0hm for 1.8V interface

[12] Recommended C_{REG} minimum 2.2uF

8.3 Bus Signal Levels

As the bus can be supplied with a variable supply voltage, all signal levels are related to the supply voltage.

Figure 12: Bus Signal Levels



8.3.1 Open-drain Mode Bus Signal Level

Table 20: Open-drain Bus Signal Level

Parameter[13]	Symbol	Min	Max.	Unit	Conditions
Output HIGH voltage	VOH	VDD – 0.2		V	IOH = -100 µA
Output LOW voltage	VOL		0.3	V	IOL = 2 mA

8.3.2 Push-pull mode bus signal level– e·MMC

The device input and output voltages shall be within the following specified ranges for any V_{DD} of the allowed voltage range

For 2.7V-3.6V V_{CCQ} range (compatible with JESD8C.01):

Table 21: Push-pull Signal Level—High-voltage e·MMC

Parameter	Symbol	Min	Max.	Unit	Conditions
Output HIGH voltage	VOH	0.75 * V_{DD}		V	IOH = -100 µA @ V_{DD} min
Output LOW voltage	VOL		0.125 * V_{DD}	V	IOL = 100 µA @ V_{DD} min
Input HIGH voltage	VIH	0.625 * V_{DD}	V_{DD} + 0.3	V	
Input LOW voltage	VIL	VSS – 0.3	0.25 * V_{DD}	V	

For 1.65V – 1.95V V_{CCQ} range (Compatible with EIA/JEDEC Standard "EIA/JESD8-7 Normal Range" as defined in the following table):

Table 22: Push-pull Signal Level—1.65 -1.95 V_{CCQ} Voltage Range

Parameter	Symbol	Min	Max.	Unit	Conditions
Output HIGH voltage	VOH	V_{CCQ} – 0.45V		V	IOH = -2mA
Output LOW voltage	VOL		0.45V	V	IOL = 2mA
Input HIGH voltage	VIH	0.65 * V_{CCQ}[14]	V_{CCQ} + 0.3	V	
Input LOW voltage	VIL	V_{SS} – 0.3	0.32 * V_{DD}[15]	V	

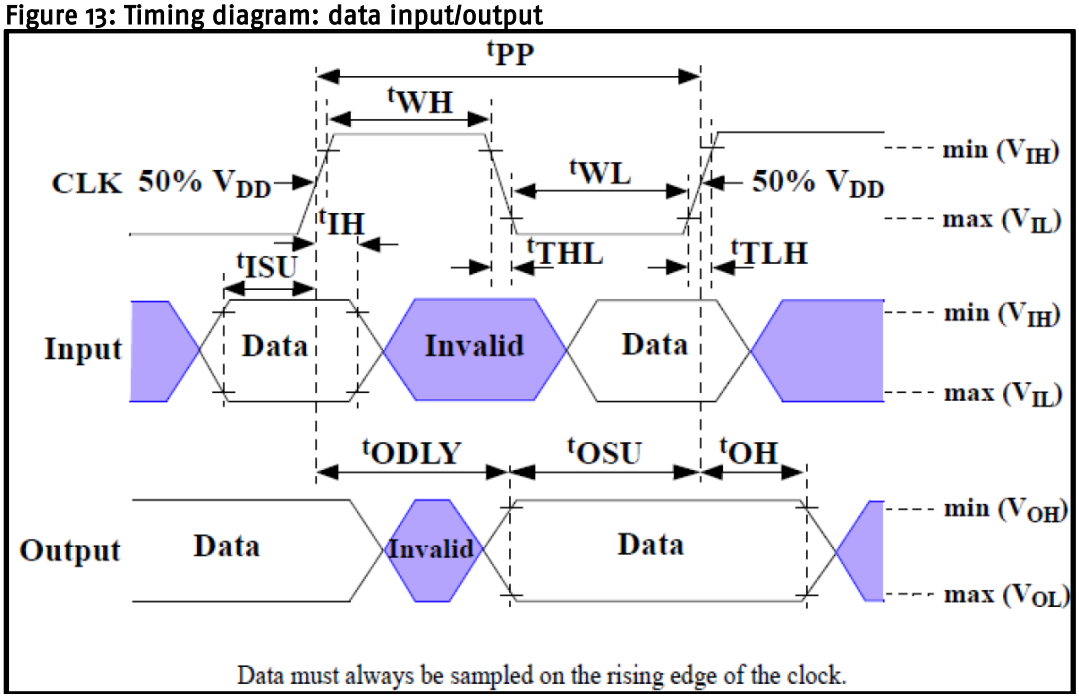
[13] The input levels are identical with the push-pull mode bus signal levels.

[14] 0.7 * VDD for MMC™4.3 and older revisions.

[15] 0.3 * VDD for MMC™4.3 and older revisions.

8.4 Bus Timing

Figure 13: Timing diagram: data input/output



8.4.1 Device Interface Timings

Table 23: High-speed Device Interface Timing

Parameter	Symbol	Min	Max.	Unit	Remark
Clock CLK[16]					
Clock frequency Data Transfer Mode (PP)[17]	fPP	0	52[18]	MHz	CL ≤ 30 pF Tolerance:+100KHz
Clock frequency Identification Mode (OD)	fOD	0	400	kHz	Tolerance: +20KHz
Clock high time	tWH	6.5		ns	CL ≤ 30 pF
Clock low time	tWL	6.5		ns	CL ≤ 30 pF
Clock rise time[19]	tTLH		3	ns	CL ≤ 30 pF
Clock fall time	tTHL		3	ns	CL ≤ 30 pF
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	tISU	3		ns	CL ≤ 30 pF
Input hold time	tIH	3		ns	CL ≤ 30 pF
Outputs CMD, DAT (referenced to CLK)					
Output delay time during data transfer	tODLY		13.7	ns	CL ≤ 30 pF
Output hold time	tOH	2.5		ns	CL ≤ 30 pF
Signal rise time[20]	tRISE		3	ns	CL ≤ 30 pF
Signal fall time	tFALL		3	ns	CL ≤ 30 pF

[16] CLK timing is measured at 50% of VDD

[17] e·MMC shall support the full frequency range from 0-26MHz or 0-52MHz

[18] Device can opperate as high-speed device interface timing at MHz clock frequency.

[19] CLK rise and fall times are measured by min (VIH) and max (VIL).

[20] Inputs CMD DAT riese and fall times are measured by min (VIH) and max (VIL) and outputs CMD DAT rise and fall times are measured by min (VOH) and max (VOL).

Backward-compatible Device Interface Timing

Parameter	Symbol	Min	Max.	Unit	Remark[21]
Clock CLK[22]					
Clock frequency Data Transfer Mode (PP)[23]	fPP	0	26	MHz	CL ≤ 30 pF
Clock frequency Identification Mode (OD)	fOD	0	400	kHz	
Clock high time	tWH	10			CL ≤ 30 pF
Clock low time	tWL	10		ns	CL ≤ 30 pF
Clock rise time[24]	tTLH		10	ns	CL ≤ 30 pF
Clock fall time	tTHL		10	ns	CL ≤ 30 pF
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	tISU	3		ns	CL ≤ 30 pF
Input hold time	tIH	3		ns	CL ≤ 30 pF
Outputs CMD, DAT (referenced to CLK)					
Output set-up time[25]	tOSU	11.7		ns	CL ≤ 30 pF
Output hold time[25]	tOH	8.3		ns	CL ≤ 30 pF

[21] The Device must always start with the backward-compatible interface timing. The timing mode can be switched to high-speed interface timing by the host sending the SWITCH command (CMD6) with the argument for high-speed interface select.

[22] CLK timing is meausred at 50% of VDD.

[23] For compatibility with devices that support the v4.2 standard or earlier, host should not use > 26 MHz before switching to high speed interface timing.

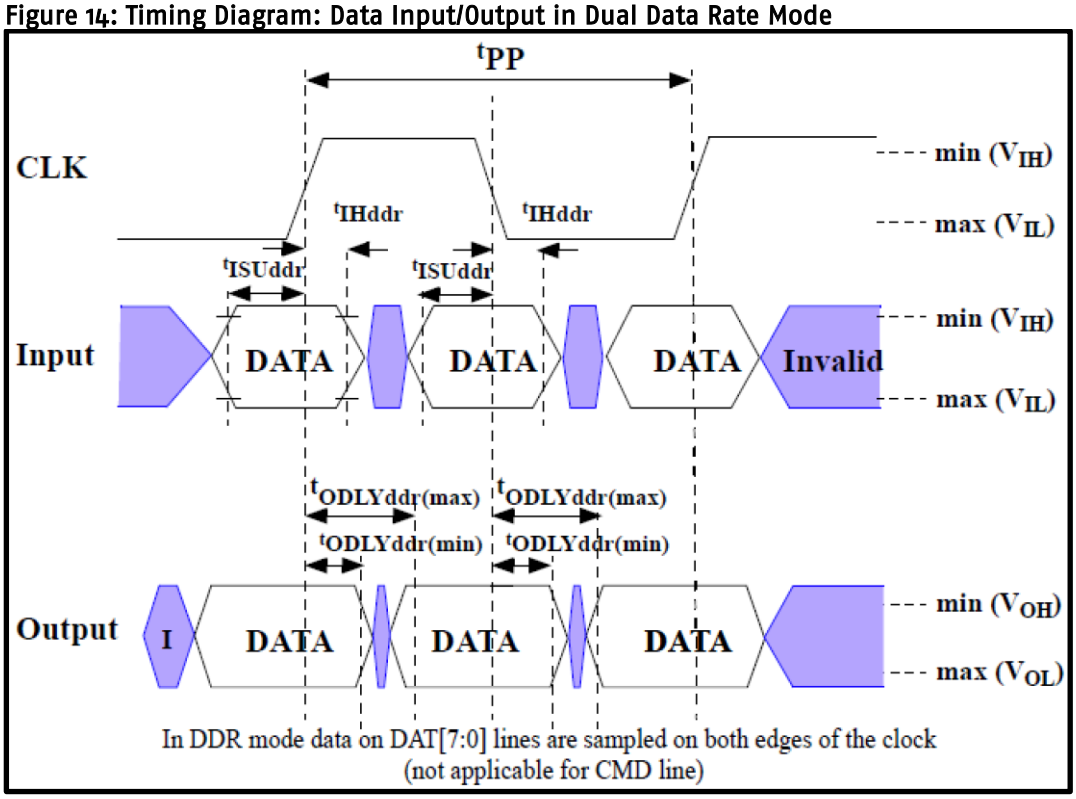
[24] CLK rise and fall times are measured by min (VIH) and max (VIL).

[25] tOSU and tOH are defined as values from clock rising edge. However, there may be Devices or devices which utilize clock falling edge to output data in backward compatibility mode. Therefore, it is recommended for hosts either to settWL value as long as possible within the range which will not go over tCK-tOH(min) in the system or to use slow clock frequency, so that host could have data set up margin for those devices. In this case, each device which utilizes clock falling edge might show the correlation either between tWL and tOSU or between tCK and tOSU for the device in its own datasheet as a note or its application notes.

8.5 Bus Timing for DAT Signals During Dual Data Rate Operation

These timings apply to the DAT[7:0] signals only when the device is configured for dual data mode operation. In this dual data mode, the DAT signals operate synchronously of both the rising and the falling edges of CLK. The CMD signal still operates synchronously of the rising edge of CLK and therefore complies with the bus timing specified in section 12.7 of JESD84-A441, therefore there is no timing change for the CMD signal.

Figure 14: Timing Diagram: Data Input/Output in Dual Data Rate Mode



8.5.1 Dual Data Rate Interface Timings

Table 24: High-speed Dual Data Rate Interface Timing

Parameter	Symbol	Min	Max.	Unit	Remark
Input CLK[26]					
Clock duty cycle		45	55	%	Includes jitter, phase noise
Input DAT (referenced to CLK-DDR mode)					
Input set-up time	tISUddr	2.5		ns	CL ≤ 20 pF
Input hold time	tIHddr	2.5		ns	CL ≤ 20 pF
Output DAT (referenced to CLK-DDR mode)					
Output delay time during data transfer	tODLYddr	1.5	7	ns	CL ≤ 20 pF
Signal rise time (all signals)[27]	tRISE		2	ns	CL ≤ 20 pF
Signal fall time (all signals)	tFALL		2	ns	CL ≤ 20 pF

[26] CLK timing is measured at 50% of VDD.

[27] Inputs CMD, DAT rise and fall times are measured by min (VIH) and max (VIL), and outputs CMD, DAT rise and fall times are measured by min (VOH) and max (VOL).

9. e·MMC Registers

Within the Device interface six registers are defined: OCR, CID, CSD, EXT_CSD, RCA and DSR. These can be accessed only by corresponding commands (see Section 7.10 of JESD84-A441).

Table 25: e·MMC Registers

Name	Width (Bytes)	Description	Implementation
CID	16	Device Identification number, an individual number for identification.	Mandatory
RCA	2	Relative Device Address is the Device system address, dynamically assigned by the host during initialization.	Mandatory
DSR	2	Driver Stage Register, to configure the Device's output drivers.	Optional, not implemented
CSD	16	Device Specific Data, information about the Device operation conditions.	Mandatory
OCR	4	Operation Conditions Register. Used by a special broadcast command to identify the voltage type of the Device.	Mandatory
EXT_CSD	512	Extended Device Specific Data. Contains information about the Device capabilities and selected modes. Introduced in standard v4.0	Mandatory

The host may reset the device by:

- Switching the power supply off and back on. The device shall have its own power-on detection circuitry which puts the device into a defined state after the power-on Device.
- A reset signal
- By sending a special command

9.1 OCR Register

The 32-bit operation conditions register (OCR) stores the VDD voltage profile of the Device and the access mode indication. In addition, this register includes a status information bit. This status bit is set if the Device power up procedure has been finished. The OCR register shall be implemented by all Devices.

Table 26: OCR register

OCR bit	VCCQ voltage window	typ. value
[6:0]	Reserved	000 0000b
[7]	1.70 – 1.95V	1b
[14:8]	2.0 – 2.6V	000 0000b
[23:15]	2.7 – 3.6V	1 1111 1111b
[28:24]	Reserved	0 0000b
[30:29]	Access Mode	10b (sector mode, for devices >2GB)[28]
[31]	Card power up status bit (0=busy; 1=ready)[29]	

9.1.1 Memory Addressing

Previous implementations of the e·MMC specification (versions up to v4.1) implemented byte addressing using a 32 bit field. This addressing mechanism permitted for e·MMC densities up to and including 2 GB. To support larger densities the addressing mechanism was update to support sector addresses (512 B sectors). The sector addresses shall be used for all devices with capacity larger than 2 GB.
To determine the addressing mode use the host should read bit [30:29] in the OCR register.

9.2 CID Register

The Card Identification (CID) register is 128 bits wide. It contains the Device identification information used during the Device identification phase (MultiMediaCard protocol). For details, refer to section 8.2 of the JEDEC Standard JESD84-A441.

[28] Bit 29 and 30 are valid, if Bit31 is high (card initialization completed).
[29] This bit is set LOW if the device has not finished the power up routine.

Table 27: CID register

Register Name	Bit Width	Description	typ. value
MID	8	Manufacture ID	0xDA (Swissbit)
–	6	Reserved	000000
CBX	2	Device/BGA	01
OID	8	OEM/Application ID	0x00
PNM	48	Product Name	e.g."00004G"
PRV	8	Product Revision	e.g. 0x10 (rev. 1.0)
PSN	32	Product Serial Number	xxxxxxxx
MDT	8	Manufacture Date	xx
CRC	7	Check sum of CID contents	CRC7 chksum
–	1	Not used; always=1	1

9.3 CSD Register

The Device-Specific Data (CSD) register provides information on how to access the Device contents. The CSD defines the data format, error correction type, maximum data access time, data transfer speed, whether the DSR register can be used etc. For details, refer to section 8.3 of the JEDEC Standard JESD84-A441.

Table 28: CSD register

Register Name	Bits	Bit Width	Description	typ. Value
CSD_STRUCTURE	127:126	2	CSD structure	0x3
SPEC_VERS	125:122	4	System Specification version	0x4
–	121:120	2	Reserved	-
TAAC	119:112	8	Data read access-time 1	0x0F
NSAC	111:104	8	Data read access-time 2 in CLK cycle (NSAC*100)	0x00
TRAN_SPEED	103:96	8	Max. bus clock frequency	0x32
CCC	95:84	12	Device command classes	0x1F5
READ_BL_LEN	83:80	4	Max. read data block length	0x9
READ_BL_PARTIAL	79	1	Partial blocks for read allowed	0x1
WRITE_BLK_MISALIGN	78	1	Write block misalignment	0x0
READ_BLK_MISALIGN	77	1	Read block misalignment	0x0
DSR_IMP	76	1	DSR implemented	0x0
–	75:74	2	Reserved	0x0
C_SIZE	73:62	12	Device size	0xFFF
VDD_R_CURR_MIN	61:59	3	Max read current @VDD min	0x7
VDD_R_CURR_MAX	58:56	3	Max read current @VDD max	0x7
VDD_W_CURR_MIN	55:53	3	Max write current @VDD min	0x7
VDD_W_CURR_MAX	52:50	3	Max write current @VDD max	0x7
C_SIZE_MULT	49:47	3	Device size multiplier	0x7
ERASE_GRP_SIZE	46:42	5	Erase group size	0x1F
ERASE_GRP_MULT	41:37	5	Erase group size multiplier	0x1F
WP_GRP_SIZE	36:32	5	Write protect group size	0x01
WP_GRP_ENABLE	31	1	Write protect group enable	0x1
DEFAULT_ECC	30:29	2	Manufacturer default ECC	0x0
R2W_FACTOR	28:26	3	Write speed factor	0x4
WRITE_BL_LEN	25:22	4	Max. write data block length	0x9
WRITE_BL_PARTIAL	21	1	Partial blocks for write allowed	0x0
–	20:17	4	Reserved	0x0
CONTENT_PROT_APP	16	1	Content protection application	0x0
FILE_FORMAT_GRP	15	1	File format group	0x0
COPY	14	1	Copy flag (OTP)	0x0
PERM_WRITE_PROTECT	13	1	Permanent write protection	0x0
TMP_WRITE_PROTECT	12	1	Temporary write protection	0x0
FILE_FORMAT	11:10	2	File format	0x0
ECC	9:8	2	ECC code	0x0
CRC	7:1	7	Checksum of CSD contents	-
–	0	1	Always=1	0x1

9.4 Extended CSD Register

The Extended CSD register defines the Device properties and selected modes. It is 512 bytes long. The most significant 320 bytes are the Properties segment, which defines the Device capabilities and cannot be modified by the host. The lower 192 bytes are the Modes segment, which defines the configuration the Device is working in. These modes can be changed by the host by means of the SWITCH command.
For details, refer to section 8.4 of the JEDEC Standard JESD84-A441.

Table 29: Extended CSD Register

Register Name	Bytes	Byte Width	Description	typ. Value
Properties Segment				
–	511:505	–	Reserved	–
S_CMD_SET	504	1	Supported Command Sets	0x00
HPI_FEATURES	503	1	HPI features	0x01
BKOPS_SUPPORT	502	1	Background operations support	0x01
–	501:270	–	Reserved	contains vendor information
DEVICE_LIFE_TIME_EST_TYP_B	269*	1	Device life time estimation type B	0x01
DEVICE_LIFE_TIME_EST_TYP_A	268*	1	Device life time estimation type A	0x01
PRE_EOL_INFO	267*	1	Pre EOL information	0x01
OPTIMAL_READ_SIZE	266*	1	Optimal read size	0x01
OPTIMAL_WRITE_SIZE	265*	1	Optimal write size	0x01
OPTIMAL_TRIM_UNIT_SIZE	264*	1	Optimal trim unit size	0x01
–	263:249	–	Reserved	contains vendor information
GENERIC_CMD6_TIME	248*	1	Generic CMD6 timeout	0x02
POWER_OFF_LONG_TIME	247*	1	Power off notification (long) timeout	0x19
BKOPS_STATUS	246	1	Background operations status	0x00
CORRECTLY_PRG_SECTORS_NUM	245:242	4	Number of correctly programmed sectors	0x00000000
INI_TIMEOUT_AP	241	1	1st initialization time after partitioning	0x0A
–	240	1	Reserved	–
PWR_CL_DDR_52_360	239	1	Power class for 52MHz, DDR at 3.6V	0x00
PWR_CL_DDR_52_360	238	1	Power class for 52MHz, DDR at 1.95V	0x00
–	237:236	2	Reserved	–
MIN_PERF_DDR_W_8_52	235	1	Minimum Write Performance for 8bit at 52MHz in DDR mode	0x00
MIN_PERF_DDR_R_8_52	234	1	Minimum Read Performance for 8bit at 52MHz in DDR mode	0x00
–	233	1	Reserved	–
TRIM_MULT	232	1	TRIM Multiplier	0x01
SEC_FEATURE_SUPPORT	231	1	Secure Feature support	0x41
SEC_ERASE_MULT	230	1	Secure Erase Multiplier	0x01
SEC_TRIM_MULT	229	1	Secure TRIM Multiplier	0x00
BOOT_INFO	228	1	Boot information	0x07
–	227	1	Reserved	–
BOOT_SIZE_MULTI	226	1	Boot partition size	0x80 (4GB)
ACC_SIZE	225	1	Access size	0x04
HC_ERASE_GRP_SIZE	224	1	High-capacity erase unit size	0x01
ERASE_TIMEOUT_MULT	223	1	High-capacity erase timeout	0x02
REL_WR_SEC_C	222	1	Reliable write sector count	0x01
HC_WP_GRP_SIZE	221	1	High-capacity write protect group size	0x02

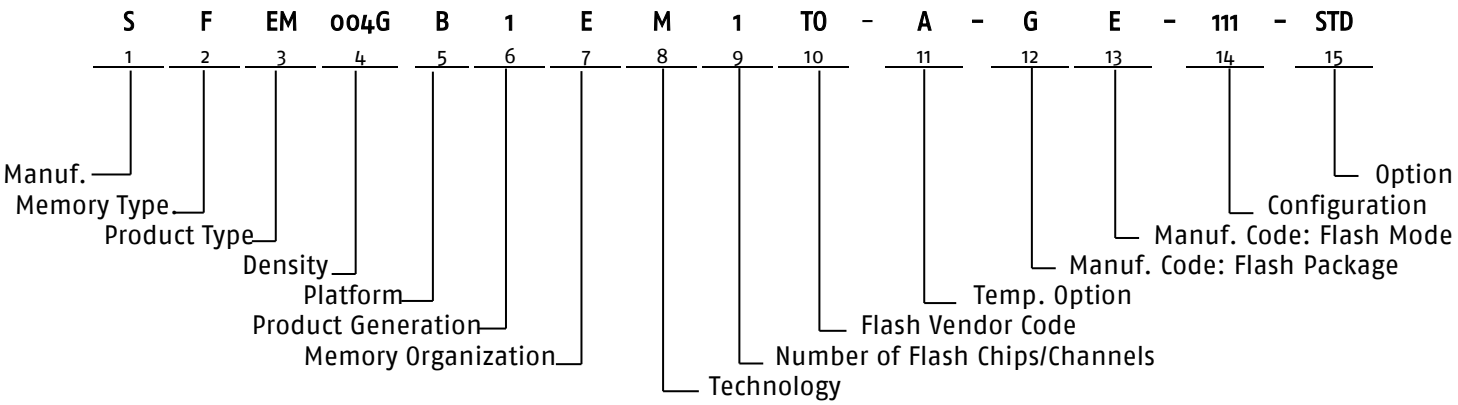
Register Name	Bytes	Byte Width	Description	typ. Value
S_C_VCC	220	1	Sleep current (VCC)	0x0B
S_C_VCCQ	219	1	Sleep current (VCCQ)	0x0B
PRODUCTION_STATE_AWARENESS_TIMEOUT	218	1	Production state awareness timeout	0x0A
S_A_TIMEOUT	217	1	Sleep/awake timeout	0x17
SLEEP_NOTIFICATION_TIME	216	1	Sleep notification timeout	0x0A
SEC_COUNT	215:212	4	Sector Count	(see chapter 4)
–	211	1	Reserved	–
MIN_PERF_W_8_52	210	1	Minimum Write Performance for 8bit at 52MHz	0x00
MIN_PERF_R_8_52	209	1	Minimum Read Performance for 8bit at 52MHz	0x00
MIN_PERF_W_8_26_4_52	208	1	Minimum Write Performance for 8bit at 26MHz, for 4bit at 52MHz	0x00
MIN_PERF_R_8_26_4_52	207	1	Minimum Read Performance for 8bit at 26MHz, for 4bit at 52MHz	0x00
MIN_PERF_W_4_26	206	1	Minimum Write Performance for 4bit at 26MHz	0x00
MIN_PERF_R_4_26	205	1	Minimum Read Performance for 4bit at 26MHz	0x00
–	204	1	Reserved	–
PWR_CL_26_360	203	1	Power class for 26MHz at 3.6V	0x00
PWR_CL_52_360	202	1	Power class for 52MHz at 3.6V	0x00
PWR_CL_26_195	201	1	Power class for 26MHz at 1.95V	0x00
PWR_CL_52_195	200	1	Power class for 52MHz at 1.95V	0x00
PARTITION_SWITCH_TIME	199	1	Partition switching timing	0x01
OUT_OF_INTERRUPT_TIME	198	1	Out-of-interrupt busy timing	0x78
–	197	1	Reserved	–
CARD_TYPE	196	1	Card type	0x03
–	195	1	Reserved	–
CSD_STRUCTURE	194	1	CSD structure version	0x02
–	193	1	Reserved	–
EXT_CSD_REV	192	1	Extended CSD revision	0x05
Modes Segment				
CMD_SET	191	1	Command set	0x00
–	190	1	Reserved	–
CMD_SET_REV	189	1	Command set revision	0x00
–	188	1	Reserved	–
POWER_CLASS	187	1	Power class	0x00
–	186	1	Reserved	–
HS_TIMING	185	1	High-speed interface timing	0x01
–	184	1	Reserved	–
BUS_WIDTH	183	1	Bus width mode	0x01
–	182	1	Reserved	–
ERASED_MEM_CONT	181	1	Erased memory content	0x00
–	180	1	Reserved	–
PARTITION_CONFIG	179	1	Partition configuration	0x00
BOOT_CONFIG_PROT	178	1	Boot config protection	0x00
BOOT_BUS_WIDTH	177	1	Boot bus width	0x00
–	176	1	Reserved	–
ERASE_GROUP_DEF	175	1	High-density erase group definition	0x00

Register Name	Bytes	Byte Width	Description	typ. Value
–	174	1	Reserved	–
BOOT_WP	173	1	Boot area write protection register	0x00
–	172	1	Reserved	–
USER_WP	171	1	User area write protection register	0x00
–	170	1	Reserved	–
FW_CONFIG	169	1	FW configuration	0x00
RPMB_SIZE_MULT	168	1	RPMB Size	0x20
WR_REL_SET	167	1	Write reliability setting register	0x00
WR_REL_PARAM	166	1	Write reliability parameter register	0x01
SANITIZE_START	165	1	Start Sanitize operation	0x00
BKOPS_START	164	1	Manually start background operations	0x00
BKOPS_EN	163	1	Enable background operations handshake	0x00
RST_n_FUNCTION	162	1	H/W reset function	0x00
HPI_MGMT	161	1	HPI management	0x00
PARTITIONING_SUPPORT	160	1	Partitioning Support	0x01
MAX_ENH_SIZE_MULT	159:157	3	Max Enhanced Area Size	0x00
PARTITIONS_ATTRIBUTE	156	1	Partitions attribute	0x00
PARTITION_SETTING_COMPLETED	155	1	Partitioning Setting	0x00
GP_SIZE_MULT	154:152	3	General Purpose Partition 4 Size	0x00
	151:149	3	General Purpose Partition 3 Size	0x00
	148:146	3	General Purpose Partition 2 Size	0x00
	145:143	3	General Purpose Partition 1 Size	0x00
ENH_SIZE_MULT	142:140	3	Enhanced User Data Area Size	0x00
ENH_START_ADDR	139:136	4	Enhanced User Data Start Address	0x00
–	135	1	Reserved	–
SEC_BAD_BLK_MGMNT	134	1	Bad Block Management mode	0x00
PRODUCTION_STATE_AWARENESS	133	1	Production state awareness	0x00
–	132:35	–	Reserved	–
POWER_OFF_NOTIFICATION	34	1	Power Off Notification	0x00
–	33:26	–	Reserved	–
PRE_LOADING_DATA_SIZE	25:22	4	Pre loading data size	0x00000000
MAX_PRE_LOADING_DATA_SIZE	21:18	4	Max pre loading data size	varying
PRODUCT_STATE_AWARENESS_ENABLEMENT	17	1	Product state awareness enablement	0x03
–	16:0	–	Reserved	–

9.5 RCA Register

The writable 16-bit Relative Device Address (RCA) register carries the Device address assigned by the host during the Device identification. This address is used for the addressed host-Device communication after the card identification procedure. The default value of the RCA register is 0x0001. The value 0x0000 is reserved to set all Devices into the *Stand-by State* with CMD7.

10. Part Number Decoder



10.1 Manufacturer

Swissbit code	S

10.2 Memory Type

Flash	F

10.3 Product Type

Embedded MMC (e·MMC)	EM

10.4 Density

2 GBytes	2048
4 GBytes	4096
8 GBytes	008G
16 GBytes	016G

10.5 Platform

BGA (embedded SSDs)	B

10.6 Product Generation

10.7 Memory Organization

Flash Products Embedded BGA	E

10.8 Technology

e·MMC controller	e·MMC 4.41	EM

10.9 Channels

1 channel	1

10.10 Flash Code

Toshiba	T0

10.11 Temperature Option

Automotive Temperature Range: -40 °C to 105 °C	A

10.12 Die Classification

MLC MONO (single die package)	G
MLC DDP (dual die package)	L
MLC QDP (quad die package)	H

10.13 Pin Mode

	COB
Single nCE and Single R/nB	E
Dual nCE and Dual R/nB	F
Quad nCE and Quad R/nB	G

10.14 Drive configuration XYZ

X = BGA Form Type

BGA Form Type	X
11.5 x 13mm, 153 ball	1

Y = Option

Option	Y
Default	1

Z = Feature

Feature	Z
Standard	1

10.15 Option

Swissbit/Standard	STD

11. Revision History

Table 30: Document Revision History

Date	Revision	Description	Revision Details
March 14, 2019	0.90	Initial preliminary release	Doc.req.no. 2832
August 27, 2019	1.00	Initial release Product code updated Registers and capacity spec. updated; parts numbers changed to industrial, automotive on request; performance and current values added; changed feature icons	Doc. req. no. 3147

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