Homework 8

Test Plan

Revision 1.1

Practicum Team 7

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Table of Contents

Table of Contents **1**

Introduction **2**

Reference Documents **2**

ORESAT C3 Overview **3**

Objectives **4**

Pretest Preparation **5**

- Required Equipment 5

Unit Tests **5**

- Power Input/Output 5
- Microcontroller 5
- Watchdog Timer 5
- Radio TX 5
- Radio RX 5
- OPD Interface 5
- MMC 5

Integration Tests **6**

- Microcontroller 6
- Watchdog Timer 6
- OPD 6
- CAN Transceivers 6
- Radios 6
- MMC 6

Acceptance Tests **6**

- Power 6
- OPD 6
- CAN 6
- Watchdog shutdown signal 6
- Radios 6
- MMC 6
- Physical Form Factor 7

Test Cases **7**

1. Introduction

This document will serve as a description of our test plan for our practicum project, ORESAT Communication Command and Control(C3) Board. Our ultimate objective is to determine whether or not our device fulfills its requirements and will be accepted by our customer, OreSat.

We will provide an overview of the OreSat C3 project, reference documents for our design process, pretest preparation measures, system test procedures and expected outcomes for each module of our project, integration testing procedures and expected outcomes, and acceptance testing procedures that will determine if our device fulfills its “must”-specified requirements as outlined in our initial product design specifications.

Because all modules are effectively integrated into a single printed circuit board, it would be highly impractical to test each module as a stand-alone block in a separate circuit without already being connected to other elements of the system. The layout of the board was designed with this in mind and includes test points. Accordingly, our build and test procedure will be roughly as follows:

1. Stuff and solder entire board with all components and test points
2. Provide current limited power source and check that power level is within expected range for all modules
3. Provide full normal operation power and test performance of each module individually
4. Test the interfaces and interactions between the various modules
5. Test that the entire system performs in accordance with the requirements

2. Reference Documents

2.1. Our **GitHub repository** has served as the central hub for all of our design work and documentation, and is available here: https://github.com/oresat/oresat-c3

2.2. Our **Product Design Specifications** document details the expected performance of the device and will be the metric with which the acceptability of our product is measured. This will serve as a useful reference for acceptance testing: https://github.com/oresat/oresat-c3/blob/master/doc/OreSat_C3_PDS.pdf

2.3. The **CAN protocol** is based on an extension of the CANopen specification known as ECSS-E-ST-50-15C – CANbus extension protocol (1 May 2015)

2.4. **OPD Endpoints** are controlled via the MAX7310 in order to activate cards and get circuit breaker status

2.5. The OreSat CLSI Application describes the overall OreSat design, purpose, and functionality for which we are building the C3 component

2.6. Our **System Functional Decomposition** document details the expected performance of each subsystem and shows how the subsystems relate to one another. This will serve as a useful reference for both Systems and Integration Testing:

2.7. https://github.com/oresat/oresat-c3/blob/master/doc/System_Design-Functional_Decomposition.pdf

3. ORESAT C3 Overview

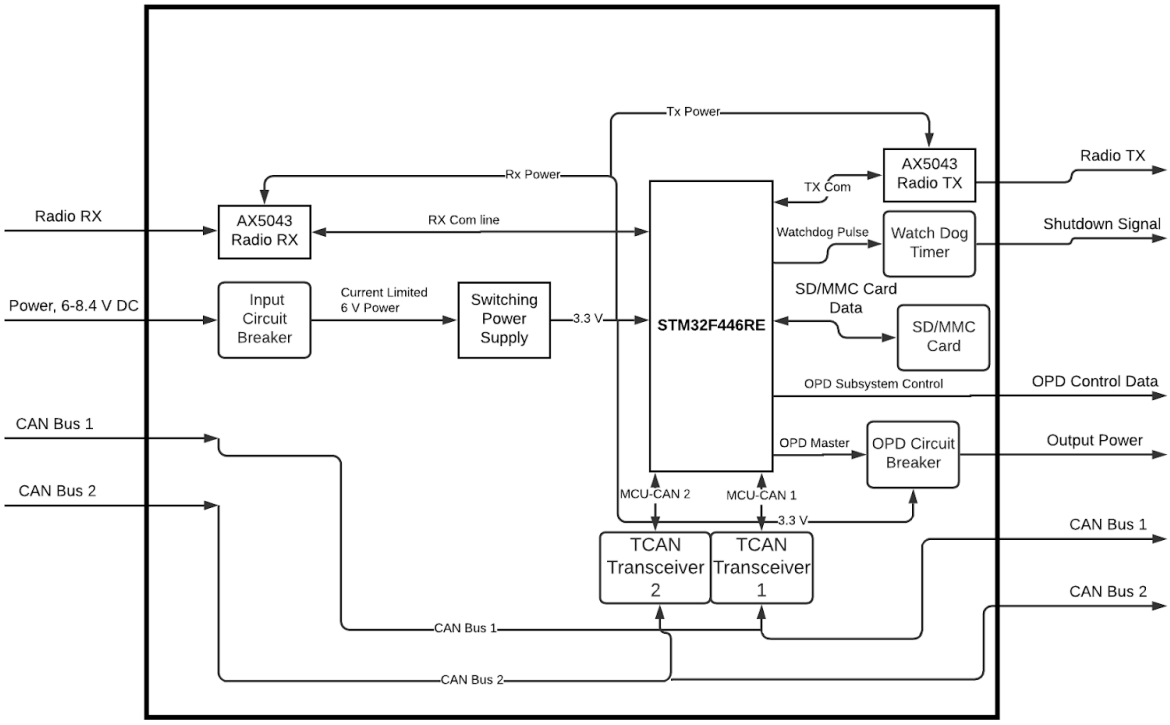

Figure 1: OreSat C3 Block Diagram

OreSat is an open-source cubesat project that is currently developing Oregon's first satellite to be launched into space. Our product is the command, control and communications (C3) module for OreSat's cubesat. It integrates several different sensors and actuators involved in the top

level control of the OreSat project. It is responsible for controlling the power and data flow to and from various subsystems within the satellite.

It receives a 6-8.4 V Power supply from an external solar cell module, which is fed into an Input Circuit Breaker module that provides overcurrent and undervoltage protection. This is then fed to a Switching Power Supply module which steps the voltage down to a regulated 3.3 V bus that is used to power an STM32 Microcontroller Unit(MCU) and is fed to the Oresat Power Domain(OPD) Circuit Breaker module, which receives control signals from the MCU and provides power to all external subsystems, and directly to the Rx and Tx Radio modules. C3 will also expect to receive radio transmissions from an external source on the Radio Rx line, which is then fed directly to the MCU through an SPI interface. The system will also receive data from external modules on the CAN Bus 1 and CAN Bus 2 lines, which are fed to TCAN Transceivers 1 and 2, and then sent to the MCU through MCU-CAN 1 and 2.

The MCU unit will also send SPI data to the Radio Tx module through the Tx Com line, which will then be sent to an external module for propagation.The MCU will also send a pulse to the Watchdog Timer, which will, in the absence of a pulse from the MCU, send a data packet down the Shutdown Signal line to an external module that will cut off power to the entire system. The MCU will also be storing data onto an MMC card, which will serve as memory storage. The MCU will also control power to the entire satellite through the OPD system by sending control signals to each external module through the OPD Control Data line, which controls power locally at each external module, and by sending signals on the OPD Master line which controls the OPD Circuit Breaker module, which provides power to all external modules in the satellite. Command and control data will also be sent from the MCU to the TCAN Transceiver 1 and 2 modules, which will then send data to external modules down the CAN Bus 1 and 2 lines.

The minimum requirements for our product is that it must:

1. Conform to OreSat card cage specifications
2. Be able to be powered from OreSat power bus
3. Be able to provide power to OreSat Power Domain
4. Be capable of interfacing with OreSat Power Domain
5. Be capable of interfacing with OreSat critical subsystems
6. Be able to reset in case of radiation induced single event latch-up of the C3 card
7. Provide communications interface with radio modules
8. Provide non-volatile data storage

4. Objectives

In order to ensure our project meets specifications, we must perform a series of tests to gradually bring up and verify components of the card, and incrementally integrate components together. The objectives of the tests are as follows

- Unit Tests: This stage of testing verifies individual subsystems of our card, such as power, work as expected. Most of this unit is applying power, testing voltages, pulling high or low different input test points, and verifying expected changes in outputs of blocks. It is done tested in discrete units.

- Integration test: This stage tests the interface between various subsystems. It verifies that subsystems can communicate correctly and that there are no unexpected conditions present in communication.
- Acceptance test: This stage tests that the entire board meets requirements previously established in our Product Design Specifications document.

5. Pretest Preparation

5.1. Required Equipment

5.1.1. Power supply capable of providing up to 8.4V and 400mA
5.1.2. Multimeter capable of measuring voltage and at least 100mA of current
5.1.3. Logic Analyzer capable of probing I2C and SPI communications
5.1.4. OreSat Protocard and FlatSat Bus to test interface with other subsystems

6. Unit Tests

6.1. Power Input/Output

6.1.1. Test the Input Circuit Breaker
6.1.2. Test the 3.3V Switching Power Supply
6.1.3. Test the OPD Circuit Breaker

6.2. Microcontroller

6.2.1. Test microcontroller is programmable with ST-LINK

6.3. Watchdog Timer

6.3.1. Test Watchdog Timer shutdown functionality

6.4. Radio TX

6.4.1. Verify power applied to TX radio and SPI lines

6.5. Radio RX

6.5.1. Verify power applied to RX radio and SPI lines

6.6. OPD Interface

6.6.1. Verify OPD I2C lines are pulled up correctly

6.7. MMC

6.7.1. Verify power control circuit for MMC card

7. Integration Tests

7.1. Microcontroller

7.1.1. Test debugging interface of microcontroller
7.1.2. Test serial interface of microcontroller

7.2. Watchdog Timer

7.2.1. Test ability to “kick” watchdog from MCU

7.3. OPD

7.3.1. Test power application to OPD circuit

7.3.2. Test I2C transaction with OPD circuit endpoint

7.4. CAN Transceivers

7.4.1. Test transmit and receive capability on CAN1 bus

7.4.2. Test transmit and receive capability on CAN2 bus

7.5. Radios

7.5.1. Test SPI communications with radios

7.6. MMC

7.6.1. Test SPI communications with MMC

7.6.2. Test ability to read and write data

8. Acceptance Tests

8.1. Power

8.1.1. Verify the voltage range of OreSat VBUS is sufficient to power the card and that circuit breakers perform as expected

8.2. OPD

8.2.1. Test that MCU can power and control OPD subsystem by issuing commands to circuit breakers on bus attached cards

8.3. CAN

8.3.1. Test that MCU can issue commands and receive telemetry from cards via the ECSS protocol on at least CAN1

8.4. Watchdog shutdown signal

8.4.1. Test that Watchdog timer will power cycle the board only if communication between it and the microcontroller ceases

8.5. Radios

8.5.1. Test communication between board and ground station

8.6. MMC

8.6.1. Test telemetry storage and retrieval from MMC card

8.7. Physical Form Factor

8.7.1. Verify card meets OreSat card specifications

9. Test Cases

Test Writer: Miles Simpson						
Test Case Name:	Test Input Circuit Breaker				**Test ID #:**	5.1.1
Description:	This test verifies proper functionality of the C3 card's input power circuit breaker. It ensures power is supplied through it to VBUSP, and that it current limits properly during a short.				**Type:**	X white box black box
Tester Information						
Name of Tester:					**Date:**	
Hardware Ver:	1.0				**Time:**	
Equipment:	Power Supply, Multimeter					
Setup:	PS set to 7.5V, 50mA max initially					
step	**Action**	**Expected Result**	**pass**	**fail**	**N/A**	**Comments**
1	Apply power to VBUS and verify VBUS and VBUSP with multimeter (VBUS pin on JP10, and TP20 respectively)	7.5V is measured at VBUS on JP10 and VBUSP at TP20, and current on power supply <50mA				
2	Increase supply current limit to 400mA and briefly short VBUSP at TP20 to ground with large gauge wire	Verifying that power supply reads ~302mA maximum current supplied to card during short				
3	Short VBUSP at TP20 to ground for extended period	Verify thermal cutoff occurs in TPS259621 within 2 seconds				
4						
5						
6						
Overall test result:						

Test Writer: Miles Simpson			
Test Case Name:	Test OPD Circuit Breaker	**Test ID #:**	5.1.3
Description:	This test verifies proper functionality of the C3 card's OPD output circuit breaker by testing the enable signal and current limiting functionality of the circuit.	**Type:**	X white box black box
Tester Information			
Name of Tester:		**Date:**	
Hardware Ver:	1.0	**Time:**	
Equipment:	Power Supply, Multimeter		
Setup:	PS set to 7.5V, 100mA max, connected to VBUS		

step	**Action**	**Expected Result**	**pass**	**fail**	**N/A**	**Comments**
1	Measure voltage of !OPD_ENABLE at TP13 using Multimeter	!OPD_ENABLE is pulled up to ~3.3V				
2	Ground TP13	Verify LED D4 turns on				
3	While grounded, measure voltage of !FAULT at TP8	!FAULT is high (~3.3V) and LED D5 is on				
4	Using 100mA multimeter current probe, short OPD_PWR to ground	Verify current does not exceed ~50mA				
5						
6						
Overall test result:						