OreSat Command, Control, and Communication (C3) Card: Project Requirements and Plan

A 2019-2020 ECE capstone project sponsored by the Portland State Aerospace Society

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Executive Summary

Our project's goal is to deliver a flight ready Command, Control, and Communication (C3) card for OreSat. OreSat is Oregon's first satellite. It is an open source 2U CubeSat being developed by the Portland State Aerospace Society (PSAS) with a target hand off date to NASA in winter 2021. The C3 card is the "system controller" for the satellite, it oversees the critical, attitude determination/control and mission subsystems.

The C3 card has the radios that link the CubeSat to the mission control on the ground. Once the CubeSat is released from the ISS, the C3 will be responsible for broadcasting a radio beacon so that the ground station can make initial contact and uniquely identify it in space. The C3 is also the heart of OreSat's radiation tolerance having the single rad-hard part in the satellite.

Project motivation

OreSat has a modular card-cage system that holds up to 20 cards. On these cards are: the critical subsystems (solar modules, batteries, and telemetry and telecommand radio systems), the attitude determination and control subsystems (IMU, GPS, Star Tracker, Reaction Wheels and Magnetorquers), and finally the mission subsystems (OreSat Live and the Cirrus Flux Camera). The C3 card ties all of these cards together into a functional satellite.

One of the challenges with developing a flight ready CubeSat is the harsh operating environment presented by space. Besides the stresses of vibration and extreme temperatures, ionizing radiation can cause CMOS devices to latch up. OreSat aims to be radiation tolerant while minimizing the use of expensive rad-hard parts. The C3 card makes this possible by retaining the ability to individually power cycle each card in the satellite thereby recovering the malfunctioning card from a single event latch up. The rad-hard watch dog on the C3 power cycles the whole satellite in the event of a latch-up on the MCU.

The C3 Card has redundant radios operating on two bands. The L-Band radio functions as a receiver only and enables the ground station to turn off the transmit/receive UHF radio in case it is stuck transmitting. This is necessary in order to comply with ITU regulations. Besides being the communications backbone, the C3 has onboard eMMC memory which serves as a buffer for mission and telemetry data in transit to and from the ground. The C3 also communicates with the critical and mission subsystems through two separate CAN buses and in this way it forms a common data hub for the whole satellite.

Product Design Specification

Concept of operations

This project aims to produce a central controller for OreSat. As mentioned above in the project motivation it is the key component that ties upto 20 distinct cards into an operational satellite. It does this by providing the following services:

- Serves as the main point of contact between the cards on the CubeSat with the ground substation
- Provides radiation tolerance to the other OreSat cards by monitoring them and resetting them through OreSat Power Domain (OPD)
- Is itself radiation tolerant since it has a rad-hard watchdog to reset the MCU in case of a latchup
- Provides a memory backed conduit for both telemetry and mission data data between the satellite subsystems and the ground

The final project will deliver a main controller card for the OreSat project. As such it will be used in a CubeSat that will be released from the ISS into orbit. While the proximate client is PSAS since the whole project is open source, other teams can take our work and either use it as is for their own CubeSat projects or else modify and remix it as needed.

The C3 card will be used internally by PSAS on the OreSat project, as such all the expertise to integrate it into the project already exists in house. We do aim to provide complete and explicit design documentation as well as SOPs so that the project could be replicated by a suitably equipped team. While the flight version of the card is single use (it will end its life after about a year in the glorious flames of reentry,) a great part of the value of this project will be the delivery of tested and proven designs contained in the open source intellectual property we will generate. This IP will remain the property of PSAS. With this in mind, even if our version of the C3 card is further improved upon prior to being flown, we will have succeeded if we go through the planned iterations culminating in a tested and functional C3 card.

Stakeholders

This project stakeholders include:

- Portland State Aerospace Society
- Portland State University
- Maseeh College of Engineering
- The capstone design team

Requirements

- Must
    - Be a fully compliant OreSat card
    - Be powered from the OreSat power bus
        - Be self isolating from the OreSat power bus in the event of an overcurrent condition
    - Provide power to the OreSat Power Domain (OPD)
        - Be fault tolerant of OPD overcurrent conditions
    - Control OPD
    - Communicate with the OreSat critical subsystem over a dedicated bus
    - Communicate with OreSat mission subsystems over a dedicated bus
    - Have an onboard radiation tolerant watchdog to reset OreSat in the event of a hung MCU
    - Have a >=8 GB data storage for gathering mission and telemetry data
    - Have and run the UHF (70cm) and L band (23cm) AX5043 sub-GHz radio ICs and downconverter for telemetry and telecommand (designs provided by PSAS)
    - Be able to power down the transmit radio to guard against a rogue transmitter
    - Handle the space environment: vacuum operation, -40 to +100 °C temperature range, and the vibration of launch
    - Be Single Event Upset and Single Event Latchup (SEU/SEL) robust
    - All intellectual property must be assigned an open source license, software under the GPL v3 and hardware under the CERN OHL v1.2.
    - All project design and documentation must be done using git on OreSat's Github pages.

Design Specifications

- OreSat protocard mechanical design
- 1x STM32F446RE MCU
    - 2x CAN
    - 1x I2C
    - 3x SPI (2x if using SDIO)
    - 1x SDIO (if not using SPI)
    - 3x GPIO for OPD_PWR Circuit Breaker
    - Watchdog interface (protocol TBD)
- 2x TCAN330
- 2x AX5043 Radios
    - 1x L-Band Rx only
    - 1x UHF Band Tx and Rx

- Power supply circuit breaker
- Dedicated Tx radio circuit breaker
- 1x Switching Power Supply for 3.3V
- OPD power supply circuit breaker
- 1x Watchdog
- Firmware based on ChibiOS RTOS
- Implements ECSS CANbus Extension Protocol for CAN interface to sensors
- Implements CCSDS recommended standards for radio interface

Deliverables

- Project proposal
- Weekly Progress Reports
- Final report
- ECE Capstone Poster Session poster
- At least one fully tested and operational C3 board
- Configuration, Software and Firmware, and EAGLE CAD files.
    - Committed to the 'oresat-c3' git repository on Github for hardware
    - Committed to the 'oresat-firmware' git repository on Github for firmware
- Complete documentation, including:
    - Source code
    - ECAD
    - Background, including research done and theory of operation
    - SOPs for operation

Initial Product Design

Taking the C3 practicum as a starting point. We propose to iteratively design, build and test an OreSat C3 board that meets the specifications above. The C3 practicum took the OreSat flat-sat prototype already implemented on a nucleo board and made a working prototype C3 card complying with the OreSat card cage specifications. This proved to be a drop-in replacement for the nucleo prototype. The two AX5043 radio modules were mated to the practicum board as daughter cards. Going forward, the most significant additions to the practicum board are the following:

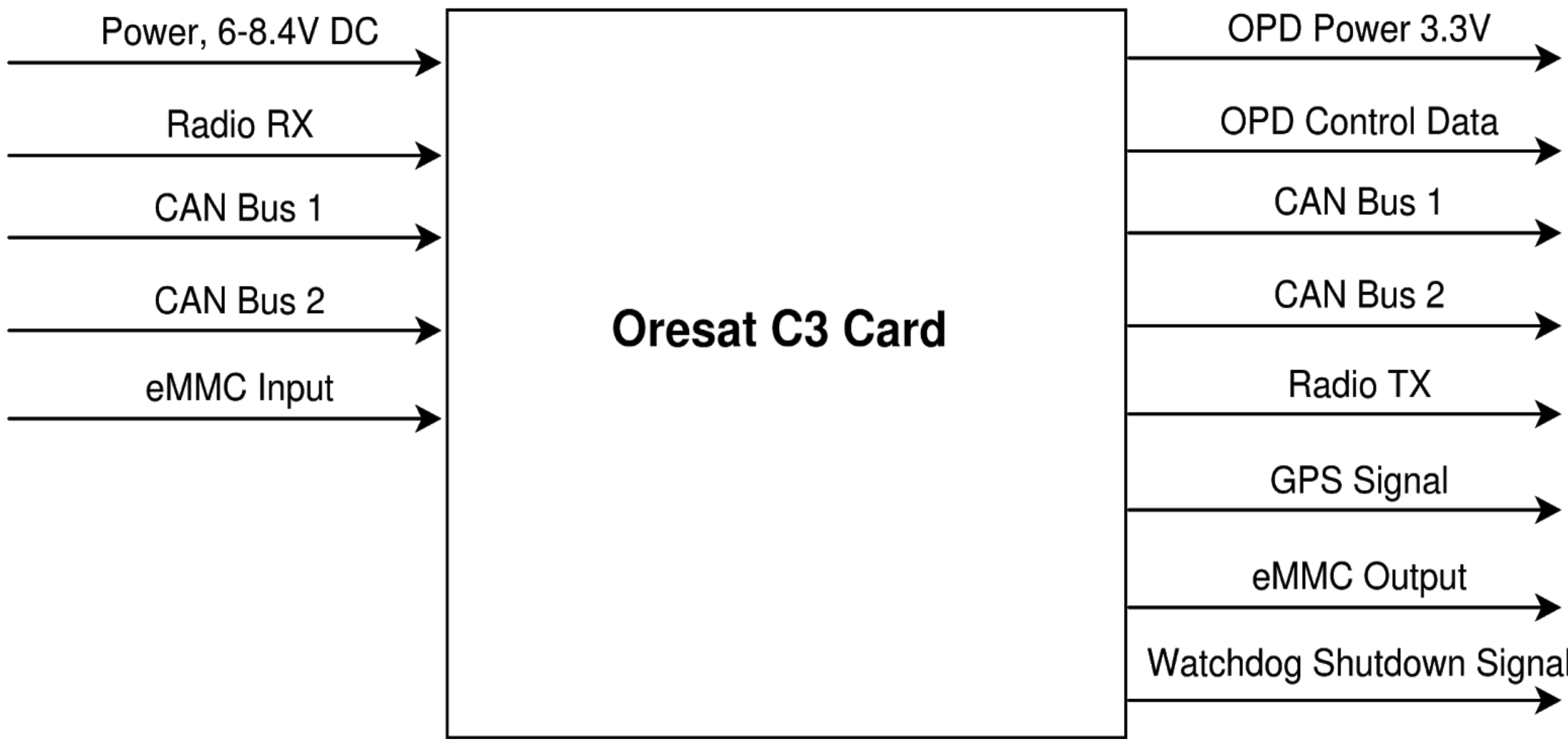
- The integration of the L band and UHF band radios as designed by another PSAS member into the C3 card. (Currently these are a series of separate RF modules.)
- The selection and integration of a rad-hard watchdog.
- The selection and integration of an appropriate eMMC module to replace the SD card from the practicum.
- The design and implementation of a TVS circuit for the OPD I^2C data lines.

Of these the biggest risks lie in the first. We are taking delivery of a mostly complete radio system. With the exception of two blocks, the individual modules have been built and tested to meet OreSat's requirements. Since however the radio system comprises both digital and RF components, migrating the system to a single board from its current modular form will change its operating characteristics. Moreover the practicum board layout will have to be reconfigured to make space for this new circuitry as well as to support the implementation of segregated RF power and ground. Beyond this a transmit power amplifier with attendant power monitoring and Tx time-out-timer logic has to be design finalized, built and tested. We do have the benefit of being able to consult with the system designers who are current PSAS members. We also have access to the expertise of the OreSat team and its resources. These considerations make this part of the project feasible in the given time frame.

Of the remaining additions, none presents a real challenge to the combined skills and abilities of the current team. The last major task will be compiling proper documentation as we implement these changes. We plan to progress in an iterative fashion with the goal of producing three tested hardware board revisions with the last fully tested and meeting the given specifications by mid May. We have access to the existing OreSat hardware and software design flow with attendant development, build and test tool chains. These represent a development platform that we can leverage without having to piece it together ourselves.

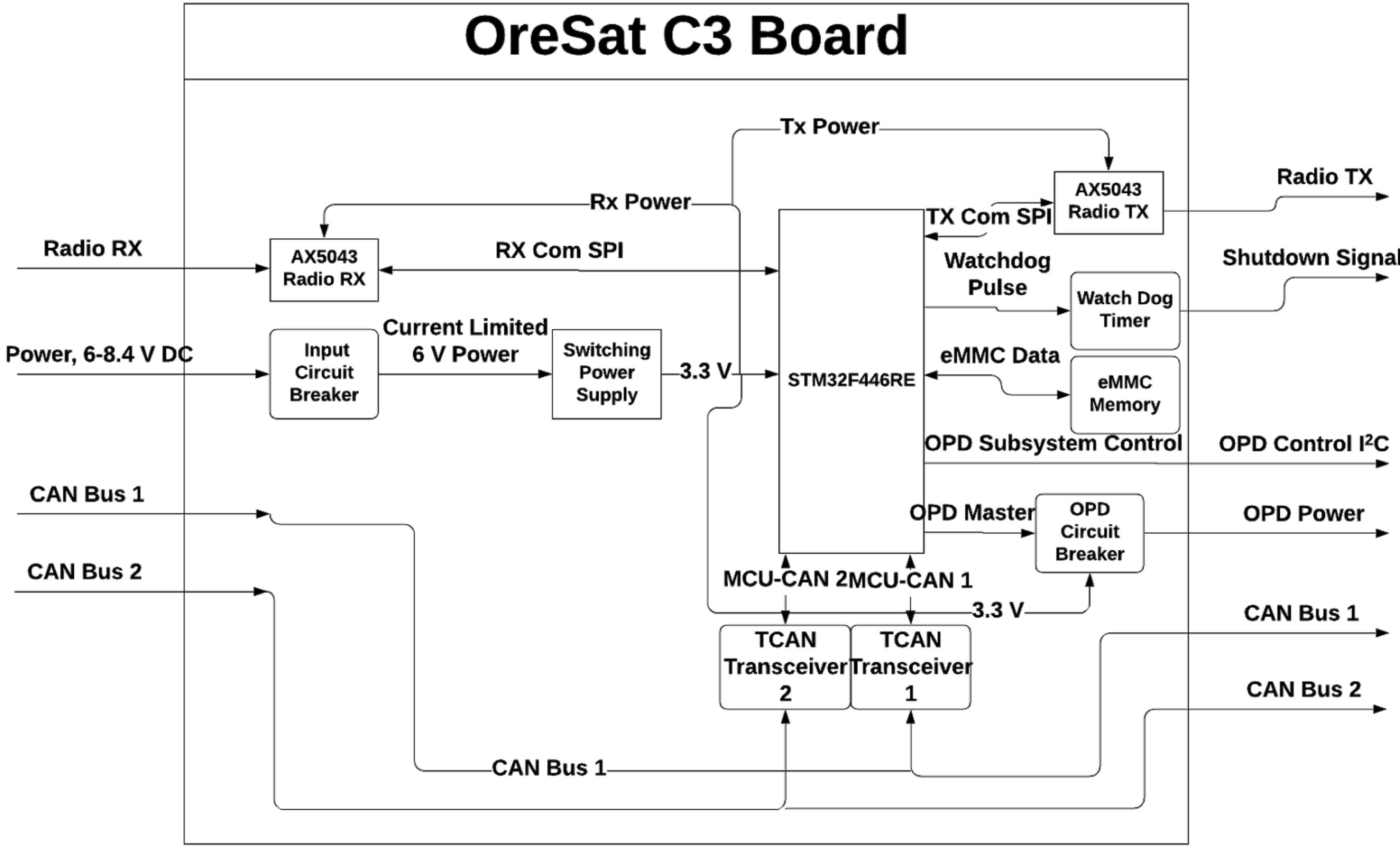
The goal of the project is an operational, space-ready RF communications module. Here too the expertise of the OreSat team is invaluable. The regulatory environment our product will be operating in has already been researched and de-risked. We are the beneficiaries of this groundwork. Close collaboration between our team members and the appropriate OreSat folks will be necessary to ensure that our designs fit this regulatory framework.

Oresat C3 Board: Level 0



Module:	Oresat C3 Card
Inputs:	Power (6-8.4 V DC) Radio RX signal (L Band and UHF Band) OPD Control Data (I2C) CAN Bus 1 (critical) CAN Bus 2 (mission) eMMC memory input
Outputs:	OPD Power (3.3 V, 50mA max) OPD Control Data (I2C) CAN Bus 1 (critical) CAN Bus 2 (mission) Radio TX (L Band and UHF Band) eMMC memory output Watchdog Shutdown Signal
Functionality:	Receive 6-8.4 V power from batteries and solar array. Step down voltage to (3.3 V, 300 mA) current limited for internal card usage. Provide power (3.3 V, 50 mA) current limited to OPD. Control Power to each subsystem via OPD Control Data. Communicate with critical subsystems via CAN 1. Communicate with mission subsystems via CAN 2. Receive commands from ground station via Radio RX signal. Cut off UHF PA in case it is stuck on. Transmit mission data via Radio TX signal. Store mission data in eMMC memory. Shutdown entire system power in case of MCU single event latchu-up via Shutdown Signal.

Oresat C3 Board: Level 1



Verification Plans

C3 subsystems will be individually tested for functionality where possible as well as interoperability. Please see functional description for functionality to be tested for each system block.

Project Management Plan

Timeline, with milestones

⊟**Board Freeze/ Board Order**	20 days	**1/6/20, 8:00 AM**	**1/31/20, 5:00 PM**
add eMMC	19.875 d...	1/6/20, 9:00 AM	1/31/20, 5:00 PM
add radios	20 days	1/6/20, 8:00 AM	1/31/20, 5:00 PM
⊟**Board Freeze/ Board Order2**	20 days?	**2/3/20, 8:00 AM**	**2/28/20, 5:00 PM**
add new watchdog	20 days	2/3/20, 8:00 AM	2/28/20, 5:00 PM
add L band Radio	10 days?	2/14/20, 9:00 AM	2/28/20, 9:00 AM
segregate ground planes	20 days	2/3/20, 8:00 AM	2/28/20, 5:00 PM
make room for radios	20 days	2/3/20, 8:00 AM	2/28/20, 5:00 PM
⊟**Board Freeze/ Board Order 3**	22 days	**3/2/20, 8:00 AM**	**3/31/20, 5:00 PM**
add UHF radio	22 days	3/2/20, 8:00 AM	3/31/20, 5:00 PM
⊟**Board Freeze/Board Order 4**	20 days	**4/1/20, 8:00 AM**	**4/28/20, 5:00 PM**
fix final mistakes	20 days	4/1/20, 8:00 AM	4/28/20, 5:00 PM
Board Freeze/ Board Order 5	21 days?	5/1/20, 7:00 AM	5/29/20, 5:00 PM
Final Documentation	13 days?	6/1/20, 8:00 AM	6/17/20, 5:00 PM

Budget and Resources

The resources we will use are as follows:

- The PSAS rocket room
- The EPL
- The Anechoic chamber
- PCB fabrication (Courtesy of OshPark)

- The expertise of the PSAS members spearheading OreSat
- Our personal computers

Our budget for this project is currently set at.

Team and development process

Our team is comprised of five team members:
- Miles Simpson: (Resident OreSat guru and firmware lead)
  - OreSat System Engineer
  - Firmware Lead
- Mikhail Mayers: (Project Manager and finisher)
  - Firmware Helper
  - EagleCAD
  - Board Stuffing
  - Organizer
  - Moral Support
- Ian Taylor: (Test and Verification)
  - Documentation
  - Board Stuffing
  - EagleCAD
  - Verification/Validation
- Marcus Chalona: (Layout Specialist)
  - EagleCAD
  - Board Stuffing
  - Documentation
  - Quality Assurance
- Robin Ekeya: (RF Specialist)
  - Analog systems development
  - RF systems development
  - EagleCAD

Following our industry sponsor's recommendation, we propose to use a spiral development method. Our plan to generate three board iterations fits this method well.

Industry Advisor Sign Off:

Name (print):	Andrew Granley
Signature:	
Date:	2020/2/28