

Layout Notes for Connector Board

20 Pin Connector

Pin Layout

Per Miles + Andrew

GND
VBUSP (jumper to USB 5V or FTDI 5V)
VCC (3V3 rail on board, for JTAG)
USART_TX (FTDI)
USART_RX (FTDI)
SWDIO (JTAG)
SWCLK (JTAG)
RESET (JTAG)
SWD (Possibly? Probably not?)
Slave D+
Slave D-
Host D+
Host D-
SPARE0
SPARE1
SPARE2
SPARE3
SPARE4

Connectors put
on prototype board

20 Pin Fcc

JTAG 10 Pin

6 Pin Serial

Micro USB (Slave)

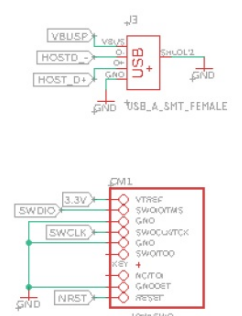
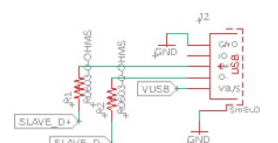
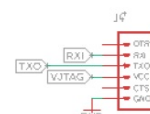
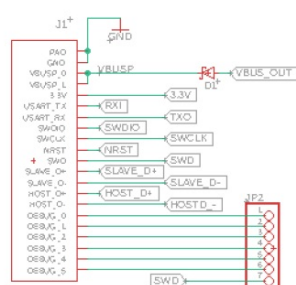
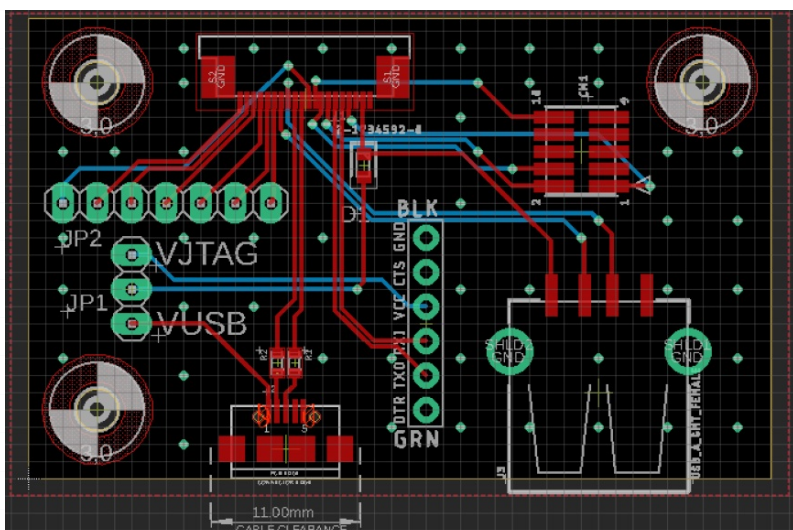
USB A (Host)

7 Pin (Debug Jumper)

Voltage Selector 3-Pin Jumper (VUSB or JTAG) Voltage Source

Connector Prototype Board Details

- 2 Layer Board
- trace width 3.048 mm (min)
- Git hub location
oresat-proto-card / card-debug-board



oresat-edge-connector.1br

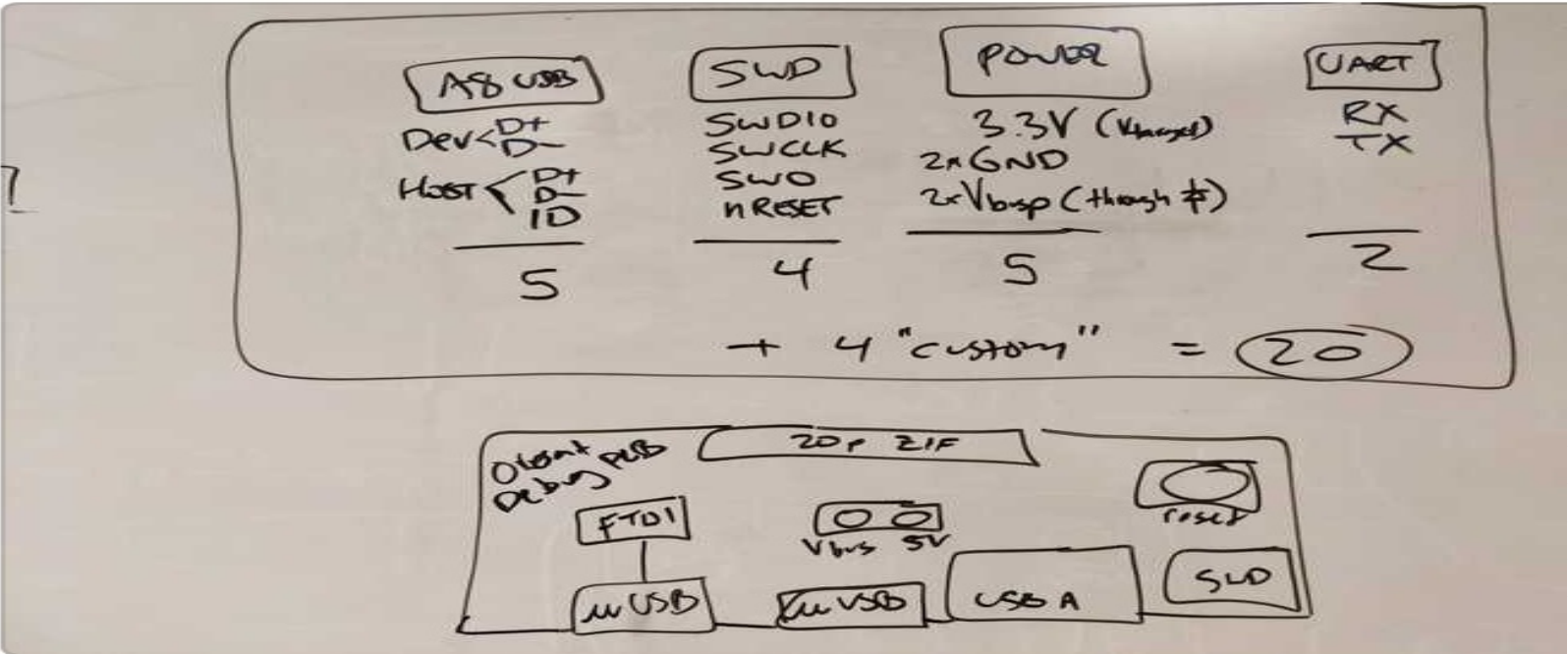
Changes / Suggestions

- Done
- Instead of a 6 pin FTDI cable which is \$19 each, let's actually add another uUSB connector and an actual FTDI USB to serial converter, like an FT232R.
 - Don't need the mounting holes. We won't be mounting these to anything.
 - VJTAG should be called "VSER" or "~~VFTDI~~" or something.
 - The 5V for the USB Type A host is provided by the card, so you'll need to add a 5V line.
 - Double up the ground line on the main connector (the PAD connector isn't actually connected to anything besides the physical pads).
 - No such thing as "SWD". It's "SWO". And it should be connected to the JTAG connector's SWO.
 - Go ahead and center the FFC connector on the board just because.
 - Change to 2 layer OSH Park design rules.
 - Don't need the resistors in the USB line.
 - Put the part number of the required FFC cable on the schematic.
- (edited)
- And then just to confuse you, this board should go into the protocard repo, maybe in oresat-~~proto-card~~/card-debug-board



OreSat debug pinout proposal.

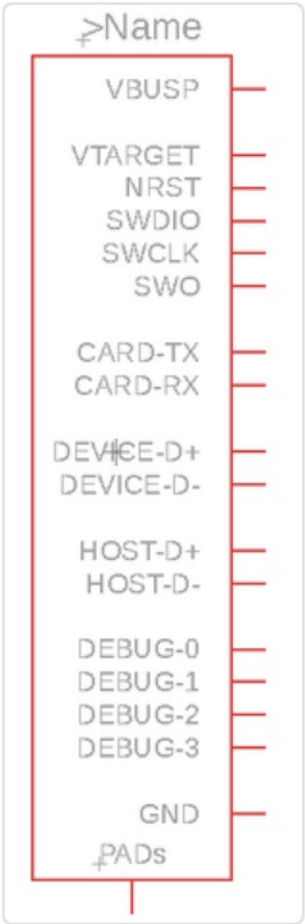
6054



Pins on top, breakout board on bottom.

Here's the pinout, which is supposed to (1) let the USB be high speed still and (2) not mind too much when the FFC cable shorts between pins, as it does sometimes.

- | | | |
|----|---|---------|
| 01 | - | VBUSP |
| 02 | - | VBUSP |
| 03 | - | GND |
| 04 | - | DEV-D+ |
| 05 | - | DEV-D- |
| 06 | - | GND |
| 07 | - | HOST-D+ |
| 08 | - | HOST-D- |
| 09 | - | GND |
| 10 | - | NRESET |
| 11 | - | VTARGET |
| 12 | - | STM-RX |
| 13 | - | STM-TX |
| 14 | - | SWDIO |
| 15 | - | SWCLK |
| 16 | - | SWO |
| 17 | - | DEBUG-0 |
| 18 | - | DEBUG-1 |
| 19 | - | DEBUG-2 |
| 20 | - | DEBUG-3 |



↑ ore sat - edge - connector.lbr

Changes / Fix Made

- route the USB D- D+, as
- differential pair (mostly length matched)
- route SWD to SWD (not to breakout)
- Add Jumper select for HOSTSV / DEBUG-0
- Add P-channel MOSFET to Power from USB via

Power Choices	Jumper
1) USB Slave	VUSB to VBUS_out
2) USB UART(us3)	VUSB to VBUS_OUT
3) USB UART(UART)	VSE1 to VBUS_out
- Made Power traces wider
- 20 Conductor 0.5 mm pitch FFC Molex 15166-0209
- Clear DRC + ERC Errors

