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# AR0130 Register Reference

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# Introduction

This register reference is provided for engineers who are designing cameras that use the AR0130.

# Register Address Space

The AR0130 provides a 16-bit register address space accessed through a serial interface. Each register location is 8 or 16 bits in size.

The address space is divided into the five major regions shown in Table 1.

**Table 1:**     **Address Space Regions**

| Address Range | Description |
|---|---|
| 0x0000–0x0FFF | Reserved |
| 0x1000–0x1FFF | Reserved |
| 0x2000–0x2FFF | Reserved |
| 0x3000–0x3FFF | Manufacturer-specific registers (read-only and read-write dynamic registers) |
| 0x4000–0xFFFF | Reserved |

# Register Notation

The underlying mechanism for reading and writing registers provides byte write capability. However, it is convenient to consider some registers as multiple adjacent bytes. The AR0130 use 8-bit, 16-bit, and 32-bit registers, all implemented as 1 or more bytes at naturally aligned, contiguous locations in the address space.

In this document, registers are described either by address or by name. When registers are described by address, the size of the registers is explicit. For example, R0x3024 is an 8-bit register at address 0x3024, and R0x3000–1 is a 16-bit register at address 0x3000–0x3001. When registers are described by name, the size of the register is implicit. It is necessary to refer to the register table to determine that model_id is a 16-bit register.

## Register Aliases

A consequence of the internal architecture of the AR0130 is that some registers are decoded at multiple addresses. Some registers in "configuration space" are also decoded in "manufacturer-specific space." To provide unique names for all registers, the name of the register within manufacturer-specific register space has a trailing underscore. For example, R0x0000–1 is model_id, and R0x3000–1 is model_id_. The effect of reading or writing a register through any of its aliases is identical.

## Bit Fields

Some registers provide control of several different pieces of related functionality, and this makes it necessary to refer to bit fields within registers. As an example of the notation used for this, the least significant 4 bits of the model_id register are referred to as model_id[3:0] or R0x0000–1[3:0].

## Byte Ordering

Registers that occupy more than 1 byte of address space are shown with the lowest address in the highest-order byte lane to match the byte-ordering on the bus. For example, the model_id register is R0x0000–1. In the register table the default value is shown as 0x2402. This means that a READ from address 0x0000 would return 0x26, and a READ from address 0x0001 would return 0x00. When reading this register as two 8-bit transfers on the serial interface, the 0x26 will appear on the serial interface first, followed by the 0x00.

## Address Alignment

All register addresses are aligned naturally. Registers that occupy two bytes of address space are aligned to even 16-bit addresses, and registers that occupy four bytes of address space are aligned to 16-bit addresses that are an integer multiple of 4.

## Bit Representation

For clarity, 32-bit hex numbers are shown with an underscore between the upper and lower 16 bits. For example: 0x3000_01AB.

## Data Format

Most registers represent an unsigned binary value or set of bit fields. For all other register formats, the format is stated explicitly at the start of the register description. The notation for these formats is shown in Table 2.

**Table 2:    Data Formats**

| Name | Description |
|---|---|
| FIX16 | Signed fixed-point, 16-bit number: two's complement number, 8 fractional bits. Examples: 0x0100 = 1.0, 0x8000 = −128, 0xFFFF = −0.0039065 |
| UFIX16 | Unsigned fixed-point, 16-bit number: 8.8 format. Examples: 0x0100 = 1.0, 0x280 = 2.5 |
| FLP32 | Signed floating-point, 32-bit number: IEEE 754 format. Example: 0x4280_0000 = 64.0 |

# Register Behavior

Registers vary from "read-only," "read/write," and "read, write-1-to-clear."

## Double-Buffered Registers

Some sensor settings cannot be changed during frame readout. For example, changing x_addr_start partway through frame readout would result in inconsistent row lengths within a frame. To avoid this, the AR0130 double-buffer many registers by implementing a "pending" and a "live" version. READs and WRITEs access the pending register; the live register controls the sensor operation.

The value in the pending register is transferred to a live register at a fixed point in the frame timing, called frame start. Frame start is defined as the point at which the first dark row is read out internally to the sensor. In the register tables the "Sync'd" column shows which registers or register fields are double-buffered in this way.

## Bad Frames

A bad frame is a frame where all rows do not have the same integration time or where offsets to the pixel values have changed during the frame.

Many changes to the sensor register settings can cause a bad frame. For example, when line_length_pck is changed, the new register value does not affect sensor behavior until the next frame start. However, the frame that would be read out at that frame start will have been integrated using the old row width, so reading it out using the new row width would result in a frame with an incorrect integration time.

By default, bad frames are not masked. If the masked bad frame option is enabled, both LV and FV are inhibited for these frames so that the vertical blanking time between frames is extended by the frame time.

In the register tables, the "Bad Frame" column shows where changing a register or register field will cause a bad frame. This notation is used:
   N—No. Changing the register value will not produce a bad frame.
   Y—Yes. Changing the register value might produce a bad frame.
   YM—Yes; but the bad frame will be masked out when mask_corrupted_frames (R0x0105) is set to "1."

# Register Summary Table

**Note:** Green1 (G1) corresponds to greenR (Gr); green2 (G2) corresponds to greenB (Gb).

**Caution** **Writing and changing the value of a reserved register (word or bit) puts the device in an unknown state and may damage the device.**

## Manufacturer-Specific Register List and Default Values

**Table 1:** **Manufacturer-Specific Register List and Default Values**
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

| Register Dec(Hex) | Name | Data Format (Binary) | Default Value Dec(Hex) |
|---|---|---|---|
| R12288 (R0x3000) | chip_version_reg | dddd dddd dddd dddd | 9218 (0x2402) |
| R12290 (R0x3002) | y_addr_start | 0000 00dd dddd dddd | 2 (0x0002) |
| R12292 (R0x3004) | x_addr_start | 0000 0ddd dddd dddd | 0 (0x0000) |
| R12294 (R0x3006) | y_addr_end | 0000 00dd dddd dddd | 965 (0x03C5) |
| R12296 (R0x3008) | x_addr_end | 0000 0ddd dddd dddd | 1283 (0x0503) |
| R12298 (R0x300A) | frame_length_lines | dddd dddd dddd dddd | 990 (0x03DE) |
| R12300 (R0x300C) | line_length_pck | dddd dddd dddd ddd0 | 1430 (0x0596) |
| R12302 (R0x300E) | revision_number | dddd dddd | 16 (0x10) |
| R12304 (R0x3010) | lock_control | dddd dddd dddd dddd | 48879 (0xBEEF) |
| R12306 (R0x3012) | coarse_integration_time | dddd dddd dddd dddd | 16 (0x0010) |
| R12308 (R0x3014) | fine_integration_time | dddd dddd dddd dddd | 0 (0x0000) |
| R12310 (R0x3016) | coarse_integration_time_cb | dddd dddd dddd dddd | 16 (0x0010) |
| R12312 (R0x3018) | fine_integration_time_cb | dddd dddd dddd dddd | 0 (0x0000) |
| R12314 (R0x301A) | reset_register | d00d dddd dddd dddd | 88 (0x0058) |
| R12318 (R0x301E) | data_pedestal | 0000 dddd dddd dddd | 168 (0x00A8) |
| R12326 (R0x3026) | gpi_status | 0000 0000 0000 ???? | 0 (0x0000) |
| R12328 (R0x3028) | row_speed | 0000 0000 0ddd 0000 | 16 (0x0010) |
| R12330 (R0x302A) | vt_pix_clk_div | 0000 0000 dddd dddd | 6 (0x0006) |

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**Table 1:** **Manufacturer-Specific Register List and Default Values (continued)**
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

| Register Dec(Hex) | Name | Data Format (Binary) | Default Value Dec(Hex) |
|---|---|---|---|
| R12332 (R0x302C) | vt_sys_clk_div | 0000 0000 000d dddd | 1 (0x0001) |
| R12334 (R0x302E) | pre_pll_clk_div | 0000 0000 00dd dddd | 2 (0x0002) |
| R12336 (R0x3030) | pll_multiplier | 0000 0000 dddd dddd | 44 (0x002C) |
| R12338 (R0x3032) | digital_binning | 0000 0000 00dd 00dd | 0 (0x0000) |
| R12346 (R0x303A) | frame_count | dddd dddd dddd dddd | 65535 (0xFFFF) |
| R12348 (R0x303C) | frame_status | 0000 0000 0000 00?? | 0 (0x0000) |
| R12352 (R0x3040) | read_mode | dd00 0000 0000 0000 | 0 (0x0000) |
| R12356 (R0x3044) | dark_control | dddd ddd0 d000 dd00 | 0 (0x0000) |
| R12358 (R0x3046) | flash | ??00 000d d000 0000 | 0 (0x0000) |
| R12374 (R0x3056) | green1_gain | 0000 0000 dddd dddd | 32 (0x0020) |
| R12376 (R0x3058) | blue_gain | 0000 0000 dddd dddd | 32 (0x0020) |
| R12378 (R0x305A) | red_gain | 0000 0000 dddd dddd | 32 (0x0020) |
| R12380 (R0x305C) | green2_gain | 0000 0000 dddd dddd | 32 (0x0020) |
| R12382 (R0x305E) | global_gain | 0000 0000 dddd dddd | 32 (0x0020) |
| R12388 (R0x3064) | embedded_data_ctrl | 000d dddd d000 dddd | 6530 (0x1982) |
| R12398 (R0x306E) | datapath_select | dddd dddd 000d 00dd | 37392 (0x9210) |
| R12400 (R0x3070) | test_pattern_mode | 0000 000d 0000 0ddd | 0 (0x0000) |
| R12402 (R0x3072) | test_data_red | 0000 dddd dddd dddd | 0 (0x0000) |
| R12404 (R0x3074) | test_data_greenr | 0000 dddd dddd dddd | 0 (0x0000) |
| R12406 (R0x3076) | test_data_blue | 0000 dddd dddd dddd | 0 (0x0000) |
| R12408 (R0x3078) | test_data_greenb | 0000 dddd dddd dddd | 0 (0x0000) |
| R12410 (R0x307A) | test_raw_mode | 0000 0000 0000 00dd | 0 (0x0000) |
| R12412 (R0x307C) | exposure_t2 | ???? ???? ???? ???? | 0 (0x0000) |
| R12416 (R0x3080) | exposure_t3 | ???? ???? ???? ???? | 0 (0x0000) |

**Table 1: Manufacturer-Specific Register List and Default Values (continued)**
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

| Register Dec(Hex) | Name | Data Format (Binary) | Default Value Dec(Hex) |
|---|---|---|---|
| R12418 (R0x3082) | operation_mode_ctrl | 0000 0000 00dd dddd | 41 (0x0029) |
| R12420 (R0x3084) | operation_mode_ctrl_cb | 0000 0000 00dd dd00 | 0 (0x0000) |
| R12422 (R0x3086) | seq_data_port | dddd dddd dddd dddd | 0 (0x0000) |
| R12424 (R0x3088) | seq_ctrl_port | ?d00 000d dddd dddd | 49152 (0xC000) |
| R12426 (R0x308A) | x_addr_start_cb | 0000 0ddd dddd dddd | 0 (0x0000) |
| R12428 (R0x308C) | y_addr_start_cb | 0000 00dd dddd dddd | 2 (0x0002) |
| R12430 (R0x308E) | x_addr_end_cb | 0000 0ddd dddd dddd | 1283 (0x0503) |
| R12432 (R0x3090) | y_addr_end_cb | 0000 00dd dddd dddd | 965 (0x03C5) |
| R12448 (R0x30A0) | x_even_inc | 0000 0000 0000 000? | 1 (0x0001) |
| R12450 (R0x30A2) | x_odd_inc | 0000 0000 0000 000d | 1 (0x0001) |
| R12452 (R0x30A4) | y_even_inc | 0000 0000 0000 000? | 1 (0x0001) |
| R12454 (R0x30A6) | y_odd_inc | 0000 0000 0ddd dddd | 1 (0x0001) |
| R12456 (R0x30A8) | y_odd_inc_cb | 0000 0000 0ddd dddd | 1 (0x0001) |
| R12458 (R0x30AA) | frame_length_lines_cb | dddd dddd dddd dddd | 990 (0x03DE) |
| R12460 (R0x30AC) | exposure_t1 | ???? ???? ???? ???? | 16 (0x0010) |
| R12464 (R0x30B0) | digital_test | dddd dddd dddd 0dd0 | 4096 (0x1000) |
| R12466 (R0x30B2) | tempsens_data | 0000 00dd dddd dddd | 0 (0x0000) |
| R12468 (R0x30B4) | tempsens_ctrl | 0000 0000 00dd dddd | 0 (0x0000) |
| R12474 (R0x30BA) | digital_ctrl | 0000 0000 000d dddd | 3 (0x0003) |
| R12476 (R0x30BC) | green1_gain_cb | 0000 0000 dddd dddd | 32 (0x0020) |
| R12478 (R0x30BE) | blue_gain_cb | 0000 0000 dddd dddd | 32 (0x0020) |
| R12480 (R0x30C0) | red_gain_cb | 0000 0000 dddd dddd | 32 (0x0020) |
| R12482 (R0x30C2) | green2_gain_cb | 0000 0000 dddd dddd | 32 (0x0020) |
| R12484 (R0x30C4) | global_gain_cb | 0000 0000 dddd dddd | 32 (0x0020) |

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**Table 1:     Manufacturer-Specific Register List and Default Values (continued)**
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

| Register Dec(Hex) | Name | Data Format (Binary) | Default Value Dec(Hex) |
|---|---|---|---|
| R12486 (R0x30C6) | tempsens_calib1 | dddd dddd dddd dddd | 291 (0x0123) |
| R12488 (R0x30C8) | tempsens_calib2 | dddd dddd dddd dddd | 17767 (0x4567) |
| R12490 (R0x30CA) | tempsens_calib3 | dddd dddd dddd dddd | 35243 (0x89AB) |
| R12492 (R0x30CC) | tempsens_calib4 | dddd dddd dddd dddd | 52719 (0xCDEF) |
| R12500 (R0x30D4) | column_correction | ddd0 0000 0000 dddd | 49159 (0xC007) |
| R12522 (R0x30EA) | gain_offset_ctrl | dddd dd0d dddd dddd | 3072 (0x0C00) |
| R12544 (R0x3100) | ae_ctrl_reg | 0000 0000 dddd dddd | 0 (0x0000) |
| R12546 (R0x3102) | ae_luma_target_reg | dddd dddd dddd dddd | 6000 (0x1770) |
| R12548 (R0x3104) | ae_hist_target_reg | dddd dddd dddd dddd | 49152 (0xC000) |
| R12550 (R0x3106) | ae_hysteresis_reg | dddd dddd dddd dddd | 29491 (0x7333) |
| R12552 (R0x3108) | ae_min_ev_step_reg | 0000 0000 dddd dddd | 16 (0x0010) |
| R12554 (R0x310A) | ae_max_ev_step_reg | 0000 0000 dddd dddd | 2 (0x0002) |
| R12556 (R0x310C) | ae_damp_offset_reg | dddd dddd dddd dddd | 16 (0x0010) |
| R12558 (R0x310E) | ae_damp_gain_reg | dddd dddd dddd dddd | 16 (0x0010) |
| R12560 (R0x3110) | ae_damp_max_reg | dddd dddd dddd dddd | 224 (0x00E0) |
| R12562 (R0x3112) | ae_dcg_exposure_high_reg | dddd dddd dddd dddd | 10240 (0x2800) |
| R12564 (R0x3114) | ae_dcg_exposure_low_reg | dddd dddd dddd dddd | 2048 (0x0800) |
| R12566 (R0x3116) | ae_dcg_gain_factor_reg | dddd dddd dddd dddd | 1024 (0x0400) |
| R12568 (R0x3118) | ae_dcg_gain_factor_inv_reg | dddd dddd dddd dddd | 64 (0x0040) |
| R12572 (R0x311C) | ae_max_exposure_reg | dddd dddd dddd dddd | 672 (0x02A0) |
| R12574 (R0x311E) | ae_min_exposure_reg | dddd dddd dddd dddd | 1 (0x0001) |
| R12576 (R0x3120) | ae_low_mean_target_reg | dddd dddd dddd dddd | 100 (0x0064) |
| R12578 (R0x3122) | ae_hist_low_thresh_reg | dddd dddd dddd dddd | 3932 (0x0F5C) |
| R12580 (R0x3124) | ae_dark_cur_thresh_reg | dddd dddd dddd dddd | 32767 (0x7FFF) |

**Table 1:    Manufacturer-Specific Register List and Default Values (continued)**
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

| Register Dec(Hex) | Name | Data Format (Binary) | Default Value Dec(Hex) |
|---|---|---|---|
| R12582 (R0x3126) | ae_alpha_v1_reg | dddd dddd dddd dddd | 80 (0x0050) |
| R12584 (R0x3128) | ae_alpha_coef_reg | dddd dddd dddd dddd | 1260 (0x04EC) |
| R12586 (R0x312A) | ae_current_gains | 0000 0??? ???? ???? | 32 (0x0020) |
| R12608 (R0x3140) | ae_roi_x_start_offset | 0000 0ddd dddd ddd0 | 0 (0x0000) |
| R12610 (R0x3142) | ae_roi_y_start_offset | 0000 00dd dddd ddd0 | 0 (0x0000) |
| R12612 (R0x3144) | ae_roi_x_size | 0000 0ddd dddd ddd0 | 1284 (0x0504) |
| R12614 (R0x3146) | ae_roi_y_size | 0000 00dd dddd ddd0 | 964 (0x03C4) |
| R12616 (R0x3148) | ae_hist_begin_perc | dddd dddd dddd dddd | 656 (0x0290) |
| R12618 (R0x314A) | ae_hist_end_perc | dddd dddd dddd dddd | 65535 (0xFFFF) |
| R12620 (R0x314C) | ae_hist_div | dddd dddd dddd dddd | 256 (0x0100) |
| R12622 (R0x314E) | ae_norm_width_min | dddd dddd dddd dddd | 32 (0x0020) |
| R12624 (R0x3150) | ae_mean_h | 0000 0000 0000 ???? | 0 (0x0000) |
| R12626 (R0x3152) | ae_mean_l | ???? ???? ???? ???? | 0 (0x0000) |
| R12628 (R0x3154) | ae_hist_begin_h | 0000 0000 0000 ???? | 0 (0x0000) |
| R12630 (R0x3156) | ae_hist_begin_l | ???? ???? ???? ???? | 0 (0x0000) |
| R12632 (R0x3158) | ae_hist_end_h | 0000 0000 0000 ???? | 0 (0x0000) |
| R12634 (R0x315A) | ae_hist_end_l | ???? ???? ???? ???? | 0 (0x0000) |
| R12636 (R0x315C) | ae_hist_end_mean_h | 0000 0000 0000 ???? | 0 (0x0000) |
| R12638 (R0x315E) | ae_hist_end_mean_l | ???? ???? ???? ???? | 0 (0x0000) |
| R12640 (R0x3160) | ae_perc_low_end | ???? ???? ???? ???? | 0 (0x0000) |
| R12642 (R0x3162) | ae_norm_abs_dev | ???? ???? ???? ???? | 0 (0x0000) |
| R12644 (R0x3164) | ae_coarse_integration_time | ???? ???? ???? ???? | 1 (0x0001) |
| R12646 (R0x3166) | ae_ag_exposure_hi | dddd dddd dddd dddd | 671 (0x029F) |
| R12648 (R0x3168) | ae_ag_exposure_lo | dddd dddd dddd dddd | 280 (0x0118) |

**Table 1:** **Manufacturer-Specific Register List and Default Values (continued)**
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

| Register Dec(Hex) | Name | Data Format (Binary) | Default Value Dec(Hex) |
|---|---|---|---|
| R12650 (R0x316A) | ae_ag_gain1 | dddd dddd dddd dddd | 512 (0x0200) |
| R12652 (R0x316C) | ae_ag_gain2 | dddd dddd dddd dddd | 512 (0x0200) |
| R12654 (R0x316E) | ae_ag_gain3 | dddd dddd dddd dddd | 512 (0x0200) |
| R12656 (R0x3170) | ae_inv_ag_gain1 | dddd dddd dddd dddd | 128 (0x0080) |
| R12658 (R0x3172) | ae_inv_ag_gain2 | dddd dddd dddd dddd | 128 (0x0080) |
| R12660 (R0x3174) | ae_inv_ag_gain3 | dddd dddd dddd dddd | 128 (0x0080) |
| R12672 (R0x3180) | delta_dk_control | dddd 0000 0000 0000 | 32768 (0x8000) |
| R12674 (R0x3182) | delta_dk_clip | dddd dddd dddd dddd | 32767 (0x7FFF) |
| R12676 (R0x3184) | delta_dk_t1 | ???? ???? ???? ???? | 0 (0x0000) |
| R12678 (R0x3186) | delta_dk_t2 | ???? ???? ???? ???? | 0 (0x0000) |
| R12680 (R0x3188) | delta_dk_t3 | ???? ???? ???? ???? | 0 (0x0000) |
| R12682 (R0x318A) | hdr_mc_ctrl1 | 0000 dddd dddd dddd | 4000 (0x0FA0) |
| R12684 (R0x318C) | hdr_mc_ctrl2 | dddd dddd dddd dddd | 64 (0x0040) |
| R12686 (R0x318E) | hdr_mc_ctrl3 | dddd 00dd dddd dddd | 272 (0x0110) |
| R12688 (R0x3190) | hdr_mc_ctrl4 | dddd dddd dddd dddd | 19360 (0x4BA0) |
| R12690 (R0x3192) | hdr_mc_ctrl5 | 000d dddd dddd dddd | 1024 (0x0400) |
| R12692 (R0x3194) | hdr_mc_ctrl6 | 0000 dddd dddd dddd | 3000 (0x0BB8) |
| R12694 (R0x3196) | hdr_mc_ctrl7 | 0000 dddd dddd dddd | 3500 (0x0DAC) |
| R12696 (R0x3198) | hdr_mc_ctrl8 | 0000 dddd dddd dddd | 4000 (0x0FA0) |
| R12698 (R0x319A) | hdr_comp_knee1 | 000? ???? 000? ???? | 4107 (0x100B) |
| R12700 (R0x319C) | hdr_comp_knee2 | 0000 0000 000? ???? | 20 (0x0014) |
| R12702 (R0x319E) | hdr_mc_ctrl9 | dddd dddd dddd dddd | 24704 (0x6080) |
| R12704 (R0x31A0) | hdr_mc_ctrl10 | 0000 dddd dddd dddd | 2976 (0x0BA0) |
| R12706 (R0x31A2) | hdr_mc_ctrl11 | 0000 dddd dddd dddd | 3000 (0x0BB8) |

**Table 1:** **Manufacturer-Specific Register List and Default Values (continued)**
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

| Register Dec(Hex) | Name | Data Format (Binary) | Default Value Dec(Hex) |
|---|---|---|---|
| R12736 (R0x31C0) | hispi_timing | 0ddd dddd dddd dddd | 0 (0x0000) |
| R12742 (R0x31C6) | hispi_control_status | ??00 00dd dddd dd00 | 32768 (0x8000) |
| R12744 (R0x31C8) | hispi_crc_0 | ???? ???? ???? ???? | 65535 (0xFFFF) |
| R12746 (R0x31CA) | hispi_crc_1 | ???? ???? ???? ???? | 65535 (0xFFFF) |
| R12748 (R0x31CC) | hispi_crc_2 | ???? ???? ???? ???? | 65535 (0xFFFF) |
| R12750 (R0x31CE) | hispi_crc_3 | ???? ???? ???? ???? | 65535 (0xFFFF) |
| R12752 (R0x31D0) | hdr_comp | 0000 0000 0000 0ddd | 0 (0x0000) |
| R12754 (R0x31D2) | stat_frame_id | dddd dddd dddd dddd | 0 (0x0000) |
| R12758 (R0x31D6) | i2c_wrt_checksum | dddd dddd dddd dddd | 65535 (0xFFFF) |
| R12768 (R0x31E0) | pix_def_id | d000 0000 0000 00dd | 0 (0x0000) |
| R12770 (R0x31E2) | pix_def_id_base_ram | 000d dddd dddd dddd | 0 (0x0000) |
| R12772 (R0x31E4) | pix_def_id_stream_ram | 000d dddd dddd dddd | 0 (0x0000) |
| R12774 (R0x31E6) | pix_def_ram_rd_addr | d000 0000 dddd dddd | 0 (0x0000) |
| R12776 (R0x31E8) | horizontal_cursor_position | 0000 00dd dddd dddd | 0 (0x0000) |
| R12778 (R0x31EA) | vertical_cursor_position | 0000 0ddd dddd dddd | 0 (0x0000) |
| R12780 (R0x31EC) | horizontal_cursor_width | 0000 00dd dddd dddd | 0 (0x0000) |
| R12782 (R0x31EE) | vertical_cursor_width | 0000 0ddd dddd dddd | 0 (0x0000) |
| R12788 (R0x31F4) | fuse_id1 | dddd dddd dddd dddd | 0 (0x0000) |
| R12790 (R0x31F6) | fuse_id2 | dddd dddd dddd dddd | 0 (0x0000) |
| R12792 (R0x31F8) | fuse_id3 | dddd dddd dddd dddd | 0 (0x0000) |
| R12794 (R0x31FA) | fuse_id4 | dddd dddd dddd dddd | 0 (0x0000) |
| R12796 (R0x31FC) | i2c_ids | dddd dddd dddd dddd | 12320 (0x3020) |
| R14336 (R0x3800) | otpm_data_0 | dddd dddd dddd dddd | 0 (0x0000) |
| R14338 (R0x3802) | otpm_data_1 | dddd dddd dddd dddd | 0 (0x0000) |

**Table 1:** **Manufacturer-Specific Register List and Default Values (continued)**
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

| Register Dec(Hex) | Name | Data Format (Binary) | Default Value Dec(Hex) |
|---|---|---|---|
| R14340 (R0x3804) | otpm_data_2 | dddd dddd dddd dddd | 0 (0x0000) |
| R14342 (R0x3806) | otpm_data_3 | dddd dddd dddd dddd | 0 (0x0000) |
| R14344 (R0x3808) | otpm_data_4 | dddd dddd dddd dddd | 0 (0x0000) |
| R14346 (R0x380A) | otpm_data_5 | dddd dddd dddd dddd | 0 (0x0000) |
| R14348 (R0x380C) | otpm_data_6 | dddd dddd dddd dddd | 0 (0x0000) |
| R14350 (R0x380E) | otpm_data_7 | dddd dddd dddd dddd | 0 (0x0000) |
| R14352 (R0x3810) | otpm_data_8 | dddd dddd dddd dddd | 0 (0x0000) |
| R14354 (R0x3812) | otpm_data_9 | dddd dddd dddd dddd | 0 (0x0000) |
| R14356 (R0x3814) | otpm_data_10 | dddd dddd dddd dddd | 0 (0x0000) |
| R14358 (R0x3816) | otpm_data_11 | dddd dddd dddd dddd | 0 (0x0000) |
| R14360 (R0x3818) | otpm_data_12 | dddd dddd dddd dddd | 0 (0x0000) |
| R14362 (R0x381A) | otpm_data_13 | dddd dddd dddd dddd | 0 (0x0000) |
| R14364 (R0x381C) | otpm_data_14 | dddd dddd dddd dddd | 0 (0x0000) |
| R14366 (R0x381E) | otpm_data_15 | dddd dddd dddd dddd | 0 (0x0000) |
| R14368 (R0x3820) | otpm_data_16 | dddd dddd dddd dddd | 0 (0x0000) |
| R14370 (R0x3822) | otpm_data_17 | dddd dddd dddd dddd | 0 (0x0000) |
| R14372 (R0x3824) | otpm_data_18 | dddd dddd dddd dddd | 0 (0x0000) |
| R14374 (R0x3826) | otpm_data_19 | dddd dddd dddd dddd | 0 (0x0000) |
| R14376 (R0x3828) | otpm_data_20 | dddd dddd dddd dddd | 0 (0x0000) |
| R14378 (R0x382A) | otpm_data_21 | dddd dddd dddd dddd | 0 (0x0000) |
| R14380 (R0x382C) | otpm_data_22 | dddd dddd dddd dddd | 0 (0x0000) |
| R14382 (R0x382E) | otpm_data_23 | dddd dddd dddd dddd | 0 (0x0000) |
| R14384 (R0x3830) | otpm_data_24 | dddd dddd dddd dddd | 0 (0x0000) |
| R14386 (R0x3832) | otpm_data_25 | dddd dddd dddd dddd | 0 (0x0000) |

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**Table 1:** **Manufacturer-Specific Register List and Default Values (continued)**
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

| Register Dec(Hex) | Name | Data Format (Binary) | Default Value Dec(Hex) |
|---|---|---|---|
| R14388 (R0x3834) | otpm_data_26 | dddd dddd dddd dddd | 0 (0x0000) |
| R14390 (R0x3836) | otpm_data_27 | dddd dddd dddd dddd | 0 (0x0000) |
| R14392 (R0x3838) | otpm_data_28 | dddd dddd dddd dddd | 0 (0x0000) |
| R14394 (R0x383A) | otpm_data_29 | dddd dddd dddd dddd | 0 (0x0000) |
| R14396 (R0x383C) | otpm_data_30 | dddd dddd dddd dddd | 0 (0x0000) |
| R14398 (R0x383E) | otpm_data_31 | dddd dddd dddd dddd | 0 (0x0000) |
| R14400 (R0x3840) | otpm_data_32 | dddd dddd dddd dddd | 0 (0x0000) |
| R14402 (R0x3842) | otpm_data_33 | dddd dddd dddd dddd | 0 (0x0000) |
| R14404 (R0x3844) | otpm_data_34 | dddd dddd dddd dddd | 0 (0x0000) |
| R14406 (R0x3846) | otpm_data_35 | dddd dddd dddd dddd | 0 (0x0000) |
| R14408 (R0x3848) | otpm_data_36 | dddd dddd dddd dddd | 0 (0x0000) |
| R14410 (R0x384A) | otpm_data_37 | dddd dddd dddd dddd | 0 (0x0000) |
| R14412 (R0x384C) | otpm_data_38 | dddd dddd dddd dddd | 0 (0x0000) |
| R14414 (R0x384E) | otpm_data_39 | dddd dddd dddd dddd | 0 (0x0000) |
| R14416 (R0x3850) | otpm_data_40 | dddd dddd dddd dddd | 0 (0x0000) |
| R14418 (R0x3852) | otpm_data_41 | dddd dddd dddd dddd | 0 (0x0000) |
| R14420 (R0x3854) | otpm_data_42 | dddd dddd dddd dddd | 0 (0x0000) |
| R14422 (R0x3856) | otpm_data_43 | dddd dddd dddd dddd | 0 (0x0000) |
| R14424 (R0x3858) | otpm_data_44 | dddd dddd dddd dddd | 0 (0x0000) |
| R14426 (R0x385A) | otpm_data_45 | dddd dddd dddd dddd | 0 (0x0000) |
| R14428 (R0x385C) | otpm_data_46 | dddd dddd dddd dddd | 0 (0x0000) |
| R14430 (R0x385E) | otpm_data_47 | dddd dddd dddd dddd | 0 (0x0000) |
| R14432 (R0x3860) | otpm_data_48 | dddd dddd dddd dddd | 0 (0x0000) |
| R14434 (R0x3862) | otpm_data_49 | dddd dddd dddd dddd | 0 (0x0000) |

**Table 1:** **Manufacturer-Specific Register List and Default Values (continued)**
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

| Register Dec(Hex) | Name | Data Format (Binary) | Default Value Dec(Hex) |
|---|---|---|---|
| R14436 (R0x3864) | otpm_data_50 | dddd dddd dddd dddd | 0 (0x0000) |
| R14438 (R0x3866) | otpm_data_51 | dddd dddd dddd dddd | 0 (0x0000) |
| R14440 (R0x3868) | otpm_data_52 | dddd dddd dddd dddd | 0 (0x0000) |
| R14442 (R0x386A) | otpm_data_53 | dddd dddd dddd dddd | 0 (0x0000) |
| R14444 (R0x386C) | otpm_data_54 | dddd dddd dddd dddd | 0 (0x0000) |
| R14446 (R0x386E) | otpm_data_55 | dddd dddd dddd dddd | 0 (0x0000) |
| R14448 (R0x3870) | otpm_data_56 | dddd dddd dddd dddd | 0 (0x0000) |
| R14450 (R0x3872) | otpm_data_57 | dddd dddd dddd dddd | 0 (0x0000) |
| R14452 (R0x3874) | otpm_data_58 | dddd dddd dddd dddd | 0 (0x0000) |
| R14454 (R0x3876) | otpm_data_59 | dddd dddd dddd dddd | 0 (0x0000) |
| R14456 (R0x3878) | otpm_data_60 | dddd dddd dddd dddd | 0 (0x0000) |
| R14458 (R0x387A) | otpm_data_61 | dddd dddd dddd dddd | 0 (0x0000) |
| R14460 (R0x387C) | otpm_data_62 | dddd dddd dddd dddd | 0 (0x0000) |
| R14462 (R0x387E) | otpm_data_63 | dddd dddd dddd dddd | 0 (0x0000) |
| R14464 (R0x3880) | otpm_data_64 | dddd dddd dddd dddd | 0 (0x0000) |
| R14466 (R0x3882) | otpm_data_65 | dddd dddd dddd dddd | 0 (0x0000) |
| R14468 (R0x3884) | otpm_data_66 | dddd dddd dddd dddd | 0 (0x0000) |
| R14470 (R0x3886) | otpm_data_67 | dddd dddd dddd dddd | 0 (0x0000) |
| R14472 (R0x3888) | otpm_data_68 | dddd dddd dddd dddd | 0 (0x0000) |
| R14474 (R0x388A) | otpm_data_69 | dddd dddd dddd dddd | 0 (0x0000) |
| R14476 (R0x388C) | otpm_data_70 | dddd dddd dddd dddd | 0 (0x0000) |
| R14478 (R0x388E) | otpm_data_71 | dddd dddd dddd dddd | 0 (0x0000) |
| R14480 (R0x3890) | otpm_data_72 | dddd dddd dddd dddd | 0 (0x0000) |
| R14482 (R0x3892) | otpm_data_73 | dddd dddd dddd dddd | 0 (0x0000) |

**Table 1:** **Manufacturer-Specific Register List and Default Values (continued)**
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

| Register Dec(Hex) | Name | Data Format (Binary) | Default Value Dec(Hex) |
|---|---|---|---|
| R14484 (R0x3894) | otpm_data_74 | dddd dddd dddd dddd | 0 (0x0000) |
| R14486 (R0x3896) | otpm_data_75 | dddd dddd dddd dddd | 0 (0x0000) |
| R14488 (R0x3898) | otpm_data_76 | dddd dddd dddd dddd | 0 (0x0000) |
| R14490 (R0x389A) | otpm_data_77 | dddd dddd dddd dddd | 0 (0x0000) |
| R14492 (R0x389C) | otpm_data_78 | dddd dddd dddd dddd | 0 (0x0000) |
| R14494 (R0x389E) | otpm_data_79 | dddd dddd dddd dddd | 0 (0x0000) |
| R14496 (R0x38A0) | otpm_data_80 | dddd dddd dddd dddd | 0 (0x0000) |
| R14498 (R0x38A2) | otpm_data_81 | dddd dddd dddd dddd | 0 (0x0000) |
| R14500 (R0x38A4) | otpm_data_82 | dddd dddd dddd dddd | 0 (0x0000) |
| R14502 (R0x38A6) | otpm_data_83 | dddd dddd dddd dddd | 0 (0x0000) |
| R14504 (R0x38A8) | otpm_data_84 | dddd dddd dddd dddd | 0 (0x0000) |
| R14506 (R0x38AA) | otpm_data_85 | dddd dddd dddd dddd | 0 (0x0000) |
| R14508 (R0x38AC) | otpm_data_86 | dddd dddd dddd dddd | 0 (0x0000) |
| R14510 (R0x38AE) | otpm_data_87 | dddd dddd dddd dddd | 0 (0x0000) |
| R14512 (R0x38B0) | otpm_data_88 | dddd dddd dddd dddd | 0 (0x0000) |
| R14514 (R0x38B2) | otpm_data_89 | dddd dddd dddd dddd | 0 (0x0000) |
| R14516 (R0x38B4) | otpm_data_90 | dddd dddd dddd dddd | 0 (0x0000) |
| R14518 (R0x38B6) | otpm_data_91 | dddd dddd dddd dddd | 0 (0x0000) |
| R14520 (R0x38B8) | otpm_data_92 | dddd dddd dddd dddd | 0 (0x0000) |
| R14522 (R0x38BA) | otpm_data_93 | dddd dddd dddd dddd | 0 (0x0000) |
| R14524 (R0x38BC) | otpm_data_94 | dddd dddd dddd dddd | 0 (0x0000) |
| R14526 (R0x38BE) | otpm_data_95 | dddd dddd dddd dddd | 0 (0x0000) |
| R14528 (R0x38C0) | otpm_data_96 | dddd dddd dddd dddd | 0 (0x0000) |
| R14530 (R0x38C2) | otpm_data_97 | dddd dddd dddd dddd | 0 (0x0000) |

**Table 1:    Manufacturer-Specific Register List and Default Values (continued)**
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

| Register Dec(Hex) | Name | Data Format (Binary) | Default Value Dec(Hex) |
|---|---|---|---|
| R14532 (R0x38C4) | otpm_data_98 | dddd dddd dddd dddd | 0 (0x0000) |
| R14534 (R0x38C6) | otpm_data_99 | dddd dddd dddd dddd | 0 (0x0000) |
| R14536 (R0x38C8) | otpm_data_100 | dddd dddd dddd dddd | 0 (0x0000) |
| R14538 (R0x38CA) | otpm_data_101 | dddd dddd dddd dddd | 0 (0x0000) |
| R14540 (R0x38CC) | otpm_data_102 | dddd dddd dddd dddd | 0 (0x0000) |
| R14542 (R0x38CE) | otpm_data_103 | dddd dddd dddd dddd | 0 (0x0000) |
| R14544 (R0x38D0) | otpm_data_104 | dddd dddd dddd dddd | 0 (0x0000) |
| R14546 (R0x38D2) | otpm_data_105 | dddd dddd dddd dddd | 0 (0x0000) |
| R14548 (R0x38D4) | otpm_data_106 | dddd dddd dddd dddd | 0 (0x0000) |
| R14550 (R0x38D6) | otpm_data_107 | dddd dddd dddd dddd | 0 (0x0000) |
| R14552 (R0x38D8) | otpm_data_108 | dddd dddd dddd dddd | 0 (0x0000) |
| R14554 (R0x38DA) | otpm_data_109 | dddd dddd dddd dddd | 0 (0x0000) |
| R14556 (R0x38DC) | otpm_data_110 | dddd dddd dddd dddd | 0 (0x0000) |
| R14558 (R0x38DE) | otpm_data_111 | dddd dddd dddd dddd | 0 (0x0000) |
| R14560 (R0x38E0) | otpm_data_112 | dddd dddd dddd dddd | 0 (0x0000) |
| R14562 (R0x38E2) | otpm_data_113 | dddd dddd dddd dddd | 0 (0x0000) |
| R14564 (R0x38E4) | otpm_data_114 | dddd dddd dddd dddd | 0 (0x0000) |
| R14566 (R0x38E6) | otpm_data_115 | dddd dddd dddd dddd | 0 (0x0000) |
| R14568 (R0x38E8) | otpm_data_116 | dddd dddd dddd dddd | 0 (0x0000) |
| R14570 (R0x38EA) | otpm_data_117 | dddd dddd dddd dddd | 0 (0x0000) |
| R14572 (R0x38EC) | otpm_data_118 | dddd dddd dddd dddd | 0 (0x0000) |
| R14574 (R0x38EE) | otpm_data_119 | dddd dddd dddd dddd | 0 (0x0000) |
| R14576 (R0x38F0) | otpm_data_120 | dddd dddd dddd dddd | 0 (0x0000) |
| R14578 (R0x38F2) | otpm_data_121 | dddd dddd dddd dddd | 0 (0x0000) |

**Table 1:    Manufacturer-Specific Register List and Default Values (continued)**

1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

| Register Dec(Hex) | Name | Data Format (Binary) | Default Value Dec(Hex) |
|---|---|---|---|
| R14580 (R0x38F4) | otpm_data_122 | dddd dddd dddd dddd | 0 (0x0000) |
| R14582 (R0x38F6) | otpm_data_123 | dddd dddd dddd dddd | 0 (0x0000) |
| R14584 (R0x38F8) | otpm_data_124 | dddd dddd dddd dddd | 0 (0x0000) |
| R14586 (R0x38FA) | otpm_data_125 | dddd dddd dddd dddd | 0 (0x0000) |
| R14588 (R0x38FC) | otpm_data_126 | dddd dddd dddd dddd | 0 (0x0000) |
| R14590 (R0x38FE) | otpm_data_127 | dddd dddd dddd dddd | 0 (0x0000) |
| R14592 (R0x3900) | otpm_data_128 | dddd dddd dddd dddd | 0 (0x0000) |
| R14594 (R0x3902) | otpm_data_129 | dddd dddd dddd dddd | 0 (0x0000) |
| R14596 (R0x3904) | otpm_data_130 | dddd dddd dddd dddd | 0 (0x0000) |
| R14598 (R0x3906) | otpm_data_131 | dddd dddd dddd dddd | 0 (0x0000) |
| R14600 (R0x3908) | otpm_data_132 | dddd dddd dddd dddd | 0 (0x0000) |
| R14602 (R0x390A) | otpm_data_133 | dddd dddd dddd dddd | 0 (0x0000) |
| R14604 (R0x390C) | otpm_data_134 | dddd dddd dddd dddd | 0 (0x0000) |
| R14606 (R0x390E) | otpm_data_135 | dddd dddd dddd dddd | 0 (0x0000) |
| R14608 (R0x3910) | otpm_data_136 | dddd dddd dddd dddd | 0 (0x0000) |
| R14610 (R0x3912) | otpm_data_137 | dddd dddd dddd dddd | 0 (0x0000) |
| R14612 (R0x3914) | otpm_data_138 | dddd dddd dddd dddd | 0 (0x0000) |
| R14614 (R0x3916) | otpm_data_139 | dddd dddd dddd dddd | 0 (0x0000) |
| R14616 (R0x3918) | otpm_data_140 | dddd dddd dddd dddd | 0 (0x0000) |
| R14618 (R0x391A) | otpm_data_141 | dddd dddd dddd dddd | 0 (0x0000) |
| R14620 (R0x391C) | otpm_data_142 | dddd dddd dddd dddd | 0 (0x0000) |
| R14622 (R0x391E) | otpm_data_143 | dddd dddd dddd dddd | 0 (0x0000) |
| R14624 (R0x3920) | otpm_data_144 | dddd dddd dddd dddd | 0 (0x0000) |
| R14626 (R0x3922) | otpm_data_145 | dddd dddd dddd dddd | 0 (0x0000) |

**Table 1: Manufacturer-Specific Register List and Default Values (continued)**
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

| Register Dec(Hex) | Name | Data Format (Binary) | Default Value Dec(Hex) |
|---|---|---|---|
| R14628 (R0x3924) | otpm_data_146 | dddd dddd dddd dddd | 0 (0x0000) |
| R14630 (R0x3926) | otpm_data_147 | dddd dddd dddd dddd | 0 (0x0000) |
| R14632 (R0x3928) | otpm_data_148 | dddd dddd dddd dddd | 0 (0x0000) |
| R14634 (R0x392A) | otpm_data_149 | dddd dddd dddd dddd | 0 (0x0000) |
| R14636 (R0x392C) | otpm_data_150 | dddd dddd dddd dddd | 0 (0x0000) |
| R14638 (R0x392E) | otpm_data_151 | dddd dddd dddd dddd | 0 (0x0000) |
| R14640 (R0x3930) | otpm_data_152 | dddd dddd dddd dddd | 0 (0x0000) |
| R14642 (R0x3932) | otpm_data_153 | dddd dddd dddd dddd | 0 (0x0000) |
| R14644 (R0x3934) | otpm_data_154 | dddd dddd dddd dddd | 0 (0x0000) |
| R14646 (R0x3936) | otpm_data_155 | dddd dddd dddd dddd | 0 (0x0000) |
| R14648 (R0x3938) | otpm_data_156 | dddd dddd dddd dddd | 0 (0x0000) |
| R14650 (R0x393A) | otpm_data_157 | dddd dddd dddd dddd | 0 (0x0000) |
| R14652 (R0x393C) | otpm_data_158 | dddd dddd dddd dddd | 0 (0x0000) |
| R14654 (R0x393E) | otpm_data_159 | dddd dddd dddd dddd | 0 (0x0000) |
| R14656 (R0x3940) | otpm_data_160 | dddd dddd dddd dddd | 0 (0x0000) |
| R14658 (R0x3942) | otpm_data_161 | dddd dddd dddd dddd | 0 (0x0000) |
| R14660 (R0x3944) | otpm_data_162 | dddd dddd dddd dddd | 0 (0x0000) |
| R14662 (R0x3946) | otpm_data_163 | dddd dddd dddd dddd | 0 (0x0000) |
| R14664 (R0x3948) | otpm_data_164 | dddd dddd dddd dddd | 0 (0x0000) |
| R14666 (R0x394A) | otpm_data_165 | dddd dddd dddd dddd | 0 (0x0000) |
| R14668 (R0x394C) | otpm_data_166 | dddd dddd dddd dddd | 0 (0x0000) |
| R14670 (R0x394E) | otpm_data_167 | dddd dddd dddd dddd | 0 (0x0000) |
| R14672 (R0x3950) | otpm_data_168 | dddd dddd dddd dddd | 0 (0x0000) |
| R14674 (R0x3952) | otpm_data_169 | dddd dddd dddd dddd | 0 (0x0000) |

**Table 1: Manufacturer-Specific Register List and Default Values (continued)**

1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

| Register Dec(Hex) | Name | Data Format (Binary) | Default Value Dec(Hex) |
|---|---|---|---|
| R14676 (R0x3954) | otpm_data_170 | dddd dddd dddd dddd | 0 (0x0000) |
| R14678 (R0x3956) | otpm_data_171 | dddd dddd dddd dddd | 0 (0x0000) |
| R14680 (R0x3958) | otpm_data_172 | dddd dddd dddd dddd | 0 (0x0000) |
| R14682 (R0x395A) | otpm_data_173 | dddd dddd dddd dddd | 0 (0x0000) |
| R14684 (R0x395C) | otpm_data_174 | dddd dddd dddd dddd | 0 (0x0000) |
| R14686 (R0x395E) | otpm_data_175 | dddd dddd dddd dddd | 0 (0x0000) |
| R14688 (R0x3960) | otpm_data_176 | dddd dddd dddd dddd | 0 (0x0000) |
| R14690 (R0x3962) | otpm_data_177 | dddd dddd dddd dddd | 0 (0x0000) |
| R14692 (R0x3964) | otpm_data_178 | dddd dddd dddd dddd | 0 (0x0000) |
| R14694 (R0x3966) | otpm_data_179 | dddd dddd dddd dddd | 0 (0x0000) |
| R14696 (R0x3968) | otpm_data_180 | dddd dddd dddd dddd | 0 (0x0000) |
| R14698 (R0x396A) | otpm_data_181 | dddd dddd dddd dddd | 0 (0x0000) |
| R14700 (R0x396C) | otpm_data_182 | dddd dddd dddd dddd | 0 (0x0000) |
| R14702 (R0x396E) | otpm_data_183 | dddd dddd dddd dddd | 0 (0x0000) |
| R14704 (R0x3970) | otpm_data_184 | dddd dddd dddd dddd | 0 (0x0000) |
| R14706 (R0x3972) | otpm_data_185 | dddd dddd dddd dddd | 0 (0x0000) |
| R14708 (R0x3974) | otpm_data_186 | dddd dddd dddd dddd | 0 (0x0000) |
| R14710 (R0x3976) | otpm_data_187 | dddd dddd dddd dddd | 0 (0x0000) |
| R14712 (R0x3978) | otpm_data_188 | dddd dddd dddd dddd | 0 (0x0000) |
| R14714 (R0x397A) | otpm_data_189 | dddd dddd dddd dddd | 0 (0x0000) |
| R14716 (R0x397C) | otpm_data_190 | dddd dddd dddd dddd | 0 (0x0000) |
| R14718 (R0x397E) | otpm_data_191 | dddd dddd dddd dddd | 0 (0x0000) |
| R14720 (R0x3980) | otpm_data_192 | dddd dddd dddd dddd | 0 (0x0000) |
| R14722 (R0x3982) | otpm_data_193 | dddd dddd dddd dddd | 0 (0x0000) |

**Table 1:** **Manufacturer-Specific Register List and Default Values (continued)**
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

| Register Dec(Hex) | Name | Data Format (Binary) | Default Value Dec(Hex) |
|---|---|---|---|
| R14724 (R0x3984) | otpm_data_194 | dddd dddd dddd dddd | 0 (0x0000) |
| R14726 (R0x3986) | otpm_data_195 | dddd dddd dddd dddd | 0 (0x0000) |
| R14728 (R0x3988) | otpm_data_196 | dddd dddd dddd dddd | 0 (0x0000) |
| R14730 (R0x398A) | otpm_data_197 | dddd dddd dddd dddd | 0 (0x0000) |
| R14732 (R0x398C) | otpm_data_198 | dddd dddd dddd dddd | 0 (0x0000) |
| R14734 (R0x398E) | otpm_data_199 | dddd dddd dddd dddd | 0 (0x0000) |
| R14736 (R0x3990) | otpm_data_200 | dddd dddd dddd dddd | 0 (0x0000) |
| R14738 (R0x3992) | otpm_data_201 | dddd dddd dddd dddd | 0 (0x0000) |
| R14740 (R0x3994) | otpm_data_202 | dddd dddd dddd dddd | 0 (0x0000) |
| R14742 (R0x3996) | otpm_data_203 | dddd dddd dddd dddd | 0 (0x0000) |
| R14744 (R0x3998) | otpm_data_204 | dddd dddd dddd dddd | 0 (0x0000) |
| R14746 (R0x399A) | otpm_data_205 | dddd dddd dddd dddd | 0 (0x0000) |
| R14748 (R0x399C) | otpm_data_206 | dddd dddd dddd dddd | 0 (0x0000) |
| R14750 (R0x399E) | otpm_data_207 | dddd dddd dddd dddd | 0 (0x0000) |
| R14752 (R0x39A0) | otpm_data_208 | dddd dddd dddd dddd | 0 (0x0000) |
| R14754 (R0x39A2) | otpm_data_209 | dddd dddd dddd dddd | 0 (0x0000) |
| R14756 (R0x39A4) | otpm_data_210 | dddd dddd dddd dddd | 0 (0x0000) |
| R14758 (R0x39A6) | otpm_data_211 | dddd dddd dddd dddd | 0 (0x0000) |
| R14760 (R0x39A8) | otpm_data_212 | dddd dddd dddd dddd | 0 (0x0000) |
| R14762 (R0x39AA) | otpm_data_213 | dddd dddd dddd dddd | 0 (0x0000) |
| R14764 (R0x39AC) | otpm_data_214 | dddd dddd dddd dddd | 0 (0x0000) |
| R14766 (R0x39AE) | otpm_data_215 | dddd dddd dddd dddd | 0 (0x0000) |
| R14768 (R0x39B0) | otpm_data_216 | dddd dddd dddd dddd | 0 (0x0000) |
| R14770 (R0x39B2) | otpm_data_217 | dddd dddd dddd dddd | 0 (0x0000) |

**Table 1:** **Manufacturer-Specific Register List and Default Values (continued)**
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

| Register Dec(Hex) | Name | Data Format (Binary) | Default Value Dec(Hex) |
|---|---|---|---|
| R14772 (R0x39B4) | otpm_data_218 | dddd dddd dddd dddd | 0 (0x0000) |
| R14774 (R0x39B6) | otpm_data_219 | dddd dddd dddd dddd | 0 (0x0000) |
| R14776 (R0x39B8) | otpm_data_220 | dddd dddd dddd dddd | 0 (0x0000) |
| R14778 (R0x39BA) | otpm_data_221 | dddd dddd dddd dddd | 0 (0x0000) |
| R14780 (R0x39BC) | otpm_data_222 | dddd dddd dddd dddd | 0 (0x0000) |
| R14782 (R0x39BE) | otpm_data_223 | dddd dddd dddd dddd | 0 (0x0000) |
| R14784 (R0x39C0) | otpm_data_224 | dddd dddd dddd dddd | 0 (0x0000) |
| R14786 (R0x39C2) | otpm_data_225 | dddd dddd dddd dddd | 0 (0x0000) |
| R14788 (R0x39C4) | otpm_data_226 | dddd dddd dddd dddd | 0 (0x0000) |
| R14790 (R0x39C6) | otpm_data_227 | dddd dddd dddd dddd | 0 (0x0000) |
| R14792 (R0x39C8) | otpm_data_228 | dddd dddd dddd dddd | 0 (0x0000) |
| R14794 (R0x39CA) | otpm_data_229 | dddd dddd dddd dddd | 0 (0x0000) |
| R14796 (R0x39CC) | otpm_data_230 | dddd dddd dddd dddd | 0 (0x0000) |
| R14798 (R0x39CE) | otpm_data_231 | dddd dddd dddd dddd | 0 (0x0000) |
| R14800 (R0x39D0) | otpm_data_232 | dddd dddd dddd dddd | 0 (0x0000) |
| R14802 (R0x39D2) | otpm_data_233 | dddd dddd dddd dddd | 0 (0x0000) |
| R14804 (R0x39D4) | otpm_data_234 | dddd dddd dddd dddd | 0 (0x0000) |
| R14806 (R0x39D6) | otpm_data_235 | dddd dddd dddd dddd | 0 (0x0000) |
| R14808 (R0x39D8) | otpm_data_236 | dddd dddd dddd dddd | 0 (0x0000) |
| R14810 (R0x39DA) | otpm_data_237 | dddd dddd dddd dddd | 0 (0x0000) |
| R14812 (R0x39DC) | otpm_data_238 | dddd dddd dddd dddd | 0 (0x0000) |
| R14814 (R0x39DE) | otpm_data_239 | dddd dddd dddd dddd | 0 (0x0000) |
| R14816 (R0x39E0) | otpm_data_240 | dddd dddd dddd dddd | 0 (0x0000) |
| R14818 (R0x39E2) | otpm_data_241 | dddd dddd dddd dddd | 0 (0x0000) |

**Table 1:** **Manufacturer-Specific Register List and Default Values (continued)**
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

| Register Dec(Hex) | Name | Data Format (Binary) | Default Value Dec(Hex) |
|---|---|---|---|
| R14820 (R0x39E4) | otpm_data_242 | dddd dddd dddd dddd | 0 (0x0000) |
| R14822 (R0x39E6) | otpm_data_243 | dddd dddd dddd dddd | 0 (0x0000) |
| R14824 (R0x39E8) | otpm_data_244 | dddd dddd dddd dddd | 0 (0x0000) |
| R14826 (R0x39EA) | otpm_data_245 | dddd dddd dddd dddd | 0 (0x0000) |
| R14828 (R0x39EC) | otpm_data_246 | dddd dddd dddd dddd | 0 (0x0000) |
| R14830 (R0x39EE) | otpm_data_247 | dddd dddd dddd dddd | 0 (0x0000) |
| R14832 (R0x39F0) | otpm_data_248 | dddd dddd dddd dddd | 0 (0x0000) |
| R14834 (R0x39F2) | otpm_data_249 | dddd dddd dddd dddd | 0 (0x0000) |
| R14836 (R0x39F4) | otpm_data_250 | dddd dddd dddd dddd | 0 (0x0000) |
| R14838 (R0x39F6) | otpm_data_251 | dddd dddd dddd dddd | 0 (0x0000) |
| R14840 (R0x39F8) | otpm_data_252 | dddd dddd dddd dddd | 0 (0x0000) |
| R14842 (R0x39FA) | otpm_data_253 | dddd dddd dddd dddd | 0 (0x0000) |
| R14844 (R0x39FC) | otpm_data_254 | dddd dddd dddd dddd | 0 (0x0000) |
| R14846 (R0x39FE) | otpm_data_255 | dddd dddd dddd dddd | 0 (0x0000) |
| R16100 (R0x3EE4) | dac_ld_24_25 | dddd dddd dddd dddd | 53768 (0xD208) |
| R16336 (R0x3FD0) | bist_buffers_control1 | 0000 dddd dddd dddd | 0 (0x0000) |
| R16338 (R0x3FD2) | bist_buffers_control2 | 0000 0ddd dddd dddd | 0 (0x0000) |
| R16340 (R0x3FD4) | bist_buffers_status1 | 0000 0??? ???? ???? | 0 (0x0000) |
| R16342 (R0x3FD6) | bist_buffers_status2 | 0000 0??? ???? ???? | 0 (0x0000) |
| R16344 (R0x3FD8) | bist_buffers_data1 | 000? ???? ???? ???? | 0 (0x0000) |
| R16346 (R0x3FDA) | bist_buffers_data2 | 000? ???? ???? ???? | 0 (0x0000) |

# Register Descriptions

## Manufacturer-Specific Register Descriptions

**Table 2:** **Manufacturer-Specific Register Descriptions**
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

| Register Dec(Hex) | Bits | Default | Name | Frame Sync'd | Bad Frame |
|---|---|---|---|---|---|
| 12288 R0x3000 | 15:0 | 0x2402 | chip_version_reg (R/W) | N | N |
| | Model ID. Read-only. Can be made read/write by clearing R0x301A-B[3]. | | | | |
| 12290 R0x3002 | 15:0 | 0x0002 | y_addr_start (R/W) | Y | YM |
| | The first row of visible pixels to be read out (not counting any dark rows that may be read). To move the image window, set this register to the starting Y value. | | | | |
| 12292 R0x3004 | 15:0 | 0x0000 | x_addr_start (R/W) | Y | N |
| | The first column of visible pixels to be read out (not counting any dark columns that may be read). To move the image window, set this register to the starting X value. | | | | |
| 12294 R0x3006 | 15:0 | 0x03C5 | y_addr_end (R/W) | Y | YM |
| | The last row of visible pixels to be read out. | | | | |
| 12296 R0x3008 | 15:0 | 0x0503 | x_addr_end (R/W) | Y | N |
| | The last column of visible pixels to be read out. | | | | |
| 12298 R0x300A | 15:0 | 0x03DE | frame_length_lines (R/W) | Y | YM |
| | The number of complete lines (rows) in the output frame. This includes visible lines and vertical blanking lines. The rows included are:<br>Column correction (tied) rows. Default 8.<br>Delta dark rows. Default 6.<br>Extra reset. 4 rows (2 used for embedded data when enabled),<br>Image data (y_addr_end - y_addr_start +1)<br>Extra reset. 4 rows (2 used for embedded stats data when enabled).<br>Zebra Test rows. Default 4.<br><br>Note: In ERS linear mode, the actual frame time (FV high + FV low) will be one row longer than the value in this register. To get an even numbered frame time, an odd (-1) value must be programmed. | | | | |
| 12300 R0x300C | 15:0 | 0x0596 | line_length_pck (R/W) | Y | YM |
| | The number of pixel clock periods in one line (row) time. This includes visible pixels and horizontal blanking time.<br>The minimum value supported is 0x56E. | | | | |
| 12302 R0x300E | 7:0 | 0x10 | revision_number (R/W) | N | N |
| | 7:4 | 0x0001 | Silicon revision | N | N |
| | 3:0 | 0x0000 | OTPM revision | N | N |
| 12304 R0x3010 | 15:0 | 0xBEEF | lock_control (R/W) | N | N |
| | This register protects the mirror mode select (register read mode).<br>When set to value 0xBEEF, the horizontal and vertical mirror modes can be changed, otherwise these values are locked. | | | | |
| 12306 R0x3012 | 15:0 | 0x0010 | coarse_integration_time (R/W) | Y | N |
| | Integration time specified in multiples of line_length_pck_. The minimum coarse integration time supported is 1 row time. | | | | |

**Table 2:** **Manufacturer-Specific Register Descriptions (continued)**
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

| Register Dec(Hex) | Bits | Default | Name | Frame Sync'd | Bad Frame |
|---|---|---|---|---|---|
| 12308 R0x3014 | 15:0 | 0x0000 | fine_integration_time (R/W) | Y | N |
| | \multicolumn{5}{l}{In linear ERS mode, fine integration is used to delay the reset operation. Thus, the integration time is decreased. The resolution is 1 pixel clock time. Maximum value for fine integration is line length pixel clocks - 611. Where 611 is the number of pixel clocks from the start of row to end of row reset.} | | | | |
| 12310 R0x3016 | 15:0 | 0x0010 | coarse_integration_time_cb (R/W) | N | N |
| | \multicolumn{5}{l}{Coarse integration time in context B.} | | | | |
| 12312 R0x3018 | 15:0 | 0x0000 | fine_integration_time_cb (R/W) | N | N |
| | \multicolumn{5}{l}{Fine integration time in context B.} | | | | |

**Table 2:** **Manufacturer-Specific Register Descriptions (continued)**
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

| Register Dec(Hex) | Bits | Default | Name | Frame Sync'd | Bad Frame |
|---|---|---|---|---|---|
| 12314 R0x301A | 15:0 | 0x0058 | reset_register (R/W) | N | Y |
| | 15 | 0x0000 | grouped_parameter_hold<br>0 = Update of many of the registers is synchronized to frame start.<br>1 = Inhibit register updates; register changes will remain pending until this bit is returned to 0. When this bit is returned to 0, all pending register updates will be made on the next frame start. | N | N |
| | 14:13 | X | Reserved | | |
| | 12 | 0x0000 | smia_serialiser_dis<br>This bit disables the serial (HISPI) interface | N | N |
| | 11 | 0x0000 | forced_pll_on<br>When set, enables the PLL immediately. | N | N |
| | 10 | 0x0000 | restart_bad<br>1 = a restart is forced any time a bad frame is detected. This can shorten the delay when waiting for a good frame, since the delay for masking out a bad frame will be the integration time rather than the full-frame time. | N | N |
| | 9 | 0x0000 | mask_bad<br>0 = The sensor will produce bad (corrupted) frames as a result of some register changes.<br>1 = Bad (corrupted) frames are masked within the sensor by extending the vertical blanking time for the duration of the bad frame. | N | N |
| | 8 | 0x0000 | gpi_en<br>0 = the primary input buffers associated with the OUTPUT_ENABLE_N, TRIGGER and STANDBY inputs are powered down and cannot be used.<br>1 = the input buffers are enabled and can be read through R0x3026-7. | N | N |
| | 7 | 0x0000 | parallel_en<br>0 = The parallel data interface (DOUT[11:0], LINE_VALID, FRAME_VALID, and PIXCLK) is disabled and the outputs are placed in a high-impedance state.<br>1 = The parallel data interface is enabled. The output signals can be switched between a driven and a high-impedance state using output-enable control. | N | N |
| | 6 | 0x0001 | drive_pins<br>0 = The parallel data interface (DOUT[11:0], LINE_VALID, FRAME_VALID, and PIXCLK) may enter a high-impedance state (depending upon the enabling and use of the pad OUTPUT_ENABLE_N)<br>1 = The parallel data interface is driven.<br>This bit is "do not care" unless bit[7]=1. | N | N |
| | 5 | 0x0000 | reg_rd_en<br>Enable signal to allow read from fuse ID registers. | N | N |
| | 4 | 0x0001 | stdby_eof<br>0 = Transition to standby is synchronized to the end of a sensor row readout (held-off until LINE_VALID has fallen).<br>1 = Transition to standby is synchronized to the end of a frame. | N | Y |
| | 3 | 0x0001 | lock_reg<br>Many parameter limitation registers that are specified as read-only are actually implemented as read/write registers. Clearing this bit allows such registers to be written. | N | N |

**Table 2:** **Manufacturer-Specific Register Descriptions (continued)**
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

| Register Dec(Hex) | Bits | Default | Name | Frame Sync'd | Bad Frame |
|---|---|---|---|---|---|
| | 2 | 0x0000 | stream<br>Setting this bit places the sensor in streaming mode. Clearing this bit places the sensor in a low power mode. The result of clearing this bit depends upon the operating mode of the sensor.<br>Entry and exit from streaming mode can also be controlled from the signal interface. | Y | N |
| | 1 | 0x0000 | restart<br>This bit always reads as 0. Setting this bit causes the sensor to truncate the current frame at the end of the current row and start resetting (integrating) the first row. The delay before the first valid frame is read out is equal to the integration time. | N | Y |
| | 0 | 0x0000 | reset<br>This bit always reads as 0. Setting this bit initiates a reset sequence: the frame being generated will be truncated. | N | Y |
| | | | Controls the operation of the sensor. For details see the bit field descriptions. | | |
| 12318<br>R0x301E | 15:0 | 0x00A8 | data_pedestal (R/W) | N | Y |
| | | | Constant offset that is added to pixel values at the end of data path (after all corrections). | | |
| 12326<br>R0x3026 | 15:0 | 0x0000 | gpi_status (RO) | N | N |
| | 15:4 | X | Reserved | | |
| | 3 | RO | standby<br>Read-only. Return the current state of the STANDBY input pin. Invalid if R0x301A-B[8]=0. | N | N |
| | 2 | RO | trigger<br>Read-only. Return the current state of the TRIGGER input pin. Invalid if R0x301A-B[8]=0. | N | N |
| | 1 | RO | oe_n<br>Read-only. Return the current state of the OUTPUT_ENABLE_N input pin. Invalid if R0x301A-B[8]=0. | N | N |
| | 0 | RO | saddr<br>Read-only. Return the current state of the pin S$_{ADDR}$ input pin.<br>This pad is not controlled by gpi_en. | N | N |
| | | | Reflects the status of the input pins:<br>STANDBY(3), TRIGGER(2), OUTPUT_ENABLE_N(1).<br>Bit 0 is not used. | | |
| 12328<br>R0x3028 | 15:0 | 0x0010 | row_speed (R/W) | N | N |
| | | | Bits [6:4] of this register define the phase of the output pixclk.<br>2 set of values are correct:<br>a) 000, 010, 100, 110 => 0 delay (rising edge of pixclk coincides DOUT change).<br>b) 001, 011, 101, 111 => 1/2 clk delay (falling edge of pixclk coincides DOUT change). | | |
| 12330<br>R0x302A | 15:0 | 0x0006 | vt_pix_clk_div (R/W) | N | N |
| | | | Sets the ratio of the serial output clock and sensor operation clock (P2 clock divider in PLL). | | |
| 12332<br>R0x302C | 15:0 | 0x0001 | vt_sys_clk_div (R/W) | N | N |
| | | | Sets the ratio of the VCO clk and the serial output clock (P1 divider in PLL). | | |
| 12334<br>R0x302E | 15:0 | 0x0002 | pre_pll_clk_div (R/W) | N | N |
| | | | Referring to the PLL documentation: shows the n+1 value. | | |

**Table 2: Manufacturer-Specific Register Descriptions (continued)**
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

| Register Dec(Hex) | Bits | Default | Name | Frame Sync'd | Bad Frame |
|---|---|---|---|---|---|
| 12336 R0x3030 | 15:0 | 0x002C | pll_multiplier (R/W) | N | N |
| | PLL_MULTIPLIER: shows 2m value. | | | | |
| 12338 R0x3032 | 15:0 | 0x0000 | digital_binning (R/W) | N | N |
| | 15:6 | X | Reserved | | |
| | 5:4 | 0x0000 | digital_binning_cb<br>SCALING_MODE for context B<br><br>00: No binning<br>01: Horizontal only binning<br>10: Horizontal and Vertical binning | N | N |
| | 3:2 | X | Reserved | | |
| | 1:0 | 0x0000 | digital_binning_ca<br>DIGITAL_BINNING for context A<br><br>00: No binning<br>01: Horizontal only binning<br>10: Horizontal and Vertical binning | N | N |
| 12346 R0x303A | 15:0 | 0xFFFF | frame_count (R/W) | N | N |
| | Counts the number of output frames. At the startup is initialized to 0xffff. | | | | |
| 12348 R0x303C | 15:0 | 0x0000 | frame_status (RO) | N | N |
| | 15:2 | X | Reserved | | |
| | 1 | RO | standby_status<br>This bit indicates that the sensor is in standby state. It can be polled after standby is entered to see when the real low-power state is entered; which can happen at the end of row or frame depending on bit R0x301A[4]. | N | N |
| | 0 | RO | framesync<br>Set on register write and reset on frame synchronization. Acts as debug flag to verify that register writes completed before last frame synchronization. | N | N |
| 12352 R0x3040 | 15:0 | 0x0000 | read_mode (R/W) | Y | YM |
| | 15 | 0x0000 | vert_flip<br>0: Normal readout<br>1: Readout is flipped (mirrored) vertically so that the row specified by y_addr_end_ is read out of the sensor first.<br><br>Changing this register can only be done when streaming is disabled | Y | YM |
| | 14 | 0x0000 | horiz_mirror<br>0: Normal readout<br>1: Readout is mirrored horizontally so that the column specified by x_addr_end_ is read out of the sensor first.<br><br>Changing this register can only be done when streaming is disabled | Y | YM |
| | 13:0 | X | Reserved | | |

**Table 2:** **Manufacturer-Specific Register Descriptions (continued)**
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

| Register Dec(Hex) | Bits | Default | Name | Frame Sync'd | Bad Frame |
|---|---|---|---|---|---|
| 12356 R0x3044 | 15:0 | 0x0000 | dark_control (R/W) | N | N |
| | 15 | 0x0000 | show_reset_level<br>1: The digital CDS is disabled and reset level is output. | Y | N |
| | 14 | 0x0000 | show_signal_level<br>1: Disables digital CDS and outputs the signal level.<br>0: The signal minus reset level is output. | Y | N |
| | 13 | 0x0000 | cancel_tx_frame<br>Disables TX during sampling to produce a complete dark image. | N | N |
| | 12 | 0x0000 | show_colcorr_rows<br>When set, the column correction rows and delta dark rows (including guard rows) will be included in FV and output.<br>The order of output rows will be:<br>column correction rows, delta dark rows, embedded data, image.<br>No correction (except offset correction and gain equalization when AGS enabled) will be applied to the data. | N | N |
| | 11 | 0x0000 | show_dark_extra_rows<br>When set, the delta dark rows (including guard rows) will be included in FV and output.<br>The order of output rows will be:<br>delta dark rows, embedded data, image.<br>No correction (except offset correction and gain equalization when AGS enabled) will be applied to the data. | N | N |
| | 10 | 0x0000 | row_noise_correction_en<br>0: Row-noise cancellation algorithm is disabled.<br>1: Row-noise cancellation algorithm is enabled. | N | N |
| | 9 | 0x0000 | show_dark_cols<br>When set, dark columns (tied) used for row noise correction are included to LV and output.<br>No correction (except offset correction and gain equalization when AGS enabled) will be applied to the data. Displaying dark columns can only be enabled if x_addr_start is set to 0 | N | N |
| | 8 | X | Reserved | | |
| | 7 | 0x0000 | show_zebra_test_rows<br>When set, the zebra test rows are included in FV (after stats data rows) and will be output.<br>No correction (except offset correction and gain equalization when AGS enabled) will be applied to the data. | N | N |
| | 6:4 | X | Reserved | | |
| | 3 | 0x0000 | physical_addressing<br>Enables physical addressing. | N | N |
| | 2 | 0x0000 | cancel_tx_col_corr<br>Enables canceling of TX pulse when in column correction rows. | N | N |
| | 1:0 | X | Reserved | | |

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**Table 2:     Manufacturer-Specific Register Descriptions (continued)**
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

| Register Dec(Hex) | Bits | Default | Name | Frame Sync'd | Bad Frame |
|---|---|---|---|---|---|
| 12358 R0x3046 | 15:0 | 0x0000 | flash (R/W) | Y | Y |
| | 15 | RO | strobe<br>Reflects the current state of the FLASH output signal. Read-only. | N | N |
| | 14 | RO | triggered<br>Indicates that the FLASH output signal was asserted for the current frame. Read-only. | N | N |
| | 13:9 | X | Reserved | | |
| | 8 | 0x0000 | en_flash<br>Enables the flash.<br>The flash is asserted when an integration (either T1, T2 or T3 is ongoing). | Y | Y |
| | 7 | 0x0000 | invert_flash<br>Invert flash output signal. When set, the FLASH output signal will be active low. | N | N |
| | 6:0 | X | Reserved | | |
| 12374 R0x3056 | 15:0 | 0x0020 | green1_gain (R/W) | Y | N |
| | Digital gain for green1 (Gr) pixels, in format of xxx.yyyyy. | | | | |
| 12376 R0x3058 | 15:0 | 0x0020 | blue_gain (R/W) | Y | N |
| | Digital gain for Blue pixels, in format of xxx.yyyyy. | | | | |
| 12378 R0x305A | 15:0 | 0x0020 | red_gain (R/W) | Y | N |
| | Digital gain for Red pixels, in format of xxx.yyyyy. | | | | |
| 12380 R0x305C | 15:0 | 0x0020 | green2_gain (R/W) | Y | N |
| | Digital gain for green2 (Gb) pixels in format of xxx.yyyyy. | | | | |
| 12382 R0x305E | 15:0 | 0x0020 | global_gain (R/W) | Y | N |
| | Writing a gain to this register is equivalent to writing that code to each of the 4 color-specific gain registers. Reading from this register returns the value most recently written to the green1_gain register. | | | | |
| 12388 R0x3064 | 15:0 | 0x1982 | embedded_data_ctrl (R/W) | N | N |
| | 15:13 | X | Reserved | | |
| | 12 | 0x0001 | Reserved | | |
| | 11:10 | 0x0002 | Reserved | | |
| | 9 | 0x0000 | Reserved | | |
| | 8 | 0x0001 | embedded_data<br>0: Frames out of the sensor exclude the embedded data.<br>1: Frames of data out of the sensor include 2 rows of embedded data. This register field should only be change while the sensor is in software standby. | N | N |
| | 7 | 0x0001 | embedded_stats_en<br>Enables two rows of statistical data (used by external AE, ..) after the transmission image data. Can not be enabled unless EMBEDDED_DATA_EN is enabled. | N | Y |
| | 6:4 | X | Reserved | | |
| | 3:0 | 0x0002 | Reserved | | |

**Table 2:** **Manufacturer-Specific Register Descriptions (continued)**
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

| Register Dec(Hex) | Bits | Default | Name | Frame Sync'd | Bad Frame |
|---|---|---|---|---|---|
| 12398 R0x306E | 15:0 | 0x9210 | datapath_select (R/W) | N | N |
| | 15:13 | 0x0004 | slew_rate_ctrl_parallel<br>Selects the slew (edge) rate for the DOUT[9:0], FRAME_VALID, LINE_VALID and FLASH outputs. Only affects the FLASH output when parallel data output is disabled. The value 7 results in the fastest edge rates on these signals. Slowing down the edge rate can reduce ringing and electro-magnetic emissions. | N | N |
| | 12:10 | 0x0004 | slew_rate_ctrl_pixclk<br>Selects the slew (edge) rate for the PIXCLK output. Has no effect when parallel data output is disabled. The value 7 results in the fastest edge rates on this signal. Slowing down the edge rate can reduce ringing and electromagnetic emissions. | N | N |
| | 9 | 0x0001 | high_vcm<br>0: For SLVS low vcm, $V_{DD}$_SLVS must be 0.4V<br>1: For sub-SLVS high vcm, $V_{DD}$_SLVS = $V_{DD}$_IO = 1.8V | N | N |
| | 8 | 0x0000 | postscaler_data_sel<br>0: Statistics data are generated from pixel data before scaler.<br>1: Statistics data are generated from pixel data after scaler. | N | N |
| | 7:5 | X | Reserved | | |
| | 4 | 0x0001 | true_bayer<br>Enables true Bayer scaling mode. | N | N |
| | 3:2 | X | Reserved | | |
| | 1:0 | 0x0000 | special_line_valid<br>00: Normal behavior of LINE_VALID<br>01: LINE_VALID is driven continuously (continue generating LINE_VALID during vertical blanking)<br>10: LINE_VALID is driven continuously as LINE_VALID XOR FRAME_VALID | N | N |
| 12400 R0x3070 | 15:0 | 0x0000 | test_pattern_mode (R/W) | N | Y |
| | 0: Normal operation. Generate output data from pixel array<br>1: Solid color test pattern<br>2: Full color bar test pattern<br>3: Fade to gray color bar test pattern<br>256: Walking 1 test pattern (12 bit)<br>Other = Reserved. | | | |
| 12402 R0x3072 | 15:0 | 0x0000 | test_data_red (R/W) | N | Y |
| | The value for red pixels in the Bayer data used for the solid color test pattern and the test cursors. | | | |
| 12404 R0x3074 | 15:0 | 0x0000 | test_data_greenr (R/W) | N | Y |
| | The value for green pixels in red/green rows of the Bayer data used for the solid color test pattern and the test cursors. | | | |
| 12406 R0x3076 | 15:0 | 0x0000 | test_data_blue (R/W) | N | Y |
| | The value for blue pixels in the Bayer data used for the solid color test pattern and the test cursors. | | | |
| 12408 R0x3078 | 15:0 | 0x0000 | test_data_greenb (R/W) | N | Y |
| | The value for green pixels in blue/green rows of the Bayer data used for the solid color test pattern and the test cursors. | | | |

**Table 2:** **Manufacturer-Specific Register Descriptions (continued)**
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

| Register Dec(Hex) | Bits | Default | Name | Frame Sync'd | Bad Frame |
|---|---|---|---|---|---|
| 12410 R0x307A | 15:0 | 0x0000 | test_raw_mode (R/W) | N | N |
| | 15:2 | X | Reserved | | |
| | 1 | 0x0000 | Reserved | | |
| | 0 | 0x0000 | Reserved | | |
| 12412 R0x307C | 15:0 | 0x0000 | exposure_t2 (RO) | N | N |
| | T2 exposure time in rows. | | | | |
| 12416 R0x3080 | 15:0 | 0x0000 | exposure_t3 (RO) | N | N |
| | Actual T3 time in pixel clocks. Read only. | | | | |
| 12418 R0x3082 | 15:0 | 0x0029 | operation_mode_ctrl (R/W) | N | Y |
| | 15:6 | X | Reserved | | |
| | 5:4 | 0x0002 | ratio_t2_t3<br>Requested integration time ratio (T2 to T3):<br>00: 4<br>01: 8<br>10: 16<br>11: 32 | N | Y |
| | 3:2 | 0x0002 | ratio_t1_t2<br>Requested integration time ratio (T1 t0 T2):<br>00: 4<br>01: 8<br>10: 16<br>11: 32 | N | Y |
| | 1:0 | 0x0001 | operation_mode<br>00: Not valid.<br>01: ERS Linear mode<br>10: Not valid.<br>11: Not valid. | N | Y |
| 12420 R0x3084 | 15:0 | 0x0000 | operation_mode_ctrl_cb (R/W) | N | N |
| | 15:6 | X | Reserved | | |
| | 5:4 | 0x0000 | ratio_t2_t3_cb<br>RATIO_T2_T3_CB | N | N |
| | 3:2 | 0x0000 | ratio_t1_t2_cb<br>RATIO_T1_T2_CB | N | N |
| | 1:0 | X | Reserved | | |
| 12422 R0x3086 | 15:0 | 0x0000 | seq_data_port (R/W) | N | N |
| | Register used to write to or read from the sequencer RAM. | | | | |

**Table 2: Manufacturer-Specific Register Descriptions (continued)**
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

| Register Dec(Hex) | Bits | Default | Name | Frame Sync'd | Bad Frame |
|---|---|---|---|---|---|
| 12424 R0x3088 | 15:0 | 0xC000 | seq_ctrl_port (R/W) | N | N |
| | 15 | RO | sequencer_stopped<br>Showing that sequencer is stopped (STANDBY mode) and the RAM is available for read or write. | N | N |
| | 14 | 0x0001 | auto_inc_on_read<br>If 1 => The access_address is incremented (by 1) after each read operation from seq_data_port (which returns only1 byte) | N | N |
| | 13:9 | X | Reserved | | |
| | 8:0 | 0x0000 | access_address<br>When in STANDBY (not streaming) mode: address pointer to the sequencer RAM. | N | N |
| | | | Register controlling the read and write to sequencer RAM. | | |
| 12426 R0x308A | 15:0 | 0x0000 | x_addr_start_cb (R/W) | N | N |
| | | | x_address_start context B | | |
| 12428 R0x308C | 15:0 | 0x0002 | y_addr_start_cb (R/W) | N | N |
| | | | Y_ADDR_START for context B | | |
| 12430 R0x308E | 15:0 | 0x0503 | x_addr_end_cb (R/W) | N | N |
| | | | X_ADDR_END for context B | | |
| 12432 R0x3090 | 15:0 | 0x03C5 | y_addr_end_cb (R/W) | N | N |
| | | | Y_ADDR_END for context B | | |
| 12448 R0x30A0 | 15:0 | 0x0001 | x_even_inc (RO) | N | N |
| | | | Read-only. | | |
| 12450 R0x30A2 | 15:0 | 0x0001 | x_odd_inc (R/W) | Y | YM |
| | | | Not used. Do not change. | | |
| 12452 R0x30A4 | 15:0 | 0x0001 | y_even_inc (RO) | N | N |
| | | | Read-only. | | |
| 12454 R0x30A6 | 15:0 | 0x0001 | y_odd_inc (R/W) | Y | YM |
| | | | Not supported. Do not change. | | |
| 12456 R0x30A8 | 15:0 | 0x0001 | y_odd_inc_cb (R/W) | N | N |
| | | | Y_ODD_INC context B | | |
| 12458 R0x30AA | 15:0 | 0x03DE | frame_length_lines_cb (R/W) | N | N |
| | | | FRAME_LENGTH_LINES context B.<br>See description for R0x3012 | | |
| 12460 R0x30AC | 15:0 | 0x0010 | exposure_t1 (RO) | N | N |
| | | | Shows the t1 exposure time in HDR mode (in rows) and not used in linear mode. | | |

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**Table 2: Manufacturer-Specific Register Descriptions (continued)**
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

| Register Dec(Hex) | Bits | Default | Name | Frame Sync'd | Bad Frame |
|---|---|---|---|---|---|
| 12464 R0x30B0 | 15:0 | 0x1000 | digital_test (R/W) | N | Y |
| | 15 | 0x0000 | Reserved | | |
| | 14 | 0x0000 | pll_complete_bypass<br>When set, the EXTCLK will be used and PLL will be bypassed. Note that the serial interface would not function. | N | N |
| | 13 | 0x0000 | context_b<br>0: Use context A<br>1: Use Context B | N | N |
| | 12:10 | 0x0004 | zebra_test_row_nr<br>Number of the zebra test rows. | N | N |
| | 9:8 | 0x0000 | col_gain_cb<br>Column gain for Context B | N | N |
| | 7 | 0x0000 | mono_chrome<br>When set the CFA is mono chrome and not color. Some features like skipping and corrections are affected. | N | N |
| | 6 | 0x0000 | ags_enable<br>When set, AGS is enabled. | N | N |
| | 5:4 | 0x0000 | col_gain<br>Column gain:<br>00: 1<br>01: 2<br>10: 4<br>11: 8 | N | N |
| | 3 | X | Reserved | | |
| | 2 | 0x0000 | ags_enable_t2<br>When set, AGS is enabled for T2. | N | N |
| | 1 | 0x0000 | no_sh_jump_limit<br>When set, prevents logic from limiting the shutter increase. Normally shutter increase is limited to 4 *(ratio_t1_t2).<br>To ensure this mode operate correctly, the frame_length_lines must be increased by 52 more than needed (meaning that VB is increased by 52). | N | N |
| | 0 | X | Reserved | | |
| 12466 R0x30B2 | 15:0 | 0x0000 | tempsens_data (R/W) | Y | N |
| | | | Output value from temperature sensor. | | |

**Table 2:** **Manufacturer-Specific Register Descriptions (continued)**
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

| Register Dec(Hex) | Bits | Default | Name | Frame Sync'd | Bad Frame |
|---|---|---|---|---|---|
| 12468 R0x30B4 | 15:0 | 0x0000 | tempsens_ctrl (R/W) | N | N |
| | 15:6 | X | Reserved | | |
| | 5 | 0x0000 | temp_clear_value<br>Clear data register (sanity check). | N | N |
| | 4 | 0x0000 | temp_start_conversion<br>When asserted, a new temp value will be generated for each frame capture. When asserted in standby mode, a new temp value will be generated. | N | N |
| | 3:1 | 0x0000 | tempsens_test_ctrl<br>Temp sensor test modes:<br>0: Normal operation<br>1d: Vb output on vtest_in_out<br>2d: Vctat output on vtest_in_out<br>3d: ADC conversion w/vtest_in_out replacing Vctat<br>4d: ADC conversion w/vtest_in_out replacing both Vctat and Vbg (expected output is zero). | N | N |
| | 0 | 0x0000 | tempsens_power_on<br>tempsens_power_on | N | N |
| | | | Control register for temperature sensor | | |
| 12474 R0x30BA | 15:0 | 0x0003 | digital_ctrl (R/W) | Y | N |
| | 15:5 | X | Reserved | | |
| | 4 | 0x0000 | dcds_mode<br>When set (=1) DCDS mode enabled. | N | N |
| | 3 | 0x0000 | colcorr_correct_always<br>1: Column FPN correction is applied also during collection and re-calculation of new column FPN correction values. | N | N |
| | 2 | 0x0000 | Reserved | | |
| | 1 | 0x0001 | enable_ags_colcorr_retrigg<br>When set the AGS (analog/ column gain) change will retrigger the column FPN correction algorithm. | Y | N |
| | 0 | 0x0001 | enable_dcg_colcorr_retrigg<br>When set, a DCG change will retrigger the column FPN correction algorithm. | Y | N |
| 12476 R0x30BC | 15:0 | 0x0020 | green1_gain_cb (R/W) | N | N |
| | | | Digital gain green1 context B | | |
| 12478 R0x30BE | 15:0 | 0x0020 | blue_gain_cb (R/W) | N | N |
| | | | digital gain blue context B | | |
| 12480 R0x30C0 | 15:0 | 0x0020 | red_gain_cb (R/W) | N | N |
| | | | digital gain red context B | | |
| 12482 R0x30C2 | 15:0 | 0x0020 | green2_gain_cb (R/W) | | |
| | | | digital gain green 2 context B | | |
| 12484 R0x30C4 | 15:0 | 0x0020 | global_gain_cb (R/W) | N | N |
| | | | global digital gain context B | | |
| 12486 R0x30C6 | 15:0 | 0x0123 | tempsens_calib1 (R/W) | | |

**Table 2: Manufacturer-Specific Register Descriptions (continued)**
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

| Register Dec(Hex) | Bits | Default | Name | Frame Sync'd | Bad Frame |
|---|---|---|---|---|---|
| 12488 R0x30C8 | 15:0 | 0x4567 | tempsens_calib2 (R/W) | N | N |
| 12490 R0x30CA | 15:0 | 0x89AB | tempsens_calib3 (R/W) | N | N |
| 12492 R0x30CC | 15:0 | 0xCDEF | tempsens_calib4 (R/W) | N | N |
| 12500 R0x30D4 | 15:0 | 0xC007 | column_correction (R/W) | N | N |
| | 15 | 0x0001 | enable<br>Enable column correction. | N | N |
| | 14 | 0x0001 | double_range<br>Double the range of the correction value but halves the precision. | N | N |
| | 13 | 0x0000 | double_samples<br>Makes the column correction use 128 rows instead of 64. Adds 64 to the minimum frame blanking. | N | N |
| | 12:4 | X | Reserved | | |
| | 3:0 | 0x0007 | colcorr_rows<br>value showing the number of column correction rows - 1. | N | N |
| 12522 R0x30EA | 15:0 | 0x0C00 | gain_offset_ctrl (R/W) | N | N |
| | 15 | 0x0000 | Reserved | | |
| | 14 | 0x0000 | Reserved | | |
| | 13 | 0x0000 | Reserved | | |
| | 12 | 0x0000 | Reserved | | |
| | 11 | 0x0001 | Reserved | | |
| | 10 | 0x0001 | Reserved | | |
| | 9 | X | Reserved | | |
| | 8:0 | 0x0000 | Reserved | | |

**Table 2:     Manufacturer-Specific Register Descriptions (continued)**
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

| Register Dec(Hex) | Bits | Default | Name | Frame Sync'd | Bad Frame |
|---|---|---|---|---|---|
| 12544 R0x3100 | 15:0 | 0x0000 | ae_ctrl_reg (R/W) | | |
| | 15:8 | X | Reserved | | |
| | 7 | 0x0000 | dcg_manual_set_cb<br>Manual dcg value used in context B. | N | N |
| | 6:5 | 0x0000 | min_ana_gain<br>Minimum analog gain to be used by AE.<br>00: 1x (default)<br>01: 2x<br>10: 4x<br>11: 8x | N | N |
| | 4 | 0x0000 | auto_dg_en<br>Automatic control of digital gain by AE is enabled. | N | N |
| | 3 | 0x0000 | auto_dcg_enable<br>Enables automatic (AE controlled) DCG control. | N | N |
| | 2 | 0x0000 | dcg_manual_set<br>If AE is disabled or automatic DCG is disabled, this bit will be used to decide the DCG gain.<br>0: Low gain.<br>1: High gain. | N | N |
| | 1 | 0x0000 | auto_ag_en<br>When set, enables the automatic ae control of analogue gain. | N | N |
| | 0 | 0x0000 | ae_enable<br>1: Enables the on-chip AE algorithm | N | N |
| 12546 R0x3102 | 15:0 | 0x1770 | ae_luma_target_reg (R/W) | N | N |
| | Average luma target value to be reached by the auto exposure | | | | |
| 12548 R0x3104 | 15:0 | 0xC000 | ae_hist_target_reg (R/W) | | |
| | Histogram high end target / 16 | | | | |
| 12550 R0x3106 | 15:0 | 0x7333 | ae_hysteresis_reg (R/W) | | |
| | Hysteresis coefficient for histogram high end exposure ratio. Calculation of default value: Hysteresis * 32768 = 0.9 *32768 = 29491 = 0x7333. | | | | |
| 12552 R0x3108 | 15:0 | 0x0010 | ae_min_ev_step_reg (R/W) | | |
| | Minimum exposure value step size<br>[15:8]: Reserved<br>[7:0] : Min_EV_stepsize = (min step size)*256.<br>Since Min_EV_stip sizes are small and they are typically less than 1 e.g. 1/16, 7/16 etc... these are multiplied by 256 and then the value is written to this register. | | | | |
| 12554 R0x310A | 15:0 | 0x0002 | ae_max_ev_step_reg (R/W) | | |
| | Maximum exposure value step size.<br>Note that since this value is always greater than 1 there is no need to multiply by 256 as in the case of min_EV_stepsize. | | | | |
| 12556 R0x310C | 15:0 | 0x0010 | ae_damp_offset_reg (R/W) | | |
| | Adjusts step size and settling speed. | | | | |
| 12558 R0x310E | 15:0 | 0x0010 | ae_damp_gain_reg (R/W) | | |
| | Adjusts step size and settling speed. | | | | |

**Table 2:** **Manufacturer-Specific Register Descriptions (continued)**
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

| Register Dec(Hex) | Bits | Default | Name | Frame Sync'd | Bad Frame |
|---|---|---|---|---|---|
| 12560 R0x3110 | 15:0 | 0x00E0 | ae_damp_max_reg (R/W) | | |
| | | | Max value allowed for recursiveDamp (multiplied by 256 since internal value is typical <1). For most applications, the value of recursiveDamp should be <1, otherwise AE will overshoot the target. For applications with fast settling required, it may be desirable to allow recursiveDamp >1. Default value: 0.875 * 256 = 0x00E0 | | |
| 12562 R0x3112 | 15:0 | 0x2800 | ae_dcg_exposure_high_reg (R/W) | | |
| | | | Integration time above which AE (if enabled) switches to DCG high gain. The value must be greater than: AEDCGGAINFACTOR (reg 0x3114) * AEDCGEXPOSURELOW (reg. 0x3116) | | |
| 12564 R0x3114 | 15:0 | 0x0800 | ae_dcg_exposure_high_reg (R/W) | | |
| | | | Integration time below which AE (if enabled) switches to DCG lo gain. | | |
| 12566 R0x3116 | 15:0 | 0x0400 | ae_dcg_gain_factor_reg (R/W) | | |
| | | | Ratio gain between DCG Hi and DCG Lo (multiplied by 256). Tuned to match the DCG gain characteristics of the sensor. | | |
| 12568 R0x3118 | 15:0 | 0x0040 | ae_dcg_gain_factor_inv_reg (R/W) | N | N |
| | | | Inverse of gain ratio between DCG Hi and DCG Lo (multiplied by 256). Tuned to match the DCG gain characteristics of the sensor. | | |
| 12572 R0x311C | 15:0 | 0x02A0 | ae_max_exposure_reg (R/W) | N | N |
| | | | Maximum integration (exposure) time in rows to be used by AE. | | |
| 12574 R0x311E | 15:0 | 0x0001 | ae_min_exposure_reg (R/W) | N | N |
| | | | Minimum integration (exposure) time in rows to be used by AE. | | |
| 12576 R0x3120 | 15:0 | 0x0064 | ae_low_mean_target_reg (R/W) | N | N |
| | | | Target value for low end mean (LEM). A means to specify how much of the dark region may be sacrificed and at what point the dark region is considered sacrificed. The chosen point at which the dark region is considered sacrificed will vary based on the user's desired minimum SNR. This choice is set using the LEM_min parameter. The perc_lowEnd_thresh parameter specifies what percentage of pixels may be ignored in the histogram low end. If the percentage of low end pixels exceeds perc_lowEnd_thresh, the minimum acceptable low end mean parameter (LEM_min) is applied. This forces the histogram to increase exposure until the minimum low end mean is met. | | |
| 12578 R0x3122 | 15:0 | 0x0F5C | ae_hist_low_thresh_reg (R/W) | N | N |
| | | | Percentage of pixels that must be in the histogram low end before low end mean limiting is applied. Percentage * 65536. Default: 6% * 65536 = 3932 = 0x0F5C | | |
| 12580 R0x3124 | 15:0 | 0x7FFF | ae_dark_cur_thresh_reg (R/W) | | |
| | | | The dark current level that stops AE from increasing integration time. Note that increased integration time would increase dark current as well and signal level (SNR) would drop because photo diode well capacity is limited. | | |
| 12582 R0x3126 | 15:0 | 0x0050 | ae_alpha_v1_reg (R/W) | N | N |
| | | | Alpha V1 coefficient weighting of mean and hist end targets. | | |
| 12584 R0x3128 | 15:0 | 0x04EC | ae_alpha_coef_reg (R/W) | | |
| | | | Slope ratio for alpha calculation [1/(v2-v1)]*128 Alpha coefficient is a weighting of mean and hist end targets. | | |

**Table 2: Manufacturer-Specific Register Descriptions (continued)**
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

| Register Dec(Hex) | Bits | Default | Name | Frame Sync'd | Bad Frame |
|---|---|---|---|---|---|
| 12586 R0x312A | 15:0 | 0x0020 | ae_current_gains (RO) | N | N |
| | 15:11 | X | Reserved | | |
| | 10 | RO | ae_conv_gain<br>The gain decided by AE, when it is enabled and can control the conversion gain. | N | N |
| | 9:8 | RO | ae_ana_gain<br>The gain decided by AE, when it is enabled and can control the analogue gain. | N | N |
| | 7:0 | RO | ae_dig_gain<br>The gain decided by AE, when it is enabled and can control the digital gain. | N | N |
| | Shows the gain settings decided by AE. | | | | |
| 12608 R0x3140 | 15:0 | 0x0000 | ae_roi_x_start_offset (R/W) | N | N |
| | Number of pixels into each row before the ROI starts<br>NOTE: if statistics are being gathered from a scaled image then the 'number of pixels' value must be the number of scaled pixels | | | | |
| 12610 R0x3142 | 15:0 | 0x0000 | ae_roi_y_start_offset (R/W) | N | N |
| | Number of rows into each frame before the ROI starts | | | | |
| 12612 R0x3144 | 15:0 | 0x0504 | ae_roi_x_size (R/W) | N | N |
| | Number of columns in the ROI | | | | |
| 12614 R0x3146 | 15:0 | 0x03C4 | ae_roi_y_size (R/W) | N | N |
| | Number of rows in the ROI | | | | |
| 12616 R0x3148 | 15:0 | 0x0290 | ae_hist_begin_perc (R/W) | | |
| | Defines the percentage of Gr pixels that must have values below hist_begin. Specified as a number < 1 = 0.xx...xx | | | | |
| 12618 R0x314A | 15:0 | 0xFFFF | ae_hist_end_perc (R/W) | N | N |
| | Defines the percentage of Gr pixels that must have values below hist_end. Specified as a number < 1 = 0.xx...xx. A value of all 1s is treated as a special case and equates to 1.0 (100%) | | | | |
| 12620 R0x314C | 15:0 | 0x0100 | ae_hist_div (R/W) | N | N |
| | Defines the point at which the histogram is divided into the low and high end. Boundary value = hist_div*16 | | | | |
| 12622 R0x314E | 15:0 | 0x0020 | ae_norm_width_min (R/W) | N | N |
| | Defines the minimum histogram width normalization factor (=norm_width_min*16), for norm_abs_dev calculation. A value of all 1s turns off the norm_width_min option i.e.,. all absolute deviation is normalized by hist_end - hist_begin | | | | |
| 12624 R0x3150 | 15:0 | 0x0000 | ae_mean_h (RO) | | |
| | The true mean of all Gr pixels in the ROI (higher bits) | | | | |
| 12626 R0x3152 | 15:0 | 0x0000 | ae_mean_l (RO) | | |
| | The true mean of all Gr pixels in the ROI (16 least significant bits) | | | | |
| 12628 R0x3154 | 15:0 | 0x0000 | ae_hist_begin_h (RO) | N | N |
| | Code value corresponding to the histogram bin below which(hist_begin_perc*100)% of pixels exist (higher bits) | | | | |
| 12630 R0x3156 | 15:0 | 0x0000 | ae_hist_begin_l (RO) | | |
| | Code value corresponding to the histogram bin below which (hist_begin_perc*100)% of pixels exist (lower 16 bits) | | | | |

**Table 2: Manufacturer-Specific Register Descriptions (continued)**
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

| Register Dec(Hex) | Bits | Default | Name | Frame Sync'd | Bad Frame |
|---|---|---|---|---|---|
| 12632 R0x3158 | 15:0 | 0x0000 | ae_hist_end_h (RO) | N | N |
| | | | Code value corresponding to the histogram bin below which(hist_end_perc*100)% of pixels exist (higher bits) | | |
| 12634 R0x315A | 15:0 | 0x0000 | ae_hist_end_l (RO) | N | N |
| | | | Code value corresponding to the histogram bin below which(hist_end_perc*100)% of pixels exist (lower 16 bits) | | |
| 12636 R0x315C | 15:0 | 0x0000 | ae_hist_end_mean_h (RO) | N | N |
| | | | The true mean of all Gr pixels in the ROI that fall into the low end of the histogram (where low end is defined by hist_div) (higher bits) | | |
| 12638 R0x315E | 15:0 | 0x0000 | ae_hist_end_mean_l (RO) | N | N |
| | | | The true mean of all Gr pixels in the ROI that fall into the low end of the histogram (where low end is defined by hist_div) (lower 16 bits) | | |
| 12640 R0x3160 | 15:0 | 0x0000 | ae_perc_low_end (RO) | N | N |
| | | | Percentage of Gr pixels in ROI that fall into the low end of the histogram. Specified as a number < 1 = 0.xx...xxx | | |
| 12642 R0x3162 | 15:0 | 0x0000 | ae_norm_abs_dev (RO) | N | N |
| | | | Percentage of Gr pixels in ROI that fall into the low end of the histogram. Specified as a number < 1 = 0.xx...xxx | | |
| 12644 R0x3164 | 15:0 | 0x0001 | ae_coarse_integration_time (RO) | N | N |
| | | | The integration time decided by AE. | | |
| 12646 R0x3166 | 15:0 | 0x029F | ae_ag_exposure_hi (R/W) | N | N |
| | | | At this integration time, the analog gain is increased (when AE is enabled to control also the analog gain). | | |
| 12648 R0x3168 | 15:0 | 0x0118 | ae_ag_exposure_lo (R/W) | N | N |
| | | | At this integration time, the AE is reduced (when AE is enabled to control the analog gain also), | | |
| 12650 R0x316A | 15:0 | 0x0200 | ae_ag_gain1 (R/W) | N | N |
| | | | Real gain ratio between analog gain 0 and 1. | | |
| 12652 R0x316C | 15:0 | 0x0200 | ae_ag_gain2 (R/W) | N | N |
| | | | The real gain ratio between analog gain 2 and 1. | | |
| 12654 R0x316E | 15:0 | 0x0200 | ae_ag_gain3 (R/W) | N | N |
| | | | The real gain ratio between analog gain2 and gain3. | | |
| 12656 R0x3170 | 15:0 | 0x0080 | ae_inv_ag_gain1 (R/W) | | |
| | | | The real inverse gain ratio between  analog gain 0 and 1. | | |
| 12658 R0x3172 | 15:0 | 0x0080 | ae_inv_ag_gain2 (R/W) | N | N |
| | | | The real inverse gain ratio (1 to 2). | | |
| 12660 R0x3174 | 15:0 | 0x0080 | ae_inv_ag_gain3 (R/W) | | |
| | | | The real inverse gain ratio (2 to 3). | | |

**Table 2:** **Manufacturer-Specific Register Descriptions (continued)**
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

| Register Dec(Hex) | Bits | Default | Name | Frame Sync'd | Bad Frame |
|---|---|---|---|---|---|
| 12672 R0x3180 | 15:0 | 0x8000 | delta_dk_control (R/W) | | |
| | 15 | 0x0001 | delta_dk_sub_en<br>Enabling the delta dark correction. | N | N |
| | 14 | 0x0000 | delta_dk_every_frame<br>Runnig the delta dark algorithm every frame or when gain, integration time is changing. | N | N |
| | 13 | 0x0000 | delta_dk_clip_en<br>Enables the clipping of dark current. If the measured dark current is higher than clip level, only the clip level is used. See register 0x3182. | N | N |
| | 12 | 0x0000 | Reserved | | |
| | 11:0 | X | Reserved | | |
| 12674 R0x3182 | 15:0 | 0x7FFF | delta_dk_clip (R/W) | N | N |
| | Clip level for measured dark level. | | | | |
| 12676 R0x3184 | 15:0 | 0x0000 | delta_dk_t1 (RO) | N | N |
| | Measured dark current for exposure T1 | | | | |
| 12678 R0x3186 | 15:0 | 0x0000 | delta_dk_t2 (RO) | N | N |
| | Measured dark current for exposure T2 | | | | |
| 12680 R0x3188 | 15:0 | 0x0000 | delta_dk_t3 (RO) | N | N |
| | Measured dark current for exposure T3 | | | | |
| 12682 R0x318A | 15:0 | 0x0FA0 | hdr_mc_ctrl1 (R/W) | N | N |
| | 15:12 | X | Reserved | | |
| | 11:0 | 0x0FA0 | s2_threshold | N | N |
| 12684 R0x318C | 15:0 | 0x0040 | hdr_mc_ctrl2 (R/W) | N | N |
| | 15 | 0x0000 | mc_noise_filter_en | N | N |
| | 14 | 0x0000 | motion_correction_en<br>0: Disable motion detection and correction<br>1: Enable motion detection and correction | N | N |
| | 13:12 | 0x0000 | bypass_pix_comb<br>00: Smooth combination of three components.<br>01: T1 data<br>10: T2 data<br>11: T3 data | N | N |
| | 11:0 | 0x0040 | mc_diff_threshold | N | N |

**Table 2:** **Manufacturer-Specific Register Descriptions (continued)**
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

| Register Dec(Hex) | Bits | Default | Name | Frame Sync'd | Bad Frame |
|---|---|---|---|---|---|
| 12686 R0x318E | 15:0 | 0x0110 | hdr_mc_ctrl3 (R/W) | N | N |
| | 15:14 | 0x0000 | pixel_build_mode_cb<br>00: Normal hdr pixel build<br>01: Discard t3_data ie. region 4 or 5 data treated as region 3<br>10: Discard t2_data and t3_data, i.e., all data treated as region 1<br>11: Discard t1_data and t2_data, i.e., all data treated as region 5 | N | N |
| | 13:12 | 0x0000 | pixel_build_mode<br>00: Normal HDR pixel build<br>01: Discard t3_data ie. region 4 or 5 data treated as region 3<br>10: Discard t2_data and t3_data, i.e., all data treated as region 1<br>11 : Discard t1_data and t2_data, i.e., all data treated as region 5 | N | N |
| | 11:10 | X | Reserved | | |
| | 9 | 0x0000 | motion2_en<br>0: Motion type 2 is ignored when detecting motion<br>1: Motion type 2 is considered when detecting motion | N | N |
| | 8 | 0x0001 | motion_correct_2d_en<br>0: Perform 1D motion detection and correction (if motion_correction_en = 1)<br>1: Perform 2D motion detection and correction (if motion_correction_en = 1) | N | N |
| | 7:0 | 0x0010 | mc_count_threshold | N | N |
| 12688 R0x3190 | 15:0 | 0x4BA0 | hdr_mc_ctrl4 (R/W) | N | N |
| | 15 | 0x0000 | noise_filter_dlo_quad<br>0: Linear weighting function for the digital lateral overflow noise filter.<br>1: Quadratic weighting function for the digital lateral overflow noise filter. | N | N |
| | 14 | 0x0001 | noise_filter_dlo_en<br>Enable noise filtering in the digital lateral overflow pixel combination. | N | N |
| | 13 | 0x0000 | pixel_build_dlo<br>0: Use the smooth combination method for combining t1, t2 and t3 data.<br>1: Use the digital lateral overflow method for combining t1, t2 and t3 data. This also overrides R0x318c[14], MOTION_CORRECTION_EN, which gets disabled. | Y | N |
| | 12 | 0x0000 | mc_t1_sel<br>0: Regular motion correction<br>1: Motion corrupted pixels forced to use T1 data | N | N |
| | 11:0 | 0x0BA0 | t2_no_corr_threshold | N | N |
| 12690 R0x3192 | 15:0 | 0x0400 | hdr_mc_ctrl5 (R/W) | N | N |
| | 15:13 | X | Reserved | | |
| | 12:0 | 0x0400 | s12_range | N | N |
| 12692 R0x3194 | 15:0 | 0x0BB8 | hdr_mc_ctrl6 (R/W) | N | N |
| | 15:12 | X | Reserved | | |
| | 11:0 | 0x0BB8 | t1_barrier<br>Barrier for clipping T1 data in the digital lateral overflow combination method. | Y | N |

**Table 2:** **Manufacturer-Specific Register Descriptions (continued)**
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

| Register Dec(Hex) | Bits | Default | Name | Frame Sync'd | Bad Frame |
|---|---|---|---|---|---|
| 12694 R0x3196 | 15:0 | 0x0DAC | hdr_mc_ctrl7 (R/W) | Y | N |
| | 15:12 | X | Reserved | | |
| | 11:0 | 0x0DAC | t2_barrier<br>Barrier for clipping T2 data in the digital lateral overflow combination method. | Y | N |
| 12696 R0x3198 | 15:0 | 0x0FA0 | hdr_mc_ctrl8 (R/W) | Y | N |
| | 15:12 | X | Reserved | | |
| | 11:0 | 0x0FA0 | t3_barrier<br>Barrier for clipping T3 data in the digital lateral overflow combination method. | Y | N |
| 12698 R0x319A | 15:0 | 0x100B | hdr_comp_knee1 (RO) | N | N |
| | 15:13 | X | Reserved | | |
| | 12:8 | RO | p2_comp_knee | N | N |
| | 7:5 | X | Reserved | | |
| | 4:0 | RO | p1_comp_knee | N | N |
| 12700 R0x319C | 15:0 | 0x0014 | hdr_comp_knee2 (RO) | N | N |
| | 15:5 | X | Reserved | | |
| | 4:0 | RO | pmax_comp_knee | N | N |
| 12702 R0x319E | 15:0 | 0x6080 | hdr_mc_ctrl9 (R/W) | Y | N |
| | 15:12 | 0x0006 | s12_dlo_range<br>Range of code values for the noise filter weighting transfer function for digital lateral overflow defined by s2_dlo - s1_dlo<br>4'b0000 = 1<br>4'b0001 = 2<br>4'b0010 = 4<br>4'b0011 = 8<br>4'b0100 = 16<br>4'b0101 = 32<br>4'b0110 = 64<br>4'b0111 = 128<br>4'b1000 = 256<br>4'b1001 = 512<br>4'b1010 = 1024<br>4'b1011 = 2048<br>4'b1100 = 4096<br>>= 4'b1101 = 8192<br><br>Setting the range to 8192 effectively sets s1 to -4095 and s2 to 4095. | Y | N |
| | 11:0 | 0x0080 | s2_dlo_threshold<br>Threshold level for end point of noise filter weighting transfer function for digital lateral overflow. | Y | N |
| 12704 R0x31A0 | 15:0 | 0x0BA0 | hdr_mc_ctrl10 (R/W) | N | N |
| | 15:12 | X | Reserved | | |
| | 11:0 | 0x0BA0 | s1_mc_threshold<br>Separate S1 threshold (start of weighting function for smooth HDR pixel combination) for motion compensation. | N | N |

**Table 2:** **Manufacturer-Specific Register Descriptions (continued)**
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

| Register Dec(Hex) | Bits | Default | Name | Frame Sync'd | Bad Frame |
|---|---|---|---|---|---|
| 12706 R0x31A2 | 15:0 | 0x0BB8 | hdr_mc_ctrl11 (R/W) | | |
| | 15:12 | X | Reserved | | |
| | 11:0 | 0x0BB8 | noise_dlo_dis_threshold<br>For the digital lateral overflow method, if either T1 data, T2 data or T3 data is greater than this threshold, noise filtering is turned off. Evaluated on a single pixel. | N | N |
| 12736 R0x31C0 | 15:0 | 0x0000 | hispi_timing (R/W) | | |
| | Bits (2:0) = DLL delay setting for data lane 0<br>Bits (5:3) = DLL delay setting for data lane 1<br>Bits (8:6) = DLL delay setting for data lane 2<br>Bits (11:9) = DLL delay setting for data lane 3<br>Bits (14:12) = DLL delay setting for clock lane<br><br>The delay setting selects a tap along a delay element. Each stage is 1/8 of a symbol period. When the delay is set to zero, the delay element is powered down. | | | | | |
| 12742 R0x31C6 | 15:0 | 0x8000 | hispi_control_status (R/W) | | |
| | 15:14 | RO | hispi_status | N | N |
| | 13:10 | X | Reserved | | |
| | 9:2 | 0x0000 | hispi_control<br>bit[0] => stream mode enable.<br>bit[1] => Enable 3 lanes for compressed data<br>bit[2:4]=> test mode defined as:<br>  000 => transmit constant 0 on all enabled data lanes.<br>  001 => transmit constant 1 on all enabled data lanes.<br>  010 => transmit square wave at the half the potential serial data rate on all the enabled lanes.<br>  011=> transmit square wave at the pixel data rate on all the enabled lanes.<br>  100 => transmit a continuous, repeated, sequence of pseudo random data, with no SAV code, copied on all enabled data lanes.<br>  101 => replace pixel data with a known sequence (PN9), copied on all the enabled data lanes.<br><br>bit[5] => test mode enable<br>bit[6]=> io test enable<br>bit[7] => frame wide checksum test enable | N | N |
| | 1:0 | X | Reserved | | |
| | See descriptions in the bit fields. | | | | |
| 12744 R0x31C8 | 15:0 | 0xFFFF | hispi_crc_0 (RO) | N | N |
| 12746 R0x31CA | 15:0 | 0xFFFF | hispi_crc_1 (RO) | N | N |
| 12748 R0x31CC | 15:0 | 0xFFFF | hispi_crc_2 (RO) | N | N |

**Table 2: Manufacturer-Specific Register Descriptions (continued)**
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

| Register Dec(Hex) | Bits | Default | Name | Frame Sync'd | Bad Frame |
|---|---|---|---|---|---|
| 12750 R0x31CE | 15:0 | 0xFFFF | hispi_crc_3 (RO) | N | N |
| 12752 R0x31D0 | 15:0 | 0x0000 | hdr_comp (R/W) | N | N |
| | 15:3 | X | Reserved | | |
| | 2 | 0x0000 | compand_mode<br>Compand Mode set to<br>0: Input data is (wrongly) clipped at input<br>1: Input data is always treated as 20-bit | N | N |
| | 1 | 0x0000 | compand_14bits<br>0: Compand to 12 bits.<br>1: Compand to 14 bits | N | N |
| | 0 | 0x0000 | compand_en<br>Enables companding | N | N |
| 12754 R0x31D2 | 15:0 | 0x0000 | stat_frame_id (R/W) | N | N |
| 12758 R0x31D6 | 15:0 | 0xFFFF | i2c_wrt_checksum (R/W) | N | N |
| | Checksum of I2C write operations. | | | | |
| 12768 R0x31E0 | 15:0 | 0x0000 | pix_def_id (R/W) | | |
| | 15 | 0x0000 | test<br>When set, the pixel defect ID block is set in test mode. The contents of the defect RAMS can then be read at registers 0x31e2-3 and 0x31e4-5. To move to next entry, it is necessary to write to register bits 0x31e0-1[14:13].<br>This bit needs to be set to 0 before streaming. | N | Y |
| | 14:2 | X | Reserved | | |
| | 1 | 0x0000 | correction_mode<br>Mode of pixel defect correction.<br>0: Tag bad pixels with the reserved value 0.<br>1: Correct bad pixels, using Micron's traditional 1D correction scheme. | N | Y |
| | 0 | 0x0000 | enable<br>Enable pixel defect correction. | N | Y |
| 12770 R0x31E2 | 15:0 | 0x0000 | pix_def_id_base_ram (R/W) | N | N |
| | Data to be written to or read from the BASE RAM must be written to or read from this register. | | | | |
| 12772 R0x31E4 | 15:0 | 0x0000 | pix_def_id_stream_ram (R/W) | N | N |
| | Data to be read from the STREAM RAM must be read from this register. | | | | |
| 12774 R0x31E6 | 15:0 | 0x0000 | pix_def_ram_rd_addr (R/W) | N | N |
| | 15 | 0x0000 | Reserved | | |
| | 14:8 | X | Reserved | | |
| | 7:0 | 0x0000 | Reserved | | |
| | The content of this register points to location in the BASE and/or STREAM RAM to be read by I2C transaction. There is no auto increment on read, This register must be updated before read.<br>Bit [15] indicate if base_ram_end_addr should be updated with the address in bits [7]:[0]. No data will be written to BASE RAM when bit [15] is activated. | | | | |
| 12776 R0x31E8 | 15:0 | 0x0000 | horizontal_cursor_position (R/W) | N | N |
| | Specify the start row for the test cursor. | | | | |

**Table 2:** **Manufacturer-Specific Register Descriptions (continued)**
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

| Register Dec(Hex) | Bits | Default | Name | Frame Sync'd | Bad Frame |
|---|---|---|---|---|---|
| 12778 R0x31EA | 15:0 | 0x0000 | vertical_cursor_position (R/W) | N | N |
| | Specify the start column for the test cursor. | | | | |
| 12780 R0x31EC | 15:0 | 0x0000 | horizontal_cursor_width (R/W) | N | N |
| | Specify the width, in rows, of the horizontal test cursor. A width of 0 disables the cursor. | | | | |
| 12782 R0x31EE | 15:0 | 0x0000 | vertical_cursor_width (R/W) | N | N |
| | Specify the width, in columns, of the vertical test cursor. A width of 0 disables the cursor. | | | | |
| 12788 R0x31F4 | 15:0 | 0x0000 | fuse_id1 (R/W) | N | N |
| | Bits 15:0 of the fused chip ID. Read protected. Set reset_register[5] to get access to register. Before the fuses are programmed, this register will read 0x0000. After programming it will read back the programmed value. Read/Write (the programmed value can be over-written and will be restored on reset) | | | | |
| 12790 R0x31F6 | 15:0 | 0x0000 | fuse_id2 (R/W) | N | N |
| | Bits 31:16 of the fused chip ID. Read protected. Set reset_register[5] to get access to register. Before the fuses are programmed, this register will read 0x0000. After programming it will read back the programmed value. Read/Write (the programmed value can be over-written and will be restored on reset) | | | | |
| 12792 R0x31F8 | 15:0 | 0x0000 | fuse_id3 (R/W) | N | N |
| | Bits 47:32 of the fused chip ID. Read protected. Set reset_register[5] to get access to register. Before the fuses are programmed, this register will read 0x0000. After programming it will read back the programmed value. Read/Write (the programmed value can be over-written and will be restored on reset) | | | | |
| 12794 R0x31FA | 15:0 | 0x0000 | fuse_id4 (R/W) | N | N |
| | Bits 63:48 of the fused chip ID. Read protected. Set reset_register[5] to get access to register. Before the fuses are programmed, this register will read 0x0000. After programming it will read back the programmed value. Read/Write (the programmed value can be over-written and will be restored on reset) | | | | |
| 12796 R0x31FC | 15:0 | 0x3020 | i2c_ids (R/W) | N | N |
| | $I^2C$ addresses. | | | | |
| 14336 R0x3800 | 15:0 | 0x0000 | otpm_data_0 (R/W) | N | N |
| | OTPM_DATA_0 | | | | |
| 14338 R0x3802 | 15:0 | 0x0000 | otpm_data_1 (R/W) | N | N |
| | OTPM_DATA_1 | | | | |
| 14340 R0x3804 | 15:0 | 0x0000 | otpm_data_2 (R/W) | N | N |
| 14342 R0x3806 | 15:0 | 0x0000 | otpm_data_3 (R/W) | N | N |
| 14344 R0x3808 | 15:0 | 0x0000 | otpm_data_4 (R/W) | N | N |
| 14346 R0x380A | 15:0 | 0x0000 | otpm_data_5 (R/W) | N | N |
| 14348 R0x380C | 15:0 | 0x0000 | otpm_data_6 (R/W) | N | N |
| 14350 R0x380E | 15:0 | 0x0000 | otpm_data_7 (R/W) | | |
| 14352 R0x3810 | 15:0 | 0x0000 | otpm_data_8 (R/W) | N | N |
| 14354 R0x3812 | 15:0 | 0x0000 | otpm_data_9 (R/W) | N | N |

**Table 2: Manufacturer-Specific Register Descriptions (continued)**
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

| Register Dec(Hex) | Bits | Default | Name | Frame Sync'd | Bad Frame |
|---|---|---|---|---|---|
| 14356 R0x3814 | 15:0 | 0x0000 | otpm_data_10 (R/W) | N | N |
| 14358 R0x3816 | 15:0 | 0x0000 | otpm_data_11 (R/W) | N | N |
| 14360 R0x3818 | 15:0 | 0x0000 | otpm_data_12 (R/W) | N | N |
| 14362 R0x381A | 15:0 | 0x0000 | otpm_data_13 (R/W) | N | N |
| 14364 R0x381C | 15:0 | 0x0000 | otpm_data_14 (R/W) | N | N |
| 14366 R0x381E | 15:0 | 0x0000 | otpm_data_15 (R/W) | N | N |
| 14368 R0x3820 | 15:0 | 0x0000 | otpm_data_16 (R/W) | N | N |
| 14370 R0x3822 | 15:0 | 0x0000 | otpm_data_17 (R/W) | N | N |
| 14372 R0x3824 | 15:0 | 0x0000 | otpm_data_18 (R/W) | N | N |
| 14374 R0x3826 | 15:0 | 0x0000 | otpm_data_19 (R/W) | N | N |
| 14376 R0x3828 | 15:0 | 0x0000 | otpm_data_20 (R/W) | N | N |
| 14378 R0x382A | 15:0 | 0x0000 | otpm_data_21 (R/W) | N | N |
| 14380 R0x382C | 15:0 | 0x0000 | otpm_data_22 (R/W) | N | N |
| 14382 R0x382E | 15:0 | 0x0000 | otpm_data_23 (R/W) | N | N |
| 14384 R0x3830 | 15:0 | 0x0000 | otpm_data_24 (R/W) | N | N |
| 14386 R0x3832 | 15:0 | 0x0000 | otpm_data_25 (R/W) | N | N |
| 14388 R0x3834 | 15:0 | 0x0000 | otpm_data_26 (R/W) | N | N |
| 14390 R0x3836 | 15:0 | 0x0000 | otpm_data_27 (R/W) | N | N |
| 14392 R0x3838 | 15:0 | 0x0000 | otpm_data_28 (R/W) | N | N |
| 14394 R0x383A | 15:0 | 0x0000 | otpm_data_29 (R/W) | N | N |
| 14396 R0x383C | 15:0 | 0x0000 | otpm_data_30 (R/W) | N | N |
| 14398 R0x383E | 15:0 | 0x0000 | otpm_data_31 (R/W) | N | N |
| 14400 R0x3840 | 15:0 | 0x0000 | otpm_data_32 (R/W) | N | N |
| 14402 R0x3842 | 15:0 | 0x0000 | otpm_data_33 (R/W) | N | N |

**Table 2:     Manufacturer-Specific Register Descriptions (continued)**
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

| Register Dec(Hex) | Bits | Default | Name | Frame Sync'd | Bad Frame |
|---|---|---|---|---|---|
| 14404 R0x3844 | 15:0 | 0x0000 | otpm_data_34 (R/W) | N | N |
| 14406 R0x3846 | 15:0 | 0x0000 | otpm_data_35 (R/W) | N | N |
| 14408 R0x3848 | 15:0 | 0x0000 | otpm_data_36 (R/W) | N | N |
| 14410 R0x384A | 15:0 | 0x0000 | otpm_data_37 (R/W) | N | N |
| 14412 R0x384C | 15:0 | 0x0000 | otpm_data_38 (R/W) | N | N |
| 14414 R0x384E | 15:0 | 0x0000 | otpm_data_39 (R/W) | N | N |
| 14416 R0x3850 | 15:0 | 0x0000 | otpm_data_40 (R/W) | N | N |
| 14418 R0x3852 | 15:0 | 0x0000 | otpm_data_41 (R/W) | N | N |
| 14420 R0x3854 | 15:0 | 0x0000 | otpm_data_42 (R/W) | N | N |
| 14422 R0x3856 | 15:0 | 0x0000 | otpm_data_43 (R/W) | | |
| 14424 R0x3858 | 15:0 | 0x0000 | otpm_data_44 (R/W) | N | N |
| 14426 R0x385A | 15:0 | 0x0000 | otpm_data_45 (R/W) | N | N |
| 14428 R0x385C | 15:0 | 0x0000 | otpm_data_46 (R/W) | N | N |
| 14430 R0x385E | 15:0 | 0x0000 | otpm_data_47 (R/W) | N | N |
| 14432 R0x3860 | 15:0 | 0x0000 | otpm_data_48 (R/W) | | |
| 14434 R0x3862 | 15:0 | 0x0000 | otpm_data_49 (R/W) | | |
| 14436 R0x3864 | 15:0 | 0x0000 | otpm_data_50 (R/W) | | |
| 14438 R0x3866 | 15:0 | 0x0000 | otpm_data_51 (R/W) | | |
| 14440 R0x3868 | 15:0 | 0x0000 | otpm_data_52 (R/W) | | |
| 14442 R0x386A | 15:0 | 0x0000 | otpm_data_53 (R/W) | | |
| 14444 R0x386C | 15:0 | 0x0000 | otpm_data_54 (R/W) | | |
| 14446 R0x386E | 15:0 | 0x0000 | otpm_data_55 (R/W) | | |
| 14448 R0x3870 | 15:0 | 0x0000 | otpm_data_56 (R/W) | | |
| 14450 R0x3872 | 15:0 | 0x0000 | otpm_data_57 (R/W) | | |

**Table 2:    Manufacturer-Specific Register Descriptions (continued)**
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

| Register Dec(Hex) | Bits | Default | Name | Frame Sync'd | Bad Frame |
|---|---|---|---|---|---|
| 14452 R0x3874 | 15:0 | 0x0000 | otpm_data_58 (R/W) | | |
| 14454 R0x3876 | 15:0 | 0x0000 | otpm_data_59 (R/W) | | |
| 14456 R0x3878 | 15:0 | 0x0000 | otpm_data_60 (R/W) | | |
| 14458 R0x387A | 15:0 | 0x0000 | otpm_data_61 (R/W) | N | N |
| 14460 R0x387C | 15:0 | 0x0000 | otpm_data_62 (R/W) | | |
| 14462 R0x387E | 15:0 | 0x0000 | otpm_data_63 (R/W) | N | N |
| 14464 R0x3880 | 15:0 | 0x0000 | otpm_data_64 (R/W) | N | N |
| 14466 R0x3882 | 15:0 | 0x0000 | otpm_data_65 (R/W) | N | N |
| 14468 R0x3884 | 15:0 | 0x0000 | otpm_data_66 (R/W) | N | N |
| 14470 R0x3886 | 15:0 | 0x0000 | otpm_data_67 (R/W) | | |
| 14472 R0x3888 | 15:0 | 0x0000 | otpm_data_68 (R/W) | N | N |
| 14474 R0x388A | 15:0 | 0x0000 | otpm_data_69 (R/W) | N | N |
| 14476 R0x388C | 15:0 | 0x0000 | otpm_data_70 (R/W) | N | N |
| 14478 R0x388E | 15:0 | 0x0000 | otpm_data_71 (R/W) | N | N |
| 14480 R0x3890 | 15:0 | 0x0000 | otpm_data_72 (R/W) | N | N |
| 14482 R0x3892 | 15:0 | 0x0000 | otpm_data_73 (R/W) | | |
| 14484 R0x3894 | 15:0 | 0x0000 | otpm_data_74 (R/W) | N | N |
| 14486 R0x3896 | 15:0 | 0x0000 | otpm_data_75 (R/W) | N | N |
| 14488 R0x3898 | 15:0 | 0x0000 | otpm_data_76 (R/W) | | |
| 14490 R0x389A | 15:0 | 0x0000 | otpm_data_77 (R/W) | N | N |
| 14492 R0x389C | 15:0 | 0x0000 | otpm_data_78 (R/W) | N | N |
| 14494 R0x389E | 15:0 | 0x0000 | otpm_data_79 (R/W) | N | N |
| 14496 R0x38A0 | 15:0 | 0x0000 | otpm_data_80 (R/W) | N | N |
| 14498 R0x38A2 | 15:0 | 0x0000 | otpm_data_81 (R/W) | N | N |

**Table 2:    Manufacturer-Specific Register Descriptions (continued)**
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

| Register Dec(Hex) | Bits | Default | Name | Frame Sync'd | Bad Frame |
|---|---|---|---|---|---|
| 14500 R0x38A4 | 15:0 | 0x0000 | otpm_data_82 (R/W) | N | N |
| 14502 R0x38A6 | 15:0 | 0x0000 | otpm_data_83 (R/W) | N | N |
| 14504 R0x38A8 | 15:0 | 0x0000 | otpm_data_84 (R/W) | N | N |
| 14506 R0x38AA | 15:0 | 0x0000 | otpm_data_85 (R/W) | N | N |
| 14508 R0x38AC | 15:0 | 0x0000 | otpm_data_86 (R/W) | N | N |
| 14510 R0x38AE | 15:0 | 0x0000 | otpm_data_87 (R/W) | N | N |
| 14512 R0x38B0 | 15:0 | 0x0000 | otpm_data_88 (R/W) | N | N |
| 14514 R0x38B2 | 15:0 | 0x0000 | otpm_data_89 (R/W) | N | N |
| 14516 R0x38B4 | 15:0 | 0x0000 | otpm_data_90 (R/W) | N | N |
| 14518 R0x38B6 | 15:0 | 0x0000 | otpm_data_91 (R/W) | N | N |
| 14520 R0x38B8 | 15:0 | 0x0000 | otpm_data_92 (R/W) | N | N |
| 14522 R0x38BA | 15:0 | 0x0000 | otpm_data_93 (R/W) | N | N |
| 14524 R0x38BC | 15:0 | 0x0000 | otpm_data_94 (R/W) | N | N |
| 14526 R0x38BE | 15:0 | 0x0000 | otpm_data_95 (R/W) | N | N |
| 14528 R0x38C0 | 15:0 | 0x0000 | otpm_data_96 (R/W) | N | N |
| 14530 R0x38C2 | 15:0 | 0x0000 | otpm_data_97 (R/W) | N | N |
| 14532 R0x38C4 | 15:0 | 0x0000 | otpm_data_98 (R/W) | N | N |
| 14534 R0x38C6 | 15:0 | 0x0000 | otpm_data_99 (R/W) | N | N |
| 14536 R0x38C8 | 15:0 | 0x0000 | otpm_data_100 (R/W) | N | N |
| 14538 R0x38CA | 15:0 | 0x0000 | otpm_data_101 (R/W) | N | N |
| 14540 R0x38CC | 15:0 | 0x0000 | otpm_data_102 (R/W) | N | N |
| 14542 R0x38CE | 15:0 | 0x0000 | otpm_data_103 (R/W) | N | N |
| 14544 R0x38D0 | 15:0 | 0x0000 | otpm_data_104 (R/W) | N | N |
| 14546 R0x38D2 | 15:0 | 0x0000 | otpm_data_105 (R/W) | N | N |

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**Table 2:    Manufacturer-Specific Register Descriptions (continued)**
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

| Register Dec(Hex) | Bits | Default | Name | Frame Sync'd | Bad Frame |
|---|---|---|---|---|---|
| 14548 R0x38D4 | 15:0 | 0x0000 | otpm_data_106 (R/W) | N | N |
| 14550 R0x38D6 | 15:0 | 0x0000 | otpm_data_107 (R/W) | N | N |
| 14552 R0x38D8 | 15:0 | 0x0000 | otpm_data_108 (R/W) | N | N |
| 14554 R0x38DA | 15:0 | 0x0000 | otpm_data_109 (R/W) | N | N |
| 14556 R0x38DC | 15:0 | 0x0000 | otpm_data_110 (R/W) | N | N |
| 14558 R0x38DE | 15:0 | 0x0000 | otpm_data_111 (R/W) | N | N |
| 14560 R0x38E0 | 15:0 | 0x0000 | otpm_data_112 (R/W) | N | N |
| 14562 R0x38E2 | 15:0 | 0x0000 | otpm_data_113 (R/W) | N | N |
| 14564 R0x38E4 | 15:0 | 0x0000 | otpm_data_114 (R/W) | N | N |
| 14566 R0x38E6 | 15:0 | 0x0000 | otpm_data_115 (R/W) | N | N |
| 14568 R0x38E8 | 15:0 | 0x0000 | otpm_data_116 (R/W) | N | N |
| 14570 R0x38EA | 15:0 | 0x0000 | otpm_data_117 (R/W) | N | N |
| 14572 R0x38EC | 15:0 | 0x0000 | otpm_data_118 (R/W) | N | N |
| 14574 R0x38EE | 15:0 | 0x0000 | otpm_data_119 (R/W) | N | N |
| 14576 R0x38F0 | 15:0 | 0x0000 | otpm_data_120 (R/W) | N | N |
| 14578 R0x38F2 | 15:0 | 0x0000 | otpm_data_121 (R/W) | N | N |
| 14580 R0x38F4 | 15:0 | 0x0000 | otpm_data_122 (R/W) | N | N |
| 14582 R0x38F6 | 15:0 | 0x0000 | otpm_data_123 (R/W) | N | N |
| 14584 R0x38F8 | 15:0 | 0x0000 | otpm_data_124 (R/W) | N | N |
| 14586 R0x38FA | 15:0 | 0x0000 | otpm_data_125 (R/W) | N | N |
| 14588 R0x38FC | 15:0 | 0x0000 | otpm_data_126 (R/W) | N | N |
| 14590 R0x38FE | 15:0 | 0x0000 | otpm_data_127 (R/W) | N | N |
| 14592 R0x3900 | 15:0 | 0x0000 | otpm_data_128 (R/W) | N | N |
| 14594 R0x3902 | 15:0 | 0x0000 | otpm_data_129 (R/W) | N | N |

**Table 2:** **Manufacturer-Specific Register Descriptions (continued)**
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

| Register Dec(Hex) | Bits | Default | Name | Frame Sync'd | Bad Frame |
|---|---|---|---|---|---|
| 14596 R0x3904 | 15:0 | 0x0000 | otpm_data_130 (R/W) | N | N |
| 14598 R0x3906 | 15:0 | 0x0000 | otpm_data_131 (R/W) | N | N |
| 14600 R0x3908 | 15:0 | 0x0000 | otpm_data_132 (R/W) | N | N |
| 14602 R0x390A | 15:0 | 0x0000 | otpm_data_133 (R/W) | N | N |
| 14604 R0x390C | 15:0 | 0x0000 | otpm_data_134 (R/W) | N | N |
| 14606 R0x390E | 15:0 | 0x0000 | otpm_data_135 (R/W) | N | N |
| 14608 R0x3910 | 15:0 | 0x0000 | otpm_data_136 (R/W) | N | N |
| 14610 R0x3912 | 15:0 | 0x0000 | otpm_data_137 (R/W) | N | N |
| 14612 R0x3914 | 15:0 | 0x0000 | otpm_data_138 (R/W) | N | N |
| 14614 R0x3916 | 15:0 | 0x0000 | otpm_data_139 (R/W) | N | N |
| 14616 R0x3918 | 15:0 | 0x0000 | otpm_data_140 (R/W) | N | N |
| 14618 R0x391A | 15:0 | 0x0000 | otpm_data_141 (R/W) | N | N |
| 14620 R0x391C | 15:0 | 0x0000 | otpm_data_142 (R/W) | N | N |
| 14622 R0x391E | 15:0 | 0x0000 | otpm_data_143 (R/W) | N | N |
| 14624 R0x3920 | 15:0 | 0x0000 | otpm_data_144 (R/W) | N | N |
| 14626 R0x3922 | 15:0 | 0x0000 | otpm_data_145 (R/W) | N | N |
| 14628 R0x3924 | 15:0 | 0x0000 | otpm_data_146 (R/W) | N | N |
| 14630 R0x3926 | 15:0 | 0x0000 | otpm_data_147 (R/W) | N | N |
| 14632 R0x3928 | 15:0 | 0x0000 | otpm_data_148 (R/W) | N | N |
| 14634 R0x392A | 15:0 | 0x0000 | otpm_data_149 (R/W) | N | N |
| 14636 R0x392C | 15:0 | 0x0000 | otpm_data_150 (R/W) | N | N |
| 14638 R0x392E | 15:0 | 0x0000 | otpm_data_151 (R/W) | N | N |
| 14640 R0x3930 | 15:0 | 0x0000 | otpm_data_152 (R/W) | N | N |
| 14642 R0x3932 | 15:0 | 0x0000 | otpm_data_153 (R/W) | N | N |

**Table 2:** **Manufacturer-Specific Register Descriptions (continued)**
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

| Register Dec(Hex) | Bits | Default | Name | Frame Sync'd | Bad Frame |
|---|---|---|---|---|---|
| 14644 R0x3934 | 15:0 | 0x0000 | otpm_data_154 (R/W) | N | N |
| 14646 R0x3936 | 15:0 | 0x0000 | otpm_data_155 (R/W) | N | N |
| 14648 R0x3938 | 15:0 | 0x0000 | otpm_data_156 (R/W) | N | N |
| 14650 R0x393A | 15:0 | 0x0000 | otpm_data_157 (R/W) | N | N |
| 14652 R0x393C | 15:0 | 0x0000 | otpm_data_158 (R/W) | N | N |
| 14654 R0x393E | 15:0 | 0x0000 | otpm_data_159 (R/W) | N | N |
| 14656 R0x3940 | 15:0 | 0x0000 | otpm_data_160 (R/W) | N | N |
| 14658 R0x3942 | 15:0 | 0x0000 | otpm_data_161 (R/W) | N | N |
| 14660 R0x3944 | 15:0 | 0x0000 | otpm_data_162 (R/W) | N | N |
| 14662 R0x3946 | 15:0 | 0x0000 | otpm_data_163 (R/W) | N | N |
| 14664 R0x3948 | 15:0 | 0x0000 | otpm_data_164 (R/W) | N | N |
| 14666 R0x394A | 15:0 | 0x0000 | otpm_data_165 (R/W) | N | N |
| 14668 R0x394C | 15:0 | 0x0000 | otpm_data_166 (R/W) | N | N |
| 14670 R0x394E | 15:0 | 0x0000 | otpm_data_167 (R/W) | N | N |
| 14672 R0x3950 | 15:0 | 0x0000 | otpm_data_168 (R/W) | N | N |
| 14674 R0x3952 | 15:0 | 0x0000 | otpm_data_169 (R/W) | N | N |
| 14676 R0x3954 | 15:0 | 0x0000 | otpm_data_170 (R/W) | N | N |
| 14678 R0x3956 | 15:0 | 0x0000 | otpm_data_171 (R/W) | N | N |
| 14680 R0x3958 | 15:0 | 0x0000 | otpm_data_172 (R/W) | N | N |
| 14682 R0x395A | 15:0 | 0x0000 | otpm_data_173 (R/W) | N | N |
| 14684 R0x395C | 15:0 | 0x0000 | otpm_data_174 (R/W) | N | N |
| 14686 R0x395E | 15:0 | 0x0000 | otpm_data_175 (R/W) | N | N |
| 14688 R0x3960 | 15:0 | 0x0000 | otpm_data_176 (R/W) | N | N |
| 14690 R0x3962 | 15:0 | 0x0000 | otpm_data_177 (R/W) | N | N |

**Table 2: Manufacturer-Specific Register Descriptions (continued)**
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

| Register Dec(Hex) | Bits | Default | Name | Frame Sync'd | Bad Frame |
|---|---|---|---|---|---|
| 14692 R0x3964 | 15:0 | 0x0000 | otpm_data_178 (R/W) | N | N |
| 14694 R0x3966 | 15:0 | 0x0000 | otpm_data_179 (R/W) | N | N |
| 14696 R0x3968 | 15:0 | 0x0000 | otpm_data_180 (R/W) | N | N |
| 14698 R0x396A | 15:0 | 0x0000 | otpm_data_181 (R/W) | N | N |
| 14700 R0x396C | 15:0 | 0x0000 | otpm_data_182 (R/W) | N | N |
| 14702 R0x396E | 15:0 | 0x0000 | otpm_data_183 (R/W) | N | N |
| 14704 R0x3970 | 15:0 | 0x0000 | otpm_data_184 (R/W) | N | N |
| 14706 R0x3972 | 15:0 | 0x0000 | otpm_data_185 (R/W) | N | N |
| 14708 R0x3974 | 15:0 | 0x0000 | otpm_data_186 (R/W) | N | N |
| 14710 R0x3976 | 15:0 | 0x0000 | otpm_data_187 (R/W) | N | N |
| 14712 R0x3978 | 15:0 | 0x0000 | otpm_data_188 (R/W) | N | N |
| 14714 R0x397A | 15:0 | 0x0000 | otpm_data_189 (R/W) | N | N |
| 14716 R0x397C | 15:0 | 0x0000 | otpm_data_190 (R/W) | N | N |
| 14718 R0x397E | 15:0 | 0x0000 | otpm_data_191 (R/W) | N | N |
| 14720 R0x3980 | 15:0 | 0x0000 | otpm_data_192 (R/W) | N | N |
| 14722 R0x3982 | 15:0 | 0x0000 | otpm_data_193 (R/W) | N | N |
| 14724 R0x3984 | 15:0 | 0x0000 | otpm_data_194 (R/W) | N | N |
| 14726 R0x3986 | 15:0 | 0x0000 | otpm_data_195 (R/W) | N | N |
| 14728 R0x3988 | 15:0 | 0x0000 | otpm_data_196 (R/W) | N | N |
| 14730 R0x398A | 15:0 | 0x0000 | otpm_data_197 (R/W) | N | N |
| 14732 R0x398C | 15:0 | 0x0000 | otpm_data_198 (R/W) | N | N |
| 14734 R0x398E | 15:0 | 0x0000 | otpm_data_199 (R/W) | N | N |
| 14736 R0x3990 | 15:0 | 0x0000 | otpm_data_200 (R/W) | N | N |
| 14738 R0x3992 | 15:0 | 0x0000 | otpm_data_201 (R/W) | N | N |

**Table 2: Manufacturer-Specific Register Descriptions (continued)**
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

| Register Dec(Hex) | Bits | Default | Name | Frame Sync'd | Bad Frame |
|---|---|---|---|---|---|
| 14740 R0x3994 | 15:0 | 0x0000 | otpm_data_202 (R/W) | N | N |
| 14742 R0x3996 | 15:0 | 0x0000 | otpm_data_203 (R/W) | N | N |
| 14744 R0x3998 | 15:0 | 0x0000 | otpm_data_204 (R/W) | N | N |
| 14746 R0x399A | 15:0 | 0x0000 | otpm_data_205 (R/W) | N | N |
| 14748 R0x399C | 15:0 | 0x0000 | otpm_data_206 (R/W) | N | N |
| 14750 R0x399E | 15:0 | 0x0000 | otpm_data_207 (R/W) | N | N |
| 14752 R0x39A0 | 15:0 | 0x0000 | otpm_data_208 (R/W) | N | N |
| 14754 R0x39A2 | 15:0 | 0x0000 | otpm_data_209 (R/W) | N | N |
| 14756 R0x39A4 | 15:0 | 0x0000 | otpm_data_210 (R/W) | N | N |
| 14758 R0x39A6 | 15:0 | 0x0000 | otpm_data_211 (R/W) | N | N |
| 14760 R0x39A8 | 15:0 | 0x0000 | otpm_data_212 (R/W) | N | N |
| 14762 R0x39AA | 15:0 | 0x0000 | otpm_data_213 (R/W) | N | N |
| 14764 R0x39AC | 15:0 | 0x0000 | otpm_data_214 (R/W) | N | N |
| 14766 R0x39AE | 15:0 | 0x0000 | otpm_data_215 (R/W) | N | N |
| 14768 R0x39B0 | 15:0 | 0x0000 | otpm_data_216 (R/W) | N | N |
| 14770 R0x39B2 | 15:0 | 0x0000 | otpm_data_217 (R/W) | N | N |
| 14772 R0x39B4 | 15:0 | 0x0000 | otpm_data_218 (R/W) | N | N |
| 14774 R0x39B6 | 15:0 | 0x0000 | otpm_data_219 (R/W) | N | N |
| 14776 R0x39B8 | 15:0 | 0x0000 | otpm_data_220 (R/W) | N | N |
| 14778 R0x39BA | 15:0 | 0x0000 | otpm_data_221 (R/W) | N | N |
| 14780 R0x39BC | 15:0 | 0x0000 | otpm_data_222 (R/W) | N | N |
| 14782 R0x39BE | 15:0 | 0x0000 | otpm_data_223 (R/W) | N | N |
| 14784 R0x39C0 | 15:0 | 0x0000 | otpm_data_224 (R/W) | N | N |
| 14786 R0x39C2 | 15:0 | 0x0000 | otpm_data_225 (R/W) | N | N |

**Table 2: Manufacturer-Specific Register Descriptions (continued)**
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

| Register Dec(Hex) | Bits | Default | Name | Frame Sync'd | Bad Frame |
|---|---|---|---|---|---|
| 14788 R0x39C4 | 15:0 | 0x0000 | otpm_data_226 (R/W) | N | N |
| 14790 R0x39C6 | 15:0 | 0x0000 | otpm_data_227 (R/W) | N | N |
| 14792 R0x39C8 | 15:0 | 0x0000 | otpm_data_228 (R/W) | N | N |
| 14794 R0x39CA | 15:0 | 0x0000 | otpm_data_229 (R/W) | N | N |
| 14796 R0x39CC | 15:0 | 0x0000 | otpm_data_230 (R/W) | N | N |
| 14798 R0x39CE | 15:0 | 0x0000 | otpm_data_231 (R/W) | N | N |
| 14800 R0x39D0 | 15:0 | 0x0000 | otpm_data_232 (R/W) | N | N |
| 14802 R0x39D2 | 15:0 | 0x0000 | otpm_data_233 (R/W) | N | N |
| 14804 R0x39D4 | 15:0 | 0x0000 | otpm_data_234 (R/W) | N | N |
| 14806 R0x39D6 | 15:0 | 0x0000 | otpm_data_235 (R/W) | N | N |
| 14808 R0x39D8 | 15:0 | 0x0000 | otpm_data_236 (R/W) | N | N |
| 14810 R0x39DA | 15:0 | 0x0000 | otpm_data_237 (R/W) | N | N |
| 14812 R0x39DC | 15:0 | 0x0000 | otpm_data_238 (R/W) | N | N |
| 14814 R0x39DE | 15:0 | 0x0000 | otpm_data_239 (R/W) | N | N |
| 14816 R0x39E0 | 15:0 | 0x0000 | otpm_data_240 (R/W) | N | N |
| 14818 R0x39E2 | 15:0 | 0x0000 | otpm_data_241 (R/W) | N | N |
| 14820 R0x39E4 | 15:0 | 0x0000 | otpm_data_242 (R/W) | N | N |
| 14822 R0x39E6 | 15:0 | 0x0000 | otpm_data_243 (R/W) | N | N |
| 14824 R0x39E8 | 15:0 | 0x0000 | otpm_data_244 (R/W) | N | N |
| 14826 R0x39EA | 15:0 | 0x0000 | otpm_data_245 (R/W) | N | N |
| 14828 R0x39EC | 15:0 | 0x0000 | otpm_data_246 (R/W) | N | N |
| 14830 R0x39EE | 15:0 | 0x0000 | otpm_data_247 (R/W) | N | N |
| 14832 R0x39F0 | 15:0 | 0x0000 | otpm_data_248 (R/W) | N | N |
| 14834 R0x39F2 | 15:0 | 0x0000 | otpm_data_249 (R/W) | N | N |

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**Table 2: Manufacturer-Specific Register Descriptions (continued)**
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

| Register Dec(Hex) | Bits | Default | Name | Frame Sync'd | Bad Frame |
|---|---|---|---|---|---|
| 14836 R0x39F4 | 15:0 | 0x0000 | otpm_data_250 (R/W) | N | N |
| 14838 R0x39F6 | 15:0 | 0x0000 | otpm_data_251 (R/W) | N | N |
| 14840 R0x39F8 | 15:0 | 0x0000 | otpm_data_252 (R/W) | N | N |
| 14842 R0x39FA | 15:0 | 0x0000 | otpm_data_253 (R/W) | N | N |
| 14844 R0x39FC | 15:0 | 0x0000 | otpm_data_254 (R/W) | N | N |
| 14846 R0x39FE | 15:0 | 0x0000 | otpm_data_255 (R/W) | N | N |
| 16100 R0x3EE4 | 15:0 | 0xD208 | dac_ld_24_25 (R/W) | N | N |
| | 15:14 | 0x0003 | Reserved | | |
| | 13 | 0x0000 | Reserved | | |
| | 12 | 0x0001 | Reserved | | |
| | 11 | 0x0000 | Reserved | | |
| | 10 | 0x0000 | Reserved | | |
| | 9:8 | 0x0002 | ana_sreg_col_amp_gabs Absolute gain programming of column amplifier | N | N |
| | 7:6 | X | Reserved | | |
| | 5 | 0x0000 | Reserved | | |
| | 4 | 0x0000 | Reserved | | |
| | 3:0 | 0x0008 | Reserved | | |

**Table 2: Manufacturer-Specific Register Descriptions (continued)**
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

| Register Dec(Hex) | Bits | Default | Name | Frame Sync'd | Bad Frame |
|---|---|---|---|---|---|
| 16336 R0x3FD0 | 15:0 | 0x0000 | bist_buffers_control1 (R/W) | N | N |
| | 15:12 | X | Reserved | | |
| | 11 | 0x0000 | diag_whole<br>When set,<br>In diagnosis mode, test until find the first error in the unit.<br>When reset,<br>In diagnosis mode, test only the mentioned address and word. | N | N |
| | 10 | 0x0000 | test_en_s3<br>Enables BIST for S3 group of buffers | N | N |
| | 9 | 0x0000 | test_en_s2<br>enables BIST for s2 group of buffers | N | N |
| | 8 | 0x0000 | test_en_s1<br>enables BIST for s1 group of buffers | N | N |
| | 7:2 | 0x0000 | diag_unit_nr<br>Unit number for the memory that is to be tested by buffers BIST in diagnostic mode.<br>The values are:<br>0  => 47 for S1<br>48 => 51 for S2<br>52 => 53 for S3. | N | N |
| | 1 | 0x0000 | diagnostic_mode<br>When this bit and the bit bist_mode (bit 00, this address) are set, the BIST will only check the memory unit defined by the bits 7:2 (this address). | N | N |
| | 0 | 0x0000 | bist_mode<br>When set, it starts the BIST in streaming mode.<br>It must be reset after reading the results of the BIST.<br>For a new BIST test to start, it must be toggled. | N | N |
| | | | controls the operation of the special BISt for testing the delay buffers. | | |
| 16338 R0x3FD2 | 15:0 | 0x0000 | bist_buffers_control2 (R/W) | N | N |
| | 15:11 | X | Reserved | | |
| | 10:2 | 0x0000 | diag_addr<br>The address to be diagnosed (0 to 351).<br>Other values will not be found, therefore BIST will finish even if many failures exist. | N | N |
| | 1:0 | 0x0000 | diag_word<br>The word to be diagnosed (0 to 3).<br>0: Bits [12:0] of memory word<br>1: Bits [25:13] of memory word<br>2: Bits [38:26] of memory word<br>3: Bits [51:39] of memory word | N | N |

**Table 2:** **Manufacturer-Specific Register Descriptions (continued)**
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

| Register Dec(Hex) | Bits | Default | Name | Frame Sync'd | Bad Frame |
|---|---|---|---|---|---|
| 16340 R0x3FD4 | 15:0 | 0x0000 | bist_buffers_status1 (RO) | N | N |
| | 15:11 | X | Reserved | | |
| | 10:5 | RO | unit_failed_nr<br>The unit number for the first encountered failed memory unit. | N | N |
| | 4:1 | RO | test_seq<br>When test failed, these bits show the detecting sequence number. | N | N |
| | 0 | RO | test_failed<br>TEST_FAILED. | N | N |
| | Status data from BIST run. | | | | |
| 16342 R0x3FD6 | 15:0 | 0x0000 | bist_buffers_status2 (RO) | N | N |
| | 15:11 | X | Reserved | | |
| | 10:2 | RO | failed_addr<br>The address to the (first encountered) failed location in the memory.<br>Values between 0 to 351. | N | N |
| | 1:0 | RO | failed_word<br>The failed word number.<br>Each address in the memory is 52 bits, which is divided to 4 words of 13 bits.<br><br>Word_sel = 00 => bits 12:0.<br>Word_sel = 01 => bits 25:13.<br>Word_sel = 10 => bits 38:26.<br>Word_sel = 11 => bits 51:29. | N | N |
| | Status from BIST run | | | | |
| 16344 R0x3FD8 | 15:0 | 0x0000 | bist_buffers_data1 (RO) | N | N |
| | Data read from memory. | | | | |
| 16346 R0x3FDA | 15:0 | 0x0000 | bist_buffers_data2 (RO) | N | N |
| | The expected data from the memory. | | | | |

## Revision History

- Updated to ON Semiconductor template
- Removed Confidential marking

- Updated "Byte Ordering" on page 5
- Updated revision_number in Table 1, "Manufacturer-Specific Register List and Default Values," on page 7 and Table 2, "Manufacturer-Specific Register Descriptions," on page 25
- Updated descriptions of coarse_integration_time, fine_integration_time, and operation_mode in Table 2, "Manufacturer-Specific Register Descriptions," on page 25

- Updated to Production

- Initial release