





# deal.II Users and Developers Training

March 21 - 24 2016

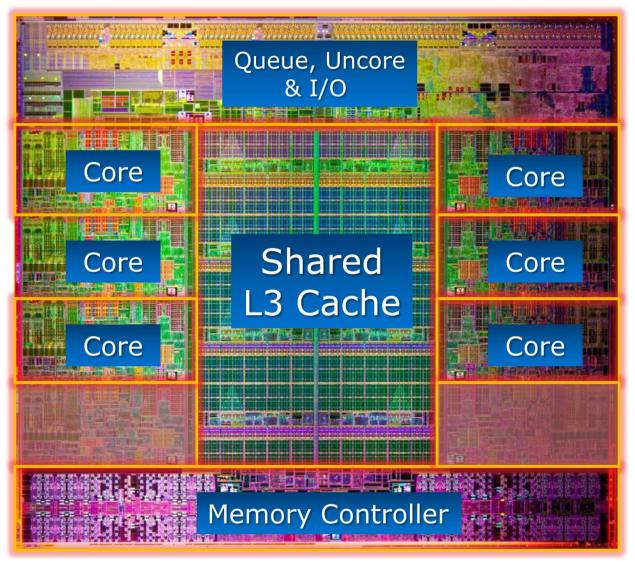
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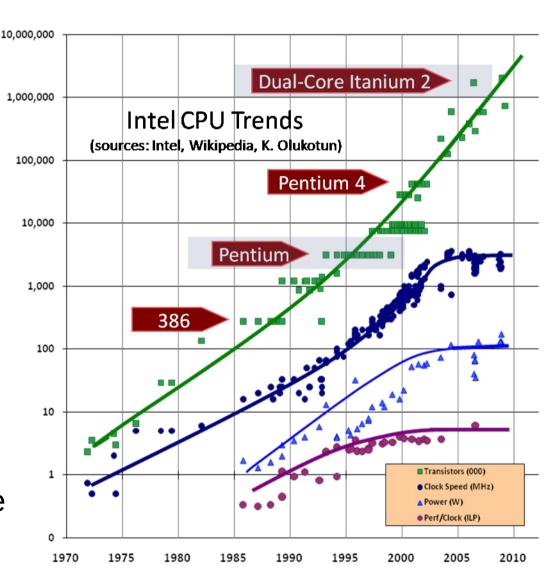
# Parallel Computing: Introduction



A modern CPU: Intel Core i7

### **Basics**

- Single cores are not getting (much) faster
- "the free lunch is over": http://www.gotw.ca/publi cations/concurrency-ddj. htm
- Concurrency is only option:
  - SIMD/vector instructions
  - Several cores
  - Several chips in one node
  - Combine nodes into supercomputer

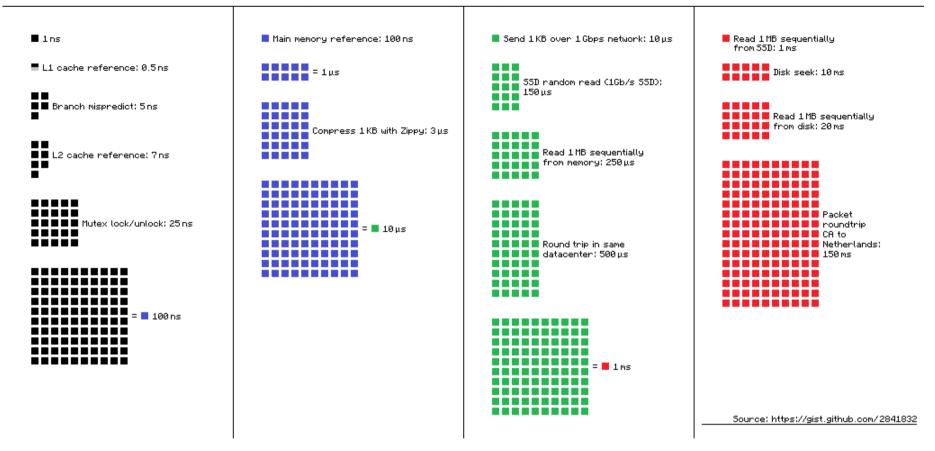


## Hierarchy of memory

- Latency: time CPU gets data after requesting
- Bandwidth: how much data per second?
- prefetching of data, "cache misses" are expensive
- automatically managed by processor

CPU		Capacity	Bandwidth	Latency
Registers	-	256 Bytes	24000 MB/s	2 ns
1. Level Cache	-	8 KBytes	16000 MB/s	2 hs
2. Level Cache	-	96 KBytes	8000 MB/s	6 hs
3. Level Cache	· —	2 MBytes	888 MB/s	24 ns
Main Memory	<b>-</b>	1536 MBytes	1000 MB/s	ll2 hs
Swap Space on Disk				

#### Latency Numbers Every Programmer Should Know



https://gist.github.com/hellerbarde/2843375

#### Amdahl's Law

- Task: serial fraction s, parallel fraction p=1-s
- N workers (whatever that means)
- Runtime: T(N) = (1-s)T(1)/N + sT(1)
- Speedup T(1)/T(N), N to infinity:
   max\_speedup = 1/ s
- http://en.wikipedia.org/wiki/Amdahl%27s\_law
- Reality:  $T(N) = (1-s)T(1)/N + sT(1) + aN + bN^2$

### Summary

- Computing much faster than memory access
- Parallel computing required: no free lunch!
- Communication is serial fraction (or worse when increasing with N!)
- Communication in Amdahl's law is main challenge in parallel computing