RE01 256KB Group

R_CORE Detailed Specification

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Introduction

This document describes the detailed specifications of the startup routine R_CORE provided in the RE01 256KB CMSIS Driver Package.

Target Device

RE01 256KB Group

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1. Overview

The following shows a list of abbreviations used in this document and a list of related documents.

Table 1-1 Abbreviation List

Name	Abbreviation
RE01 Group User's Manual: Hardware	UMH
RENESAS CMSIS-Core	R_CORE

Table 1-2 Related Document List

Document Name	Document Number
RE01 Group Products with 256-KB Flash Memory User's Manual: Hardware	r01uh0894
RE01 1500KB,256KB Group Getting Started Guide to Development Using CMSIS Package	r01an4660

2. Internal Structure of Software Components

2.1 File Structure

R_CORE is the system initialization module (CMSIS-Core) of the CMSIS Driver Package and consists of four files: startup_RE01_256KB.c, system_RE01_256KB.c, system_RE01_256KB.h, and r_core_cfg.h in the vendor-specific file storage directory.

The roles of the files are shown in Table 2-1. Figure 2-1 shows the file structure of R_CORE in the RE01 CMSIS Driver Package. The internal structure of R_CORE is shown in Figure 2-2.

Table 2-1 Roles of R_CORE Files

File Name	Description
startup_RE01_256KB.c	R_CORE startup source file. It declares vector tables and calls the system initialization function. To initialize the system, it is necessary to build this file.
system_RE01_256KB.c	R_CORE system initialization source file. It provides the entity of the system initialization function. To initialize the system, it is necessary to build this file.
system_RE01_256KB.h	R_CORE system initialization header file. It provides macro, type, and prototype declarations that can be referenced by the user. To initialize the system, it is necessary to include this file.
r_core_cfg.h	R_CORE configuration definition file. It provides configuration definitions that can be modified by the user.

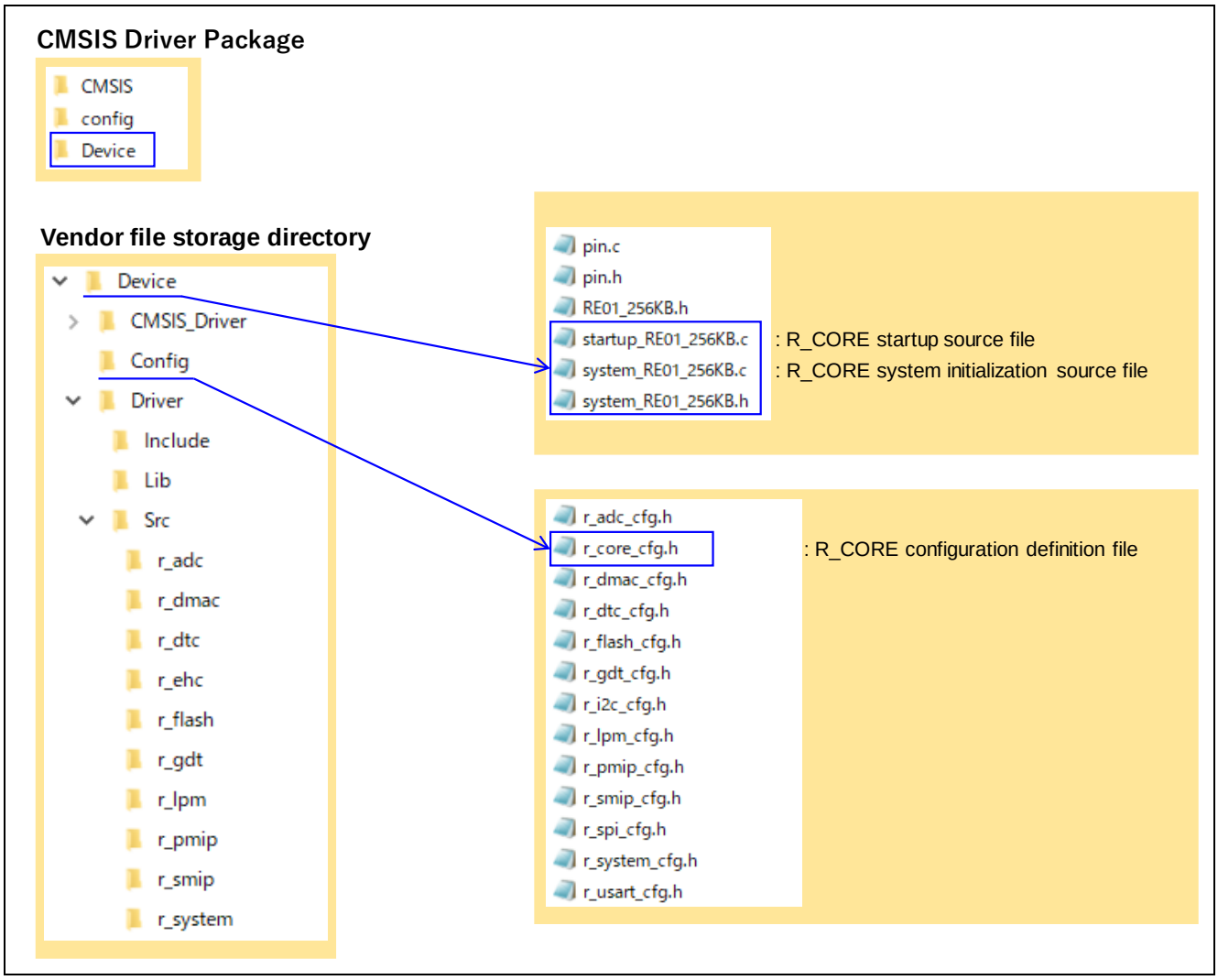
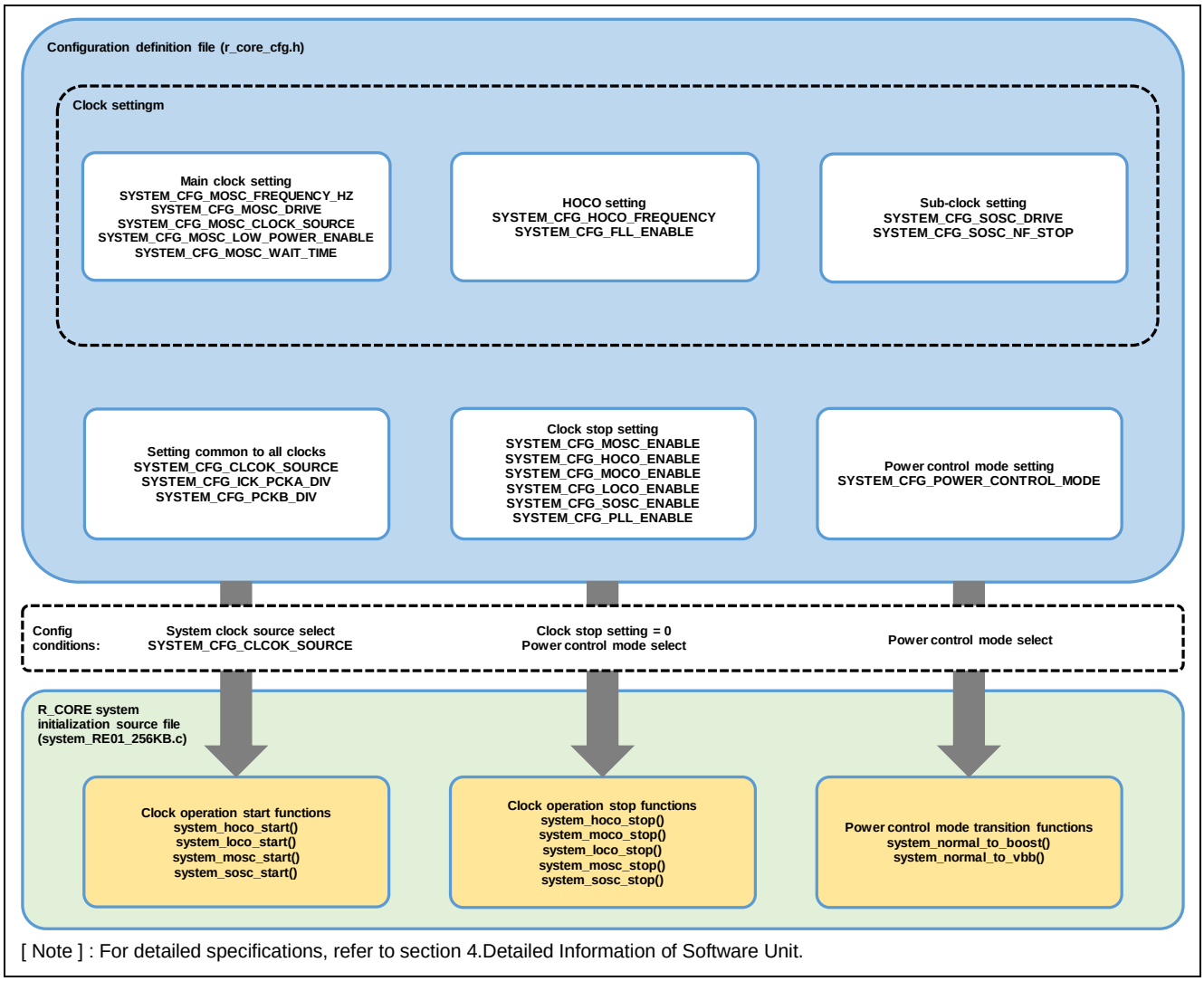


Figure 2-1 File Structure of R_CORE in CMSIS Driver Package



[Note] : For detailed specifications, refer to section 4.Detailed Information of Software Unit.

Figure 2-2 Relationship between R_CORE Functions and R_CORE Configuration Settings

3. Internal Operation of Software Components

R_CORE executes the initial operation to initialize the system by calling the Reset_Handler and SystemInit functions in startup_RE01_256KB.c. For detailed specifications, refer to section 4.3.13, Reset_Handler Function, and section 4.3.14, SystemInit Function.

3.1 Normal Startup Mode

The following shows the procedure for transition to the normal startup mode.

When the configuration definition of energy harvesting (EHC) startup mode (SYSTEM_CFG_EHC_MODE) is set to "disabled", EHC startup processing is skipped and normal startup processing is performed.

In the normal startup mode, the system and RAM are initialized after a reset, and then execution jumps to the main function.

The system initialization processing makes board-dependent initial settings of pins and specifies the operating frequencies and power-control mode in accordance with the settings in the configuration definition file.

The EHC startup mode is disabled by the default settings in the configuration definition file.

3.2 EHC Startup Mode

The following shows the procedure for transition to the EHC startup mode.

When the configuration definition of energy harvesting (EHC) startup mode (SYSTEM_CFG_EHC_MODE) is set to "enabled", EHC startup processing is performed.

In the EHC startup mode, the EHC capability is used to charge a secondary battery after a reset.

After charging is completed, the same processing as normal startup is performed — that is, the system and RAM are initialized and then execution jumps to the main function.

Note: EHC startup processing is an optional capability of R_CORE.

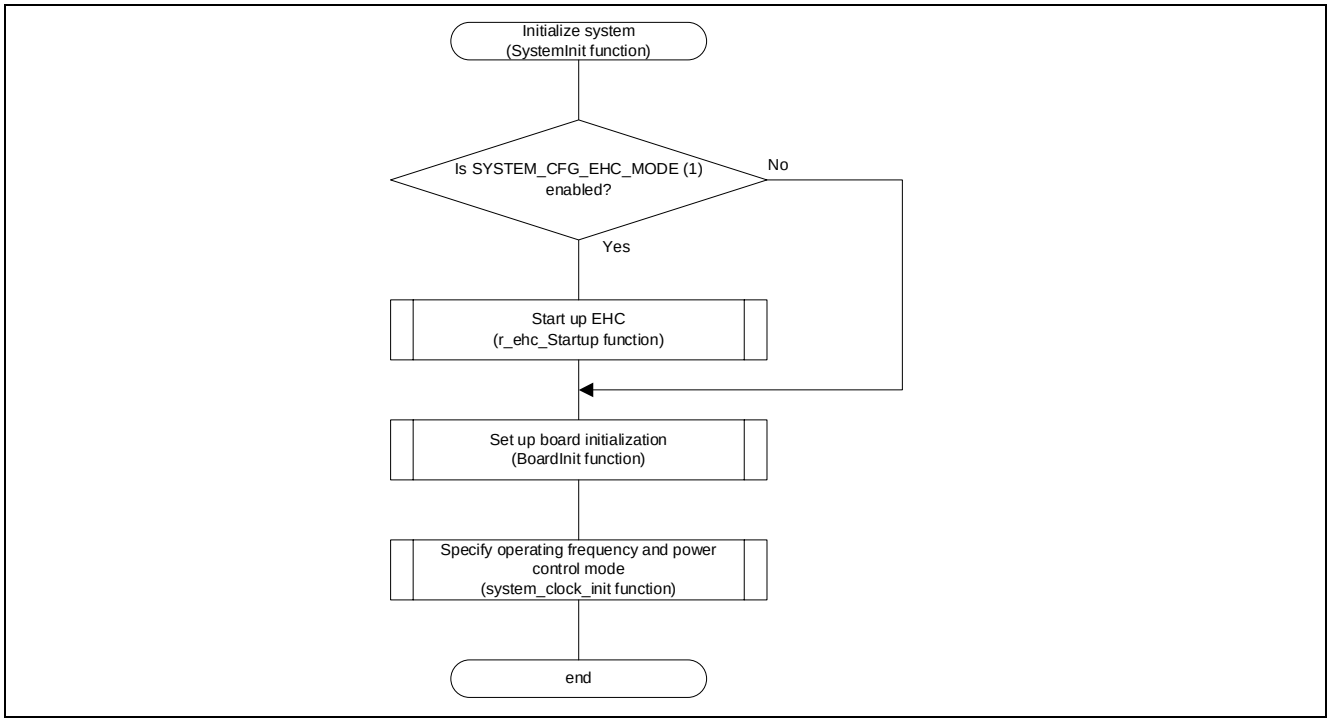


Figure 3-1 Transition to a Startup Mode by SystemInit Function

4. Detailed Information of Software Unit

4.1 Configurations

For R_CORE, configuration definitions that can be modified by the user are provided in the r_core_cfg.h file.

Table 4-1 shows a list of initial settings. For each configuration definition, refer to the corresponding section shown in the table.

Table 4-1 List of Initial Settings of R_CORE Configurations

Section	Configuration	Description	Initial Value
4.1.1	SYSTEM_CFG_MOSC_ENABLE	Specifies whether to operate or stop the main clock (MOSC).	0
4.1.2	SYSTEM_CFG_MOSC_FREQUENCY_HZ	Specifies the operating frequency of the main clock (MOSC).	32000000
4.1.3	SYSTEM_CFG_MOSC_DRIVE	Specifies the drive capability of the main clock oscillator.	7
4.1.4	SYSTEM_CFG_MOSC_CLOCK_SOURCE	Specifies the oscillation source of the main clock oscillator.	0
4.1.5	SYSTEM_CFG_MOSC_LOW_POWER_ENABLE	Specifies the low consumption oscillation function of the main clock oscillator.	0
4.1.6	SYSTEM_CFG_MOSC_WAIT_TIME	Specifies the stabilization wait time for the main clock oscillator.	5
4.1.7	SYSTEM_CFG_HOCO_ENABLE	Specifies whether to operate or stop the high-speed on-chip oscillator (HOCO).	0
4.1.8	SYSTEM_CFG_HOCO_FREQUENCY	Specifies the oscillation frequency of the high-speed on-chip oscillator (HOCO).	0
4.1.9	SYSTEM_CFG_FLL_ENABLE	Specifies whether enable or disable the FLL function.	0
4.1.10	SYSTEM_CFG_MOCO_ENABLE	Specifies whether to operate or stop the middle-speed on-chip oscillator (MOCO).	1
4.1.11	SYSTEM_CFG_LOCO_ENABLE	Specifies whether to operate or stop the low-speed on-chip oscillator (LOCO).	1
4.1.12	SYSTEM_CFG_SOSC_ENABLE	Specifies whether to operate or stop the sub-clock oscillator (SOSC).	0
4.1.13	SYSTEM_CFG_SOSC_DRIVE	Specifies the drive capability of the sub-clock oscillator.	0
4.1.14	SYSTEM_CFG_SOSC_NF_STOP	Specifies whether to operate or stop the noise filter for the sub-clock oscillator.	0
4.1.15	SYSTEM_CFG_CLCOK_SOURCE	Specifies the source of the system clock.	1
4.1.16	SYSTEM_CFG_ICK_PCKA_DIV	Specifies the frequency division of the system clock (ICLK) and peripheral module clock A (PCLKA).	0
4.1.17	SYSTEM_CFG_PCKB_DIV	Specifies the frequency division of peripheral module clock B (PCLKB).	0
4.1.18	SYSTEM_CFG_POWER_CONTROL_MODE	Specifies the power control mode.	1
4.1.19	SYSTEM_CFG_EHC_MODE	Enables or disables EHC startup processing.	0
4.1.20	SYSTEM_CFG_EHC_LVD1LVL	Specifies the Voltage Detection 1 Level in EHC startup.	7
4.1.21	SYSTEM_CFG_EHC_LVDBATLVL	Specifies the Voltage Detection BAT Level in EHC startup.	0
4.1.22	SYSTEM_CFG_OFS0	Specifies the value of option function select register 0 (OFS0).	0xFFFFFFFF
4.1.23	SYSTEM_CFG_OFS1	Specifies the value of option function select register 1 (OFS1).	0xFFFFFFFF
4.1.24	SYSTEM_CFG_SECMPU_PC0_START	Specifies security fetch region 0 (start address) in the code flash memory or SRAM.	0xFFFFFFFF
4.1.24	SYSTEM_CFG_SECMPU_PC0_END	Specifies security fetch region 0 (end address) in the code flash memory or SRAM.	0xFFFFFFFF
4.1.24	SYSTEM_CFG_SECMPU_PC1_START	Specifies security fetch region 1 (start address) in the code flash memory or SRAM.	0xFFFFFFFF

4.1.24	SYSTEM_CFG_SECMPU_PC1_END	Specifies security fetch region 1 (end address) in the code flash memory or SRAM.	0xFFFFFFFF
4.1.24	SYSTEM_CFG_SECMPU_REGION0_START	Specifies the start address of the security program and data in the code flash memory.	0xFFFFFFFF
4.1.24	SYSTEM_CFG_SECMPU_REGION0_END	Specifies the end address of the security program and data in the code flash memory.	0xFFFFFFFF
4.1.24	SYSTEM_CFG_SECMPU_REGION1_START	Specifies the start address of the security program and data in the SRAM.	0xFFFFFFFF
4.1.24	SYSTEM_CFG_SECMPU_REGION1_END	Specifies the end address of the security program and data in the SRAM.	0xFFFFFFFF
4.1.24	SYSTEM_CFG_SECMPU_REGION2_START	Specifies the start address of the security program and data in the security IP module.	0xFFFFFFFF
4.1.24	SYSTEM_CFG_SECMPU_REGION2_END	Specifies the end address of the security program and data in the security IP module.	0xFFFFFFFF
4.1.24	SYSTEM_CFG_SECMPU_CONTROL_SETTING	Enables or disables the security for each region.	0xFFFF
4.1.25	SYSTEM_CFG_ID_CODE_PROTECTION_1	Specifies an OCD or serial programmer ID (bits 0 to 31).	0xFFFFFFFF
4.1.25	SYSTEM_CFG_ID_CODE_PROTECTION_2	Specifies an OCD or serial programmer ID (bits 32 to 63).	0xFFFFFFFF
4.1.25	SYSTEM_CFG_ID_CODE_PROTECTION_3	Specifies an OCD or serial programmer ID (bits 64 to 95).	0xFFFFFFFF
4.1.25	SYSTEM_CFG_ID_CODE_PROTECTION_4	Specifies an OCD or serial programmer ID (bits 96 to 127).	0xFFFFFFFF
4.1.26	SYSTEM_CFG_AWS	Specifies the start and end block addresses of the access window, selects the startup area, and specifies protection of the selected function.	0xFFFFFFFF

When the configuration definitions are set to the initial values, the operating clock and mode settings at startup are determined as shown in Table 4-2. For the power control modes that can be specified with configuration file settings, refer to Figure 4-1.

Table 4-2 Operating Clocks and Modes at Startup

System Clock Source	System Clock Frequency Division (ICLK, PCLKA)	Peripheral Clock Frequency Division (PCLKB)	Power Supply Mode	Power Control Mode	Main Clock	Sub-clock	HOCO	LOCO
MOCO (2 MHz)	Divided by 1 (2 MHz)	Divided by 1 (2 MHz)	ALLPWON	Normal high-speed	Stopped	Stopped	Stopped	Operates

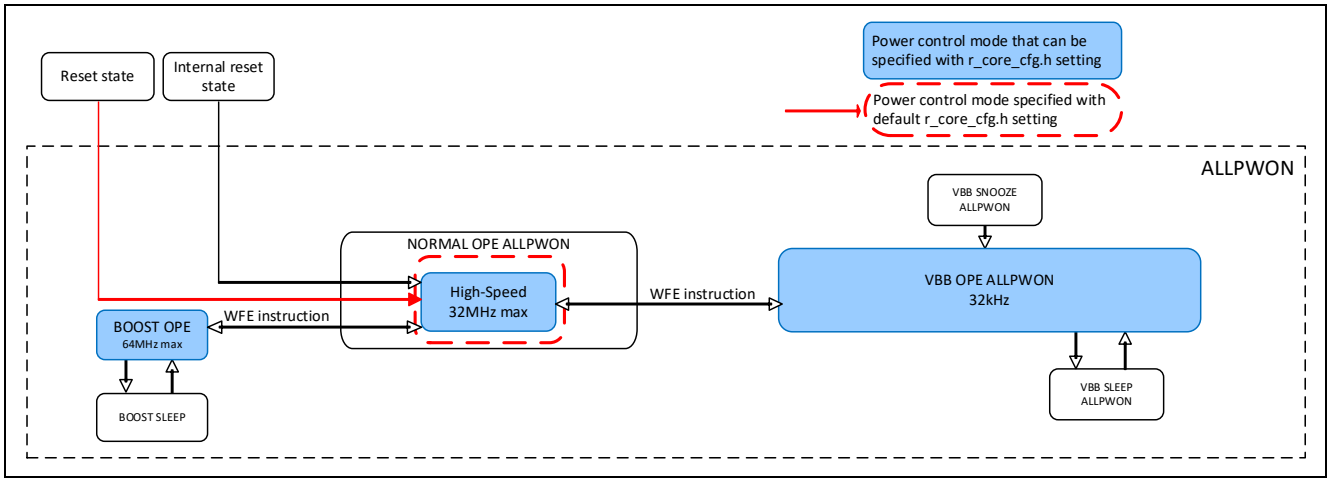


Figure 4-1 Power Control Modes that Can Be Specified with Configuration File (r_core_cfg.h) Settings

4.1.1 Main Clock Oscillator Stop (SYSTEM_CFG_MOSC_ENABLE)

This specifies whether to operate or stop the main clock (MOSC) in R_CORE.

Name: SYSTEM_CFG_MOSC_ENABLE

Table 4-3 Settings of SYSTEM_CFG_MOSC_ENABLE

Setting	Description
0 (initial value)	Stops (disables) the main clock (MOSC) when it is not selected as the clock source.
1	Operates (enables) the main clock (MOSC) when it is not selected as the clock source.

4.1.2 Main Clock Operating Frequency Setting (SYSTEM_CFG_MOSC_FREQUENCY_HZ)

This specifies the frequency of the main clock (MOSC) in R_CORE.

Name: SYSTEM_CFG_MOSC_FREQUENCY_HZ

Table 4-4 Settings of SYSTEM_CFG_MOSC_FREQUENCY_HZ

Setting	Description
32000000 (initial value)	Specifies the frequency of the main clock (MOSC) when it operates (is enabled).

4.1.3 Main Clock Oscillator Drive Capability Switching (SYSTEM_CFG_MOSC_DRIVE)

This specifies the optimum drive capability of the main clock (MOSC) in R_CORE in accordance with the resonator used.

The value of this configuration definition is specified in the MOMCR.MODRV bits.

Name: SYSTEM_CFG_MOSC_DRIVE

Table 4-5 Settings of SYSTEM_CFG_MOSC_DRIVE

Setting	Description (MOMCR.MODRV Bit Setting)
0	Setting prohibited.
1	Oscillation current is small.
:	:
7 (initial value)	Oscillation current is large.

4.1.4 Main Clock Oscillator Switching (SYSTEM_CFG_MOSC_CLOCK_SOURCE)

This specifies the oscillation source of the main clock oscillator in R_CORE.

The value of this configuration definition is specified in the MOMCR.MOSEL bit.

Name: SYSTEM_CFG_MOSC_CLOCK_SOURCE

Table 4-6 Settings of SYSTEM_CFG_MOSC_CLOCK_SOURCE

Setting	Description (MOMCR.MOSEL Bit Setting)
0 (initial value)	Resonator
1	External clock input

4.1.5 Main Clock Oscillator Low Consumption Oscillation Function Enable (SYSTEM_CFG_MOSC_LOW_POWER_ENABLE)

This enables or disables the low consumption oscillation function of the main clock oscillator in R_CORE.

The value of this configuration definition is specified in the MOMCR.OSCLPEN bit.

Name: SYSTEM_CFG_MOSC_LOW_POWER_ENABLE

Table 4-7 Settings of SYSTEM_CFG_MOSC_LOW_POWER_ENABLE

Setting	Description (MOMCR.OSCLPEN Bit Setting)
0 (initial value)	Disabled
1	Enabled

4.1.6 Main Clock Oscillator Stabilization Wait Time Setting (SYSTEM_CFG_MOSC_WAIT_TIME)

This specifies the oscillation stabilization wait time of the main clock oscillator in R_CORE.

The value of this configuration definition is specified in the MOSCWTCR.MSTS bits.

Name: SYSTEM_CFG_MOSC_WAIT_TIME

Table 4-8 Settings of SYSTEM_CFG_MOSC_WAIT_TIME

Setting	Description (MOSCWTCR.MSTS Bit Setting)
0	Setting prohibited
1	2 cycles
2	5 cycles
3	13 cycles
4	29 cycles
5 (initial value)	61 cycles
6	125 cycles
7	253 cycles
8	509 cycles
9	1021 cycles

4.1.7 HOCO Stop (SYSTEM_CFG_HOCO_ENABLE)

This specifies whether to operate or stop the high-speed on-chip oscillator (HOCO) in R_CORE.

Name: SYSTEM_CFG_HOCO_ENABLE

Table 4-9 Settings of SYSTEM_CFG_HOCO_ENABLE

Setting	Description
0 (initial value)	Stops (disables) HOCO when it is not selected as the clock source.
1	Operates (enables) HOCO when it is not selected as the clock source.

4.1.8 HOCO Operating Frequency Setting (SYSTEM_CFG_HOCO_FREQUENCY)

This specifies the frequency of the high-speed on-chip oscillator (HOCO) in R_CORE.

The value of this configuration definition is specified in the HOCOMCR.HCFRQ bits.

Name: SYSTEM_CFG_HOCO_FREQUENCY

Table 4-10 Settings of SYSTEM_CFG_HOCO_FREQUENCY

Setting	Description (HOCOMCR.HCFRQ Bit Setting)
0	Sets the frequency of HOCO to 24 MHz.
1 (initial value)	Sets the frequency of HOCO to 32 MHz.
2	Sets the frequency of HOCO to 48 MHz.
3	Sets the frequency of HOCO to 64 MHz.

4.1.9 FLL Function Enable (SYSTEM_CFG_FLL_ENABLE)

This enables or disables the FLL function of the high-speed on-chip oscillator (HOCO) in R_CORE.

Name: SYSTEM_CFG_FLL_ENABLE

Table 4-11 Settings of SYSTEM_CFG_FLL_ENABLE

Setting	Description
0 (initial value)	FLL function is disable.
1	FLL function is enable.

4.1.10 MOCO Stop (SYSTEM_CFG_MOCO_ENABLE)

This specifies whether to operate or stop the middle-speed on-chip oscillator (MOCO) in R_CORE.

Name: SYSTEM_CFG_MOCO_ENABLE

Table 4-12 Settings of SYSTEM_CFG_MOCO_ENABLE

Setting	Description
0	Stops (disables) MOCO when it is not selected as the clock source.
1 (initial value)	Does not stop (enables) MOCO when it is not selected as the clock source.

4.1.11 LOCO Stop (SYSTEM_CFG_LOCO_ENABLE)

This specifies whether to operate or stop the low-speed on-chip oscillator (LOCO) in R_CORE.

Name: SYSTEM_CFG_LOCO_ENABLE

Table 4-13 Settings of SYSTEM_CFG_LOCO_ENABLE

Setting	Description
0	Stops (disables) LOCO when it is not selected as the clock source.
1 (initial value)	Operates (enables) LOCO when it is not selected as the clock source.

4.1.12 Sub-clock Oscillator Stop (SYSTEM_CFG_SOSC_ENABLE)

This specifies whether to operate or stop the sub-clock (SOSC) in R_CORE.

Name: SYSTEM_CFG_SOSC_ENABLE

Table 4-14 Settings of SYSTEM_CFG_SOSC_ENABLE

Setting	Description
0 (initial value)	Stops (disables) the sub-clock (SOSC) when it is not selected as the clock source.
1	Operates (enables) the sub-clock (SOSC) when it is not selected as the clock source.

4.1.13 Sub-clock Oscillator Drive Capability Switching (SYSTEM_CFG_SOSC_DRIVE)

This specifies the optimum drive capability of the sub-clock (SOSC) in R_CORE in accordance with the resonator used.

The value of this configuration definition is specified in the SOMCR.SODRV bits.

Name: SYSTEM_CFG_SOSC_DRIVE

Table 4-15 Settings of SYSTEM_CFG_SOSC_DRIVE

Setting	Description (SOMCR.SODRV Bit Setting)
0 (initial value)	Drives the sub-clock (SOSC) with the standard CL.
1	Drives the sub-clock (SOSC) with the low CL6.
2	Drives the sub-clock (SOSC) with the low CL4.
3	Drives the sub-clock (SOSC) with the low CL7.

4.1.14 Sub-clock Oscillator Noise Filter Stop (SYSTEM_CFG_SOSC_NF_STOP)

This specifies whether to operate or stop the noise filter for the sub-clock (SOSC) oscillator in R_CORE.

The value of this configuration definition is specified in the SOMCR.SONFSTP bit.

Name: SYSTEM_CFG_SOSC_NF_STOP

Table 4-16 Settings of SYSTEM_CFG_SOSC_NF_STOP

Setting	Description (SOMCR.SONFSTP Bit Setting)
0 (initial value)	Operates the noise filter for the sub-clock (SOSC).
1	Stops the noise filter for the sub-clock (SOSC).

4.1.15 Clock Source Select (SYSTEM_CFG_CLOCK_SOURCE)

This specifies the source of the system clock.

The value of this configuration definition is specified in the SCKSCR.CKSEL bits.

Name: SYSTEM_CFG_CLOCK_SOURCE

Table 4-17 Settings of SYSTEM_CFG_CLOCK_SOURCE

Setting	Description (SCKSCR.CKSEL Bit Setting)
0	HOCO
1 (initial value)	MOCO
2	LOCO
3	Main clock oscillator
4	Sub-clock oscillator

4.1.16 System Clock (ICLK)/Peripheral Module Clock (PCLKA) Select (SYSTEM_CFG_ICK_PCKA_DIV)

This specifies the frequency division of the system clock used by the CPU, DMAC, and DTC, and peripheral module clock A (PCLKA).

The value of this configuration definition is specified in the SCKDIVCR.ICK bits.

Name: SYSTEM_CFG_ICK_PCKA_DIV

Table 4-18 Settings of SYSTEM_CFG_ICK_PCKA_DIV

Setting	Description (SCKDIVCR.ICK Bit Setting)
0 (initial value)	Divides the clock source frequency by 1.
1	Divides the clock source frequency by 2.
2	Divides the clock source frequency by 4.
3	Divides the clock source frequency by 8.
4	Divides the clock source frequency by 16.
5	Divides the clock source frequency by 32.
6	Divides the clock source frequency by 64.

4.1.17 Peripheral Module Clock B (PCLKB) Select (SYSTEM_CFG_PCKB_DIV)

This specifies the frequency division of peripheral module clock B (PCLKB).

The value of this configuration definition is specified in the SCKDIVCR.PCKB bits.

Name: SYSTEM_CFG_PCKB_DIV

Table 4-19 Settings of SYSTEM_CFG_PCKB_DIV

Setting	Description (SCKDIVCR.PCKB Bit Setting)
0 (initial value)	Divides the clock source frequency by 1.
1	Divides the clock source frequency by 2.
2	Divides the clock source frequency by 4.
3	Divides the clock source frequency by 8.
4	Divides the clock source frequency by 16.
5	Divides the clock source frequency by 32.
6	Divides the clock source frequency by 64.

4.1.18 Power Control Mode Select (SYSTEM_CFG_POWER_CONTROL_MODE)

This selects the boost mode (BOOST), normal mode (NORMAL), or low leakage current mode (VBB) as the power control mode. For the normal mode (NORMAL), this definition also selects high-speed mode.

Name: SYSTEM_CFG_POWER_CONTROL_MODE

Table 4-20 Settings of SYSTEM_CFG_POWER_CONTROL_MODE

Setting	Description
0	Boost mode (BOOST)
1 (initial value)	Normal mode (Normal) and high-speed mode
4	Low leakage current mode (VBB)

4.1.19 EHC Startup Mode Setting (SYSTEM_CFG_EHC_MODE)

This enables or disables EHC startup processing.

Note: The EHC startup processing is an optional capability of R_CORE.

Name: SYSTEM_CFG_EHC_MODE

Table 4-21 Settings of SYSTEM_CFG_EHC_MODE

Setting	Description
0	Disables EHC startup processing.
1	Enables EHC startup processing.

4.1.20 Voltage Detection 1 Level Setting (SYSTEM_CFG_EHC_LVD1LVL)

This specifies the Voltage Detection 1 Level. For details of the Vdet1_X, refer to UMH.

Note: The EHC startup processing is an optional capability of R_CORE.

Name: SYSTEM_CFG_EHC_LVD1LVL

Table 4-22 Settings of SYSTEM_CFG_EHC_LVD1LVL

Setting	Description
0	Vdet1_0
1	Vdet1_1
2	Vdet1_3
3	Vdet1_5
4	Vdet1_7
5	Vdet1_9
6	Vdet1_B
7 (initial value)	Vdet1_D

4.1.21 Voltage Detection BAT Level Setting (SYSTEM_CFG_EHC_LVDBATLVL)

This specifies the Voltage Detection BAT Level. For details of the VdetBAT_X, refer to UMH.

Note: The EHC startup processing is an optional capability of R_CORE.

Name: SYSTEM_CFG_EHC_LVDBATLVL

Table 4-23 Settings of SYSTEM_CFG_EHC_LVDBATLVL

Setting	Description
0 (initial value)	VdetBAT_5
1	VdetBAT_7
2	VdetBAT_8
3	VdetBAT_B
4	VdetBAT_D

4.1.22 Option-Setting Memory 0 (SYSTEM_CFG_OFS0)

This specifies the value of option function select register 0 (OFS0). For details of the register, refer to UMH.

Name: SYSTEM_CFG_OFS0

Table 4-24 Settings of SYSTEM_CFG_OFS0

Setting	Description
0xFFFFFFFF (initial value)	Value to be set in option function select register 0 (OFS0).

4.1.23 Option-Setting Memory 1 (SYSTEM_CFG_OFS1)

This specifies the value of option function select register 1 (OFS1). For details of the register, refer to UMH.

Name: SYSTEM_CFG_OFS1

Table 4-25 Settings of SYSTEM_CFG_OFS1

Setting	Description
0xFFFFFFFF (initial value)	Value to be set in option function select register 1 (OFS1).

4.1.24 Option-Setting Memory 2 (SYSTEM_CFG_SECMPU_xxx)

This specifies the value of each register associated with the security MPU function. For details of the registers, refer to UMH.

Name: SYSTEM_CFG_SECMPU_xxx

Table 4-26 Settings of SYSTEM_CFG_SECMPU_xxx

Configuration	Setting	Description
SYSTEM_CFG_SECMPU_PC0_START	0xFFFFFFFF (initial value)	Value to be set in security MPU program counter start address register 0 (SECMPUPCS0).
SYSTEM_CFG_SECMPU_PC0_END	0xFFFFFFFF (initial value)	Value to be set in security MPU program counter end address register 0 (SECMPUPCE0).
SYSTEM_CFG_SECMPU_PC1_START	0xFFFFFFFF (initial value)	Value to be set in security MPU program counter start address register 1 (SECMPUPCS1).
SYSTEM_CFG_SECMPU_PC1_END	0xFFFFFFFF (initial value)	Value to be set in security MPU program counter end address register 1 (SECMPUPCE1).
SYSTEM_CFG_SECMPU_REGION0_START	0xFFFFFFFF (initial value)	Value to be set in the security MPU region 0 start address register (SECMPUS0).
SYSTEM_CFG_SECMPU_REGION0_END	0xFFFFFFFF (initial value)	Value to be set in the security MPU region 0 end address register (SECMPUE0).
SYSTEM_CFG_SECMPU_REGION1_START	0xFFFFFFFF (initial value)	Value to be set in the security MPU region 1 start address register (SECMPUS1).
SYSTEM_CFG_SECMPU_REGION1_END	0xFFFFFFFF (initial value)	Value to be set in the security MPU region 1 end address register (SECMPUE1).
SYSTEM_CFG_SECMPU_REGION2_START	0xFFFFFFFF (initial value)	Value to be set in the security MPU region 2 start address register (SECMPUS2).
SYSTEM_CFG_SECMPU_REGION2_END	0xFFFFFFFF (initial value)	Value to be set in the security MPU region 2 end address register (SECMPUE2).
SYSTEM_CFG_SECMPU_CONTROL_SETTING	0xFFFF (initial value)	Value to be set in the security MPU access control register (SECMPUAC).

4.1.25 Option-Setting Memory 3 (SYSTEM_CFG_ID_CODE_PROTECTION_n) (n = 1 to 4)

This specifies the value of the OCD/serial programmer ID setting register (OSIS). For details of the register, refer to UMH.

Name: SYSTEM_CFG_ID_CODE_PROTECTION_n

Table 4-27 Settings of SYSTEM_CFG_ID_CODE_PROTECTION_n

Configuration	Setting	Description
SYSTEM_CFG_ID_CODE_PROTECTION_1	0xFFFFFFFF (initial value)	Value to be set in the OSIS register (bits 0 to 31).
SYSTEM_CFG_ID_CODE_PROTECTION_2	0xFFFFFFFF (initial value)	Value to be set in the OSIS register (bits 32 to 63).
SYSTEM_CFG_ID_CODE_PROTECTION_3	0xFFFFFFFF (initial value)	Value to be set in the OSIS register (bits 64 to 95).
SYSTEM_CFG_ID_CODE_PROTECTION_4	0xFFFFFFFF (initial value)	Value to be set in the OSIS register (bits 96 to 127).

4.1.26 Option-Setting Memory 4 (SYSTEM_CFG_AWS)

This specifies the value of the access window setting register (AWS). For details of the register, refer to UMH.

Table 4-28 Settings of SYSTEM_CFG_AWS

Setting	Description
0xFFFFFFFF (initial value)	Value to be set in the access window setting register (AWS).

4.1.27 Preprocessor Error Check

The correctness of the value specified for each definition shown in section 4.1, Configurations, is checked during compilation. Table 4-29 and Table 4-30 show typical error conditions. For details of the check and actions against errors, refer to section 4.4.1, List of Preprocessor Errors.

Table 4-29 Typical Error Conditions (when Selected as Clock Source)

Error Check Condition for Clock and Frequency Division Settings (Selected as Clock Source)		Boost Mode (BOOST) ≤ 64 MHz	Normal Mode (High-speed) ≤ 32 MHz	Low Leakage Current Mode (VBB) = 32.768 kHz
0	HOCO (24, 32, 48, or 64 MHz)	N/A	• HOCO setting ≥ 48 MHz	• When HOCO is selected
1	MOCO (2 MHz)	N/A	N/A	• When MOCO is selected
2	LOCO (32.768 kHz)	N/A	N/A	N/A
3	MOSC (8 to 32 MHz)	N/A	N/A	• When MOSC is selected
4	SOSC (32.768 kHz)	N/A	N/A	N/A
Frequency Division	ICLK frequency division setting	N/A	N/A	ICLK = frequency divided by 1
	PCLKB frequency division setting	ICLK ≤ PCLKB	ICLK ≤ PCLKB	ICLK ≠ PCLKB

Table 4-30 Typical Error Conditions (when Not Selected as Clock Source)

Error Check Condition for Clock and Frequency Division Settings (Clock Operation Enabled when Not Selected as Clock Source)		Boost Mode (BOOST) ≤ 64 MHz	Normal Mode (High-speed) ≤ 32 MHz	Low Leakage Current Mode (VBB) = 32.768 kHz
0	HOCO (24, 32, 48, or 64 MHz)	N/A	• HOCO setting ≥ 48 MHz	• When HOCO is selected
1	MOCO (2 MHz)	N/A	N/A	• When MOCO is selected
2	LOCO (32.768 kHz)	N/A	N/A	N/A
3	MOSC (8 to 32 MHz)	N/A	N/A	• When MOSC is selected
4	SOSC (32.768 kHz)	N/A	N/A	N/A

4.2 Constants and Macros

4.2.1 Option-Setting Memory (OptionSettingMemory)

The values specified for the option-setting memory configuration definitions in section 4.1.22, Option-Setting Memory 0 (SYSTEM_CFG_OFS0), to section 4.1.24, Option-Setting Memory 2 (SYSTEM_CFG_SECMPU_xxx), are defined as the constant OptionSettingMemory.

Name: static const uint32_t OptionSettingMemory[] __attribute__ ((section(".OptionSetting")))

Definition file: system_RE01_256KB.c

4.2.2 Serial Programmer ID Setting (OptionSettingID)

The values specified for the serial programmer ID configuration definitions in section 4.1.25, Option-Setting Memory 3 (SYSTEM_CFG_ID_CODE_PROTECTION_n) (n = 1 to 4), are defined as the constant OptionSettingID.

Name: static const uint32_t OptionSettingID[] __attribute__ ((section(".OptionSettingID")))

Definition file: system_RE01_256KB.c

4.2.3 Access Window Setting (OptionSettingAWS)

The value specified for the access window configuration definition in section 4.1.26, Option-Setting Memory 4 (SYSTEM_CFG_AWS), is defined as the constant OptionSettingAWS.

Name: static const uint32_t OptionSettingAWS[] __attribute__ ((section(".OptionSettingAWS")))

Definition file: system_RE01_256KB.c

4.2.4 System Clock Source Definition Macro (SYSTEM_CLOCK_SEL)

The oscillation frequency of the system clock source specified in section 4.1, Configurations, is calculated and reflected in this macro definition.

Name: SYSTEM_CLOCK_SEL

Definition file: system_RE01_256KB.c

Table 4-31 List of SYSTEM_CLOCK_SEL Settings

Clock Source	Selection by Configuration	SYSTEM_CLOCK_SEL Setting
HOCO (24 MHz)	SYSTEM_CFG_CLOCK_SOURCE = 0 SYSTEM_CFG_HOCO_FREQUENCY = 0	24000000U
HOCO (32 MHz)	SYSTEM_CFG_CLOCK_SOURCE = 0 SYSTEM_CFG_HOCO_FREQUENCY = 1	32000000U
HOCO (48 MHz)	SYSTEM_CFG_CLOCK_SOURCE = 0 SYSTEM_CFG_HOCO_FREQUENCY = 2	48000000U
HOCO (64 MHz)	SYSTEM_CFG_CLOCK_SOURCE = 0 SYSTEM_CFG_HOCO_FREQUENCY = 3	64000000U
MOCO	SYSTEM_CFG_CLOCK_SOURCE = 1	2000000U
LOCO	SYSTEM_CFG_CLOCK_SOURCE = 2	32768U
MOSC	SYSTEM_CFG_CLOCK_SOURCE = 3	SYSTEM_CFG_MOSC_FREQUENCY_HZ
SOSC	SYSTEM_CFG_CLOCK_SOURCE = 4	32768U

4.2.5 System Clock Definition Macro (SYSTEM_CLOCK)

The system clock setting calculated from the oscillation frequency of the system clock source in section 4.2.4, System Clock Source Definition Macro (SYSTEM_CLOCK_SEL), and the frequency division setting in section 4.1.16, System Clock (ICLK)/Peripheral Module Clock (PCLKA) Select (SYSTEM_CFG_ICK_PCKA_DIV), is reflected in this macro.

Name: SYSTEM_CLOCK

Definition file: system_RE01_256KB.c

Table 4-32 List of SYSTEM_CLOCK Settings

Selection by Configuration	SYSTEM_CLOCK Setting
SYSTEM_CFG_ICK_PCKA_DIV = 0	SYSTEM_CLOCK_SEL / 1
SYSTEM_CFG_ICK_PCKA_DIV = 1	SYSTEM_CLOCK_SEL / 2
SYSTEM_CFG_ICK_PCKA_DIV = 2	SYSTEM_CLOCK_SEL / 4
SYSTEM_CFG_ICK_PCKA_DIV = 3	SYSTEM_CLOCK_SEL / 8
SYSTEM_CFG_ICK_PCKA_DIV = 4	SYSTEM_CLOCK_SEL / 16
SYSTEM_CFG_ICK_PCKA_DIV = 5	SYSTEM_CLOCK_SEL / 32
SYSTEM_CFG_ICK_PCKA_DIV = 6	SYSTEM_CLOCK_SEL / 64

4.2.6 System Clock Wait Cycle Definitions

Definition file: system_RE01_256KB.c

Table 4-33 System Clock Wait Cycles

Macro Definition	Setting	Remarks
ICLK_1CYCLE	(1.0F / SYSTEM_CLOCK)	One ICLK-cycle time
ICLK_MOCO_1CYCLE	(0.0000005F)	One MOCO cycle time 0.5 us
MOCO_TMOCOWT_SEC	(0.000016F)	MOCO oscillation stabilization time 16 us
MOCO_RESTART_SEC	(0.0000025F)	MOCO restart time 2.5 us
LOCO_TLOCOWT_SEC	(0.000130F)	LOCO oscillation stabilization time 130 us
LOCO_RESTART_SEC	(0.0001525879F)	LOCO restart time 0.1525879 ms
SOSC_SUBOSCOWT_SEC	(3.0F)	Sub-clock oscillation stabilization time 3 s
SOSC_RESTART_SEC	(0.0001525879F)	Sub-clock restart time 0.1525879 ms
LOCO_TLOCOWT_TIME_START	(((LOCO_TLOCOWT_SEC / ICLK_MOCO_1CYCLE) / 4) + 1)	Number of software loops for LOCO oscillation stabilization
LOCO_RESTART_TIME_START	(((LOCO_RESTART_SEC / ICLK_MOCO_1CYCLE) / 4) + 1)	Number of software loops for restarting LOCO
SOSC_TSUBOSCOWT_TIME_START	(((SOSC_SUBOSCOWT_SEC / ICLK_MOCO_1CYCLE) / 4) + 1)	Number of software loops for SOSC oscillation stabilization
SOSC_RESTART_TIME_START	(((SOSC_RESTART_SEC / ICLK_MOCO_1CYCLE) / 4) + 1)	Number of software loops for restarting SOSC
MOCO_TMOCOWT_TIME_STOP	(((MOCO_TMOCOWT_SEC / ICLK_1CYCLE) / 4) + 1)	Number of software loops for MOCO oscillation stabilization
MOCO_RESTART_TIME_STOP	(((MOCO_RESTART_SEC / ICLK_1CYCLE) / 4) + 1)	Number of software loops for restarting MOCO
LOCO_TLOCOWT_TIME_STOP	(((LOCO_TLOCOWT_SEC / ICLK_1CYCLE) / 4) + 1)	Number of software loops for LOCO oscillation stabilization
LOCO_RESTART_TIME_STOP	(((LOCO_RESTART_SEC / ICLK_1CYCLE) / 4) + 1)	Number of software loops for restarting LOCO
SOSC_TSUBOSCOWT_TIME_STOP	(((SOSC_SUBOSCOWT_SEC / ICLK_1CYCLE) / 4) + 1)	Number of software loops for SOSC oscillation stabilization
SOSC_RESTART_TIME_STOP	(((SOSC_RESTART_SEC / ICLK_1CYCLE) / 4) + 1)	Number of software loops for restarting SOSC
LOCO_TLOCOWT_TIME_START_ALONE	(((LOCO_TLOCOWT_SEC / ICLK_1CYCLE) / 4) + 1)	Number of software loops for LOCO oscillation stabilization
LOCO_RESTART_TIME_START_ALONE	(((LOCO_RESTART_SEC / ICLK_1CYCLE) / 4) + 1)	Number of software loops for restarting LOCO
SOSC_TSUBOSCOWT_TIME_START_ALONE	(((SOSC_SUBOSCOWT_SEC / ICLK_1CYCLE) / 4) + 1)	Number of software loops for SOSC oscillation stabilization
SOSC_RESTART_TIME_START_ALONE	(((SOSC_RESTART_SEC / ICLK_1CYCLE) / 4) + 1)	Number of software loops for restarting SOSC

4.3 Function Specifications

4.3.1 system_clock_init Function

Table 4-34 system_clock_init Function Specifications

Format	void system_clock_init(void)
Description	Initializes the operating frequency of the clock source and the power control mode in accordance with the settings in r_core_cfg.h.
Argument	None
Return value	None
Remarks	—

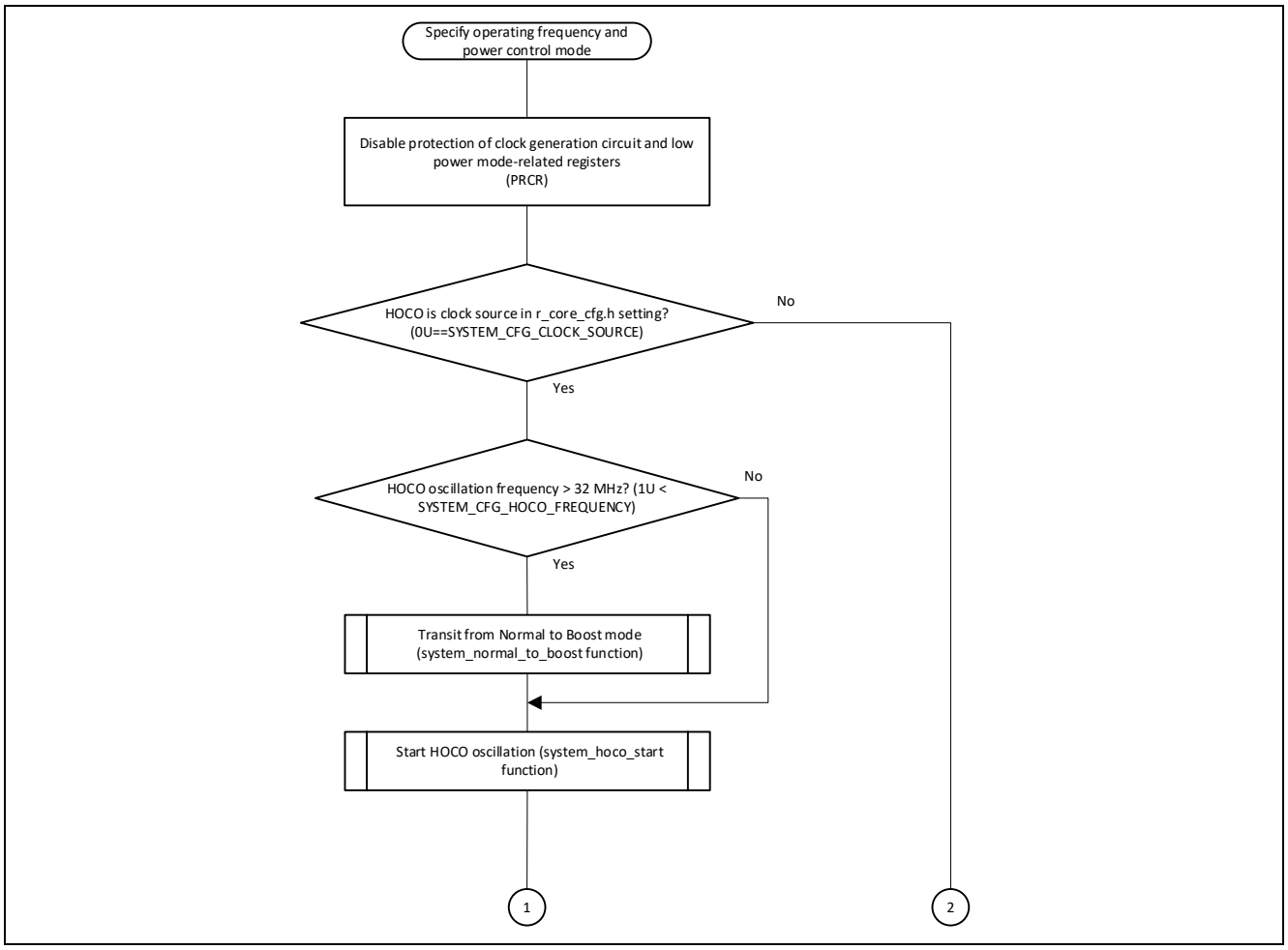


Figure 4-2 system_clock_init Function Processing Flow (1/5)

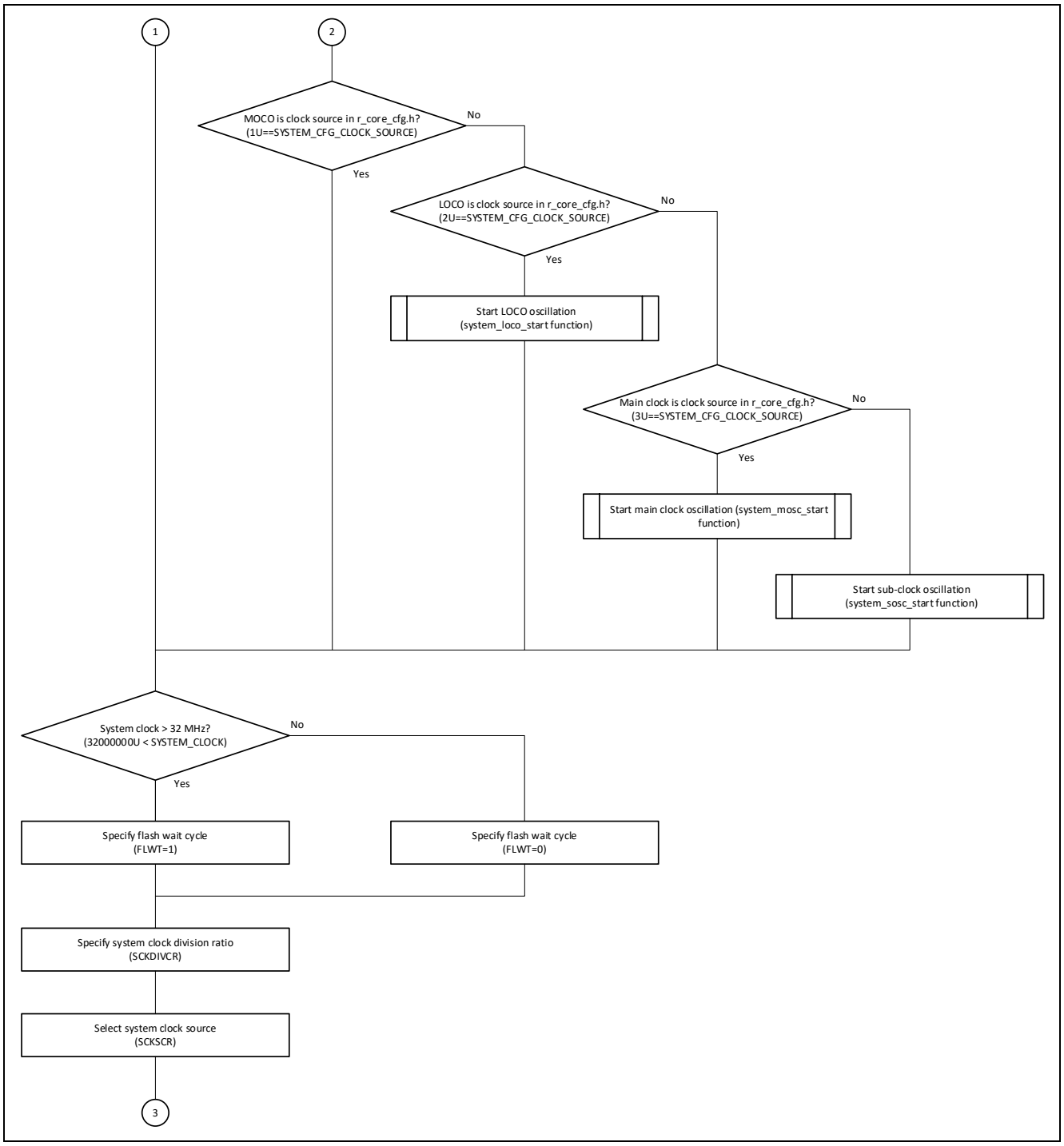


Figure 4-3 system_clock_init Function Processing Flow (2/5)

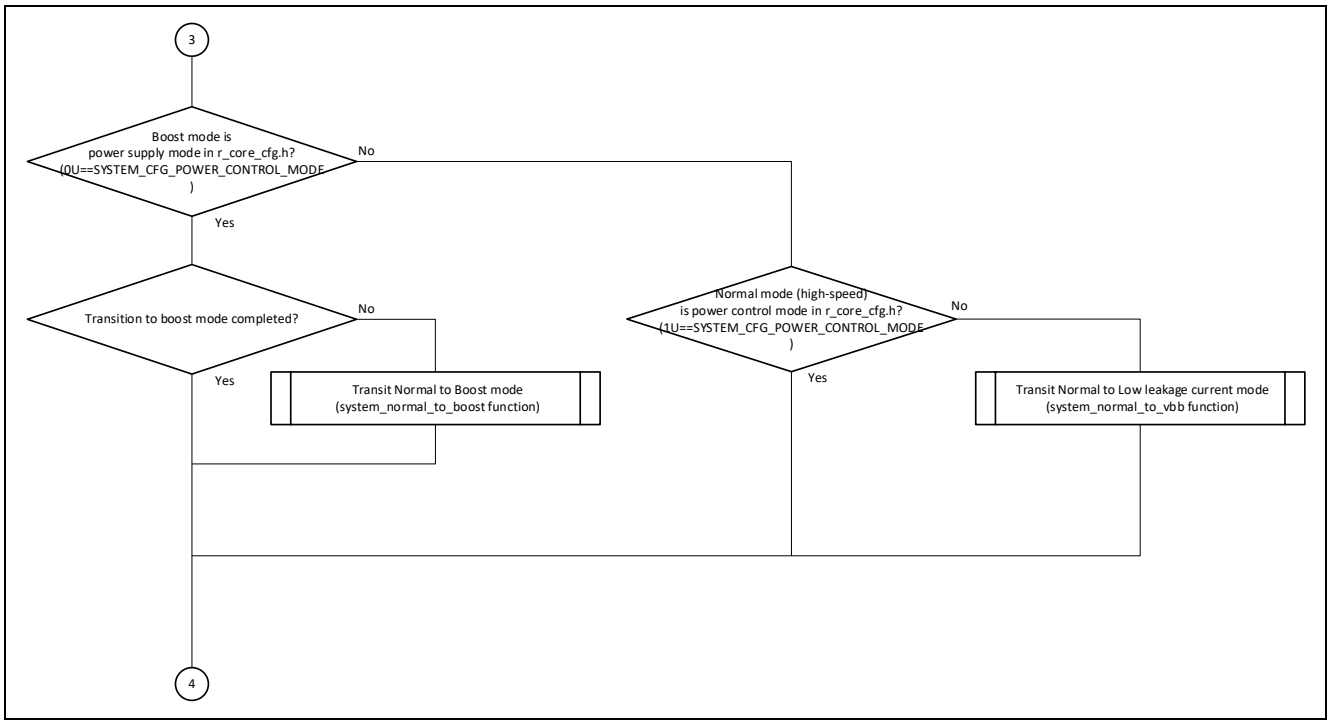


Figure 4-4 system_clock_init Function Processing Flow (3/5)

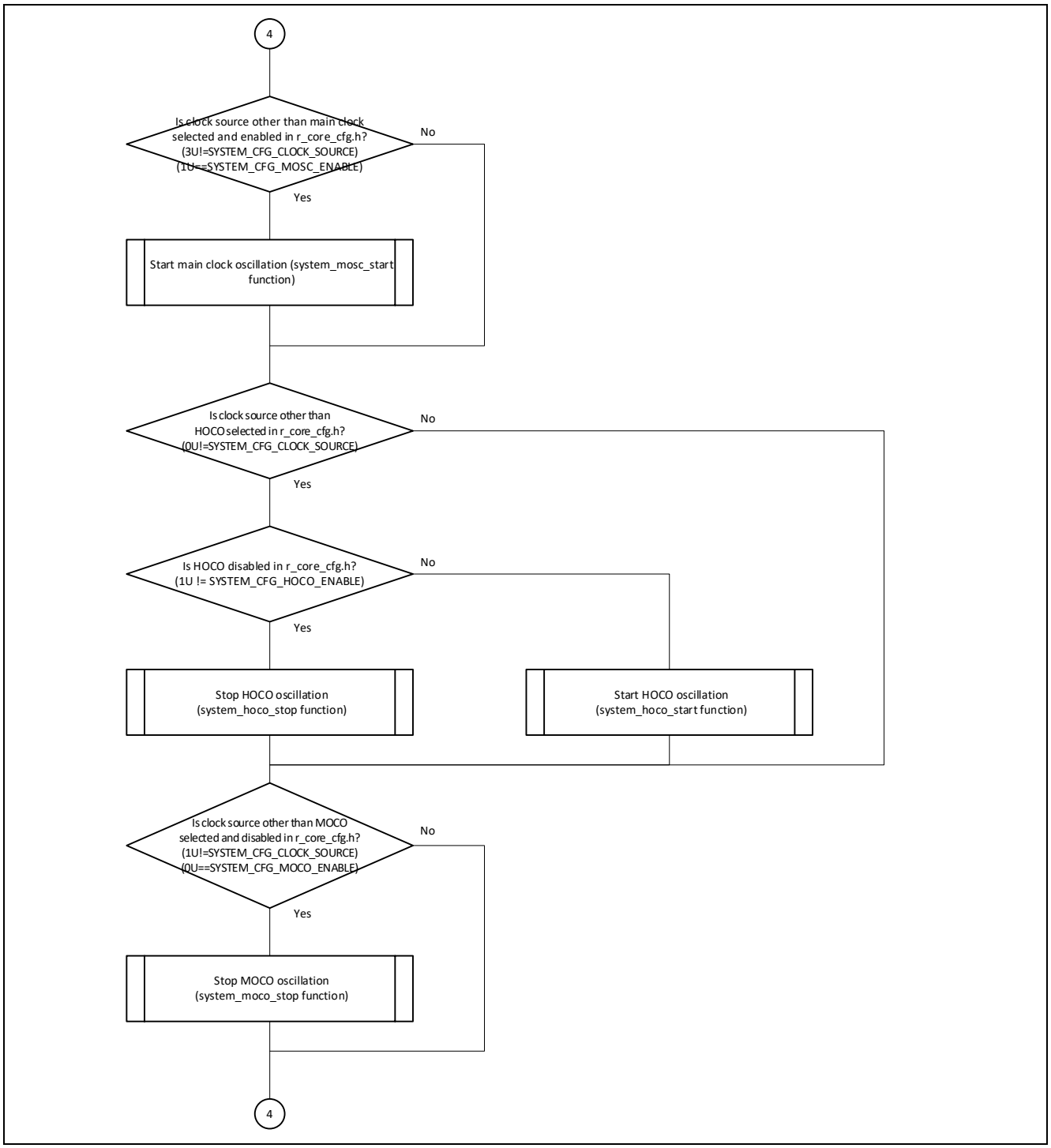


Figure 4-5 system_clock_init Function Processing Flow (4/5)

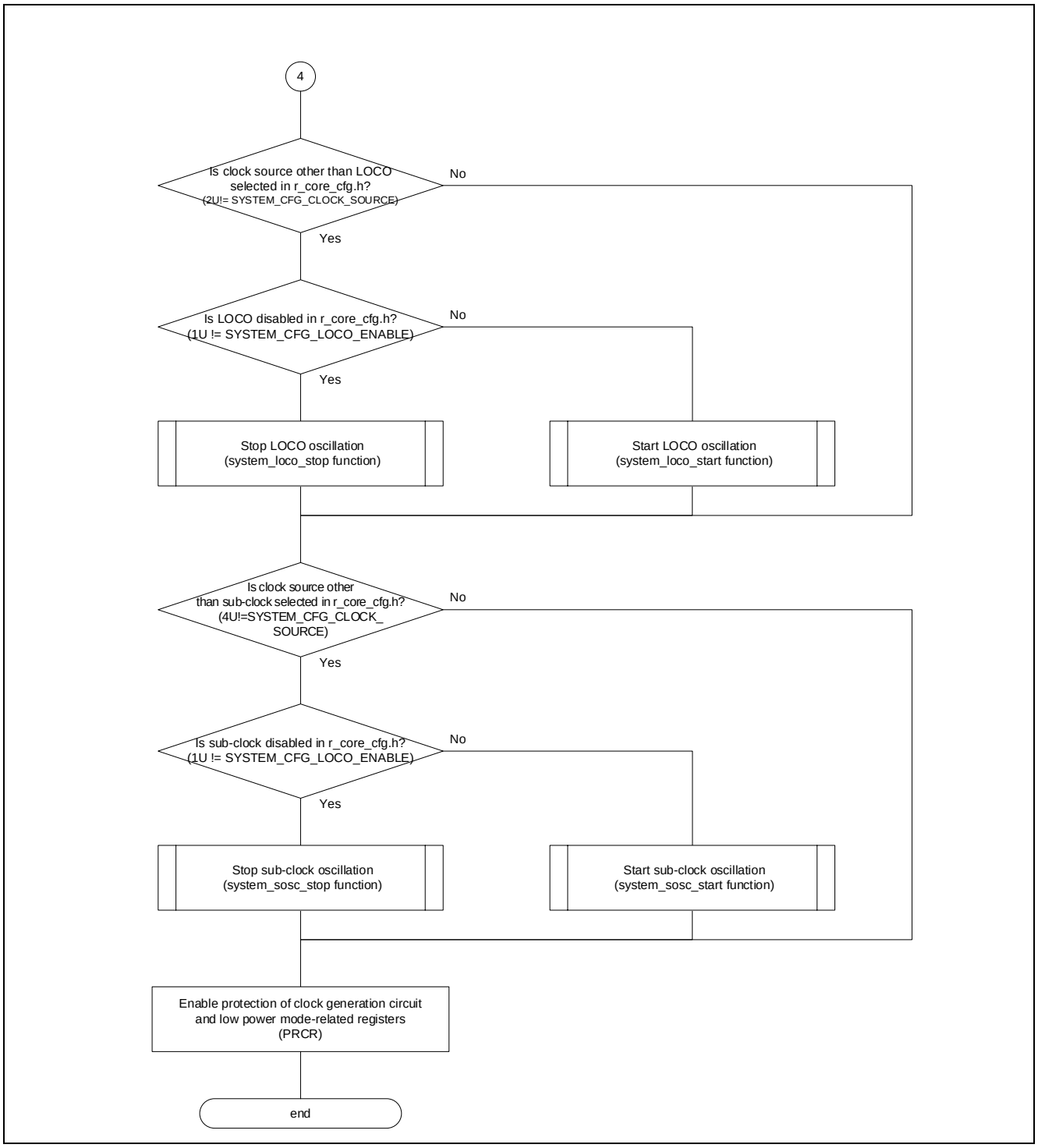


Figure 4-6 system_clock_init Function Processing Flow (5/5)

4.3.2 system_mosc_start Function

Table 4-35 system_mosc_start Function Specifications

Format	void system_mosc_start(void)
Description	Starts the operation of the main clock.
Argument	None
Return value	None
Remarks	—

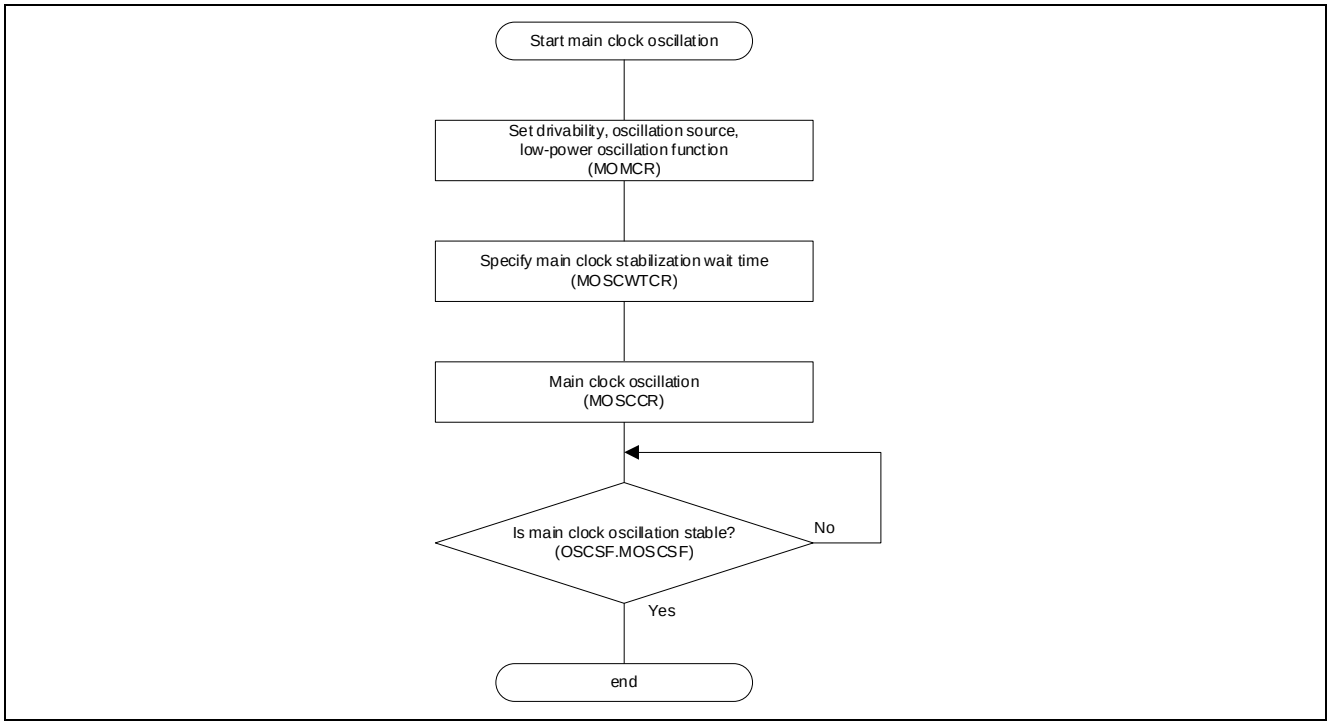


Figure 4-7 system_mosc_start Function Processing Flow

4.3.3 system_mosc_stop Function

Table 4-36 system_mosc_stop Function Specifications

Format	void system_mosc_stop(void)
Description	Stops the operation of the main clock.
Argument	None
Return value	None
Remarks	—

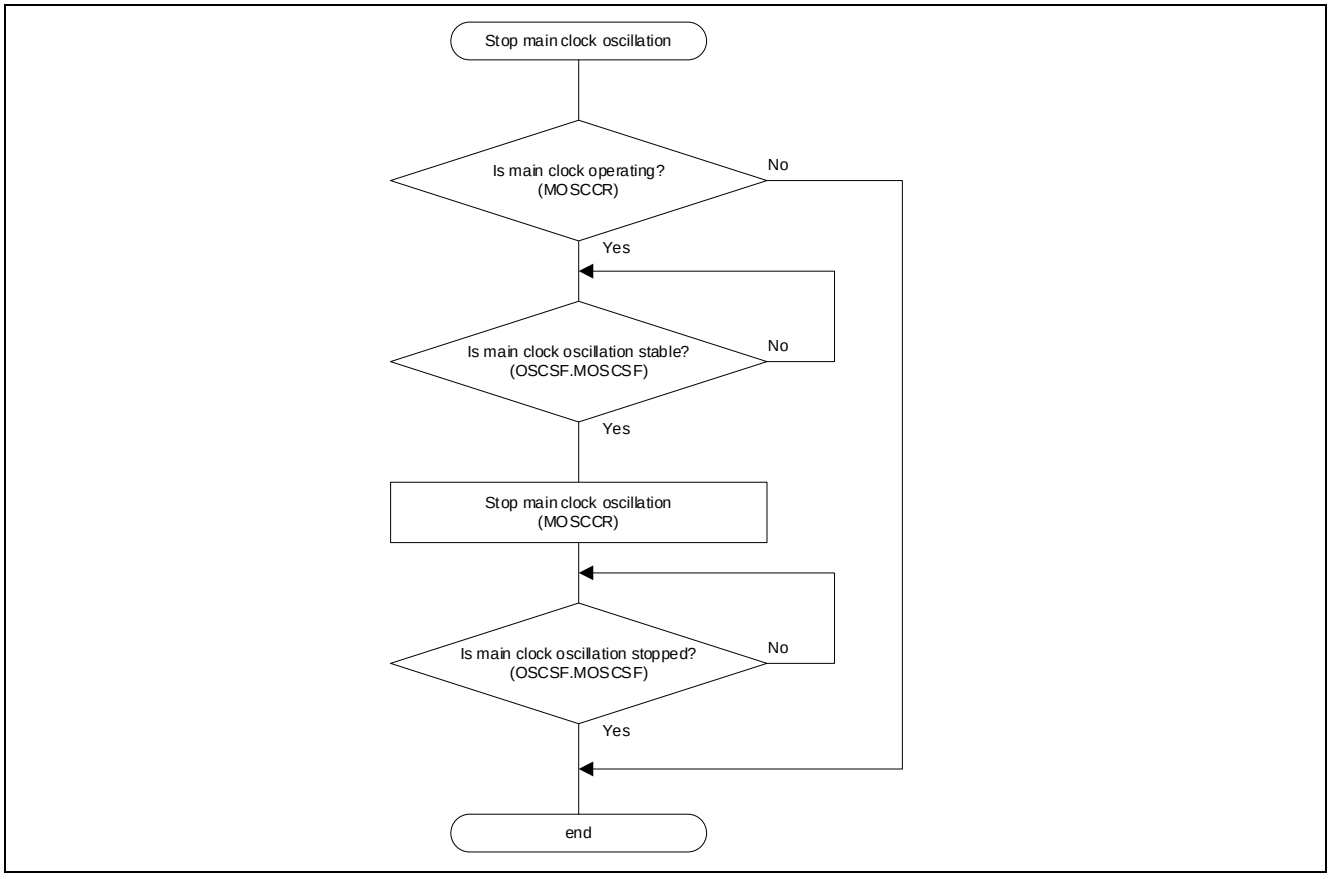


Figure 4-8 system_mosc_stop Function Processing Flow

4.3.4 system_hoco_start Function

Table 4-37 system_hoco_start Function Specifications

Format	void system_hoco_start(void)
Description	Starts the operation of the high-speed on-chip oscillator.
Argument	None
Return value	None
Remarks	—

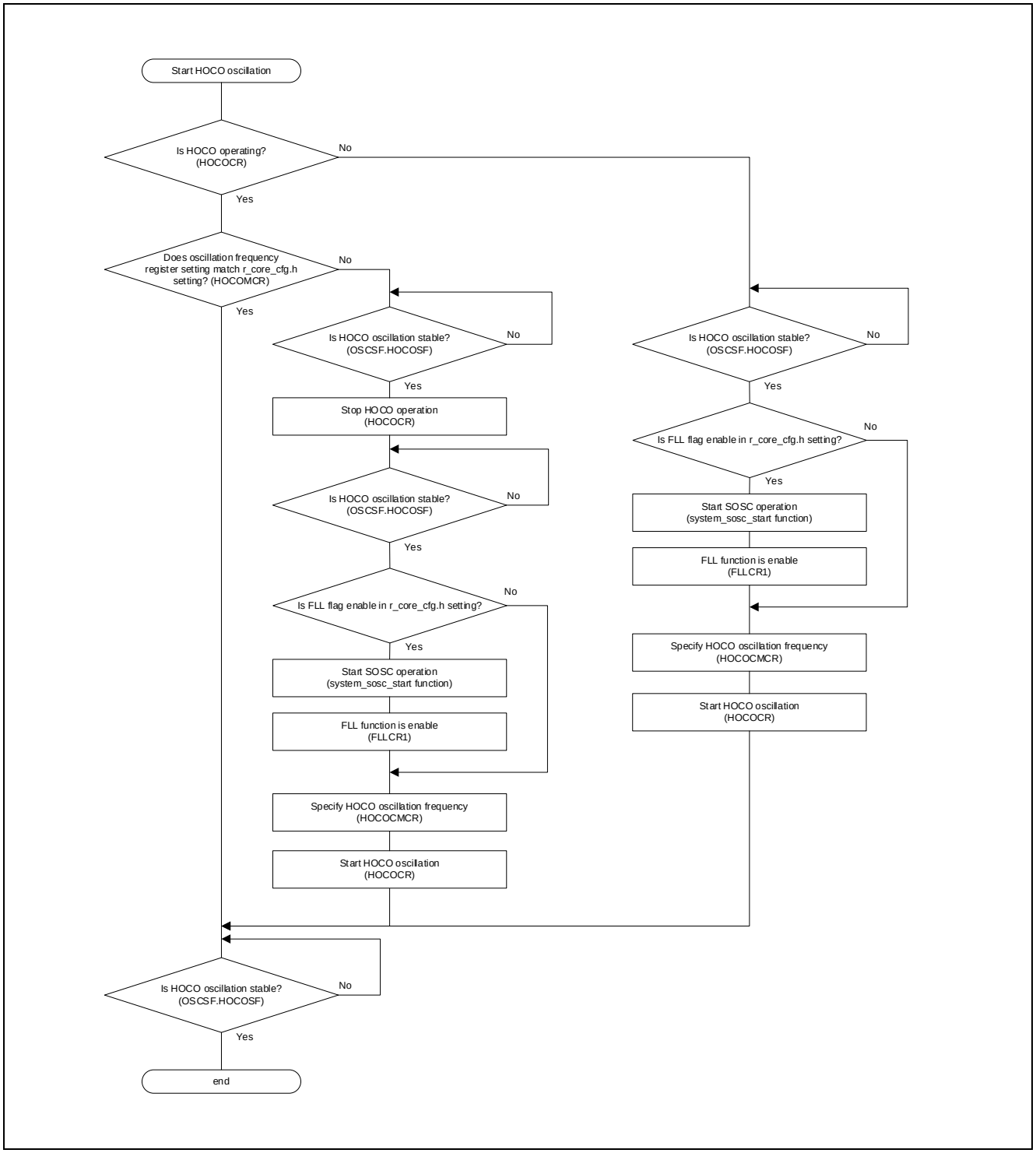


Figure 4-9 system_hoco_start Function Processing Flow

4.3.5 system_hoco_stop Function

Table 4-38 system_hoco_stop Function Specifications

Format	void system_hoco_stop(void)
Description	Stops the operation of the high-speed on-chip oscillator.
Argument	None
Return value	None
Remarks	—

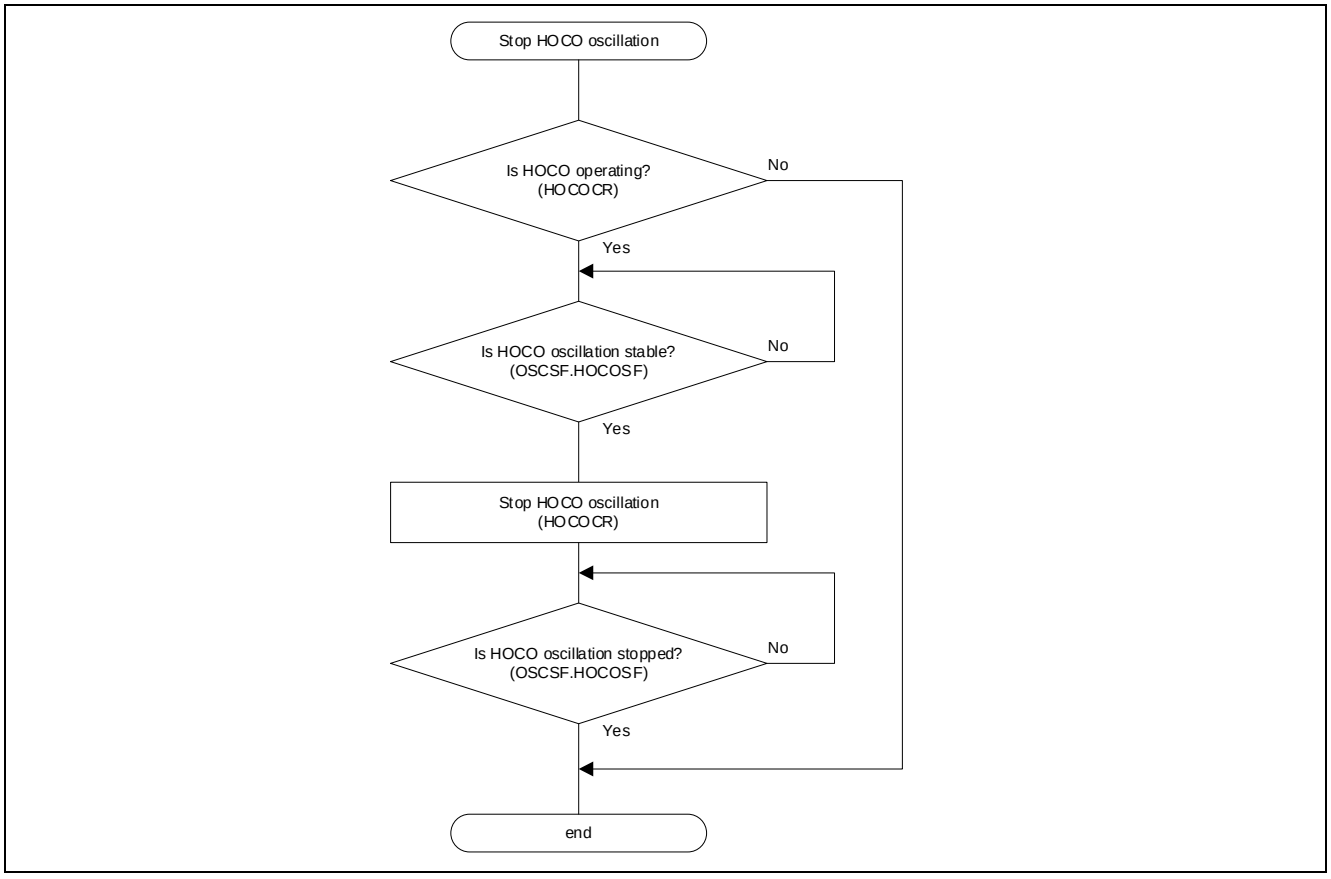


Figure 4-10 system_hoco_stop Function Processing Flow

4.3.6 system_moco_stop Function

Table 4-39 system_moco_stop Function Specifications

Format	void system_moco_stop(void)
Description	Stops the operation of the middle-speed on-chip oscillator.
Argument	None
Return value	None
Remarks	—

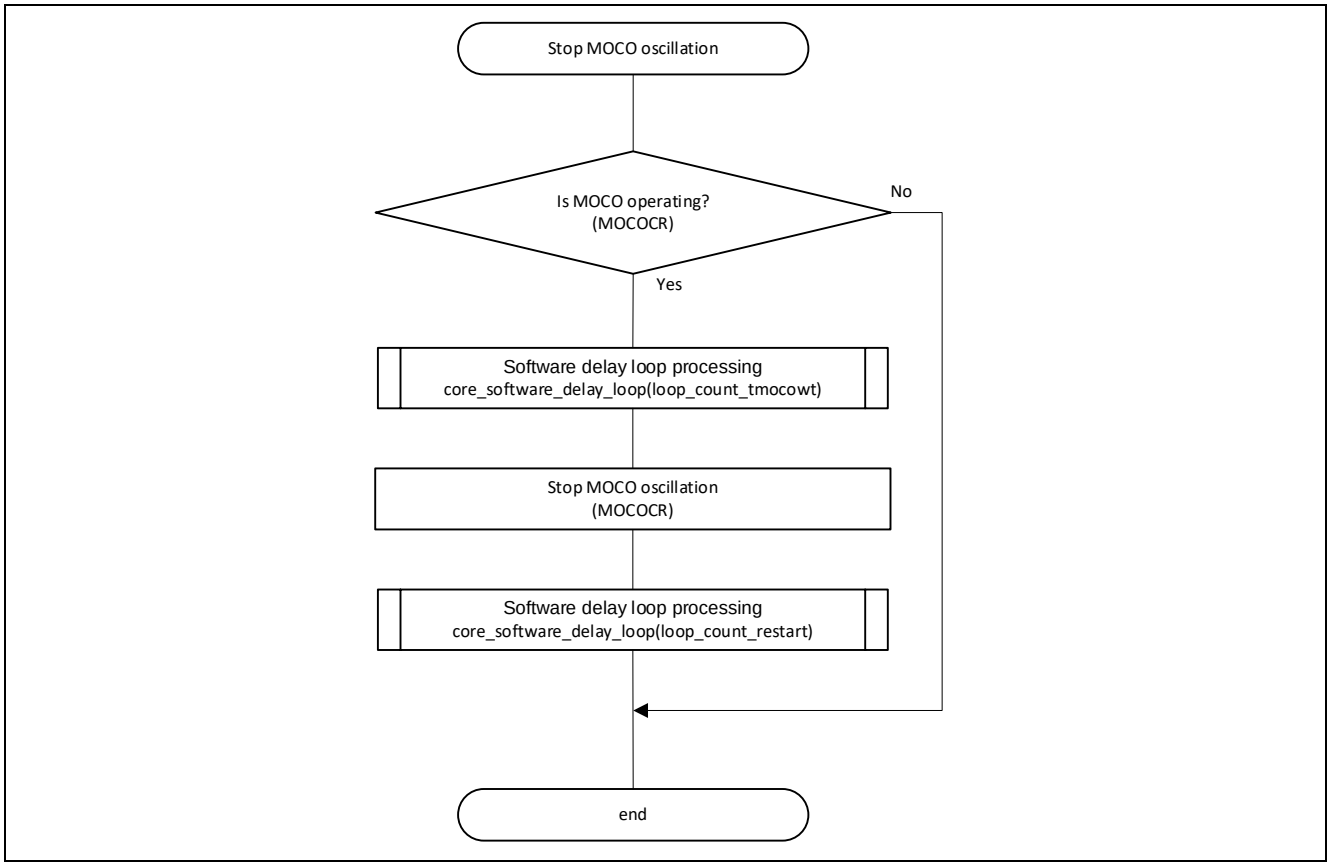


Figure 4-11 system_moco_stop Function Processing Flow

4.3.7 system_loco_start Function

Table 4-40 system_loco_start Function Specifications

Format	void system_loco_start(void)
Description	Starts the operation of the low-speed on-chip oscillator.
Argument	None
Return value	None
Remarks	—

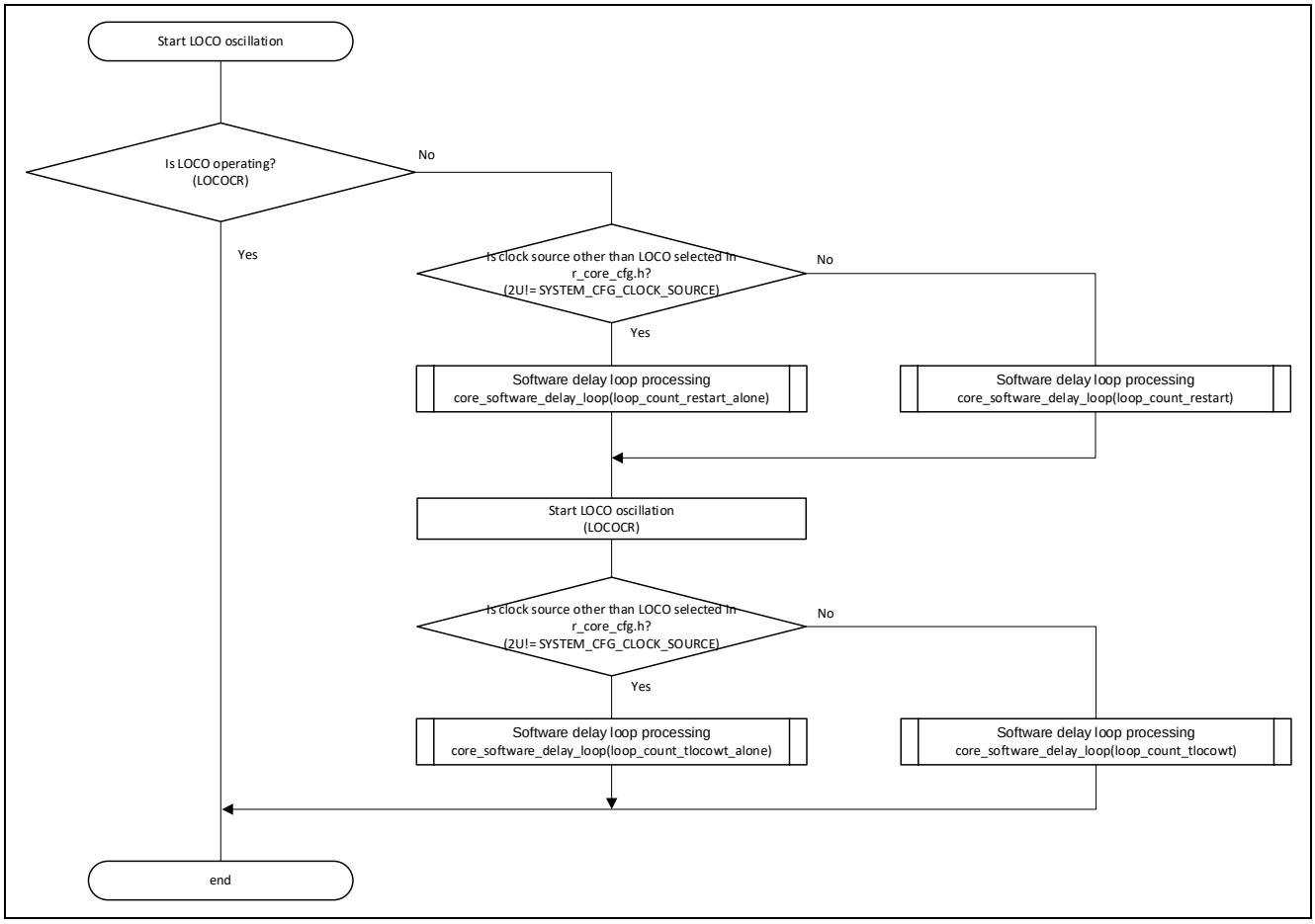


Figure 4-12 system_loco_start Function Processing Flow

4.3.8 system_loco_stop Function

Table 4-41 system_loco_stop Function Specifications

Format	void system_loco_stop(void)
Description	Stops the operation of the low-speed on-chip oscillator.
Argument	None
Return value	None
Remarks	—

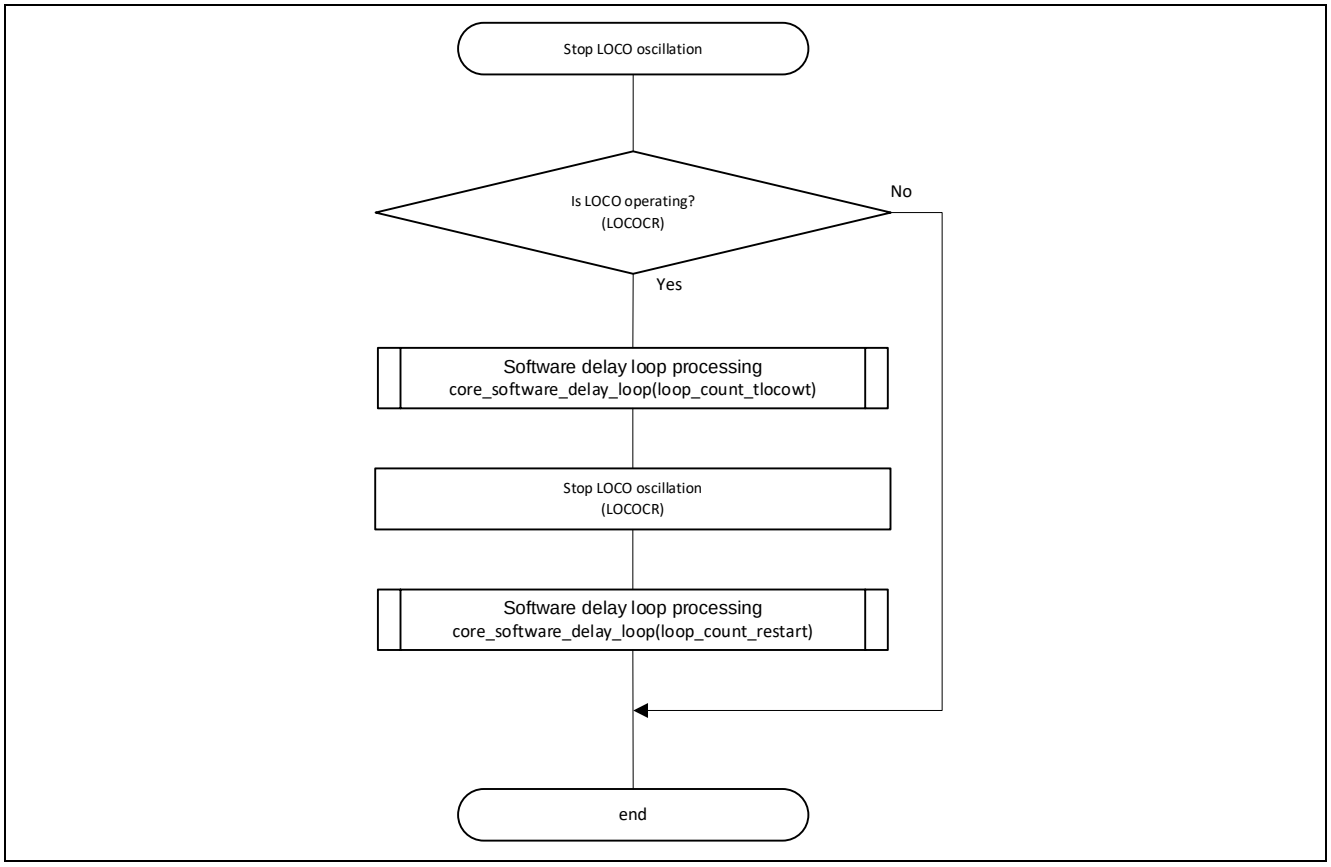


Figure 4-13 system_loco_stop Function Processing Flow

4.3.9 system_sosc_start Function

Table 4-42 system_sosc_start Function Specifications

Format	void system_sosc_start(void)
Description	Starts the operation of the sub-clock.
Argument	None
Return value	None
Remarks	—

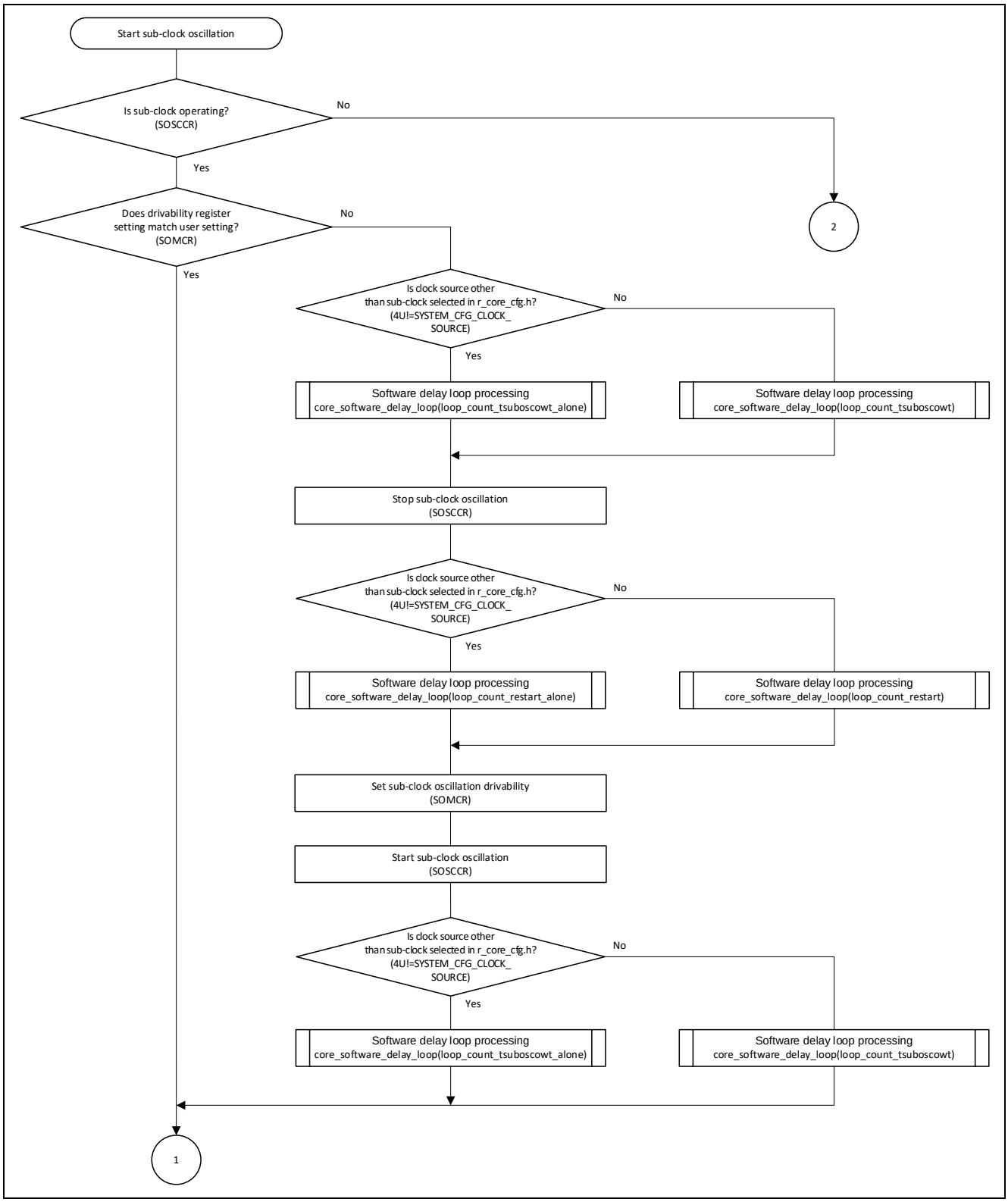


Figure 4-14 system_sosc_start Function Processing Flow (1/2)

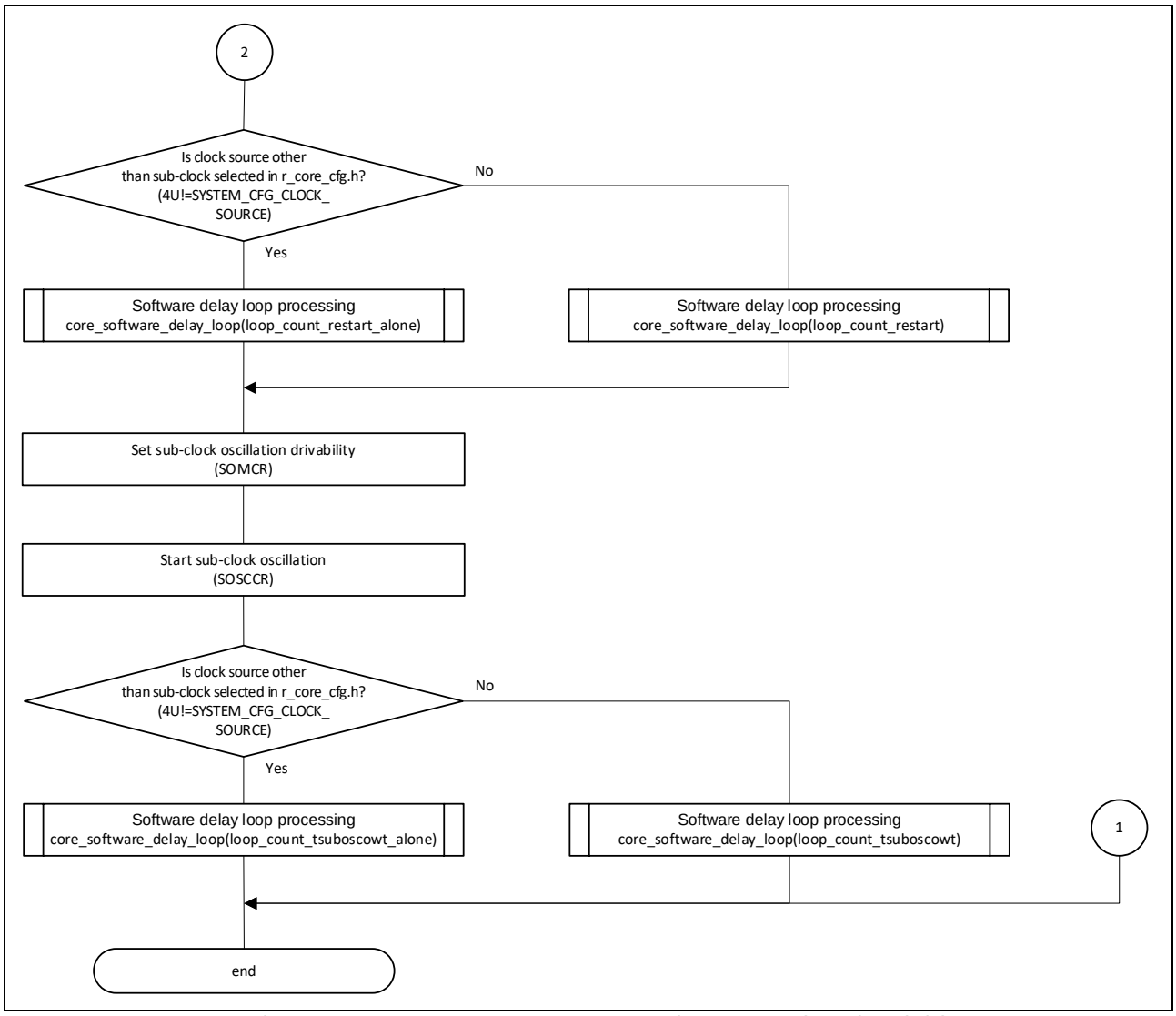


Figure 4-15 system_sosc_start Function Processing Flow (2/2)

4.3.10 system_sosc_stop Function

Table 4-43 system_sosc_stop Function Specifications

Format	void system_sosc_stop(void)
Description	Stops the operation of the sub-clock.
Argument	None
Return value	None
Remarks	—

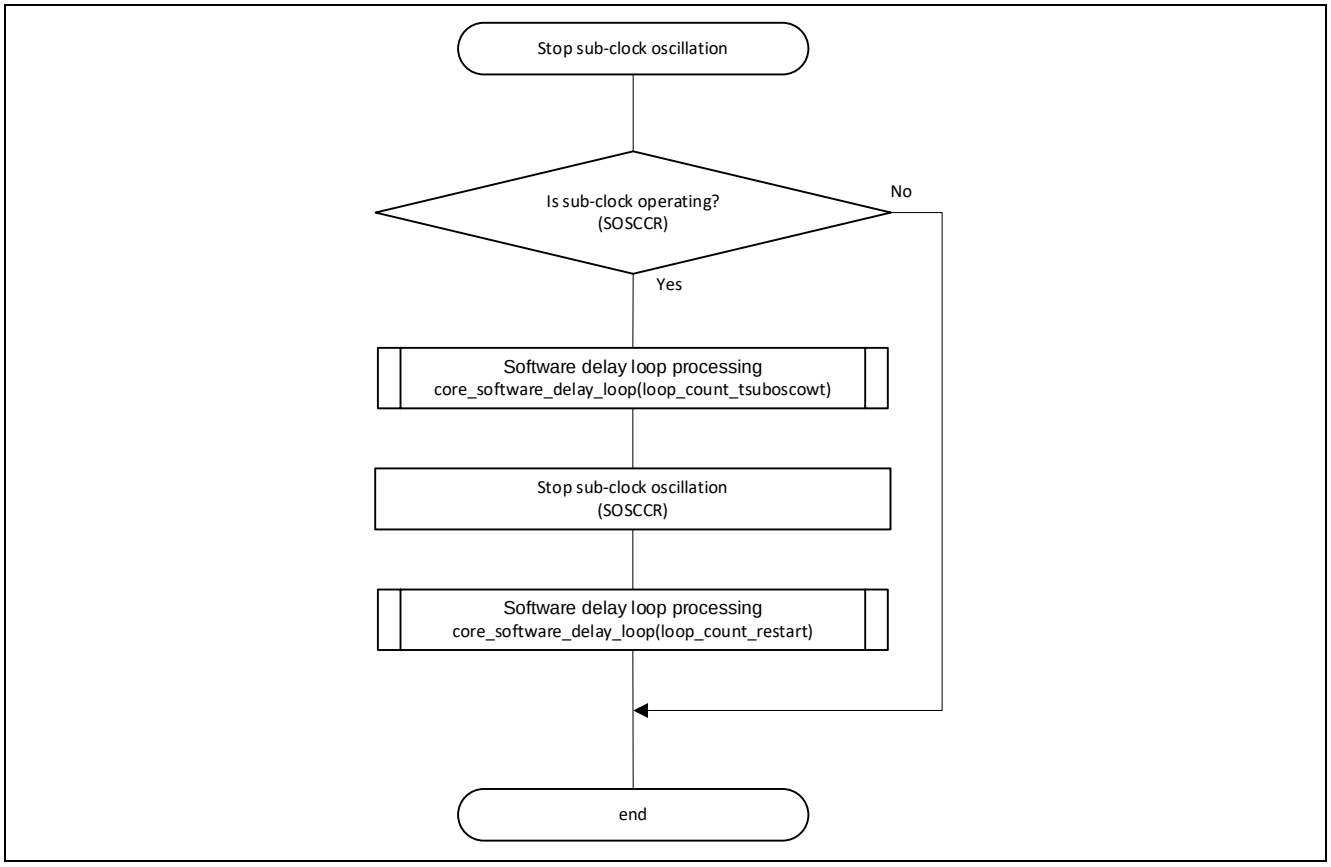


Figure 4-16 system_sosc_stop Function Processing Flow

4.3.11 system_normal_to_boost Function

Table 4-44 system_normal_to_boost Function Specifications

Format	void system_normal_to_boost(void)
Description	Switches the power control mode from normal mode (high-speed) to boost mode.
Argument	None
Return value	None
Remarks	—

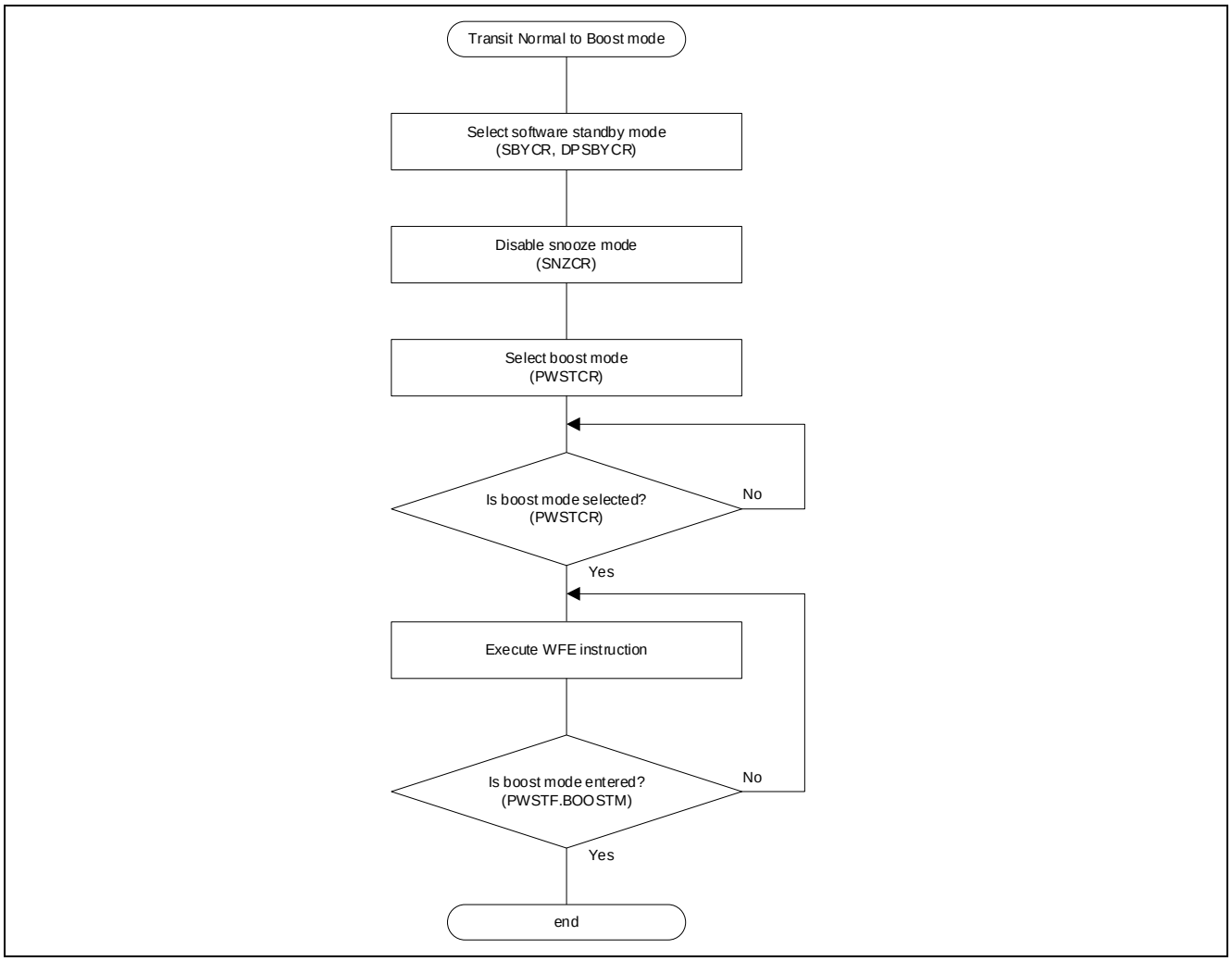


Figure 4-17 system_normal_to_boost Function Processing Flow

4.3.12 system_normal_to_vbb Function

Table 4-45 system_normal_to_vbb Function Specifications

Format	void system_normal_to_vbb(void)
Description	Switches the power control mode from normal mode (high-speed) to low leakage current (VBB) mode.
Argument	None
Return value	None
Remarks	—

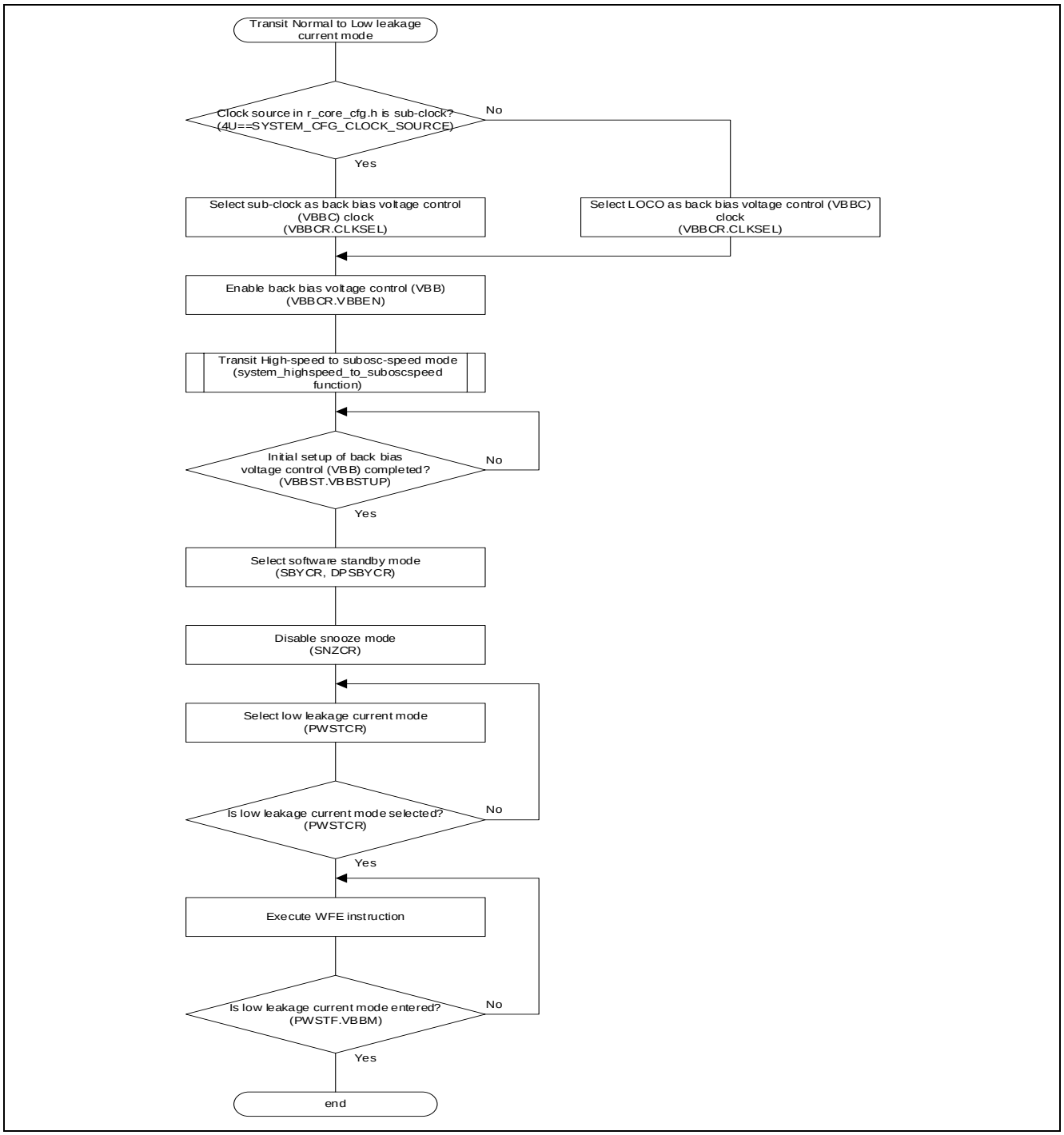


Figure 4-18 system_normal_to_vbb Function Processing Flow

4.3.13 Reset_Handler Function

Table 4-46 Reset_Handler Function Specifications

Format	void Reset_Handler(void)
Description	Performs the initial operation at startup.
Argument	None
Return value	None
Remarks	—

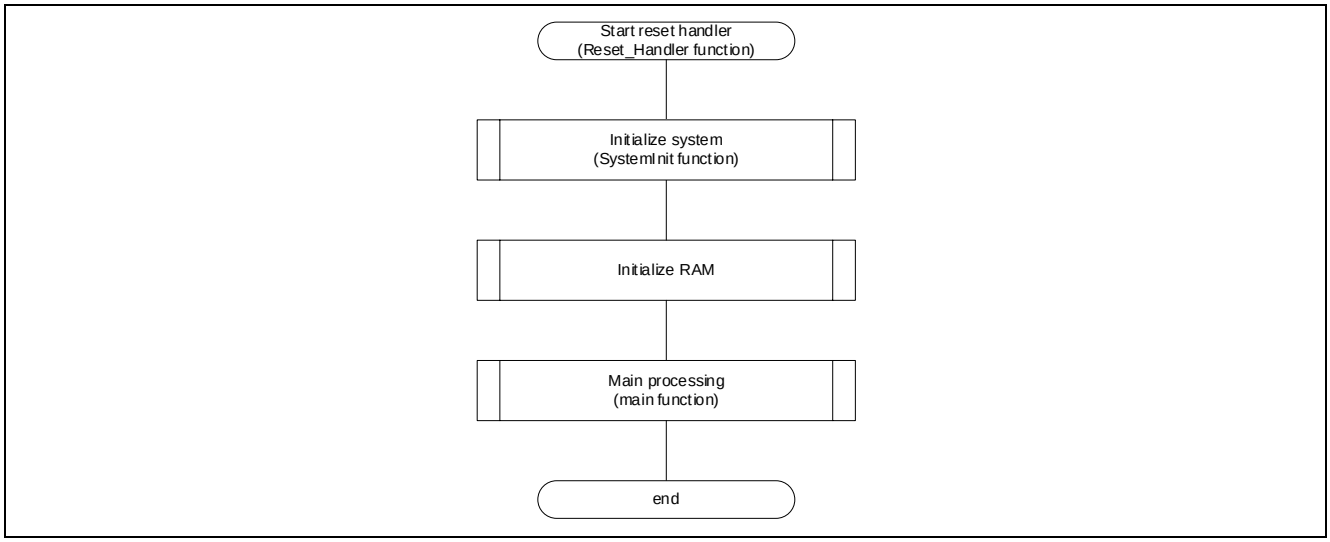


Figure 4-19 Reset_Handler Function Processing Flow

4.3.14 SystemInit Function

Table 4-47 SystemInit Function Specifications

Format	void SystemInit(void)
Description	Performs system initialization at startup.
Argument	None
Return value	None
Remarks	—

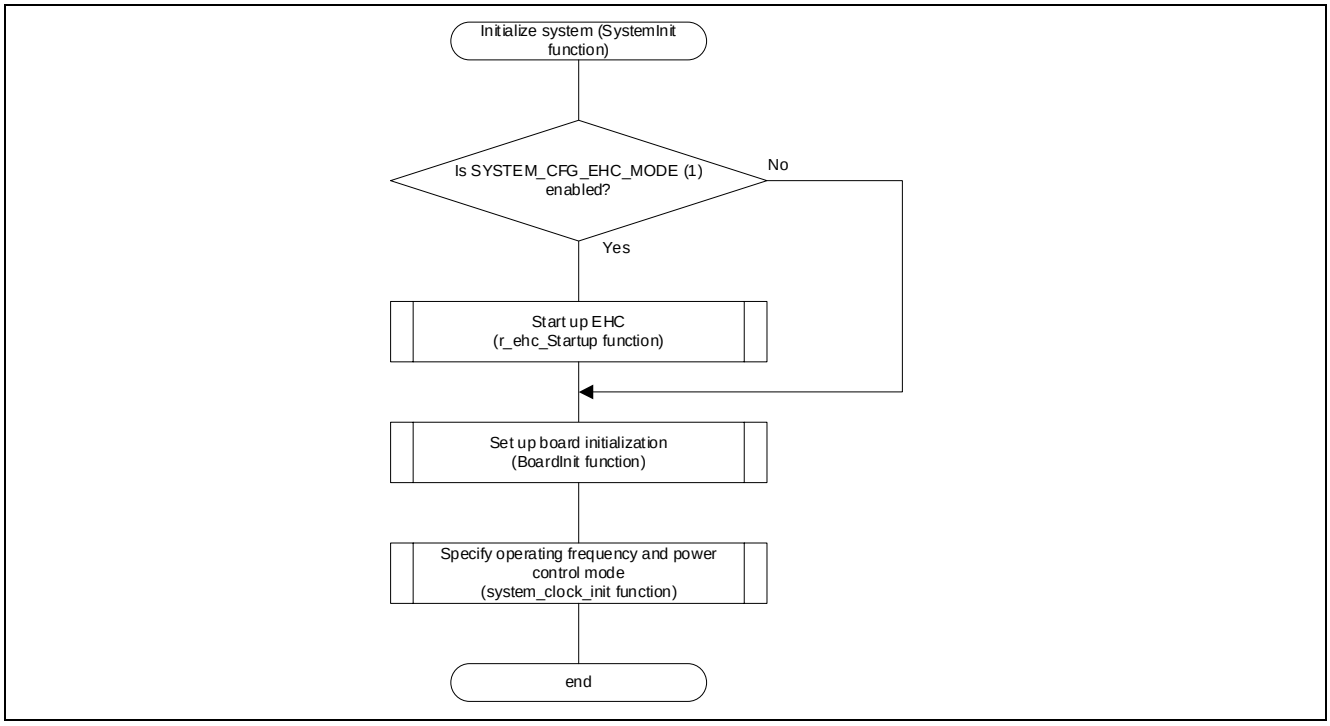


Figure 4-20 SystemInit Function Processing Flow

4.4 Appendix

4.4.1 List of Preprocessor Errors

Table 4-48 List of Preprocessor Errors

No.	Error	Configuration Check
1	"ERROR - HOCO frequency can not selected Normal mode (High-speed) (r_core_cfg.h)."	• The current configuration is illegal in normal mode (high-speed) when HOCO is selected as the system clock. Check the following configuration settings. SYSTEM_CFG_POWER_CONTROL_MODE SYSTEM_CFG_CLOCK_SOURCE SYSTEM_CFG_HOCO_FREQUENCY
2		• The current configuration is illegal when HOCO is not selected as the system clock. Check the following configuration settings. SYSTEM_CFG_HOCO_ENABLE SYSTEM_CFG_HOCO_FREQUENCY SYSTEM_CFG_POWER_CONTROL_MODE
3	"ERROR - HOCO frequency can not selected Low-Leakage-Current mode (VBB) (r_core_cfg.h)."	• The current configuration is illegal in low leakage current mode (VBB) when HOCO is selected as the system clock. Check the following configuration settings. SYSTEM_CFG_POWER_CONTROL_MODE SYSTEM_CFG_CLOCK_SOURCE
4		• The current configuration is illegal when HOCO is not selected as the system clock. Check the following configuration settings. SYSTEM_CFG_HOCO_ENABLE SYSTEM_CFG_POWER_CONTROL_MODE
5	"ERROR - HOCO frequency parameter of enable select is out of range (r_core_cfg.h)."	• The current configuration is illegal for HOCO. Check the following configuration setting. SYSTEM_CFG_HOCO_ENABLE
6	"ERROR - HOCO frequency (r_core_cfg.h)"	• The current configuration is illegal for HOCO. Check the following configuration setting. SYSTEM_CFG_HOCO_FREQUENCY
7	"ERROR - MOCO frequency can not selected Low-Leakage-Current mode (VBB) (r_core_cfg.h)"	• The current configuration is illegal in low leakage current mode (VBB) when MOCO is selected as the system clock. Check the following configuration settings. SYSTEM_CFG_POWER_CONTROL_MODE SYSTEM_CFG_CLOCK_SOURCE
8		• The current configuration is illegal when MOCO is not selected as the system clock. Check the following configuration settings. SYSTEM_CFG_MOCO_ENABLE SYSTEM_CFG_POWER_CONTROL_MODE
9	"ERROR - MOCO frequency parameter of enable select is out of range (r_core_cfg.h)."	• The current configuration is illegal for MOCO stop. Check the following configuration setting. SYSTEM_CFG_MOCO_ENABLE
10	"ERROR - LOCO frequency division ratio (r_core_cfg.h)"	• The current configuration is illegal in low leakage current mode (VBB) when LOCO is selected as the system clock.

		Check the following configuration settings. SYSTEM_CFG_POWER_CONTROL_MODE SYSTEM_CFG_CLOCK_SOURCE SYSTEM_CFG_ICK_PCKA_DIV SYSTEM_CFG_PCKB_DIV
11	"ERROR - LOCO frequency parameter of enable select is out of range (r_core_cfg.h)."	• The current configuration is illegal for LOCO stop. Check the following configuration setting. SYSTEM_CFG_LOCO_ENABLE
12	"ERROR - MOSC frequency out of range (r_core_cfg.h)"	• The current configuration is illegal when the main clock (MOSC) is selected as the system clock. Check the following configuration settings. SYSTEM_CFG_MOSC_FREQUENCY_HZ SYSTEM_CFG_CLOCK_SOURCE
13	"ERROR - MOSC frequency selected Low-Leakage-Current mode (VBB) (r_core_cfg.h)"	• The current configuration is illegal when the main clock (MOSC) is selected as the system clock. Check the following configuration settings. SYSTEM_CFG_POWER_CONTROL_MODE SYSTEM_CFG_CLOCK_SOURCE
14	"ERROR - MOSC frequency can not selected Low-Leakage-Current mode (VBB) (r_core_cfg.h)."	• The current configuration is illegal when the main clock (MOSC) is not selected as the system clock. Check the following configuration settings. SYSTEM_CFG_MOSC_ENABLE SYSTEM_CFG_POWER_CONTROL_MODE
15	"ERROR - MOSC frequency parameter of enable select is out of range (r_core_cfg.h)."	• The current configuration is illegal for the main clock (MOSC). Check the following configuration setting. SYSTEM_CFG_MOSC_ENABLE
16	"ERROR - MOSC frequency (r_core_cfg.h)"	• The current configuration is illegal for the main clock (MOSC). Check the following configuration settings. SYSTEM_CFG_MOSC_FREQUENCY_HZ SYSTEM_CFG_MOSC_CLOCK_SOURCE
17	"ERROR - MOSC frequency parameter of drive capability select is out of range (r_core_cfg.h)"	• The current configuration is illegal for the main clock (MOSC). Check the following configuration setting. SYSTEM_CFG_MOSC_DRIVE
18	"ERROR - MOSC frequency parameter of clock source select is out of range (r_core_cfg.h)."	• The current configuration is illegal for the main clock (MOSC). Check the following configuration setting. SYSTEM_CFG_MOSC_CLOCK_SOURCE
19	"ERROR - MOSC frequency parameter of low power enable select is out of range (r_core_cfg.h)."	• The current configuration is illegal for the main clock (MOSC). Check the following configuration setting. SYSTEM_CFG_MOSC_LOW_POWER_ENABLE
20	"ERROR - MOSC frequency parameter of stabilization time select is out of range (r_core_cfg.h)"	• The current configuration is illegal for the main clock (MOSC). Check the following configuration setting. SYSTEM_CFG_MOSC_WAIT_TIME
21	"ERROR - SOSC frequency division ratio (r_core_cfg.h)"	• The current configuration is illegal when the sub-clock (SOSC) is selected as the system clock. Check the following configuration settings. SYSTEM_CFG_POWER_CONTROL_MODE SYSTEM_CFG_CLOCK_SOURCE SYSTEM_CFG_ICK_PCKA_DIV

		SYSTEM_CFG_PCKB_DIV
22	"ERROR - SOSC frequency parameter of enable select is out of range (r_core_cfg.h)."	• The current configuration is illegal for the sub-clock (SOSC). Check the following configuration setting. SYSTEM_CFG_SOSC_ENABLE
23	"ERROR - SOSC frequency parameter of drive capability select is out of range (r_core_cfg.h)."	• The current configuration is illegal for the sub-clock (SOSC). Check the following configuration setting. SYSTEM_CFG_SOSC_DRIVE
24	"ERROR - SOSC frequency parameter of noise filter select is out of range (r_core_cfg.h)."	• The current configuration is illegal for the sub-clock (SOSC). Check the following configuration setting. SYSTEM_CFG_SOSC_NF_STOP
25	"ERROR - Clock source select is out of range (r_core_cfg.h)"	• The current configuration is illegal for the clock source selection. Check the following configuration setting. SYSTEM_CFG_CLOCK_SOURCE
26	"ERROR - ICLK and PCLKA frequency division ratio select is out of range (r_core_cfg.h)"	• The current configuration is illegal for the system clock (ICLK)/peripheral module clock (PCLKA) selection. Check the following configuration setting. SYSTEM_CFG_ICK_PCKA_DIV
27	"ERROR - PCLKB frequency division ratio select is out of range (r_core_cfg.h)"	• The current configuration is illegal for the peripheral module clock B (PCLKB) selection. Check the following configuration setting. SYSTEM_CFG_PCKB_DIV
28	"ERROR - Power control mode select is out of range (r_core_cfg.h)"	• The current configuration is illegal for the power state selection. Check the following configuration setting. SYSTEM_CFG_POWER_CONTROL_MODE
29	"ERROR - EHC operating mode select is out of range (r_core_cfg.h)."	• The current configuration is illegal for the EHC startup mode setting. Check the following configuration setting. SYSTEM_CFG_EHC_MODE
30	"ERROR - PCKB frequency division ratio (r_core_cfg.h)."	• The current configuration is illegal for peripheral module clock B (PCLKB). Check the following configuration settings. SYSTEM_CFG_ICK_PCKA_DIV SYSTEM_CFG_PCKB_DIV SYSTEM_CFG_HOCO_FREQUENCY SYSTEM_CFG_CLOCK_SOURCE SYSTEM_CFG_MOSC_FREQUENCY_HZ

5. EHC Startup Mode

The EHC startup mode can be used under the following conditions.

- The optional energy harvesting (EHC) startup source file (r_ehc.c) is loaded.
- The EHC startup mode is enabled in the configuration definition file (r_core_cfg.h).

5.1 File Structure

The EHC startup mode is an optional capability of the RE01 256KB CMSIS Driver Package and consists of one file: r_ehc.c in the vendor-specific file storage directory. The role of this file is shown in Table 5-1. Figure 5-1 shows r_ehc in the file structure of the RE01 256KB CMSIS Driver Package. The internal structure is shown in Figure 5-2.

Table 5-1 Role of Energy Harvesting (EHC) Startup Source File

File Name	Description
r_ehc.c	Energy harvesting (EHC) startup source file. It performs initialization required before checking the voltage charged in the secondary battery and starting the operation using the secondary battery, transition to a power control mode, and transition to a power supply mode in the EHC startup mode. To use the EHC startup mode, it is necessary to build this file.

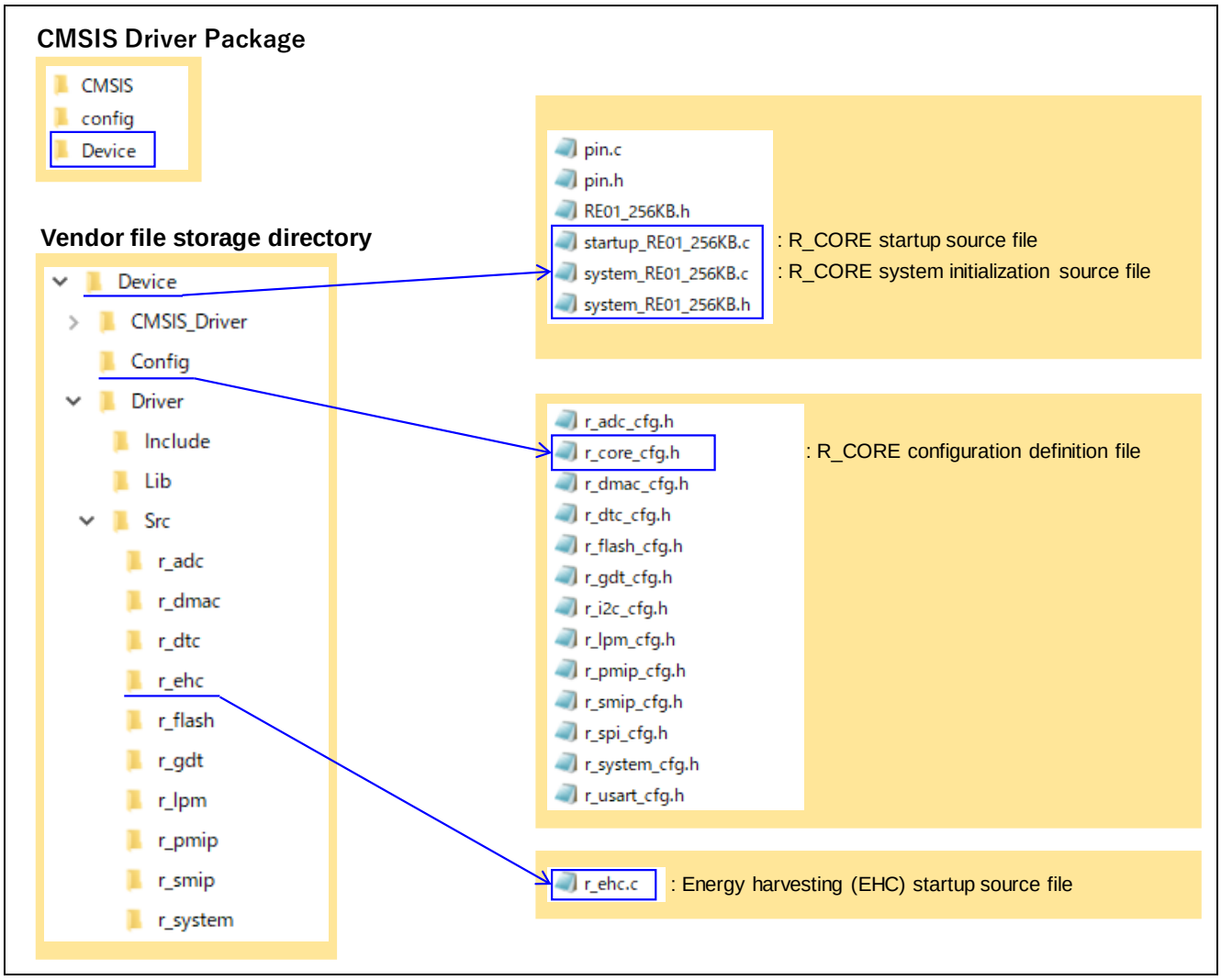
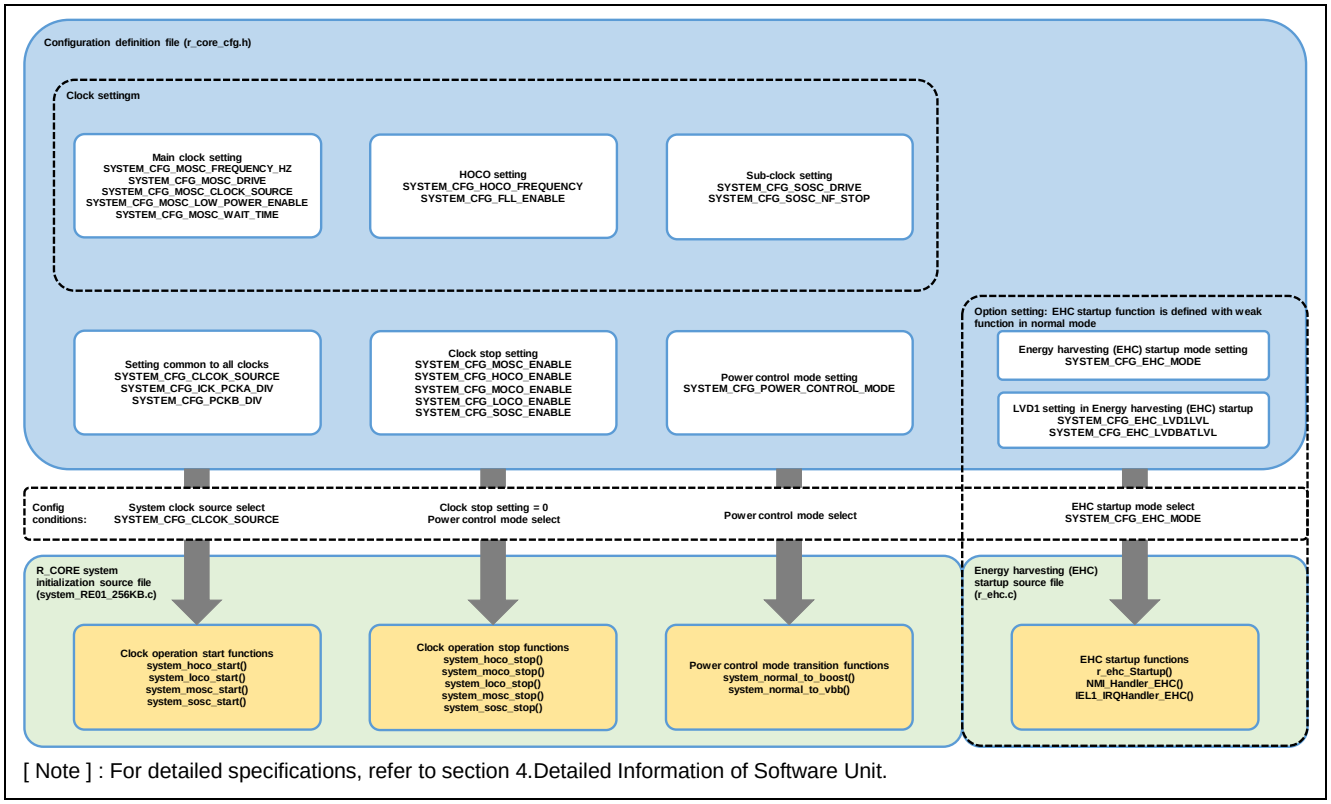


Figure 5-1 r_ehc in the File Structure of CMSIS Driver Package



[Note] : For detailed specifications, refer to section 4.Detailed Information of Software Unit.

Figure 5-2 Position of EHC in the R_CORE

5.2 Transition to EHC Startup Mode

The following shows the procedure for transition to the EHC startup mode.

When the configuration definition of energy harvesting (EHC) startup mode (SYSTEM_CFG_EHC_MODE) is set to "enabled", EHC startup processing begins with EHC initialization. When a reset is applied while the startup mode is enabled, EHC startup processing is performed again and the secondary battery is re-charged. The operation continues until an interrupt occurs due to a drop in the voltage of the secondary battery.

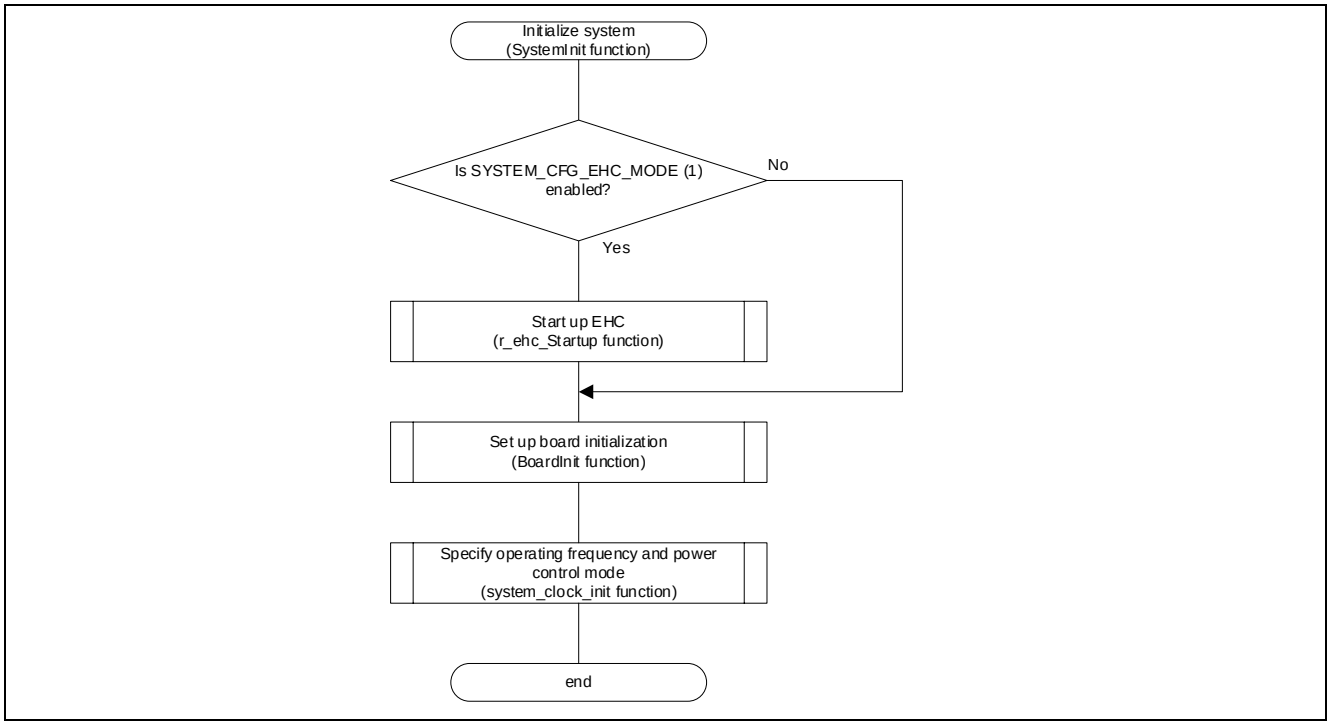


Figure 5-3 Transition to a Startup Mode by SystemInit Function

5.3 Configurations

For R_CORE, configuration definitions that can be modified by the user are provided in the r_core_cfg.h file.

Table 5-2 shows the initial setting. For the configuration definition, refer to the corresponding section shown in the table.

Table 5-2 List of Initial Settings of R_CORE Configurations

Section	Configuration	Description	Initial Value
4.1.19	SYSTEM_CFG_EHC_MODE	Enables or disables EHC startup processing.	1
4.1.20	SYSTEM_CFG_EHC_LVD1LVL	Specifies the Voltage Detection 1 Level.	7
4.1.21	SYSTEM_CFG_EHC_LVDBATLVL	Specifies the Voltage Detection BAT Level.	0

5.4 Function Specifications

In the EHC startup mode, a low power consumption mode is entered to reduce the power consumption in the device. Figure 5-4 shows state transitions in the EHC startup mode.

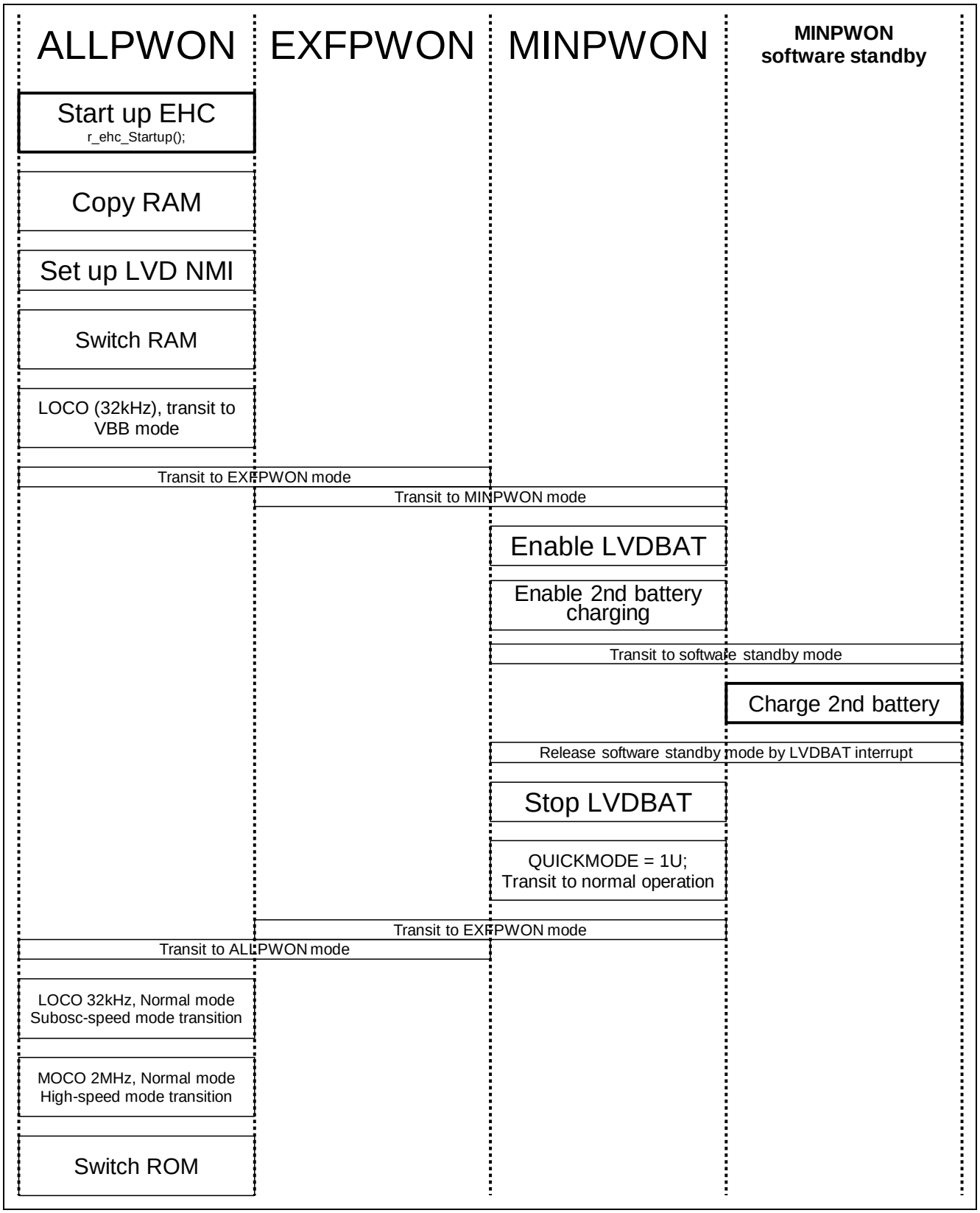


Figure 5-4 State Transitions in EHC Startup Mode

5.4.1 r_ehc_Startup Function

Table 5-3 r_ehc_Startup Function Specifications

Format	void r_ehc_Startup(void)
Description	Executes EHC startup processing.
Argument	None
Return value	None
Remarks	—

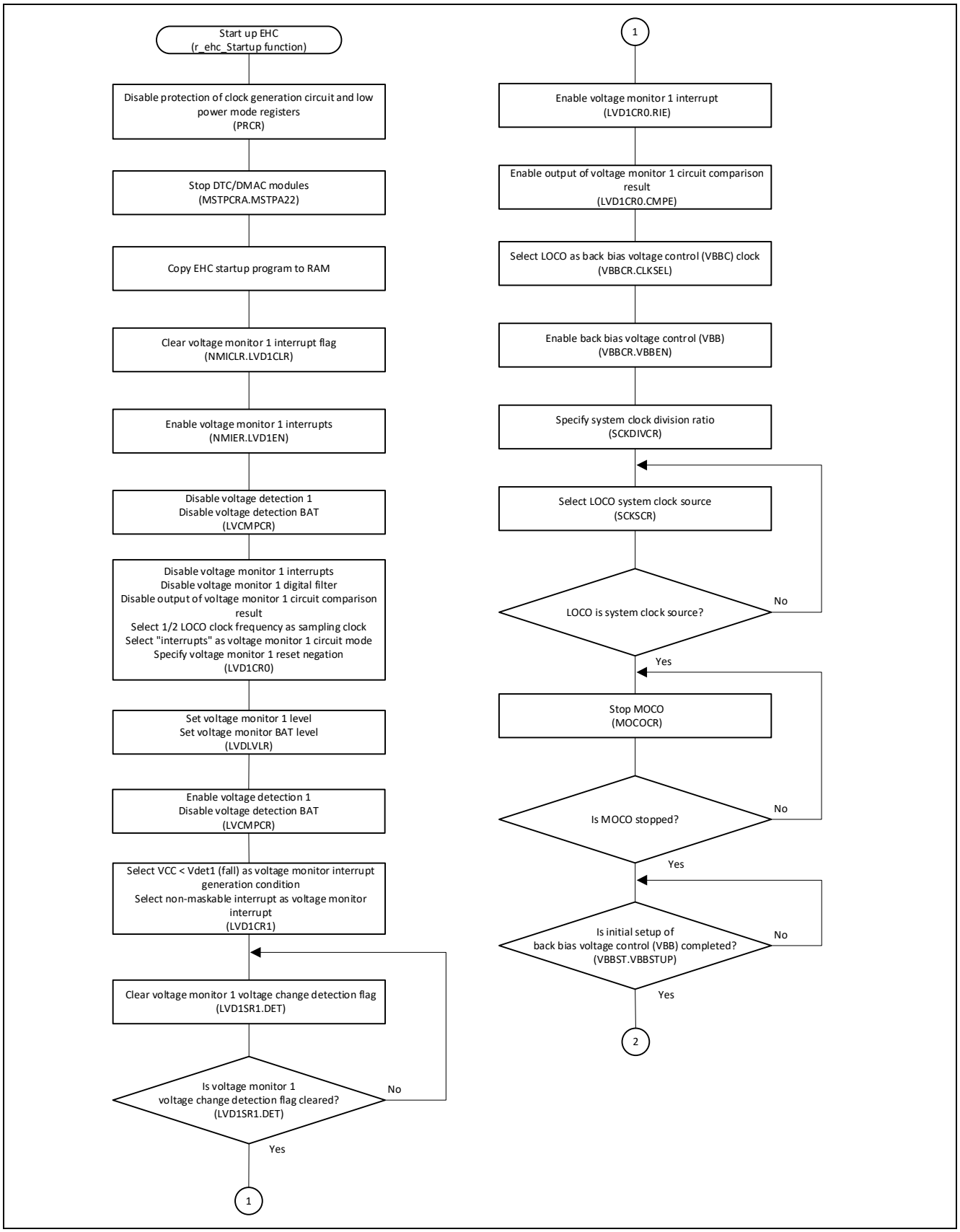


Figure 5-5 r_ehc_Startup Function Processing Flow (1/3)

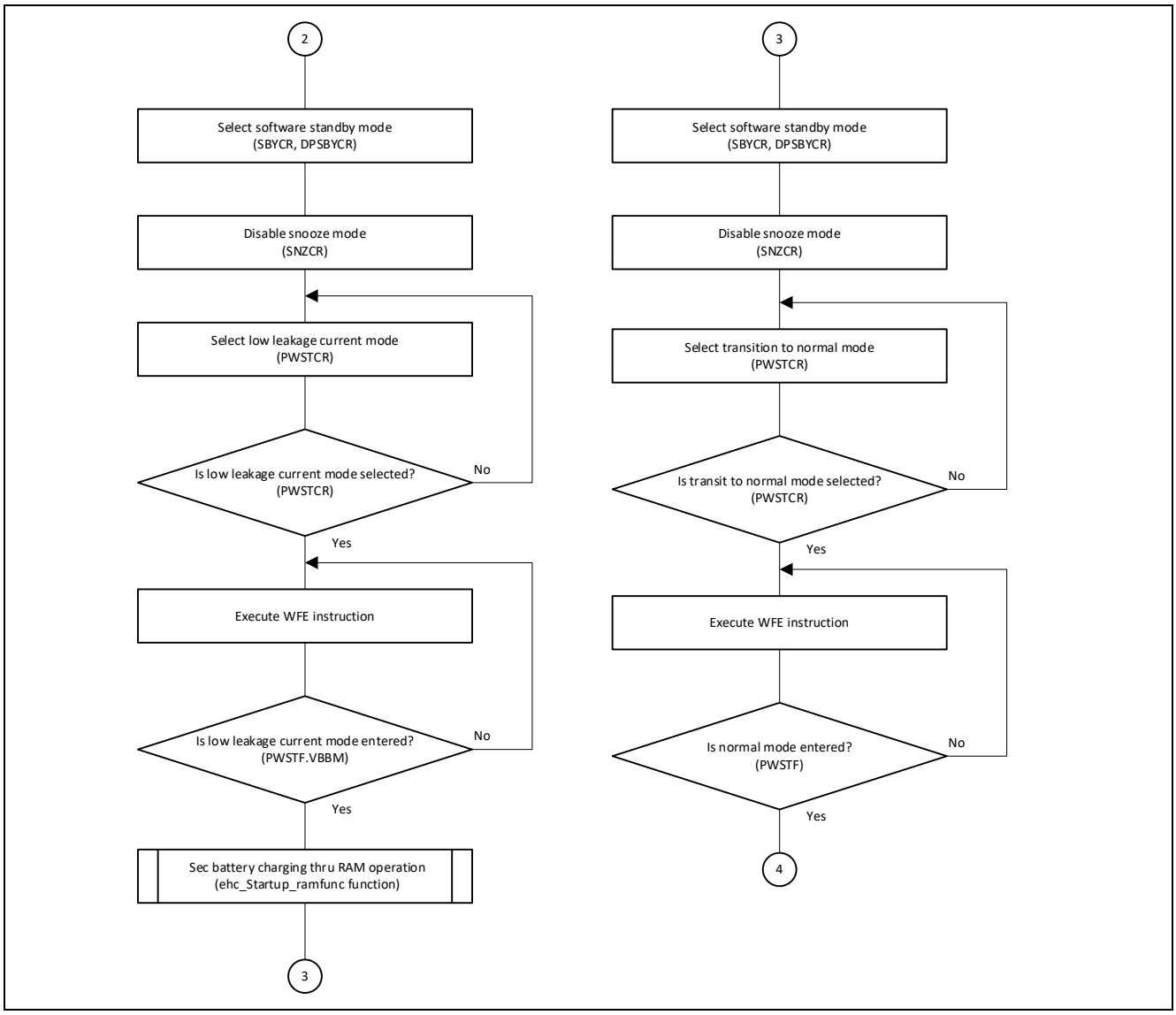


Figure 5-6 r_ehc_Startup Function Processing Flow (2/3)

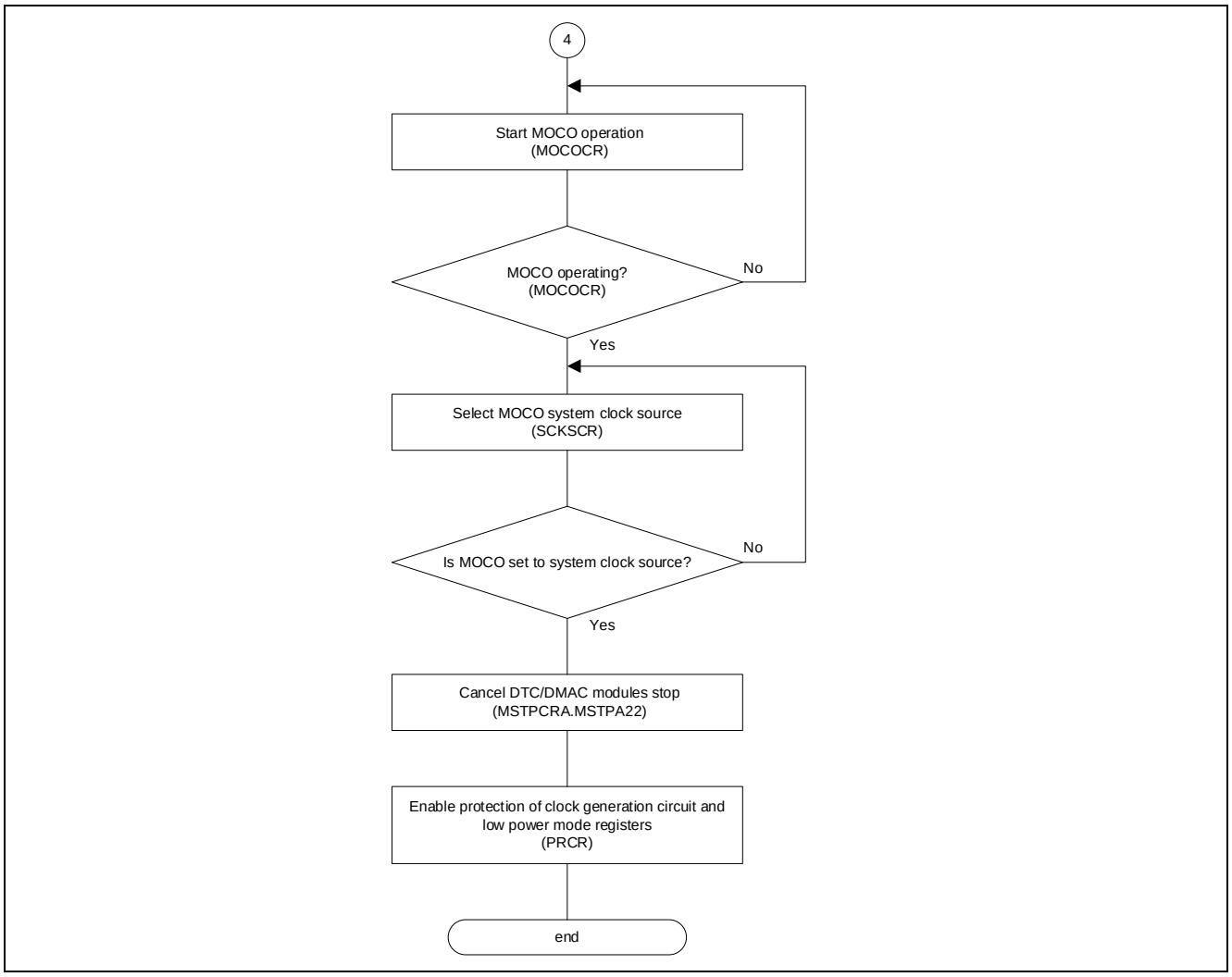


Figure 5-7 r_ehc_Startup Function Processing Flow (3/3)

5.4.2 ehc_Startup_ramfunc Function

Table 5-4 ehc_Startup_ramfunc Function Specifications

Format	void ehc_Startup_ramfunc(void)
Description	Charges the secondary battery in the EHC startup processing.
Argument	None
Return value	None
Remarks	—

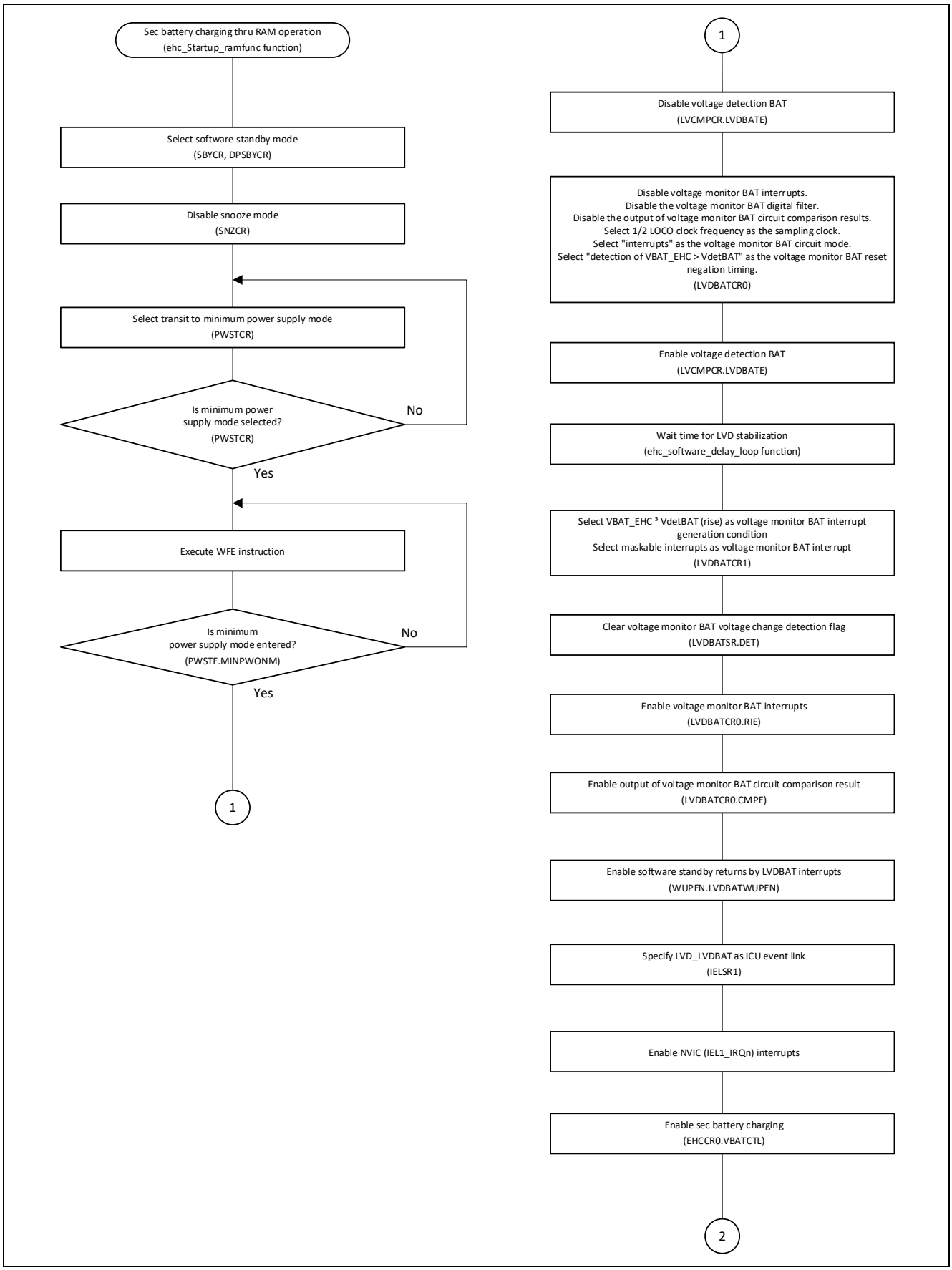


Figure 5-8 ehc_Startup_ramfunc Function Processing Flow (1/3)

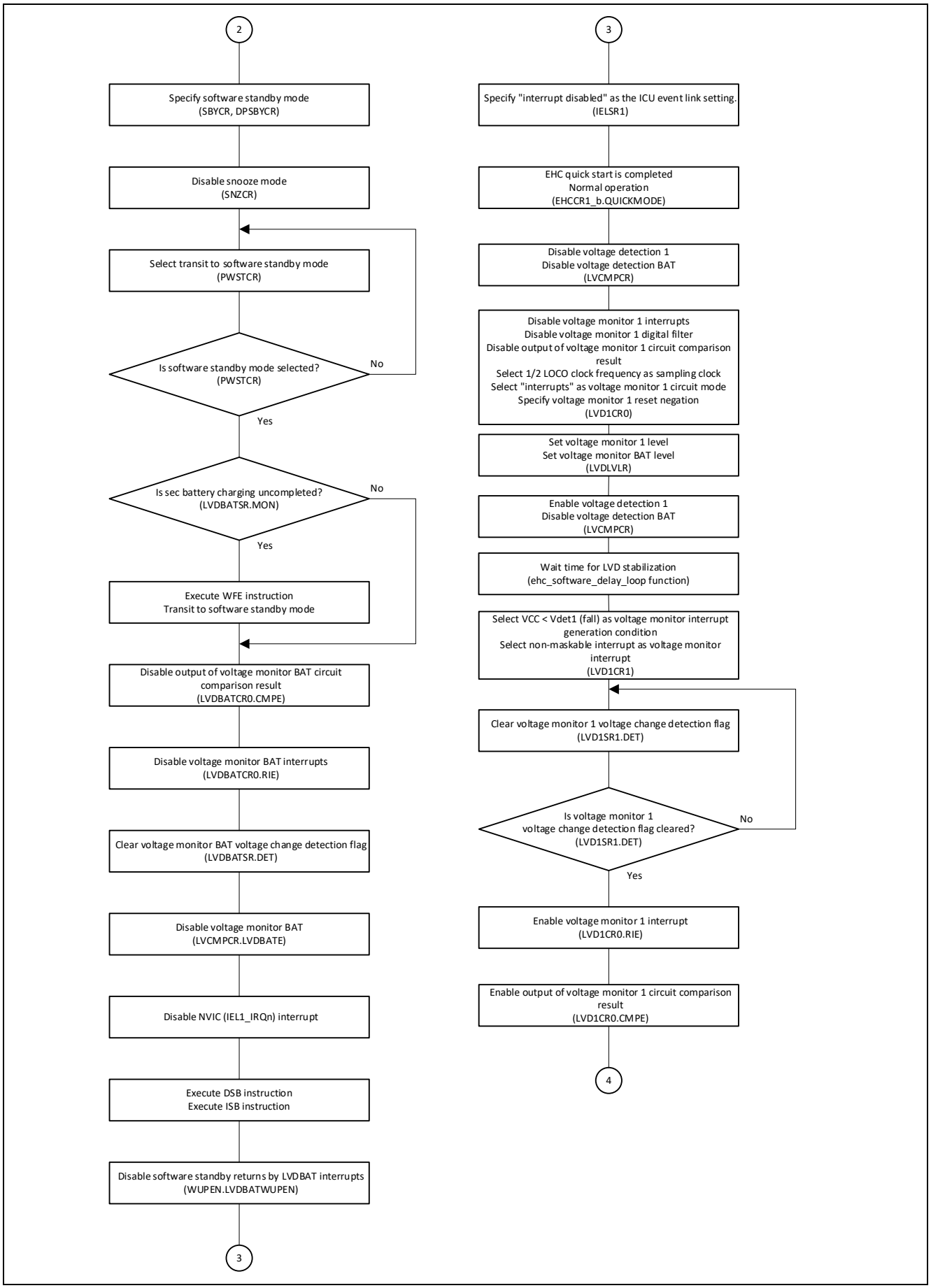


Figure 5-9 ehc_Startup_ramfunc Function Processing Flow (2/3)

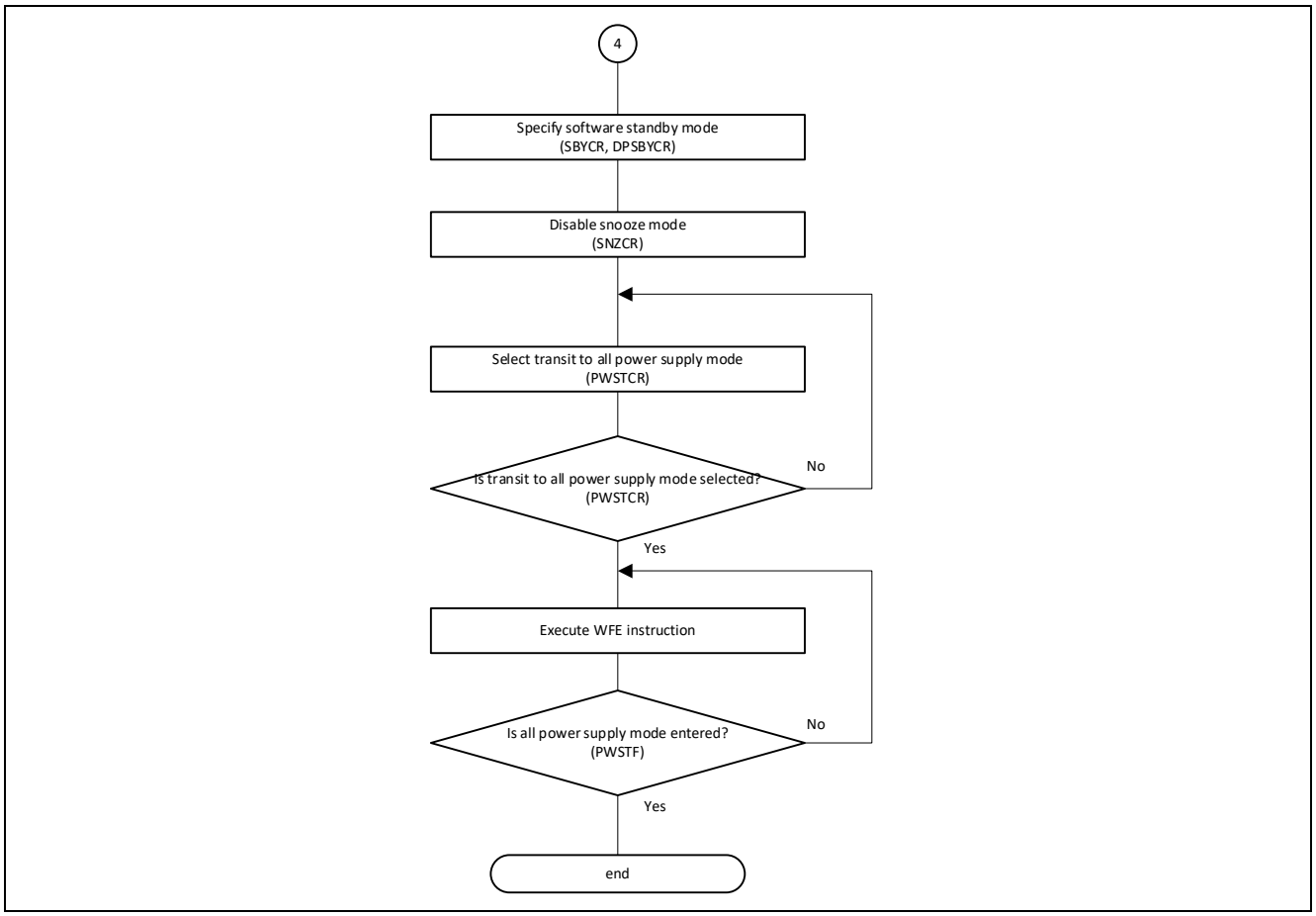


Figure 5-10 ehc_Startup_ramfunc Function Processing Flow (3/3)

5.4.3 NMI_Handler_EHC Function

Table 5-5 NMI_Handler_EHC Function Specifications

Format	void NMI_Handler_EHC(void)
Description	Execution branches to this function when a voltage monitor 1 interrupt occurs. This function initializes the EHC module.
Argument	None
Return value	None
Remarks	A voltage monitor 1 interrupt occurs when a drop in the voltage inside the MCU is detected.By initializing the EHC module, the power supply inside the MCU is stopped. The user must create an interrupt hander of the VCC voltage drops (function name : NMI_Handler).

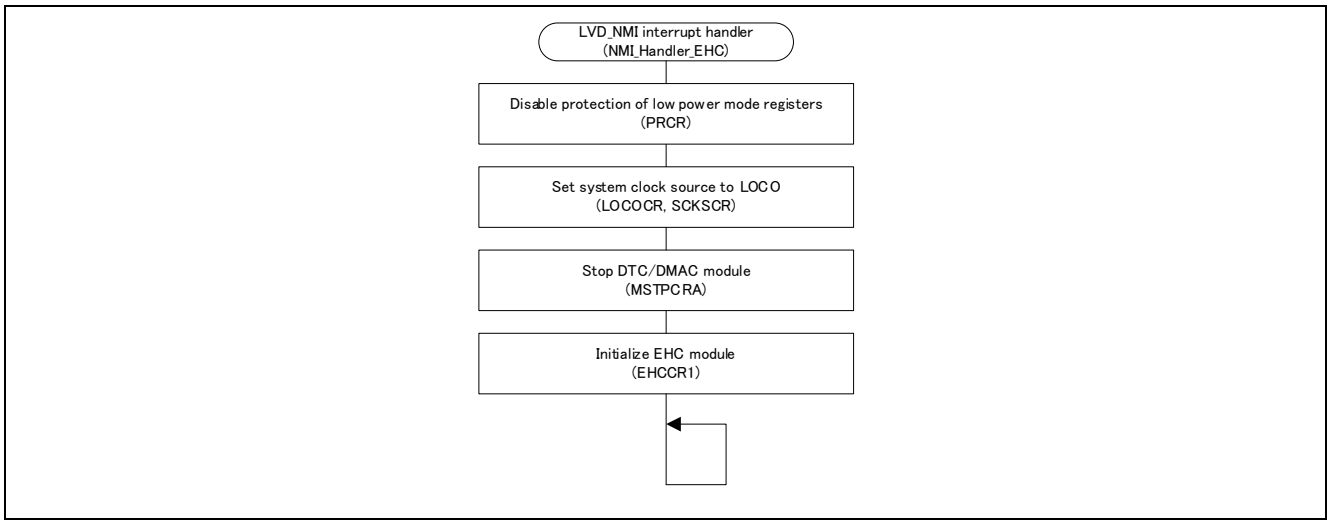


Figure 5-11 NMI_Handler_EHC Function Processing Flow

5.4.4 IEL1_IRQHandler_EHC Function

Table 5-6 IEL1_IRQHandler_EHC Function Specifications

Format	void IEL1_IRQHandler_EHC(void)
Description	Execution branches to this function when a voltage monitor BAT interrupt occurs. This function clears the status flag.
Argument	None
Return value	None
Remarks	When the completion of charging the secondary battery is detected, a voltage monitor BAT interrupt occurs and the MCU is released from software standby mode.

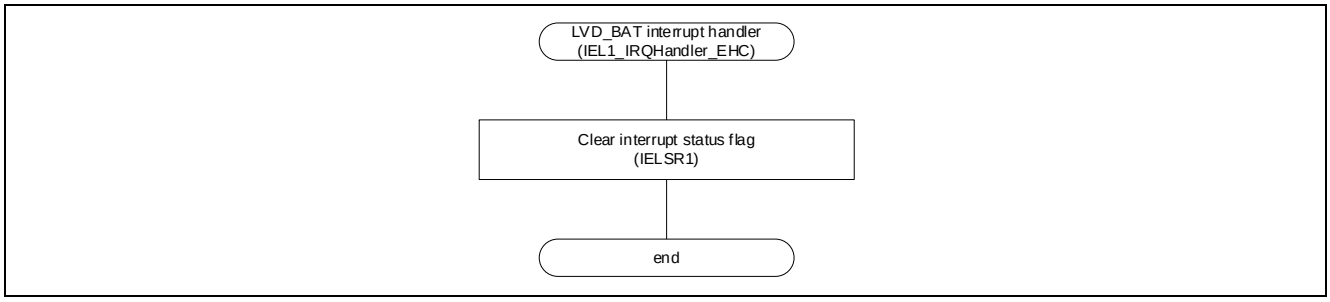


Figure 5-12 IEL1_IRQHandler_EHC Function Processing Flow

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http://www.renesas.com/

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Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Jul. 02, 2020	—	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
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