Microelectronics Reliability 52 (2012) 165–179

Contents lists available at SciVerse ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel

# On the effects of temperature on the drop reliability of electronic component boards

T.T. Mattila *, Jue Li, J.K. Kivilahti

*Department of Electronics, Helsinki University of Technology, 02015 TKK, Finland*

ARTICLE INFO

*Article history:*
Received 17 December 2009
Received in revised form 20 January 2011
Accepted 23 July 2011
Available online 6 September 2011

ABSTRACT

The effects of package temperature on failure mechanisms and lifetimes under mechanical shock loading were studied with the help of five different types of high-density packages (a WL-CSP and four CSP-BGAs) assembled on both double-layer and multi-layer FR4 boards. The localized heating of the packages by means of integrated heating elements was utilized in order to produce similar hot spots to those occurring in products in service. The results showed that the temperature can have a significant effect on the lifetimes of component boards under mechanical shock loading but that the effect varied according to the structures of the component boards. The average number of drops to failure of the WL-CSP component boards increased significantly with an increase in the temperature of the package, while the average number of drops to failure of the CSP-BGA component boards generally decreased. On the other hand, the drop reliability of one out of four CSP-BGA component board types was insensitive to temperature.

The failure modes and mechanisms were clarified with the help of physical failure analyses that revealed different failure modes in the component boards. Furthermore, depending on the component board type, the primary failure mode may change with temperature from that identified at room temperature. Particular attention was paid to the nucleation and propagation of cracks at different test temperatures. Computational case studies were designed in order to identify the significance of a change in temperature on three factors: (a) the stiffness of the PWB; (b) the strength and elastic modulus of the solder, and (c) the thermomechanical loads. The influences of each factor on the strains and stresses in the proximity of the solder interconnections were evaluated by means of the finite element method. The results of the statistical and physical failure analyses were rationalized with the help of the results from the finite element analyses. They showed that the effects of a change in temperature on the lifetimes of the component boards under mechanical shock loading can be explained by changes in the nucleation site and/or the propagation of cracks. The results presented in this paper point out that single-load reliability tests can form an incomplete understanding of the failure mechanisms in real service environments and modifications to the currently employed reliability test standards that are needed.



## 1. Introduction

Good reliability is an important product characteristic, especially for high-end portable electronic devices that are exposed to harsh operating environments. The adoption of high-density chip-scale packaging technologies and larger scales of integration have enabled numerous new functions to be introduced into novel electronic devices. However, these increasingly powerful and complex electronic devices undergo many different types of loadings during operation. Therefore it has become a challenge to ensure good product reliability before their market introduction. Most importantly, the different loadings often act simultaneously. During normal operation many electronic applications are exposed to changes in temperature caused either by internally generated heat from high-power-density integrated circuits or changes in the ambient temperature [1]. The thermomechanical loads caused by changes in temperature can be influential for the reliability of electronic circuits, because they can alter the microstructures of the solder interconnections and, thereby, affect their mechanical properties over time [2–7]. In addition to thermomechanical loads, many applications, especially portable products, are also exposed to mechanical loads, for example shocks caused by accidental drops.

Because of the complex nature of the loading conditions during the ordinary use of the products, it is important that their reliability is studied by employing test procedures that simulate their real operational loadings as realistically as possible. There are two aspects to be taken into account when we think about the thermal and mechanical loads that electronic devices are subjected to and how they interact with each other. First, drops are equally likely to take place at any time during the lifetime of products and, second, the devices may be dropped while their electronic components (and interconnections) are at different temperatures. Both these aspects are, however, neglected in the standardized

* Corresponding author.
*E-mail address:* Toni.Mattila@hut.fi (T.T. Mattila).

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doi:10.1016/j.microrel.2011.07.085

reliability tests. Currently, drop impact tests are carried out at room temperature and with as-soldered component boards [8–11].

Among the most commonly encountered loads in operating environments, the combined effects of operational power cycling and mechanical shocks (resulting from accidental drops) are the most influential, because they either alter the microstructures of the solder most strongly or can cause overloading conditions in which the solder interconnections fail suddenly. Therefore, in order to study the effect of their operational life before a drop impact, we made an earlier study of the reliability of chip-scale packaged (CSP) ball grid arrays (BGA) similar to those used in this paper under consecutively combined thermal or thermalmechanical and mechanical shock loads [12]. To simulate the use of products before a drop impact, the test boards were thermally cycled (−45 °C/+125 °C, 15-min dwell time, 750 cycles, which was known to be less than three quarters of the average lifetime of the packages under the same conditions) or isothermally annealed (125 °C, 500 h) before the standard JESD22-B111 drop test [8]. In comparison to the tests carried out in the as-soldered condition, the average number of drops required for the component boards to fail was higher when the thermal cycling aging treatment preceded the drop test. However, a drastic reduction in the average number of drops to failure was recorded when thermal annealing treatment preceded the drop test. Both the results were explained by the microstructural changes caused in the solder interconnections during the aging treatment and the resulting changes in the crack propagation paths. In the case of thermal cycling pretreatment, the crack path changed from the intermetallic layers, as observed in the as-soldered state tests, to bulk solder cracking as a consequence of the recrystallization of microstructures that commenced during the thermal cycling pretreatment. In the case of isothermal annealing pretreatment, on the other hand, the sharp decrease in the drop reliability was caused by the formation of defects in the interfacial intermetallic layers. Chiu et al., Xu et al., Zhang et al., Peng et al., and Varghese et al. have also carried out experiments that dealt with sequential thermal treatments and drop testing by employing similar BGA component boards and found similar changes in the crack path when the aging treatment preceded the drop tests [13–17].

The studies discussed above point out that operation life before a drop impact can have a significant impact on the reliability of electronic devices. However, the fact that devices may be dropped while their electronic components are at different temperatures, still needs to be clarified. It is well known that the mechanical properties of materials are temperature-dependent (see e.g. [18,19] for solders). Changes in the mechanical properties of different materials in electronic assemblies can have unexpected consequences for the failure modes and mechanisms under mechanical shock loads. Therefore in this paper the drop reliability of component boards at different temperatures is discussed with respect to five different component board assemblies. The tests were not originally designed as comparative studies and, therefore, some experimental details differ slightly. However, the results reveal useful insights and they can provide valuable inputs for further studies. This study compares the drop reliability of a wafer-level chip-scale package (WL-CSP) and four chip-scale packaged ball grid arrays (CSP-BGA) soldered onto either a double-layer FR4 or a multi-layer FR4 printed wiring board under JESD22-B111 drop testing at different temperatures.

## 2. Materials and methods

The reliability of component boards at different temperatures was studied with the help of five different package types and two different printed wiring board (PWB) structures. The details of the construction of the component boards are discussed below and are summarized in Table 1.

Both versions of the PWBs used in this study had dimensions and package layouts that conformed to the JESD22-B111 standard [8], but they had different numbers of copper layers: a double-layer FR4 PWB with two layers of copper (ISOLA Duraver-E-Cu 104i) and the "1 + 6 + 1" build-up eight-layer FR4 (Matsushita: RCCu MRG200-75T12, R-1566 inner layers). The single-package configuration defined in the JESD22-B111 standard was used in order to isolate the effect of neighboring packages and to produce a similar temperature distribution to that measured in real devices during operation [1]. An organic solderability preservative surface finish was used on the copper soldering pads of all the PWBs. The packages were reflow soldered onto the PWBs with the Sn3.8Ag0.7Cu (Multicore) solder paste.

All the drop tests were carried out according to condition B of the JESD22-B111 standard: 1500 G deceleration, 0.5 ms half-sine pulse shape. All the packages were equipped with a daisy-chain network to detect electrical failures by means of the continuous electrical monitoring of the continuity of the daisy-chain networks. A failure was recorded when the resistance of the daisy-chain network exceeded 1.5 kΩ for the duration of at least 1 μs, four times in six successive drops (Analysis Tech's event detector).

The component boards were heated up locally by integrated heating elements. The test temperatures were set by adjusting the power of the heating elements to achieve the desired test temperature as measured from the package surface. The component boards were covered with a thin layer of matt black paint with a known emissivity of 0.92 in order to accurately image and measure the temperature distributions of the heated component boards by means of an infrared camera (FLIR A20M). Because the temperature on the package surface decreased by about 5 °C during one drop, the temperature of the package surface was set to be 2–3 °C above the target temperature before each drop. The temperature of the package was checked and stabilized before every drop.

The strains on the component boards were measured (National Instruments PXI-6052E/SCI-1520/SCI-1314) by 2-mm × 1-mm strain gauges. The three directional strain gauges were attached to the PWB along the extended diagonal line of the package about 3 mm from a corner of the 12 × 12-mm CSP package (see Fig. 1c). The gauge was attached to the same location on all the component

**Table 1**
Component board specifications.

| Component type | Package dimensions (mm) | Bump pitch (mm) | Bump diameter (mm) | Bump alloy | Bump count | Under bump metallization | Printed wiring board structure | PWB protective coating | Test temperatures |
|---|---|---|---|---|---|---|---|---|---|
| WI-CSP | 3 × 3 | 0.5 | 0.3 | SAC405 | 36 | Ni(V)\|Cu | Double-layer FR4 | Cu\|OSP | RT, 75, 100, 125 |
| CSP-BGA-1 | 10 × 10 | 0.8 | 0.5 | SAC305 | 144 | Ni | Double-layer FR5 | Cu\|OSP | RT, 75, 100, 125 |
| CSP-BGA-2 | 12 × 12 | 0.8 | 0.5 | SAC305 | 144 | Cu | Multi-layer FR4 | Cu\|OSP | RT, 70, 110 |
| CSP-BGA-3 | 12 × 12 | 0.8 | 0.5 | SAC305 | 144 | Cu | Double-layer FR4 | Cu\|OSP | RT, 45, 75, 100, 125 |
| CSP-BGA-4 | 12 × 12 | 0.8 | 0.5 | SAC305 | 168 | Cu | Multi-layer FR4 | Cu\|OSP | RT, 70, 110 |

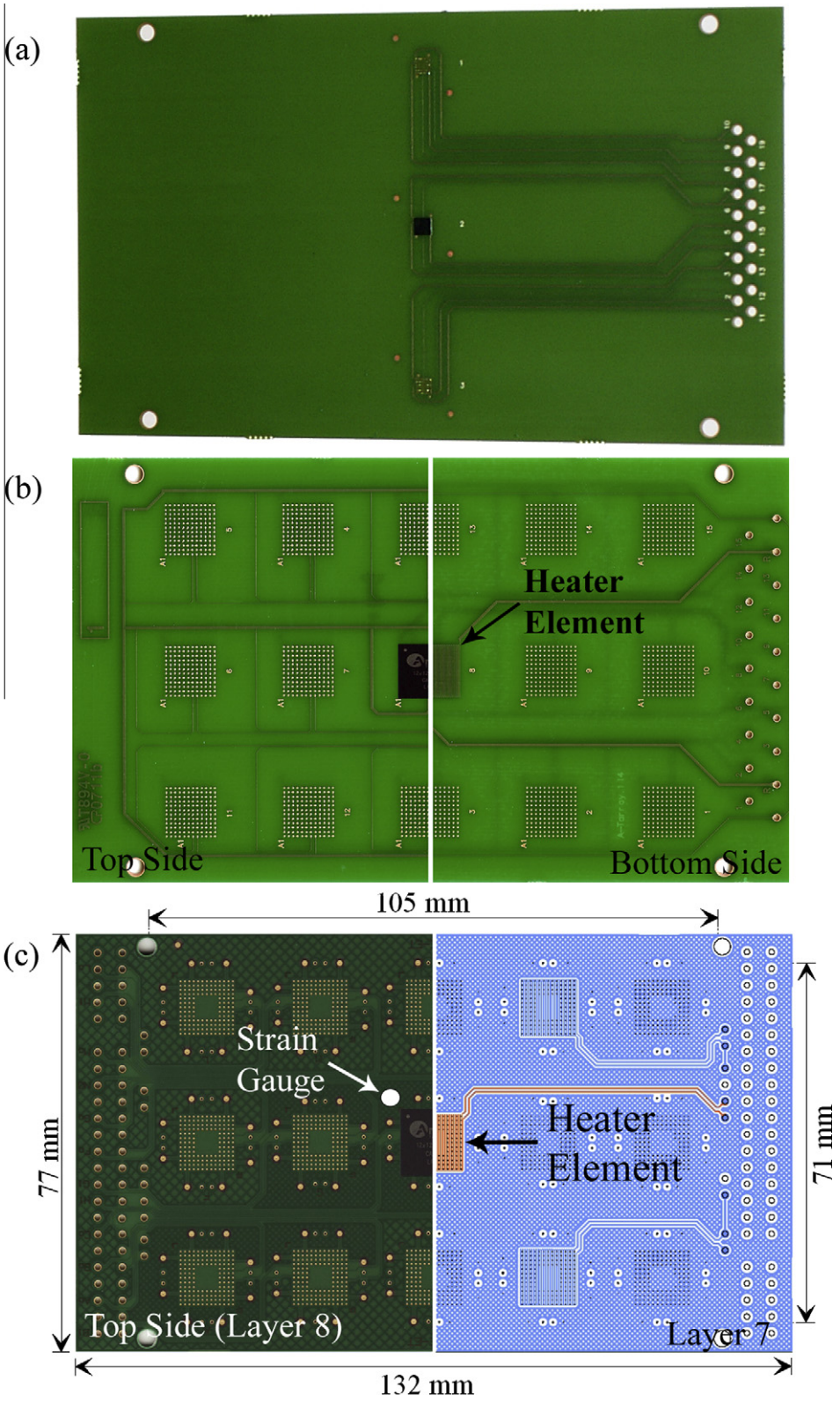


**Fig. 1.** Layouts and structures of the component boards: (a) WL-CSP, (b) CSP-BGA-1, and (c) CSP-BGA-2. All boards had the same dimensions and strain gauge location.

board types. Strain measurements during the drops at different temperatures were carried out after a temperature stabilization time of about 20 min. The strain gauges were calibrated and set to zero at each temperature before a drop to achieve strain measures that were as accurate as possible. Thus the measured strains reported in this paper do not include the strains caused by the thermal expansion of the PWBs when they were heated up from room temperature to the particular test temperature. The deceleration of the sledge was measured (National Instruments PXI-4472) simultaneously with the strain measurements.

### 2.1. The WL-CSP on the double-layer FR4

The wafer-level chip-scale package used in the study was a 3-mm × 3-mm package with 36 bumps arranged in a 6 × 6 full area array with a 0.5-mm pitch. The bump size was 0.3 mm, the under bump metallization (UBM) was Ni(V)|Cu, and the solder bump alloy was Sn4.0Ag0.5Cu (wt.%). The package was equipped with an on-chip heater element, an on-chip aluminum resistor to measure the temperature on the chip surface, and a daisy-chain network for time-to-failure measurements. The double-layer FR4 PWB was used. The drop tests were carried out at four different temperatures: room temperature (23 °C), 75 °C, 100 °C, and 125 °C. Ten component boards were tested at each temperature below 125 °C but only four at 125 °C. The WL-CSP component board is shown in Fig. 1a. See [20] for more details.

### 2.2. The CSP-BGA-1 on the double-layer FR4

The CSP-BGA 1 was a 10-mm × 10-mm package with 144 bumps arranged in a 12 × 12 full array with a 0.8-mm pitch. The bump size was 0.5 mm, the UBM was electrochemical Ni|Au, and the package was bumped with solder balls with a composition of Sn3.0Ag0.5Cu (wt.%). The package did not have an on-chip heating element and, therefore, the heating of the component boards was carried out with the help of an integrated heating element underneath the package on the opposite side of the PWB. The double-layer FR4 PWB was used. The heating element was a 10-mm × 10-mm meander pattern on the copper layer. The smaller line width of the meander regions produced the heat. The drop tests were performed at room temperature, 75 °C, 100 °C, and 125 °C. Fifteen component boards were drop-tested at each temperature. The layout and structure of the CSP-BGA-1 component boards are illustrated in Fig. 1b.

### 2.3. The CSP-BGA-2 on the multi-layer FR4

The CSP-BGA-2 was a 12-mm × 12-mm FR4-based package with 144 bumps arranged in a 13 × 13 peripheral array with a 0.8-mm pitch. The bump size was 0.5 mm and the package was bumped with solder balls with a composition of Sn3.0Ag0.5Cu (wt.%). There was no under bump metallization between the solder bumps and copper pads of the package. The multi-layer FR4 PWB was used. The heating of the component boards was carried out with an integrated heating element inside the PWBs on the nearest copper layer (layer 7) underneath the packages. The drop tests were performed at room temperature, 70 °C, and 110 °C. Twenty-three component boards were tested at each temperature. The layout and structure of the PWB are illustrated in Fig. 1c. See [21] for more details.

### 2.4. The CSP-BGA-3 on the multi-layer FR4

The CSP-BGA-3 was the same package as the CSP-BGA-2 but soldered onto the double-layer FR4. The heating of the component boards was carried out with an integrated heating element, as in the case of the CSP-BGA-1 boards. The drop tests were carried out at several different temperatures: room temperature, 50 °C, 70 °C, 75 °C, 90 °C, 100 °C, 110 °C, and 125 °C. Fourteen component boards were drop-tested at each temperature except at 50 °C, where only six boards were tested. The PWB was the same double-layer FR4 as that shown in Fig. 1b but with a different package footprint.

### 2.5. The CSP-BGA-4 on the multi-layer FR4

The CSP-BGA-4 was a 12-mm × 12-mm package with 168 bumps arranged in a 14 × 14 peripheral array with a 4 × 4 array of thermal bumps in the center. The diameter of the Sn3.0Ag0.5Cu solder bumps was 0.5 mm and the pitch was 0.8 mm. There was no under bump metallization between the solder bumps and the copper soldering pads of the package. The package was equipped with two heater elements on the silicon chip. In addition, the multi-layer FR4 PWB hosted a heater element similar to that used in the PWBs of the CSP-BGA-2. The use of the heater element on the PWBs was necessary to achieve the highest test temperature. The temperature of the package was monitored continuously during the testing with the help of a PN junction on the silicon chip. The drop tests were carried out at three different temperatures: room temperature, 70 °C, and 110 °C. Ten component boards were tested at each temperature. The PWB is the same as that shown in Fig. 1c but with a different package footprint. See [22] for more details.

### 2.6. Numerical analyses

The differences in the average number of drops to failure were analyzed statistically. The drops-to-failure data did not conform to the normal distribution as tested by the Shapiro–Wilk test for normality (risk level = 5%) and, therefore, the significance testing of the average number of drops to failure was carried out with the non-parametric Wilcoxon Rank-Sum Test by testing all the pairwise differences and reporting the risk levels ($\alpha$) of the conclusions individually with the help of the $p$-value (the probability that the null hypothesis of equal sample averages is rejected when it is in fact true). The characteristic lifetimes ($\eta$) and the shape parameters ($\beta$) of the two-parameter Weibull distribution function $F(t) = 1 - \exp[-(t/\eta)^{\beta}]$ were also estimated. The association and significance tests were carried out with Statistix (v.8.2) from Analytical Software and the Weibull analyses with Weibull ++ (v.6.0.8) from Reliasoft.

The finite element analysis was performed with the commercial finite element analysis software ABAQUS v.6.8. Only one fourth of the geometrically symmetric component board was simulated. Since the assembly has large differences in the length scales of different parts, e.g. about 100 mm for the PWBs, 10 mm for the packages, and 0.3 mm for the solder interconnections, it is necessary to employ the submodeling technique in order to obtain accurate and detailed results of the critical solder interconnections. Three models with different levels, (board, package, and interconnection levels) were established in the current study. The board-level model consisted of the PWB (shell elements), the package (shell elements), the solder interconnections (solid elements), and the supporting rod of the tester (beam elements). The package-level model (all solid elements) was composed of one fourth of the package and the board area beneath the package. The solder interconnection closest to the corner, the copper pad and trace, partial PWB, and partial package (all solid elements) were included in the interconnection-level model.

In the board-level and package-level models, the properties of all the materials were considered temperature-dependent, elastic, and isotropic, except the solder. The strain rate-dependent elastic–plastic material properties were used for the solder on all three levels of the models [19,23]. The values of the elastic modulus of essential materials for this study and the flow stress of the Sn3.4Ag0.8Cu solder at room temperature and at elevated temperature of 100 °C are presented in Table 2 and Fig. 2, respectively. The plasticity of copper was taken into account in the interconnection-level model. 1500 G of deceleration was applied at the ends of the supporting rod as the loading condition for the component board.

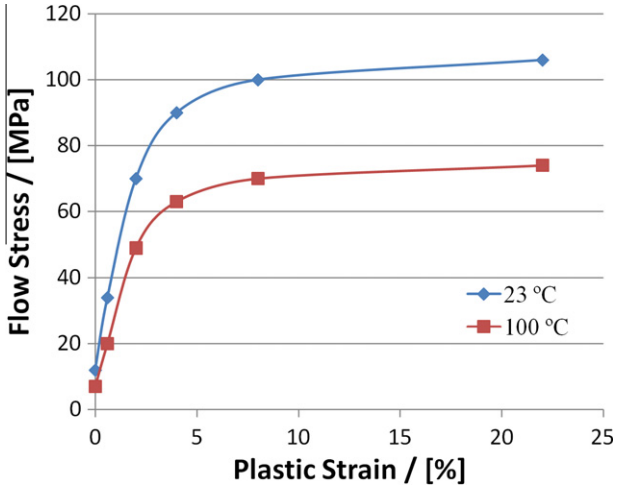


**Fig. 2.** Flow stress of the Sn3.4Ag0.8Cu solder at room temperature and elevated temperature of 100 °C [19].

In the submodeling process, the calculated displacements of the relatively coarse global model were interpolated and assigned as the boundary condition for the submodel with a finer mesh. For the cases with elevated temperatures, the experimentally measured temperature distributions of the component boards were mapped onto the mesh of the board-level model as body loads.

## 3. Results

In the following sections, the statistical analyses of the drop test data are presented. The failure modes and mechanisms are determined on the basis of the physical failure analyses of the drop-tested component boards. Particular attention will be paid to the nucleation and propagation of cracks in the different component boards. After that the effects of temperature on the failure mechanisms are discussed with the help of the stress–strain analyses carried out with the help of the finite element method. Finally, the differences between the lifetimes are discussed on the basis of the identified failure modes and the results of the case studies.

### 3.1. Effects of temperature on lifetimes under the drop test

Table 3 summarizes the statistical results of the drop tests at different temperatures. Fig. 3 shows the average number of drops to failure graphically with the corresponding standard deviations of the different component boards at the different test temperatures. The diagrams illustrate the fact that an increase in the drop test temperature can have diverse consequences for the lifetime of the component boards under test: the number of drops to failure can increase, decrease, or remain unchanged with an increase in the temperature of the packages.

The average number of drops to failure of the WL-CSP component boards increased by about 300% when the temperature was increased from room temperature to 75 °C. The difference between the average number of drops to failure was statistically significant at a risk level ($\alpha$) much less than 0.1%. When the temperature was increased further, from 75 °C to 100 °C, the average number of drops to failure increased by about 25%. However, the difference was not statistically significant ($\alpha \approx 45\%$) as a result of the high

**Table 2**
Elastic modulus of different materials at room temperature and elevated temperature of 100 °C [19].

| Material | 23 °C | 100 °C |
|---|---|---|
| FR4 | 17.1 | 14.2 |
| RCC | 6.0 | 4.9 |
| Cu | 120 | 110 |
| Solder | 50.5 | 44.0 |

**Table 3**
Numerical results of the drop tests.

| | Sample average | Standard deviation | Weibull $\eta$ | Weibull $\beta$ |
|---|---|---|---|---|
| *WL-CSP* | | | | |
| RT | 112 | 48.2 | 122 | 3.3 |
| 75 °C | 458 | 151.6 | 514 | 3.0 |
| 100 °C | 568 | 386.8 | 621 | 2.0 |
| 125 °C | 711 | 298.8 | 802 | 2.6 |
| *CSP/BGA-1* | | | | |
| RT | 25 | 13.1 | 29 | 1.4 |
| 75 °C | 32 | 23.0 | 35 | 1.6 |
| 100 °C | 27 | 17.2 | 30 | 1.7 |
| 125 °C | 23 | 12.4 | 27 | 1.9 |
| *CSP/BGA-2* | | | | |
| RT | 53 | 36.5 | 57 | 1.2 |
| 70 °C | 51 | 18.5 | 62 | 8.9 |
| 110 °C | 29 | 5.4 | 30 | 6.9 |
| *CSP/BGA-3* | | | | |
| RT | 21 | 8.2 | 23 | 2.8 |
| 45 °C | 18 | 4.4 | 20 | 4.3 |
| 70 °C | 16 | 7.3 | 18 | 2.1 |
| 75 °C | 16 | 9.6 | 18 | 2.1 |
| 100 °C | 10 | 6.4 | 10 | 1.9 |
| 110 °C | 10 | 4.8 | 11 | 2.6 |
| 125 °C | 9 | 8.0 | 10 | 1.4 |
| *CSP/BGA-4* | | | | |
| RT | 54 | 12.3 | 59 | 5.2 |
| 70 °C | 33 | 10.2 | 36 | 3.5 |
| 110 °C | 10 | 2.3 | 11 | 4.8 |

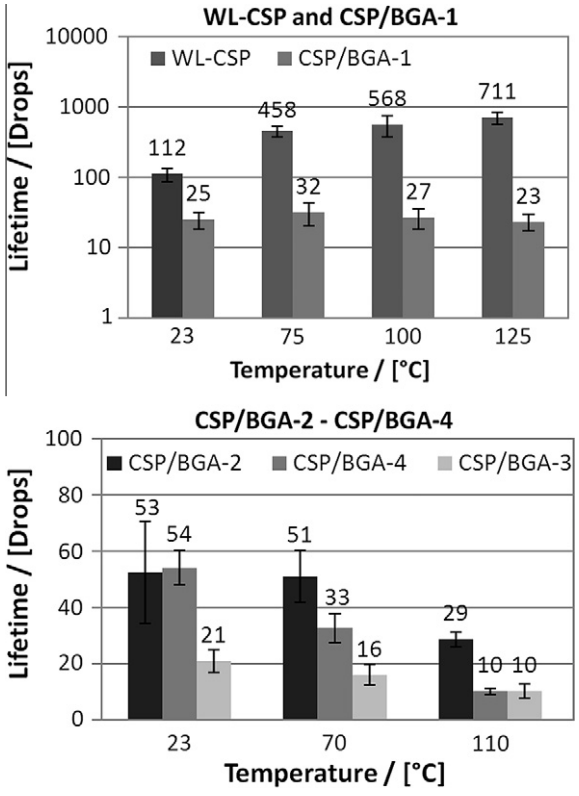


**Fig. 3.** Average number of drops to failure with standard deviations (note that the *y*-axes are on different scales).

level of deviation of the drops-to-failure data of the component boards drop-tested at 100 °C. Because of the wide variation in the average lifetime of the 100 °C drop tests, additional boards were drop-tested at 125 °C in order to find out if the average number would still show an increasing trend towards higher temperatures. Four boards were drop-tested and all of them showed a higher number of drops to failure as compared to the average value at 100 °C.

The average number of drops to failure of the CSP-BGA-1 component boards increased by about 28% with an increase in the temperature from room temperature to 75 °C but the increase was not statistically significant ($\alpha \approx 72\%$). All the average numbers of drops to failure between the different temperatures failed to show statistically significant differences in the pair-wise comparisons.

All the remaining component board types (CSP-BGA-2, CSP-BGA-3, and CSP-BGA-4) showed a similar decreasing trend in the average numbers of drops to failure with an increase in the temperature of the package. The drop test results of the CSP-BGA-2 component boards did not, however, show a statistically significant difference ($\alpha > 99.9\%$) in the average number of drops to failure when the temperature was increased from room temperature to 70 °C but as the temperature was increased from 70 °C to 110 °C the decrease was about 45% and highly significant ($\alpha \ll 0.1\%$). The results for the CSP-BGA-3 component boards showed a decrease in their lifetime with an increase in temperature from RT to 70 °C, but this difference was not statistically significant ($\alpha \approx 21\%$). However, when the temperature was increased from 70 °C to 110 °C the lifetime again increased significantly ($\alpha \approx 3\%$). Finally, the drop test results of the CSP-BGA-4 component boards showed statistically significant differences between the average number of drops to failure at each temperature, the smallest risk level being much less than 0.1%.

### 3.2. Effects of temperature on the failure modes

The failure modes were analyzed from the cross-sectional samples with the help of both optical and scanning electron microscopy. Some component boards showed more than one failure mode, but the primary failure mode was unambiguously identifiable. In this paper the term 'primary failure mode' is used to denote the failure modes that caused the breakdown of the daisy-chain networks more often than others. The primary failure mode is also often, but not necessarily, the first failure mode to initiate in the component boards. Particular attention in the failure analyses was paid to the crack nucleation sites and propagation paths at the different temperatures.

The primary failure mode in the case of the WL-CPS component boards was the cracking of the solder interconnections near the package-side interfacial regions. Small cracks were occasionally observed in the PWB-side interfacial regions at all temperatures, but they seldom propagated for more than about one third of the diameter of the interconnections. Fig. 4 shows the typical failure modes of the WL-CSP component boards drop-tested at the different temperatures. The nucleation took place between the Al|Ni(V)|Cu under the bump metallization layer and the underlying benzocyclobutane (BCB) layer, as shown in Fig. 4f. Cracks propagated first along the Al|BCB interface, then between the two Al layers for about 10–20 μm, and then shifted into the intermetallic compound (IMC) layer or bulk solder. It should be noted that the propagation path described above is very short in comparison to the entire length of the cracks through the interconnections. Furthermore, the nucleation site of the cracks was the same, regardless of the test temperature. However, differences were observed in the crack propagation paths of the component boards drop-tested at elevated temperatures in comparison to those drop-tested at room temperature. At room temperature, cracks

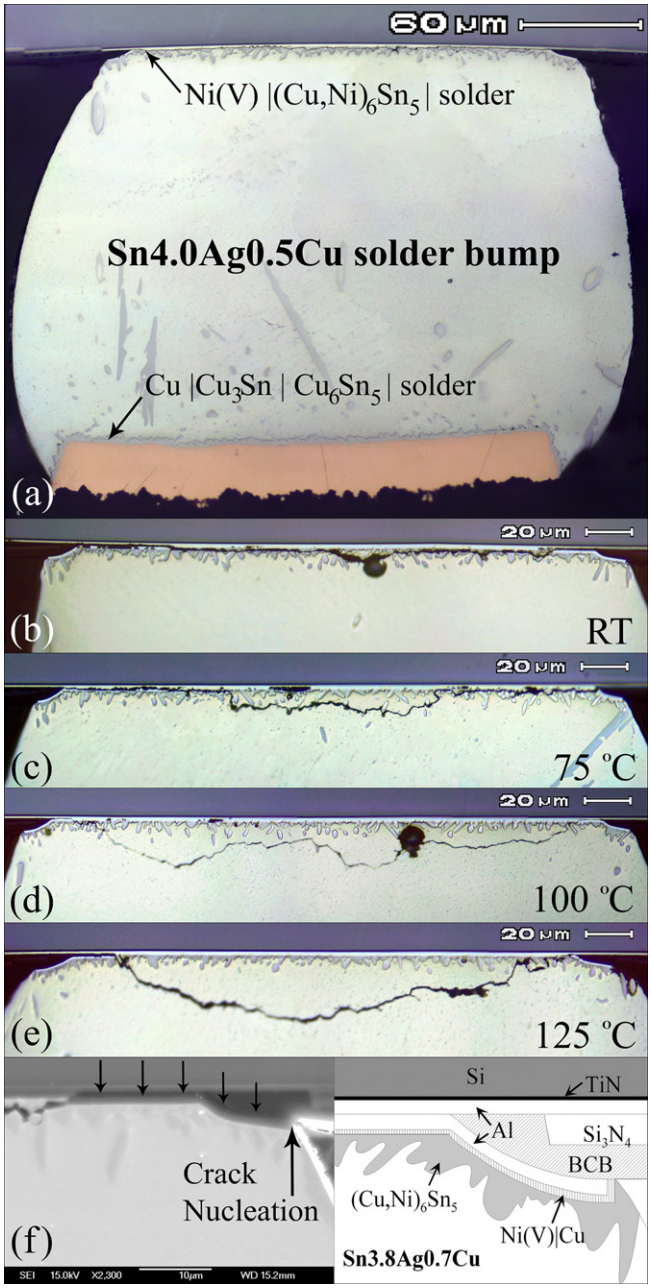


**Fig. 4.** The failure mode of the WL-CSP assemblies changed gradually from the cracking of the intermetallic layers to the cracking of the bulk solder with an increase in the temperature of the package: (a) geometry of the interconnections; (b) failure mode at room temperature; (c) failure mode at 75 °C; (d) failure mode at 100 °C; (e) failure mode at 125 °C; (f) crack nucleation site (the same at all temperatures).

propagate in the package-side $(Cu,Ni)_6Sn_5$ intermetallic layer, but, as the temperature of the package was increased, the crack propagation paths gradually changed from the interfacial layers into the bulk solder. The cracking of the intermetallic layers was rarely observed in the interconnections drop-tested at 125 °C.

The failure analyses of the CSP-BGA-1 component boards revealed a single failure mode. All the cracks that were identified were located in the package-side interfacial region of the solder interconnection (see Fig. 5) and not even crack nucleates were observed elsewhere. It is noteworthy that the shape and structure of the package side edge regions around the interconnections allowed the nucleation of cracks directly in the intermetallic layers (see Fig. 5f and g). After nucleation, cracks propagated along the

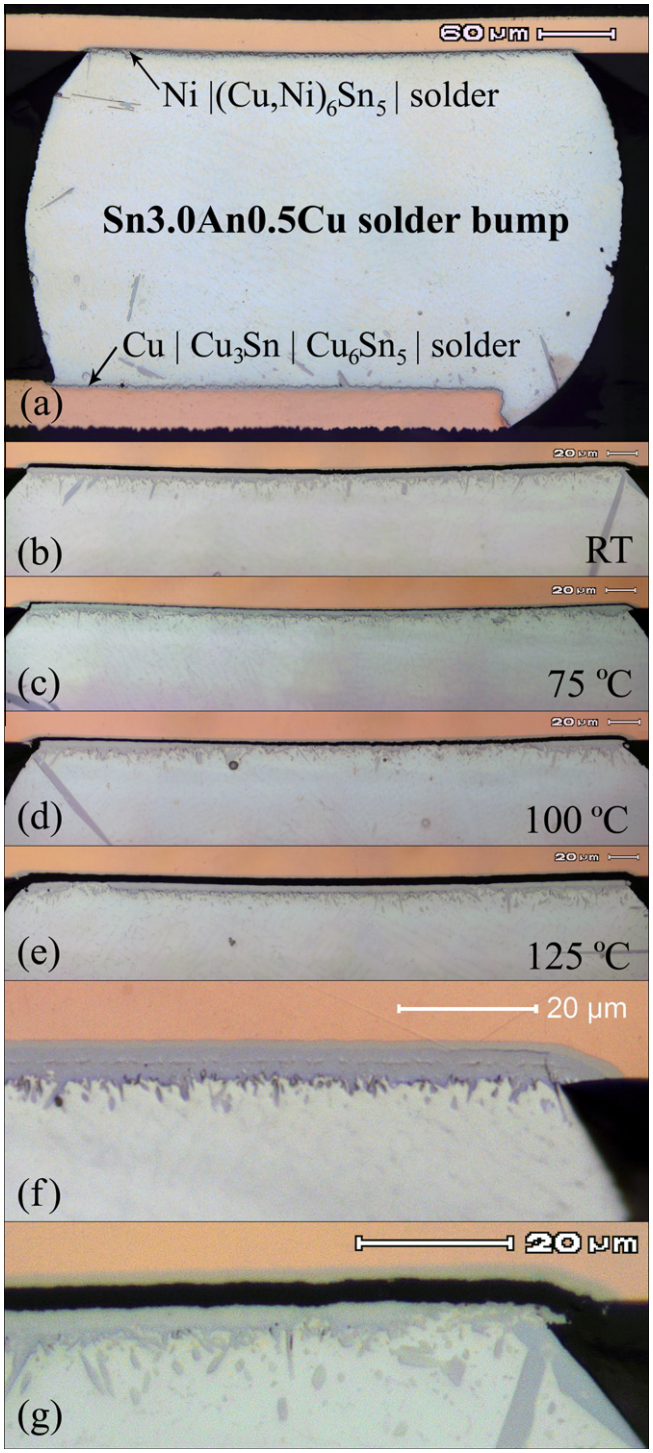


**Fig. 5.** The primary failure mode of the CSP-BGA-1 component boards at different temperatures (double-layer PWB): (a) geometry of the interconnections; (b) failure mode at room temperature; (c) failure mode at 75 °C; (d) failure mode at 100 °C; (e) failure mode at 125 °C; (f) form of the package-side edge regions of the interconnections and a crack nucleate; (g) cracks nucleated in the intermetallic layers (site did not change with temperature).

interface between the electrochemical Ni under bump metallization and the $(Cu,Ni)_6Sn_5$ layer. The propagation paths were very straight, without any distinguishable difference between different component boards drop-tested at the same or different temperatures. Neither the nucleation site nor the propagation path of the cracks changed with an increase in the temperature of the package.

The failure analyses of the CSP-BGA-2 component boards revealed a mix of different failure modes. At room temperature the primary failure mode was the cracking of the package-side interfacial layers, where the nucleation of the cracks took place at the bulk solder in the corner regions on the package side. Soon after nucleation the cracks entered the intermetallic layers, where they propagated in between the $Cu_6Sn_5$ layer and the Cu pad (see Fig. 6). The reason why the crack nucleation took place in the bulk solder instead of directly in the intermetallic layer (as in the case of CSP-BGA-1) is related to the different structure of the package-side edge regions of the interconnections (see Fig. 5f vs. Fig. 6f). The etching and cleaning treatments of the soldering pads of the package before bump attachment, together with the relatively fast dissolution of the copper during the reflow soldering, had formed a wide crater in the soldering pad and, thus, reformed the edge regions of the solidified solder interconnections. Only slight cracking was observed at the PWB side of the solder interconnection but the cracks were never observed to have propagated entirely through the interconnections. The cracking of the resin layer underneath the PWB copper pads was also identified occasionally. The cracks appeared along the outermost periphery of the solder interconnections but even though cracks appeared underneath the soldering pads, the copper trace on the PWB that comes out from the soldering pads did not fail. Thus, such under-pad cracks are not directly seen in the drops-to-failure measurements, but cracks that have developed can change the stress distribution of the interconnection and, thereby, indirectly affect the lifetime of the interconnections.

When the temperature of the component boards was increased to 70 °C the primary failure mode changed from the cracking of the package-side interfacial regions to the cracking of the copper traces on the PWB at the edges of the soldering pads. The copper traces failed in the vicinity of the cornermost interconnections of the package, as shown in Fig. 6c–e. The nucleation of the cracks took place at the interface between the solder interconnections and copper traces leading out from the interconnections. The cracks commonly propagated horizontally for about 10–30 µm in the intermetallic layers before the complete (horizontal) cracking of the copper trace. Fig. 6c and d shows that the horizontal cracking of the PWB-side intermetallic layer and the cracking of the copper trace are two competing failure mechanisms and that the IMC layer-cracking failure mode is the first to initiate but that the copper trace-cracking failure mode causes the electrical failure of the interconnections before the cracking of the IMC layer.

The failure analyses of the CSP-BGA-3 component boards revealed that the electrical breakdown of the component boards was caused by the cracking of the copper traces at the edge of the soldering pads in a similar manner as in the case of the CSP-BGA-2 boards at elevated temperatures (see Fig 7). The crack nucleation and propagation were also very similar. However, more severe cracking of the epoxy laminate underneath the soldering pads on the PWBs was noticeable at all temperatures. Furthermore, as illustrated in Fig. 7e, the cracking of the epoxy laminate took place earlier than the nucleation of the cracks in the copper trace, which was identified as the primary failure mode. It is hereby suggested that the failure mechanism of the copper trace cracking is fatigue of the copper trace, enhanced by the detachment of the soldering pad from the underlying epoxy. No other failure modes were observed and the primary failure mode was the same, regardless of the test temperature.

The micrographs shown in Fig. 8 show the primary failure mode of the CSP-BGA-4 component boards drop-tested at the different temperatures. Two different failure modes were identified – the cracking of the package-side intermetallic layers and the cracking of the PWB resin layer underneath the copper-soldering pads – but only one of them was directly responsible for the electrical

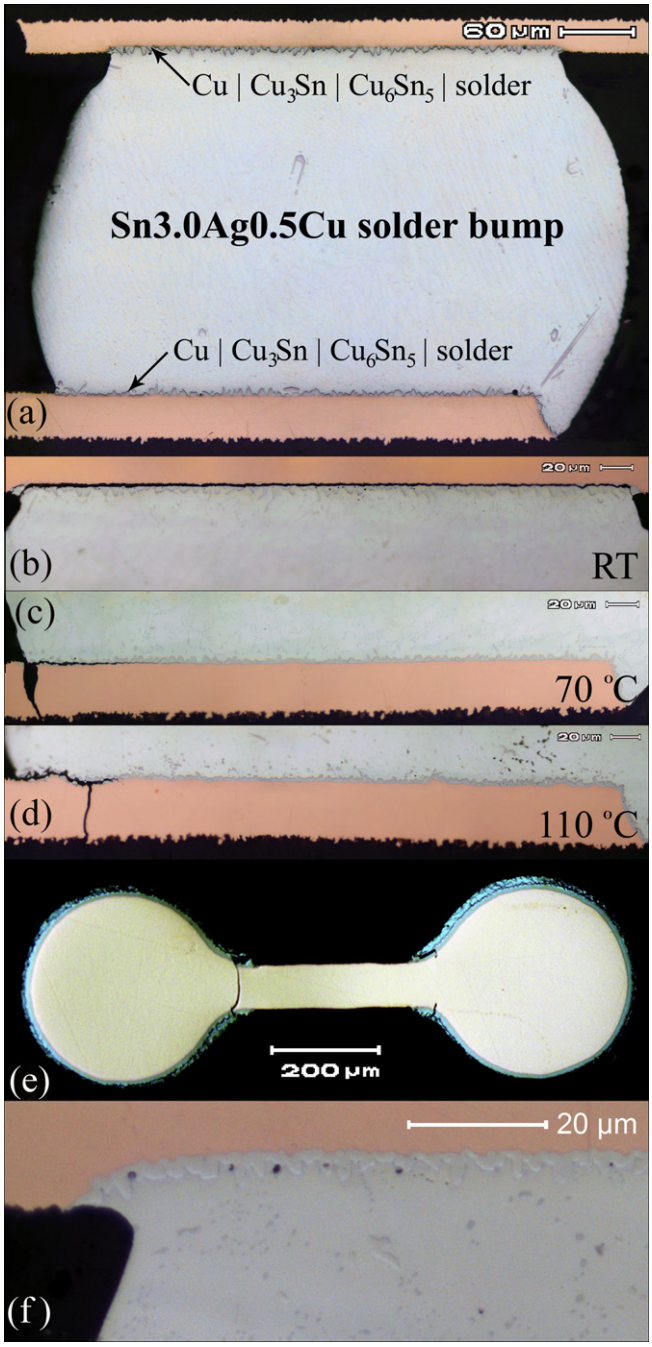


**Fig. 6.** Cross-section of the interconnections and the primary failure modes of the CSP-BGA-2 component boards at different temperatures (multi-layer PWB): (a) geometry of the interconnections; (b) failure mode at room temperature; (c) failure mode at 70 °C; (d) failure mode at 110 °C; (e) a view of the soldering pads on the PWB with the solder interconnections removed; (f) form of the package-side edge regions of the interconnections.

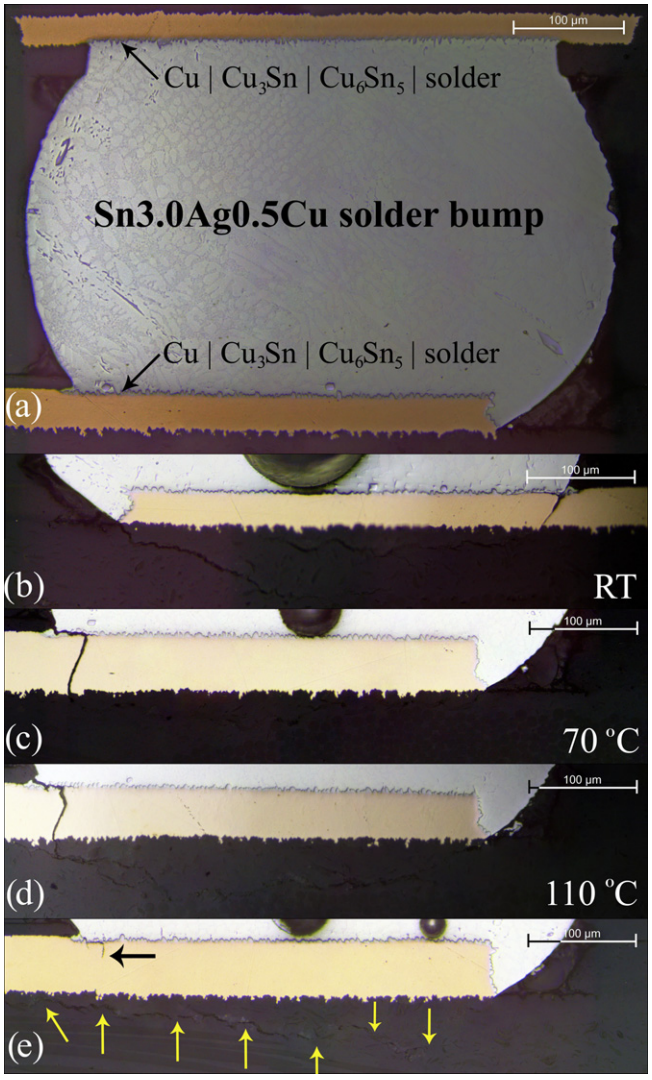


**Fig. 7.** Cross-section of the interconnections and the primary failure modes of the CSP-BGA-3 component boards at different temperatures (double-layer PWB): (a) geometry of the interconnections; (b) failure mode at room temperature; (c) failure mode at 70 °C; (d) failure mode at 110 °C; (e) development sequence of the cracks: the epoxy layer of the PWB cracks first, the pad detaches, and the copper traces fail because of fatigue.

failure of the assembly, as only the cracking of the intermetallic layer caused discontinuities in the daisy-chain networks. In all of the samples that were inspected the cracks were located in the package-side interfacial regions of the interconnection. Small cracks in the resin layer were identified at all temperatures but cracking of copper traces on the PWB was not observed. It is noticeable that the crack nucleation took place in the bulk solder on the package side, as in the case of the CSP-BGA-2 component boards (see Fig. 8e), but soon after nucleation the cracks entered the intermetallic layers, where they propagated in the $Cu_6Sn_5$ layer. The reason why the crack nucleation took place in the bulk solder is again related to the structure of the solder interconnections.

## 4. Discussion

In order to develop a more comprehensive understanding of the effects of temperature on the lifetimes of component boards undergoing drop tests, the different mechanisms by which the temperature can affect the interconnection strains and stresses during the impacts were studied in detail by taking into consideration the effects of temperature on the failure mechanisms of solder interconnections.

### *4.1. Effects of temperature on failure mechanisms*

In the JESD22-B111 drop tests the mechanical shock loads are produced by a traveling test table to which the component board is fastened at its four corners by means of screws on support poles.

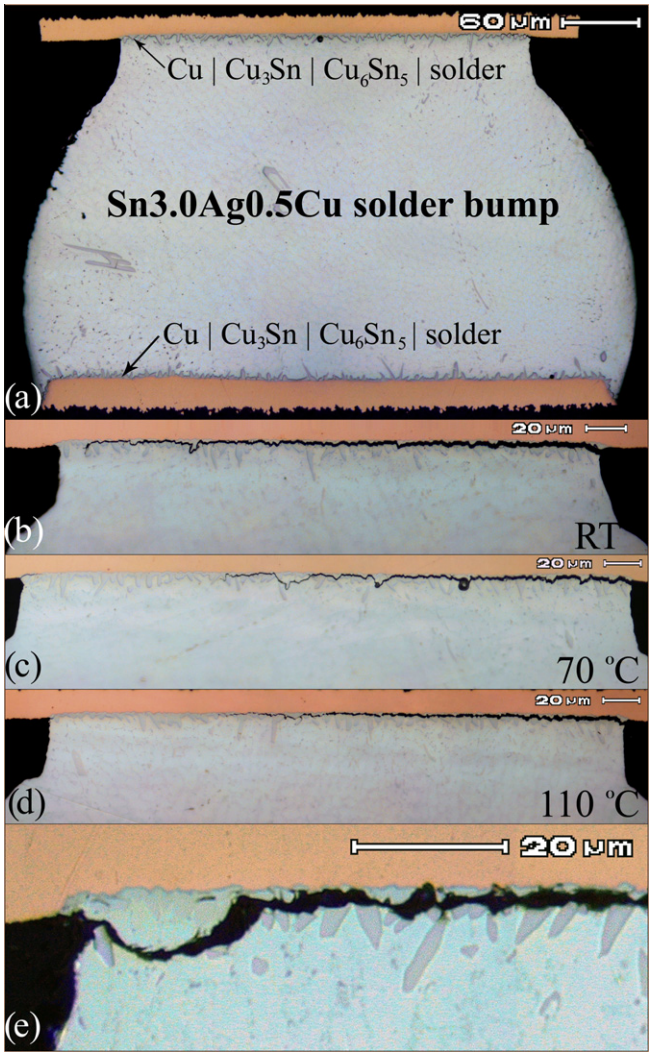


**Fig. 8.** Cross-section of the interconnections and the primary failure modes of the CSP-BGA-4 component boards at different temperatures (multi-layer PWB): (a) geometry of the interconnections; (b) failure mode at room temperature; (c) failure mode at 70 °C; (d) failure mode at 110 °C; (e) cracks nucleated in the bulk solder (site did not change with temperature).

It is well known that the failures produced during the drop tests are primarily caused by the bending of the printed wiring board, as forced by the inertia of the component board at the time of impact. After each drop impact the component board oscillates at high frequencies for about 20–30 ms. The free vibration of the component board can take place in many different modes simultaneously and the total bending of the board is the sum of these. The shapes of the natural modes depend mainly on the means of support of the component boards (four support points in this study) and its weight distribution, whereas the natural (resonant) frequencies depend on the dimensions, stiffness, and mass of the component board. However, the natural modes with lower frequencies are the most influential because their amplitudes are relatively large. The frequency of the lowest vibration mode of the JESD22-B111 compliant printed wiring boards employed in this work was about 200 ± 20 Hz and the board achieved a maximum bending displacement of about 5 ± 0.5 mm as measured from the center of the component board. The bending of the PWB causes displacements between the board and packages, the packages resist the bending of the PWB, and the interconnections between the packages and the PWB carry the induced strains and stresses. Thus the loading condition of the solder interconnections is similar to static bending, except that the strain is applied at a much faster rate than that commonly used in the bending tests. The finite element calculations presented elsewhere show that the average strain rate in the cornermost solder interconnections of a package with a very similar structure and dimensions is several hundred percent per second but that locally it can reach values above 1000% [19,24]. Within the temperature range of our study, the plastic flow of the solder is heavily strain rate-dependent and the strength increases exponentially with the strain rate. It has been proposed that under mechanical shock loading the intermetallic compound layers fail instead of the bulk solder essentially because the strain-rate hardening of the solder interconnections under fast deformation rates increases the stresses in the edge regions of the interconnections above the fracture strength of the brittle intermetallic layer [25]. Thus, in principle, under each drop load the intermetallic layers are under an over-stress condition but the component boards do not fail at the first drop impact because a certain amount of work is required to nucleate the cracks and to make them propagate through the narrow polycrystalline intermetallic layer(s) from one edge of the interconnections to the other. Readers interested in a more comprehensive discussion of the subject are referred to the literature [26–29].

A change in the component board temperature can affect the drop test failure mechanism described above in at least three different ways. An increase in the temperature: (a) reduces the stiffness of the PWBs; (b) reduces both the yield strength and the elastic modulus of the solder interconnections (that are at high homologous temperatures); and (c) introduces thermally induced stresses when the temperature of the package is increased from room temperature to the test temperature. Note, however, that the temperature during the drop testing is stabilized to within +/−5 °C of the target temperature.

Fig. 9 shows an adaptation of results published in [19,30]. The diagram shows that the strength of the solder decreases by about 45% with an increase in the testing temperature from 22 °C to 110 °C at the 100%/s strain-rate. The decrease of the elastic modulus is smaller, only about 10% [19]. Because of the reduced strength of the solder interconnections, plastic deformation of the solder interconnections during the shock impacts is more significant and the levels of the highest stresses in the interconnections are reduced. Since the strain-rate hardening of the solder bulk and increase stresses in the solder interconnections are central to the formation mechanism of the cracking of the intermetallic layer, the reduced stress levels may cause a change of failure mode from the (brittle) cracking of the intermetallic layers to the (ductile) cracking of the bulk solder.

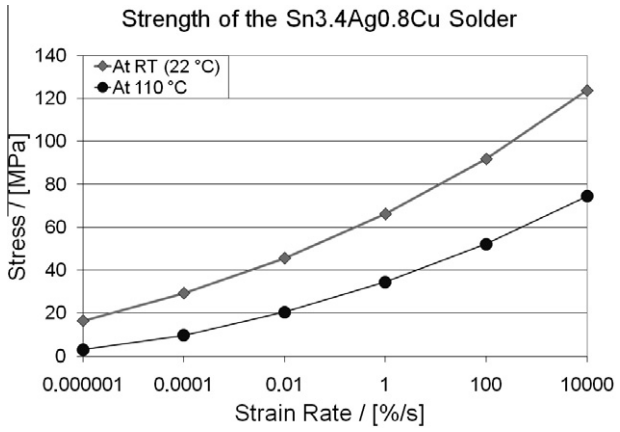


**Fig. 9.** Strain-rate sensitivity of Sn3.4Ag0.8Cu solder at 22 °C and at 110 °C [19,30].

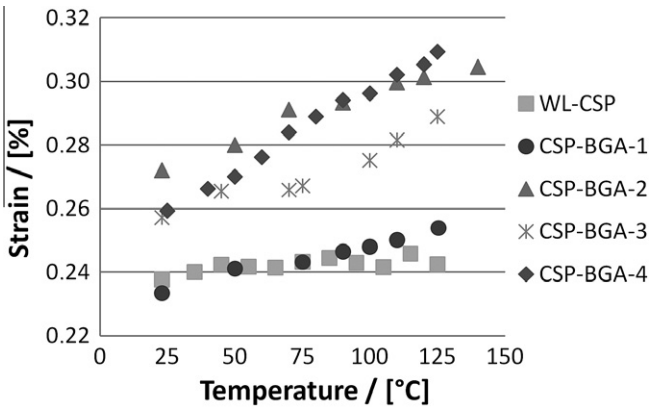


**Fig. 10.** Maximum strains on the PWB as measured by strain gauges at the location shown in Fig. 1c. The location is the same for all the measurements.

The stiffness of the PWB is also temperature-dependent and, therefore, the strains and stresses in the interconnections are consequently changed. Fig. 10 shows the maximum strains measured in the longitudinal direction on the PWBs during the drop impact at different temperatures over the temperature region of the tests. The strain gauges were calibrated and strain adjusted to zero before each measurement and, therefore, the measured values do not include the strain caused by the thermal expansion when the boards were heated up. The measured strain magnitudes of the multi-layer printed wiring boards were higher than those of the double-layer printed wiring boards. More importantly, the measurements show that the maximum strains of all the CSP-BGA component boards are increased with an increase in the temperature of the package, while the increase in the maximum strains on the WL-CSP component boards is much smaller. The fact that the bending amplitudes of the component boards with larger packages increase, while the bending of those with the smaller packages remains more or less unchanged, can be understood by comparing the infrared images of the component boards presented in Fig. 11. Because of the much higher power of the heating elements and greater heat dissipation from the large CSP-BGA packages, the heat is conducted over a much wider range in their PWBs as compared to the PWB of the WL-CSP packages. The highly localized heating in the case of the WL-CSP makes the effect of the reduced stiffness of the PWB rather insignificant, while it is highly significant in the case of the CSP-BGA package board. As can be seen from Fig. 11a, in the case of the WL-CSP packages the temperature along the shorter axis of the board (the scale on the left-hand side of the image) remains at room temperature for about two thirds of its length, while in the case of the CSP-BGAs on the multi-layer FR4 (Fig. 11c) the temperatures are above 50 °C over the entire length of the axis.

As mentioned earlier, an increase in the temperature of the package during the drop test reduces the strength of the solder, increases the bending amplitude of the PWB, and introduces thermally induced stresses. For example, the effects of increased bending amplitude and reduced solder strength on the lifetimes of the component boards are opposite. Therefore, in order to fully understand the effects of temperature on the lifetimes of the component boards under the drop tests, the stress–strain analysis must be taken to the interconnection level. But before going any further, two points should be made.

First, it is interesting to notice that the levels of the maximum strains in the case of the multi-layer boards (CSP-BGA-2 and CSP-BGA-4) are rather uniform, while those of the double-layer boards (CSP-BGA 1 and CSP-BGA-3) differ significantly. The structures of the double-layer PWBs are identical. They only have different package footprints. The materials were also ordered from the same supplier with identical specifications. The boards were manufactured at different times, however. The most likely explanation for the observed difference in their mechanical properties is the fact that the component boards must have received somewhat different temperature treatments during their manufacture. For example, the baking times of the PWBs during different manufacturing steps can significantly affect the stiffness of the boards. This is the only possible explanation known to the authors for the observed difference in the mechanical response.

Second, all the component boards that showed increased maximum strains also showed a reduced average number of drops to failure with an increase in temperature except the CSP-BGA-1 boards, whose average lifetime remained relatively constant even though the maximum strains increased. The failure analyses of the CSP-BGA-1 component boards showed that the cracks nucleated directly in the intermetallic layers and propagated along them through the interconnections. Neither the nucleation site nor the propagation path of the cracks changed with temperature. Room temperature and even the highest elevated test temperature of 125 °C are relatively low with respect to the peritectic points of the Sn–Cu intermetallic compounds (125 °C for $Cu_6Sn_5$ is about 0.6 in terms of homologous temperature) and the particular difference between room temperature and 125 °C in terms of homologous temperature is only about 0.1. Therefore one can expect the cracking of the intermetallic layers to be rather insensitive to changes in temperature within the temperature range of this study. This assumption is supported by the lifetime statistics and the failure analyses of the CSP-BGA-1 component boards. As the maximum stress levels in the interconnections remain above the fracture strength of the intermetallic layers at all the temperatures, any change in the stress–strain levels of the interconnections does not cause a difference in the lifetimes. Furthermore, the average number of drops to failure of the CSP-BGA-1 component boards was significantly lower than that of the CSP-BGA-2 or the CSP-BGA-4 component boards, which also failed as a result of the cracking of the package-side intermetallic layers. The inferior reliability can be explained by the different choice of under bump metallizations. The under bump metallization of the CSP-BGA-1 was Ni, whereas in all other CSP-BGAs of this study it was Cu. When the Cu content of the solder alloy being used is above about 0.4 wt.% (at 240 °C), the type of intermetallic layer formed at the interface between the solder and Ni or Cu is the same, $Cu_6Sn_5$, but when it is formed on Ni metallization, relatively large amounts of Ni are dissolved into the layer and is commonly denoted as $(Cu,Ni)_6Sn_5$ [31,32]. Whether intermetallic compound is $Cu_6Sn_5$ or $(Cu,Ni)_6Sn_5$, there seems to be only a little difference in terms of thickness and morphology of the layer. The morphology of the $(Cu,Ni)_6Sn_5$ is a bit more angulated than the round scallop type $Cu_6Sn_5$ layer. However, the mechanical properties seem to be different.

The effects of Ni in the reaction layers between Cu and Sn have gained a lot of attention recently as a result of the observed benefits for drop test reliability: a minor addition of Ni to SnAgCu solders (1) reduces the thickness of the $(Cu,Ni)_3Sn$ layer as the function of increased Ni content in the solder and (2) reduces the grain size of the $(Cu,Ni)_6Sn_5$ layer [33–36]. These changes can make the intermetallic layers more resistant to failures [21,34–37]. However, these benefits are associated only with minor additions of Ni to the solder. Vuorinen et al. have reported that increasing the Ni content at the solder|copper pad interface reduces the total thickness of the reaction layers only up until about 0.1 at.% of Ni, after which it starts increasing again [33]. The metastable solubility of Ni in $Cu_6Sn_5$ can be as high as 20 at.% [38], even though the stable solubility is only about 4 at.% [39]. Thus, when Ni is used as a metallization, the amount of Ni dissolved in the intermetallic layer is much larger and the effects are different. It has been observed that

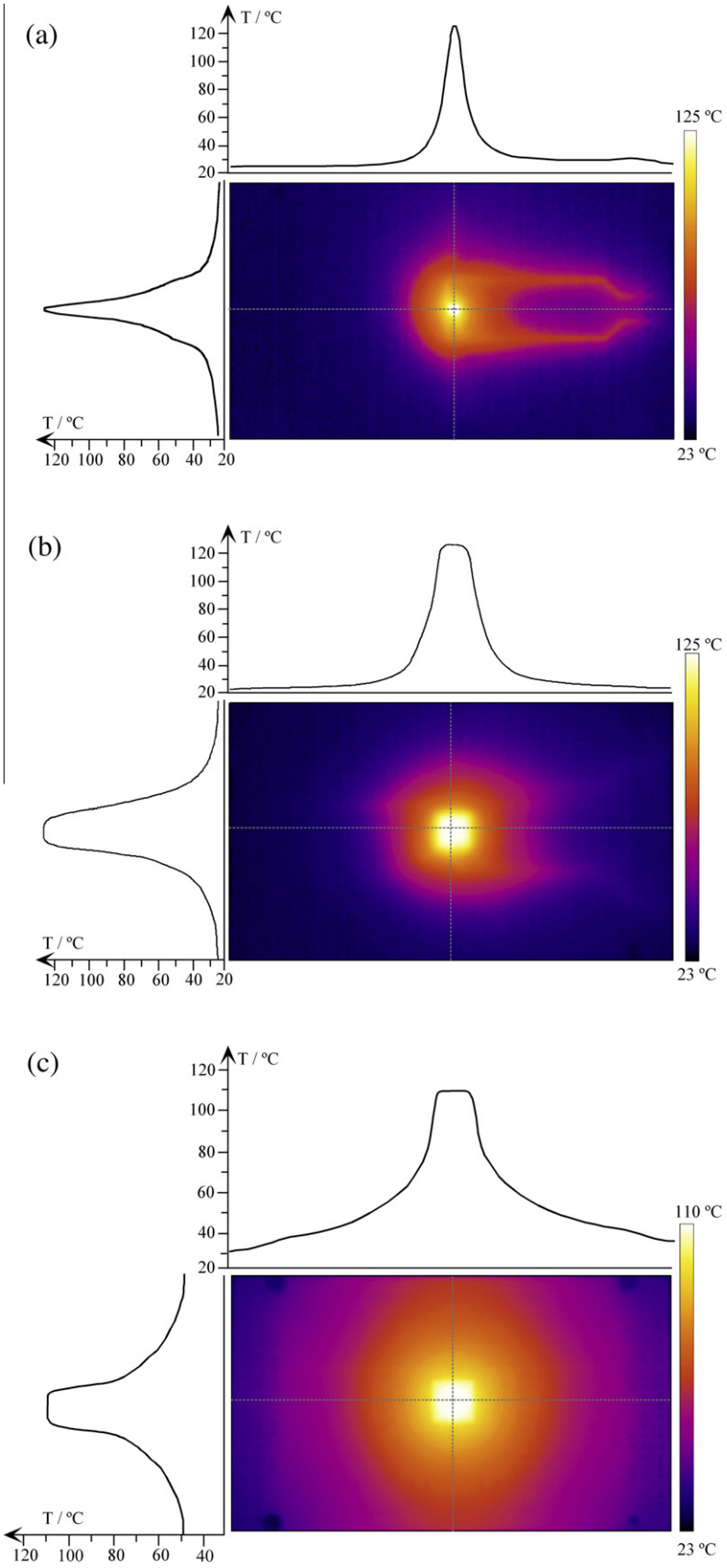


**Fig. 11.** Temperature distributions of the component boards at 125 °C (as measured from the surface of the packages): (a) the WL-CSP on the double-layer FR4; (b) the CSP-BGA on the double-layer FR4; (c) the CSP-BGA on the multi-layer FR4.

**Table 4**
The case studies constructed to quantify the effects of temperature.

| | Reference | Case I | Case II | Case III |
|---|---|---|---|---|
| The 1st step: thermomechanical | – | Included | – | – |
| The 2nd step: mechanical shock | PWB at 23 °C, solder at 23 °C | PWB at 100 °C, solder at 100 °C | PWB at 100 °C, solder at 100 °C | PWB at 100 °C, solder at 23 °C |
| Factors considered | – | a, b, c | a, b | a |

Factors: (a) change in PWB stiffness; (b) change in yield strength and elastic modulus of solder, and (c) thermomechanical strains and stresses.

large amounts of Ni can make the $Cu_6Sn_5$ more brittle [40–43]. Cracks have been observed even in samples that have been prepared after soldering (i.e. with no external load applied) [40,42]. Therefore we assume that the fracture strength of the $(Cu,Ni)_6Sn_5$ in the Ni metallization is markedly lower than that of the $Cu_6Sn_5$. This is evidence by our prior studies [26,28] and the fact that the lifetime of the CSP-BGA-1 is about half that of the CSP-BGA-2 and CSP-BGA-3. Furthermore, at the time of writing the mechanical properties of the intermetallic layers were not fully known. Because the failure mode and mechanism of the CSP-BGA-1 interconnections are chiefly dependent on the properties of the intermetallic layers, the case of CSP-BGA-1 component boards is excluded from the following numerical analyses.

### 4.2. Effects of temperature on strains and stresses in the interconnections

In order to gain a better understanding of the effects of temperature on the observed failure modes and lifetimes of the solder interconnections, a detailed stress–strain analysis was carried out by means of comparative case studies and employing the finite element method. As discussed above, the magnitude of the strains and stresses in the proximity of the solder interconnections during the drop impacts depends on the effect of the temperature on: (a) the stiffness of the PWB; (b) the yield strength and elastic modulus of the solder; and (c) the thermomechanical strains and stresses, as caused by the increase in temperature from room temperature to the test temperature. In the following discussion we refer to these effects as factors (*a*), (*b*), and (*c*), respectively. The interaction between the factors was considered negligible and, therefore, their effects on the drop reliability were studied independently. The finite element analyses of the thermomechanical and mechanical loads were carried out sequentially. The first step of the analysis was to quantify the stress–strain response of the solder interconnections to a change in the temperature from room temperature to the elevated temperature of 100 °C. The second step was to quantify the effects of the purely mechanical shock load while the assigned temperature distribution of the component board remained unchanged. To quantify the effects of the three factors, three independent case studies were designed and the results were compared to the reference case, which was calculated by using room temperature values for the material parameters (see Table 4). Case study I was calculated by including the thermomechanical stresses produced by the heating of the package, using the 100 °C values for the solder and the measured temperature distribution of the PWB in order to include the effects of all three factors in the calculation. Case study II was constructed in order to study the effects of the thermomechanical stresses produced before the drop impact (*c*), which is quantified as the difference between Case studies I and II. Case study III was introduced in order to study the effect of changes in the stiffness of the PWB as caused by the change in temperature (*a*). The effect of the reduced strength and elastic modulus of the solder (*b*) can be quantified by the difference between Case studies II and III.

**Table 5**
Calculated stresses and strains for WL-CSP component boards.

| Variable | Reference | Case I | Case II | Case III |
|---|---|---|---|---|
| Peeling stress (MPa) | 64.13 | 62.66 | 47.8 | 66.6 |
| von Mises stress (MPa) | 44.11 | 43.04 | 33.19 | 45.78 |
| Equivalent plastic strain | 1.04 | 1.65 | 1.17 | 1.09 |
| Factors considered | – | a, b, c | a, b | a |

Factors: (a) change in PWB stiffness; (b) change in yield strength and elastic modulus of solder, and (c) thermomechanical load.

#### 4.2.1. The case of WL-CPS boards

The solder interconnections with the highest strains and stresses were found in the corners of the packages in all the package types that were studied. The calculated maximum peeling stresses, von Mises stresses, and equivalent plastic strains in the package-side interfacial regions of the WL-CSP component boards are listed in Table 5. In the case of the WL-CSPs the lifetime of the component boards increased significantly with an increase in temperature, while the crack nucleation site did not change, but the crack path did change gradually from the intermetallic layers to the bulk solder. Plastic strain is a commonly used failure criterion for fatigue-based failure mechanisms, such as the cracking of the solder bulk or the copper traces also observed in this study. The plastic deformation of the solder bulk or the copper traces was quantified by the equivalent plastic strains. However, because of the brittleness of the interfacial intermetallic compound layers, stress is a more appropriate criterion for the failure modes, where cracking takes place along these layers. More specifically, the peeling stress (S33) is used as the failure criterion for intermetallic cracking. Furthermore, in all of the component boards that were studied the peeling stress (S33) was much higher than the other stress components. It is apparent that the von Mises stress follows the same trend as S33 but its magnitude is smaller. The von Mises stress was used to determine the yielding of the solder bulk or the copper trace. It should be noted that the intermetallic layers were not included in the finite element modes. They are too thin and have a highly irregular morphology, and their mechanical properties are not well enough known for them to be taken into account quantitatively. Therefore we assume that the stress values in the vicinity of the interconnections in the solder bulk can be used to represent the stresses in the intermetallic layers.

By comparing Case III and the reference case, one can conclude that the reduced stiffness of the PWB (*a*) alone causes a 3.852% increase in the peeling stress (values are reported with three decimals in order to make a point later on). However, in the comparison of Cases II, III, and the reference case, the effect of the reduced strength and elastic modulus of the solder (*b*) alone is a 29.315% decrease in the peeling stress (the effect of (*b*) is the difference between the values of Cases II and III, related to the absolute values of the reference case). Furthermore, a comparison of Cases I and II shows that the effect of the thermomechanical stresses (*c*) alone is an increase in the peeling stress by 23.172%. Summing the effects from all the three factors, the overall effect of changing temperature (*a*, *b*, *c*) is calculated: $3.852\% - 29.315\% + 23.172\% = -2.29\%$ (i.e. about 2.3% decrease in the peeling stress), which equals the relative difference between

Case I and the reference case (−2.29%) with two decimal points. This gives strong support for our assumption of the independence of the factors that were studied.

It should be noted, however, that this calculation neglects the effect of creep relaxation, which is known to be efficient for solder at such high (homologous) temperatures. Therefore, the effect of the thermomechanical load is probably somewhat exaggerated in the calculations. Since the effects of the factors are independent, on the basis of the calculations presented one can easily calculate that, for example, assuming perfect creep relaxation (i.e. disregarding factor (*c*) entirely) would result in a decrease of 25.4% in the value of the peel stress.

While the yield strength of the solder is reduced as a result of the increased temperature, the plastic strain of the solder, as quantified by the equivalent plastic strain, is increased. If Case I and the reference case are compared, a 58% increase in the plastic strain is observed. Thus it is suggested that as a result of the reduced maximum stresses and increased plastic strain, the crack path changes from the intermetallic layers to the bulk solder and the average number of drops to failure increases as a consequence of the change in the crack propagation path. The energy needed for the propagation of the cracks through the (ductile) bulk of the solder is higher than that needed for propagation through the brittle intermetallic layers and, therefore, the lifetimes under the test are different.

#### 4.2.2. The case of CSP-BGA-4 boards

In this study the effects of temperature on the failure modes and lifetimes of the CSP-BGA component boards were quite different from the case with the WL-CSP component boards. The lifetimes of the CSP-BGA component boards decreased and the failure modes may or may not change with an increase in temperature. Furthermore, even if the failure mode did not change with temperature, different types of component boards can fail in different failure modes: the cracking of the intermetallic compound layers or the copper traces was observed in this study. The calculated maximum peeling stresses, von Mises stresses, and equivalent plastic strains of the CSP-BGA-4 component boards are listed in Table 6. In this particular case, the identified failure mode was the cracking of the package-side intermetallic layers, but the nucleation of the cracks took place in the bulk solder (see Fig. 8). The site of crack nucleation or the path of crack propagation did not change with a change in temperature. Because the crack nucleation took place in the bulk solder but the crack propagation took place in the intermetallic layers, a different criterion should be used for these two phases of failure. The equivalent plastic strain is used for crack nucleation and the peeling stress is used for crack propagation.

It should be noted that the calculated stresses and strains in the CSP-BGA-4 interconnections are notably higher than those in the WL-CSP interconnections. This difference in the dimensions is the most significant reason for the differences in the interconnection stresses and strains. The effects of factors (a), (b), and (c) on the magnitude of the peeling stress was calculated in the same manner as with the WL-CSPs and the result is a 4.0% reduction in the peeling stress (+2.2%, −16.4%, and +10.2% for factors (a), (b), and (c), respectively). Thus, the significant decrease in the average lifetime with an increase in temperature cannot be explained by crack propagation as caused by the changed stresses in the solder interconnections. The fact that the influence of an increase in temperature on the peeling stress is, in fact, opposite to that on the lifetime indicates that the impact of an increase in temperature is much more significant in the crack nucleation phase than on the crack propagation phase. The values of the equivalent plastic strain reported in Table 6 show that the plastic strain in the edge regions of the solder interconnections is increased by about 63%. Therefore it is suggested that the decrease in the average number of drops to failure is caused by the enhanced nucleation (not propagation) of cracks as a consequence of an increase in temperature.

**Table 6**
Calculated stresses and strains for CSP-BGA-4 component boards.

| Variable | Reference | Case I | Case II | Case III |
|---|---|---|---|---|
| Peeling stress (MPa) | 85.01 | 81.6 | 72.89 | 86.84 |
| von Mises stress (MPa) | 73.47 | 64.53 | 58.31 | 74.78 |
| Equivalent plastic strain | 2.35 | 3.83 | 2.98 | 2.48 |
| Factors considered | – | a, b, c | a, b | a |

Factors: (a) change in PUB stiffness; (b) change yield strength and elastic modulus of solder, and (c) thermomechanical load.

#### 4.2.3. The case of CSP-BGA-2 and CSP-BGA-3 Boards

The failure analyses of the CSP-BGA-2 and CSP-BGA-3 component boards revealed another kind of failure mode, namely the cracking of the copper trace. The failure mode of the CSP-BGA-2 changed with an increase in temperature from the cracking of the intermetallic layers to copper trace cracking (see Fig. 6), whereas the failure mode of the CSP-BGA-3 component boards was copper trace cracking at all the temperatures (see Fig. 7). In both cases the average number of drops to failure decreased with an increase in the temperature. The finite element analyses were carried out in the same manner as earlier but this time the plastic deformation of the copper traces was used as the failure criterion. Fig. 12 shows two equivalent plastic strain (PEEQ) contour images of interconnections with and without a solder bump. The images illustrate how the plastic strain concentrates on the copper trace near the boundary between the solder bump and the copper trace. A comparison of the absolute plastic strain values in the copper traces of the CSP-BGA-2 and CSP-BGA-3 component boards helps us to understand the observed differences in the failure modes.

The maximum values of the PEEQ during the drop impact at the two different temperatures are listed in the table embedded in Fig. 12. For the CSP-BGA-2 component boards, the PEEQ increased

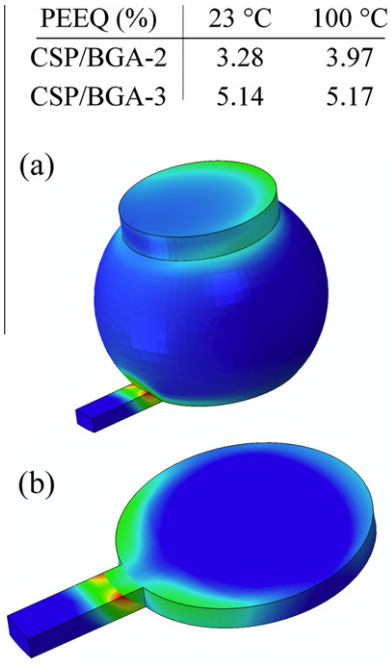


**Fig. 12.** Strain concentrations on the copper trace near the edge of the soldering pads: (a) equivalent plastic strain (PEEQ) contour of the solder bump and the copper trace; (b) enlarged view of the copper trace and pad.

by about 21% when the temperature of the package was raised from room temperature to 100 °C. In the room-temperature tests the CSP-BGA-2 component boards failed as a result of the cracking of the intermetallic layers on the package side but an increase in the package temperature to 100 °C increased the plastic strain of the copper trace significantly. The change in the failure mode cannot be explained by the increase in the plastic strain alone but the results indicate that the increase is large enough to change the primary failure mode from the intermetallic layers to copper traces on the PWBs. In the case of the CSP-BGA-3, the increase was not as significant but the absolute value of the PEEQ is relatively high at both test temperatures. The absolute value of the PEEQ in the case of the CSP-BGA-3 drop -tested at room temperature is 29% higher than that of the CSP-BGA-2 drop-tested with the package at a temperature of 100 °C. Plastic deformation of this magnitude in the copper trace seems enough to cause the cracking of the copper trace even at room temperature.

## 5. Conclusions

The effects of package temperature on the drop reliability of electronic assemblies were studied experimentally and evaluated by employing the finite element method. The temperature influences the strains and stresses in the solder interconnections through the change in (a) the stiffness of the PWB, (b) the strength and elastic modulus of the solder, and (c) the thermomechanical loads, as caused by the rise in the temperature to the elevated test temperature. The temperature change affected the mechanical properties of the solder most significantly, while its effects on the PWB stiffness were the weakest. The influence of the thermomechanical loads can be strong but it depends on the creep relaxation rate of the solder and the thermal history before shock impact, e.g. the rate of temperature change and the stabilization time before the drop.

The drop reliability of two different high-density packages (WL-CSP and CSP-BGAs) assembled on two sets of printed wiring boards (double-layer and multi-layer FR4) was studied at room temperature and at elevated temperatures. The package type had a statistically significant effect on the lifetime of the component boards, while the effect of the printed wiring board type was insignificant. The results of the **WL-CSP** component boards showed that with an increase in the temperature of the package: (i) the average number of drops to failure increased; (ii) the peeling stress in the interfacial regions of the solder interconnections decreased, while the plastic strain increased (with an increase in the temperature); and (iii) the crack path changed gradually from the intermetallic layers to the cracking of the bulk solder. It was suggested that the measured increase in the number of drops to failure is a consequence of the change in the failure mode from the brittle intermetallic layers to the more ductile bulk solder.

The statistical analyses of the drop test results showed that the average number of drops to failure of the CSP-BGA component boards decreased significantly. The drop reliability of one of the four different types of CSP-BGA component boards was insensitive to the temperature. This difference was attributed to the unfavorable effects of Ni as an under bump metallization and the design of the interconnection geometry. All the electrical failures of the **CSP-BGA** component boards were caused by the cracking of the intermetallic layers or the cracking of the PWB copper trace in the vicinity of the solder interconnections. The following conclusions were made: (i) The lifetimes of the CSP-BGA component boards decreased. (ii) regardless of the failure mode, which may or may not change with an increase in the temperature. (iii) It was suggested that the decrease in the average number of drops to failure is caused by the enhanced nucleation (not propagation) of cracks as a consequence of increased plastic strain at the nucleation site, namely at the edges of the solder interconnections or at the surface of the copper traces.

Finally, the results presented in this paper exemplify why modifications to the reliability test standards that are currently employed are needed. Single-load reliability tests can form an incomplete understanding of the failure mechanisms in real service environments, where the various loadings take place simultaneously.

## Acknowledgements

The authors wish to thank Dr. Luu Nguyen from National Semiconductor and Dr. Ahmer Syed from Amkor for their help and support for this work. The authors would also like to acknowledge the valuable help of Ms. Essi Kaloinen, Ms. Pirjo Kontio, Ms. Sini Niiranen, Ms. Riitta Viitala, Mr. Rony James, Mr. Markus Nuotto, Mr. Antti Rautiainen, Mr. Jan Šimeček, Mr. Lauri Suotula, and Dr. Vesa Vuorinen. The financial support of the Finnish Funding Agency for Technology and Innovation, the Aspocomp Group, National Semiconductor, and Nokia are also gratefully acknowledged.

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