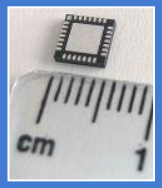




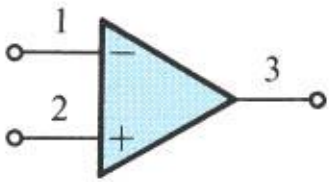
ELT 061 – Dispositivos e Circuitos Eletrônicos Básicos

Amplificadores Operacionais

DEPARTAMENTO DE ENGENHARIA ELETRÔNICA
UNIVERSIDADE FEDERAL DE MINAS GERAIS

Símbolo do Amplificador Operacional

1965 – primeiro circuito integrado – amplificador operacional µA 709



$$v_o = A(v_2 - v_1)$$

1 – entrada inversora
2 – entrada não inversora
3 – saída

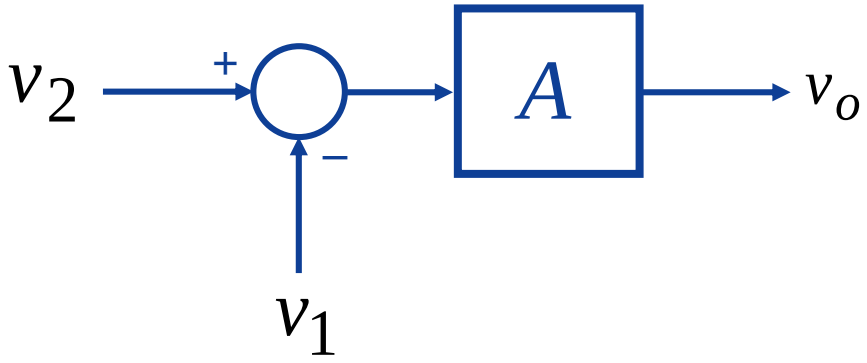
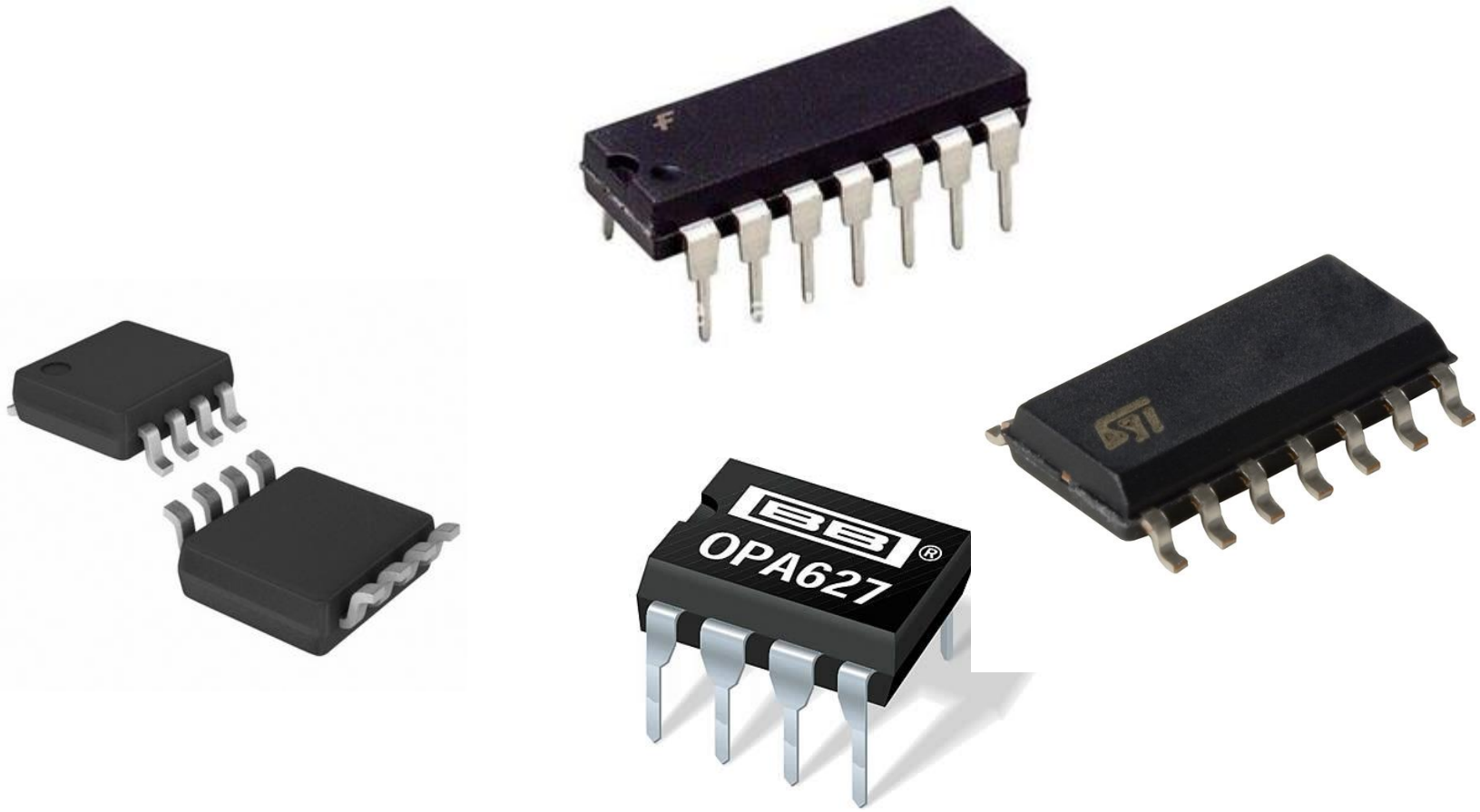


Figure 2.1 Circuit symbol for the op amp.

Encapsulamentos



Fontes de Alimentação

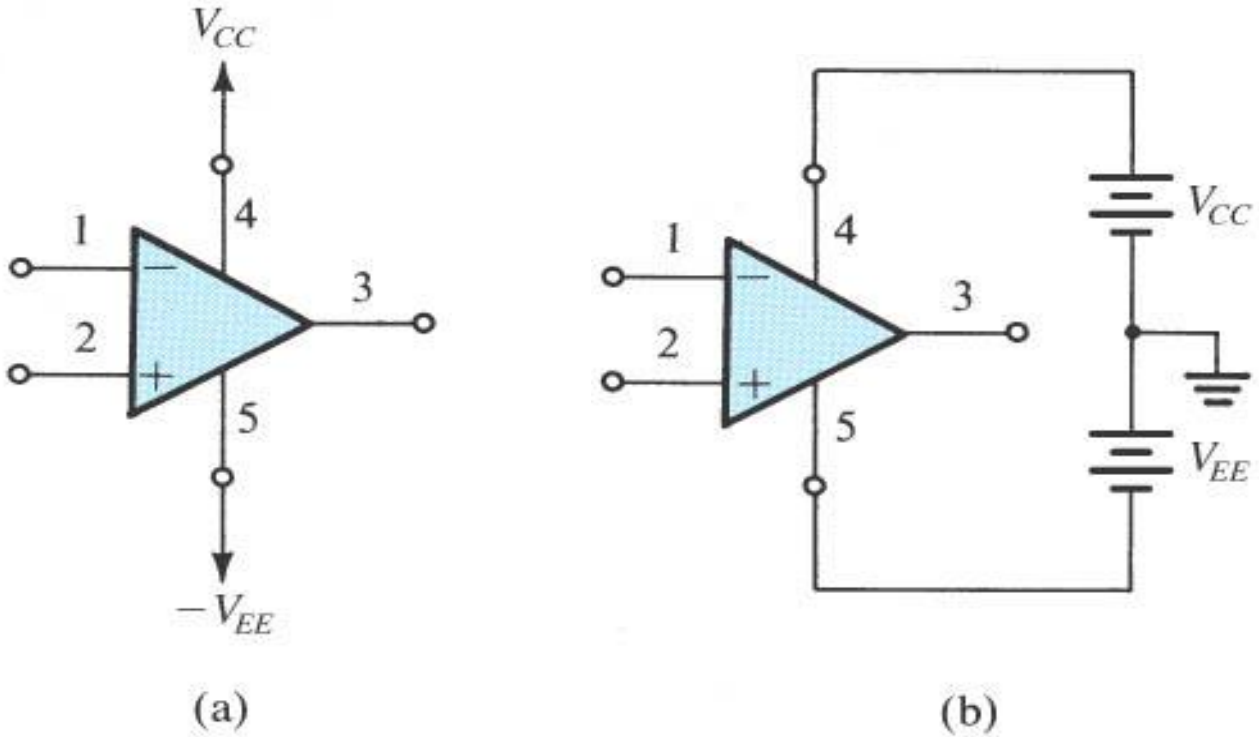


Figure 2.2 The op amp shown connected to dc power supplies.

Circuito Equivalente do A.O. ideal

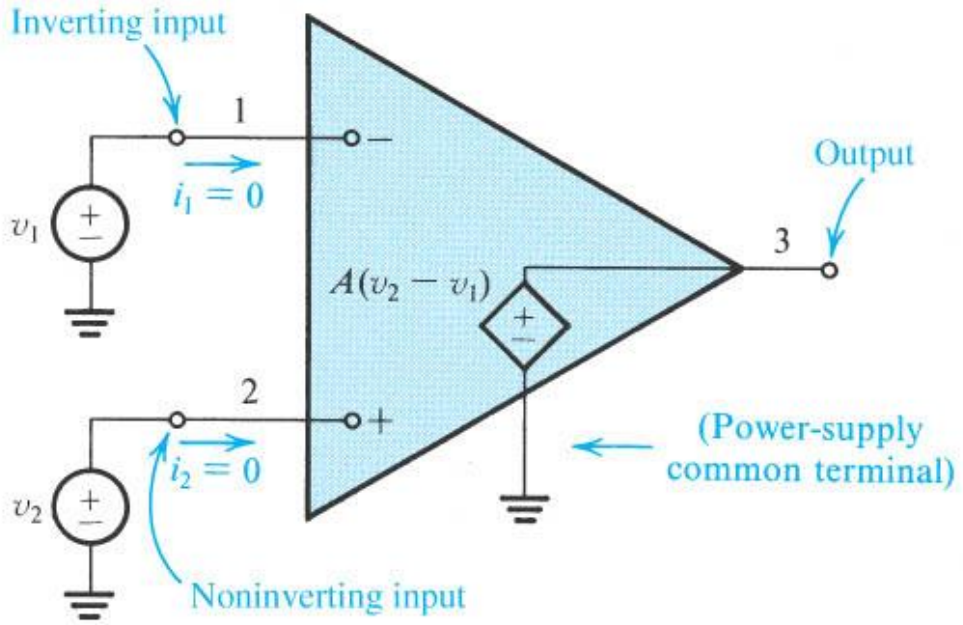


Figure 2.3 Equivalent circuit of the ideal op amp.

Características Ideais:

- Ganho diferencial infinito.
- Resistência de entrada infinita.
- Resistência de saída nula.
- Faixa de passagem infinita.

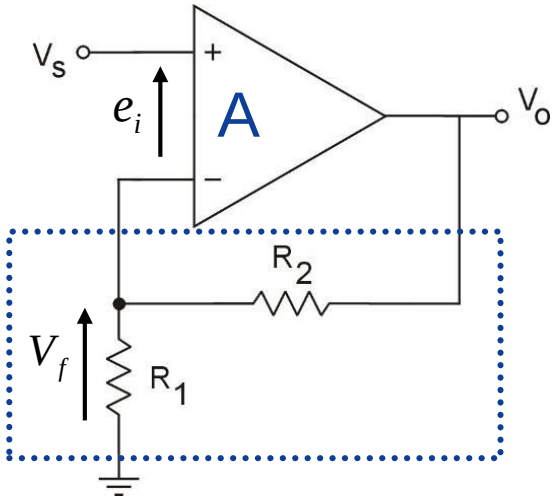
Exemplo: LM 741

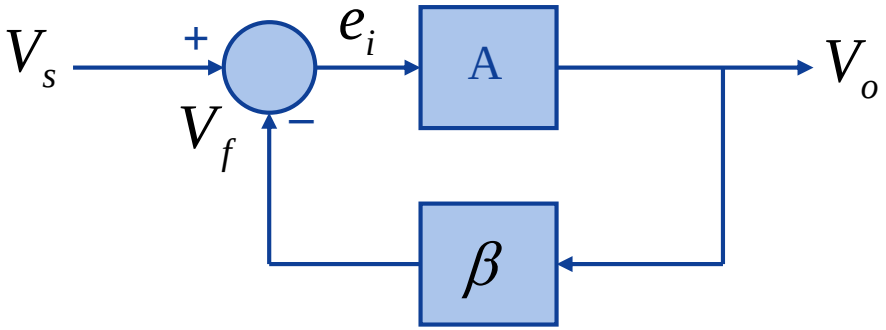
$A = 200.000$

$R_i = 2\ M\Omega$

$R_o = 75\ \Omega$

Porquê um amplificador com estas características?





$$\beta = \frac{R_1}{R_1 + R_2}$$

$$A_f = \frac{A}{1+\beta A} = \frac{V_o}{V_s}$$

$$A \to \infty \qquad e_i \to 0$$

Curto circuito virtual

$$\beta A >> 1 \to A_f \approx \frac{1}{\beta}$$

Amplificador inversor

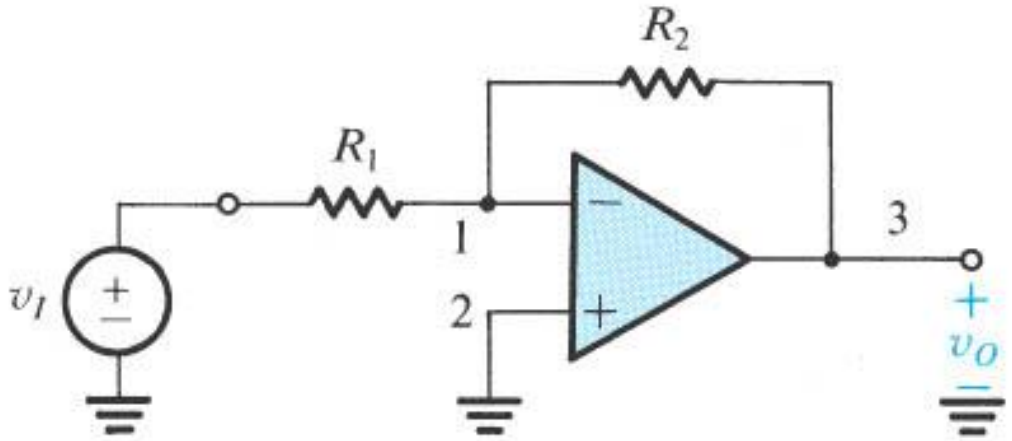


Figure 2.5 The inverting closed-loop configuration.

Análise do Amplificador inversor

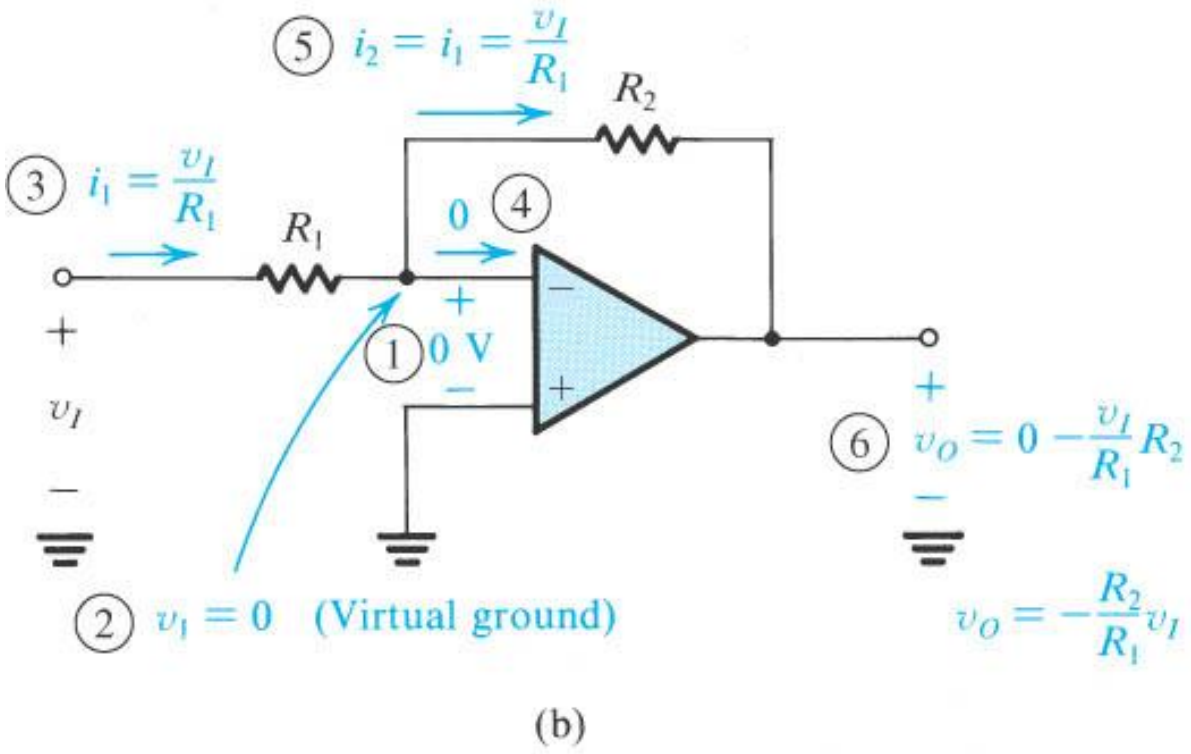


Figure 2.6 Analysis of the inverting configuration. The circled numbers indicate the order of the analysis steps.

Exemplo 2.2

Determine o ganho v_O/v_I.

Projete o circuito para ganho igual a 100 e resistência de entrada igual a1MΩ.

$$\frac{v_o}{v_i} = -\frac{R_2}{R_1}\left(1+\frac{R_4}{R_2}+\frac{R_4}{R_3}\right)$$

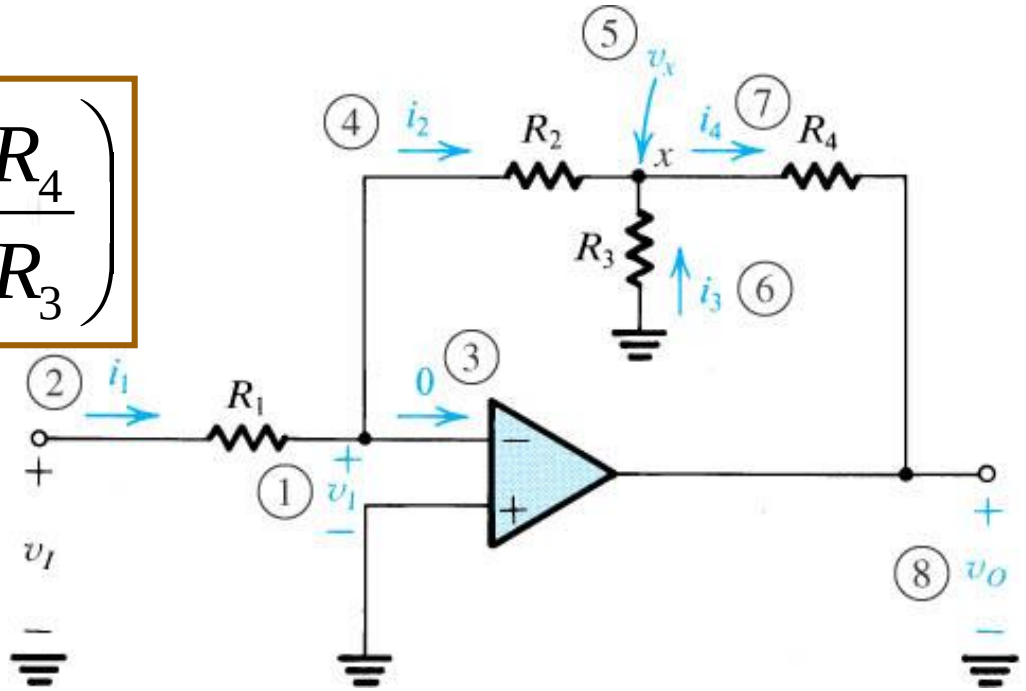


Figure 2.8 Circuit for Example 2.2. The circled numbers indicate the sequence of the steps in the analysis.

Exemplo 2.6

Determine o ganho v_o/v_i. Determine o ganho de corrente i_L/i_i.

Determine o ganho de potência P_o/P_i.

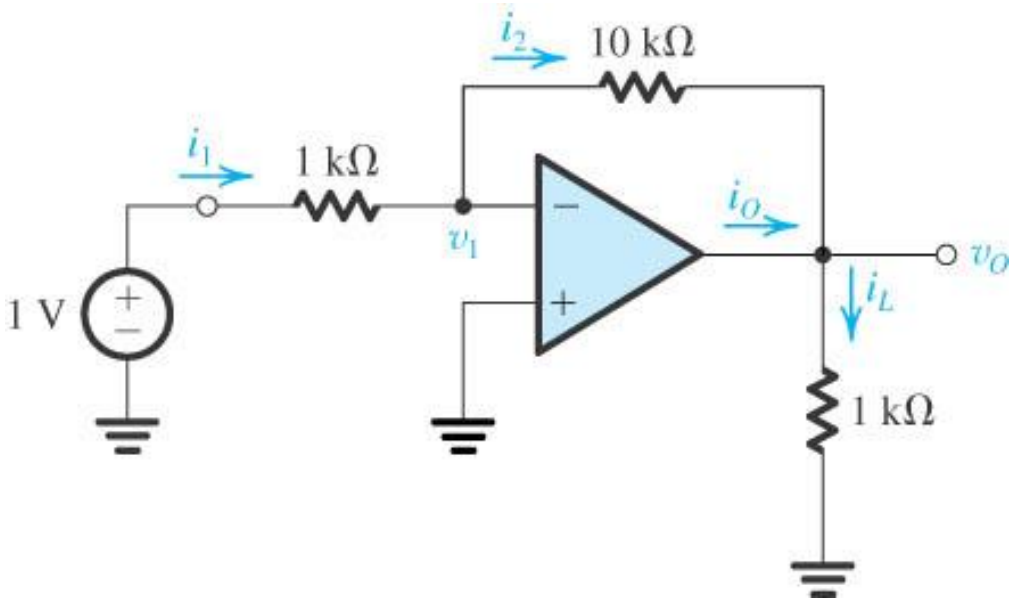
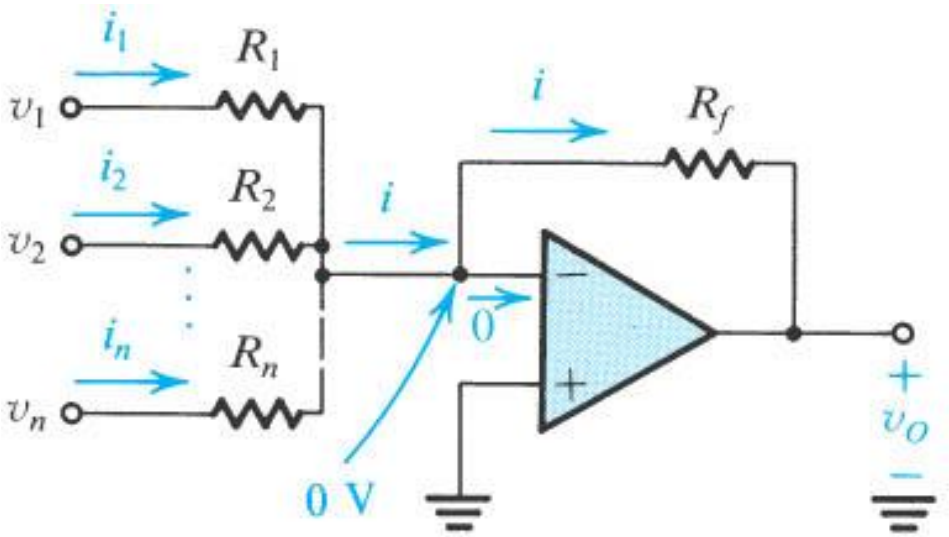


Figure E2.6

O circuito somador



$$v_O = -\left(\frac{R_f}{R_1}v_1 + \frac{R_f}{R_2}v_2 + \cdots + \frac{R_f}{R_n}v_n\right)$$

Figure 2.10 A weighted summer.

Outro somador

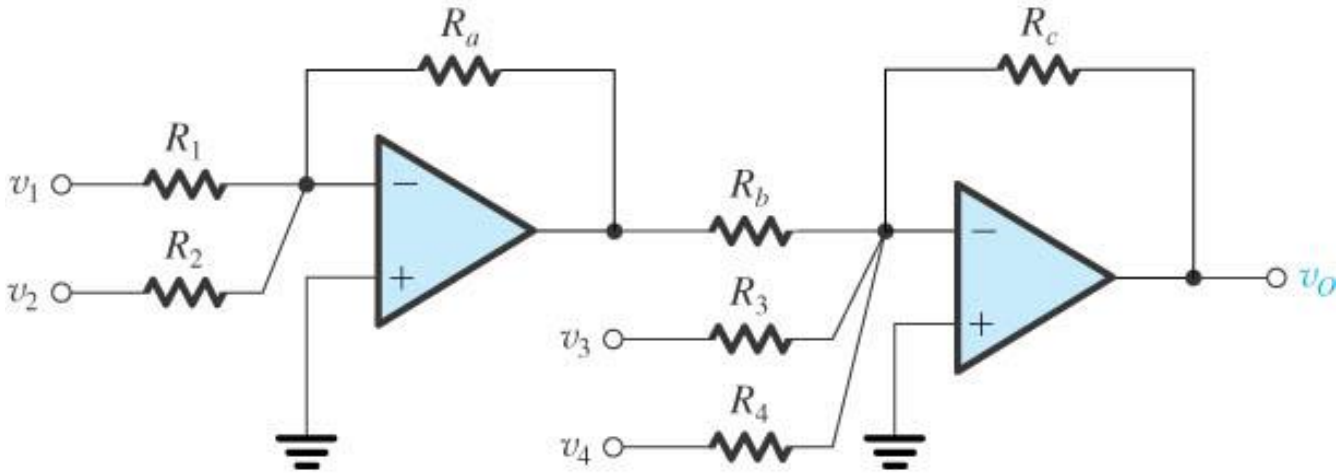


Figure 2.11 A weighted summer capable of implementing summing coefficients of both signs.

O amplificador não inversor

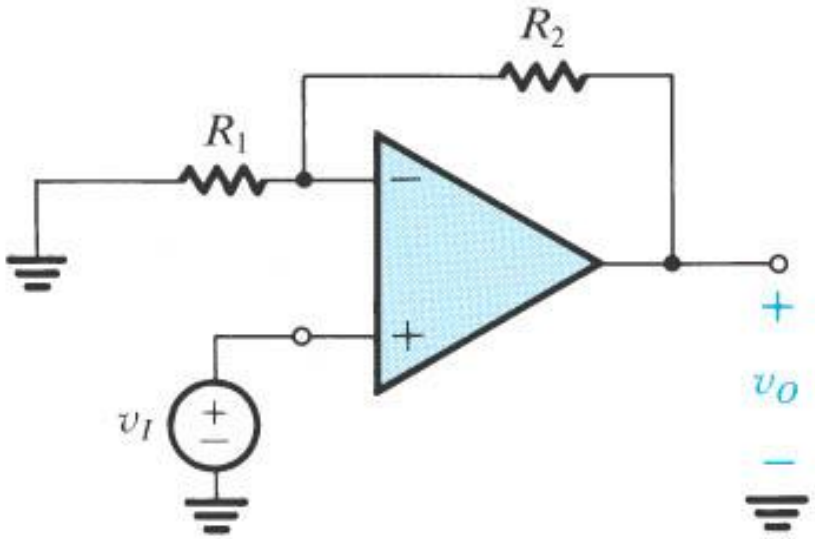
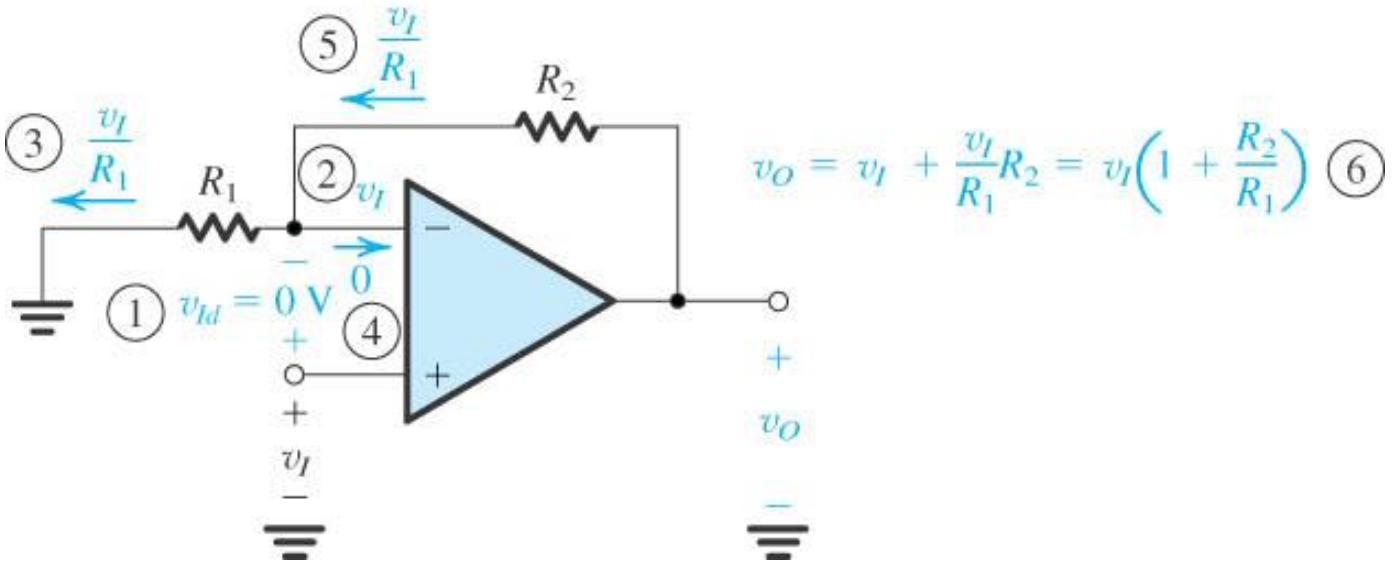


Figure 2.12 The noninverting configuration.

Análise do Amplificador não inversor



Determine o ganho deste amplificador considerando o ganho A finito.

Figure 2.13 Analysis of the noninverting circuit. The sequence of the steps in the analysis is indicated by the circled numbers.

O seguidor de tensão

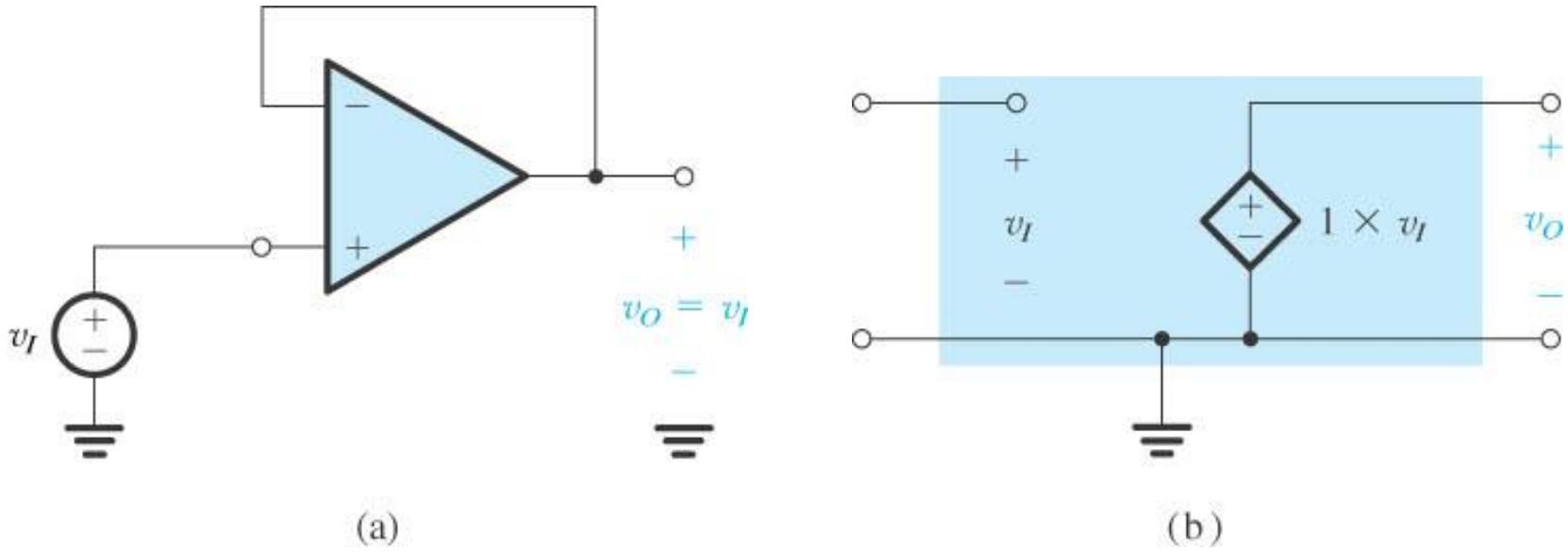


Figure 2.14 **(a)** The unity-gain buffer or follower amplifier. **(b)** Its equivalent circuit model.

Exercício 2.9

Use o teorema da superposição para determinar v_o.

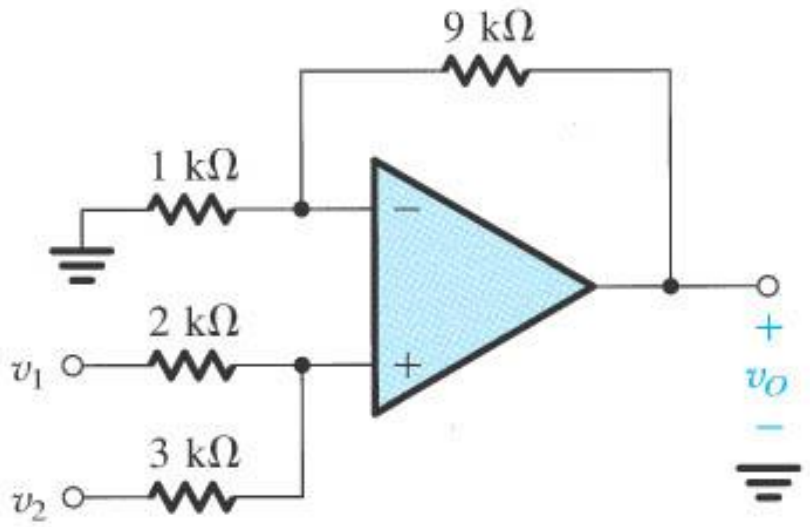


Figure E2.9

Exercício 2.13

1. Determine as correntes e tensões indicadas no circuito.

2. Determine os ganhos de tensão, corrente e potência.

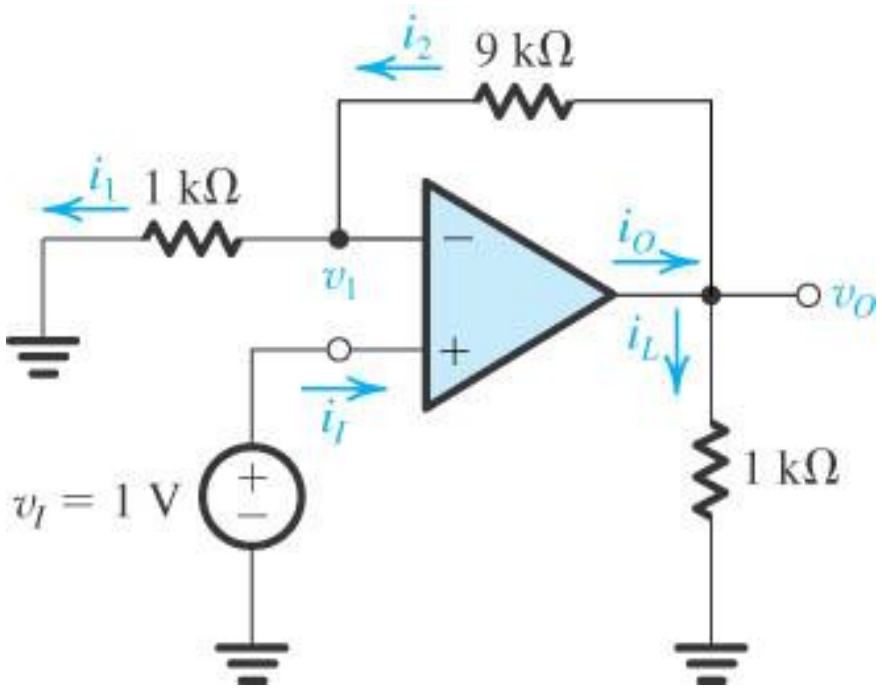
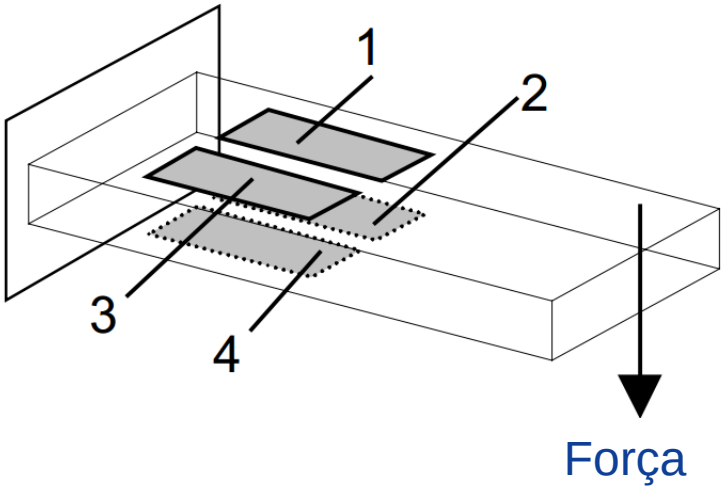
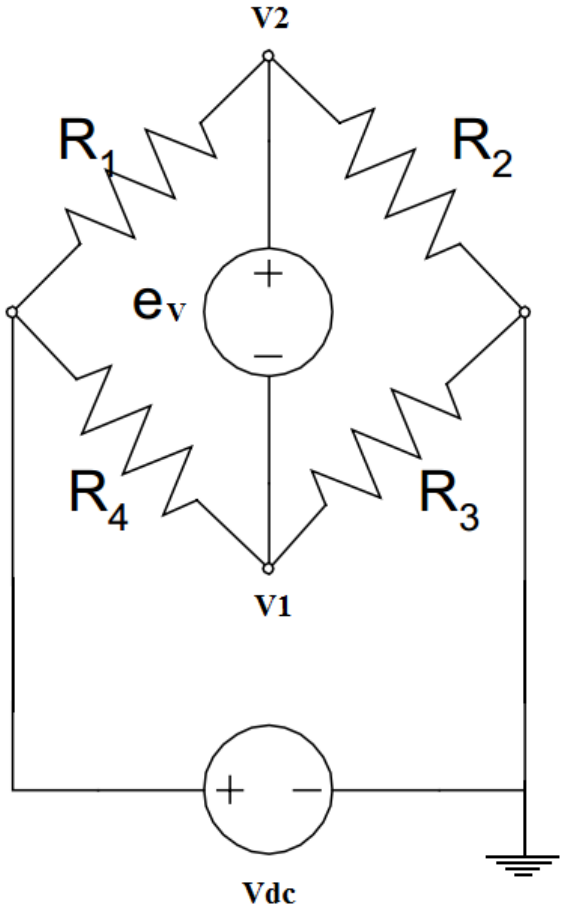


Figure E2.13

Ponte com Strain Gage

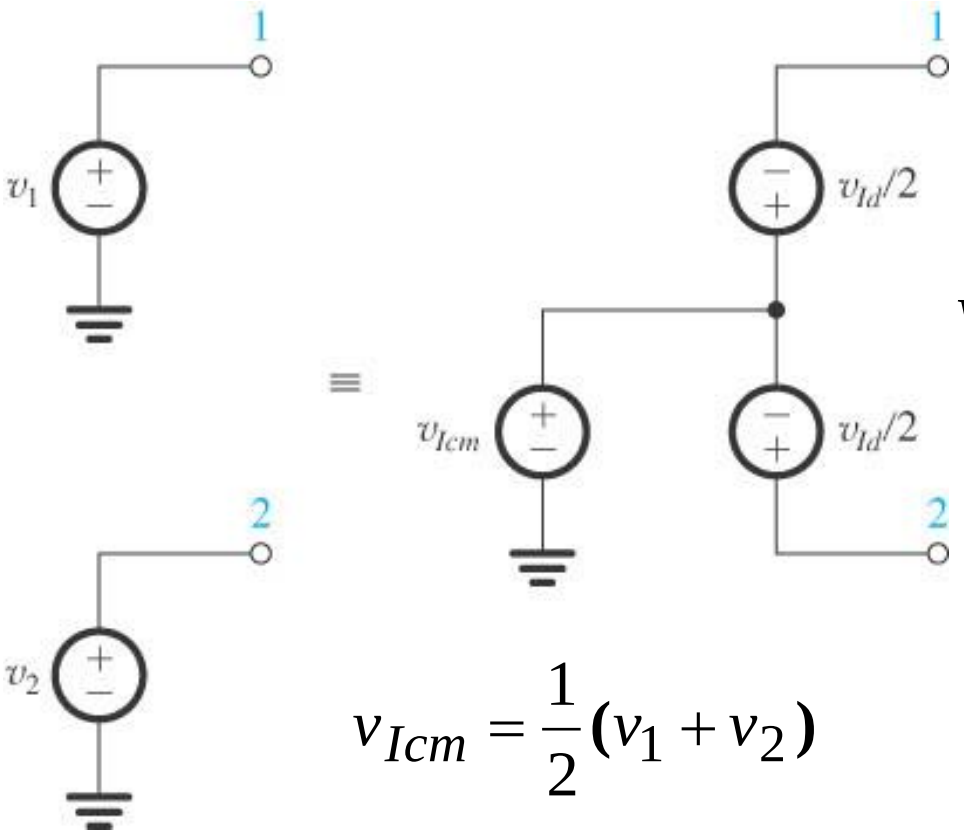




Sinais de modo diferencial e de modo comum

$$v_1 = v_{Icm} - \frac{v_{Id}}{2}$$

$$v_2 = v_{Icm} + \frac{v_{Id}}{2}$$

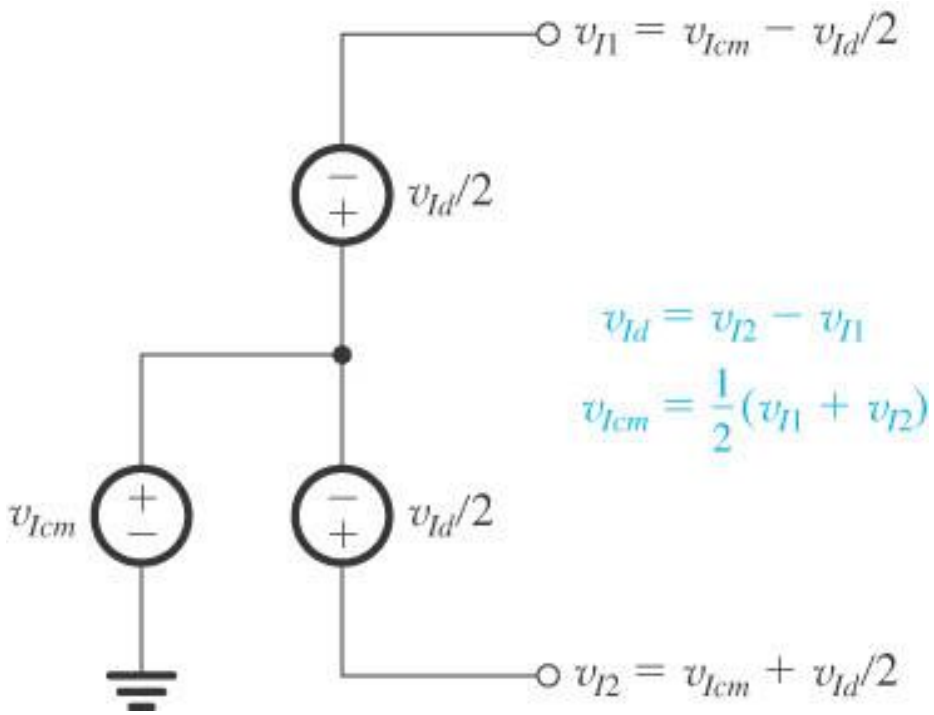


$$v_{Id} = v_2 - v_1$$

$$v_{Icm} = \frac{1}{2}(v_1 + v_2)$$

Figure 2.4 Representation of the signal sources v_1 and v_2 in terms of their differential and common-mode components.

Amplificadores de Diferenças



$$v_o = A_d v_{Id} + A_{cm} v_{Icm}$$

CMRR – Common-mode Rejection Ratio

$$CMRR = 20 \log \frac{|A_d|}{|A_{cm}|}$$

Figure 2.15 Representing the input signals to a differential amplifier in terms of their differential and common-mode components.

Amplificador de diferenças

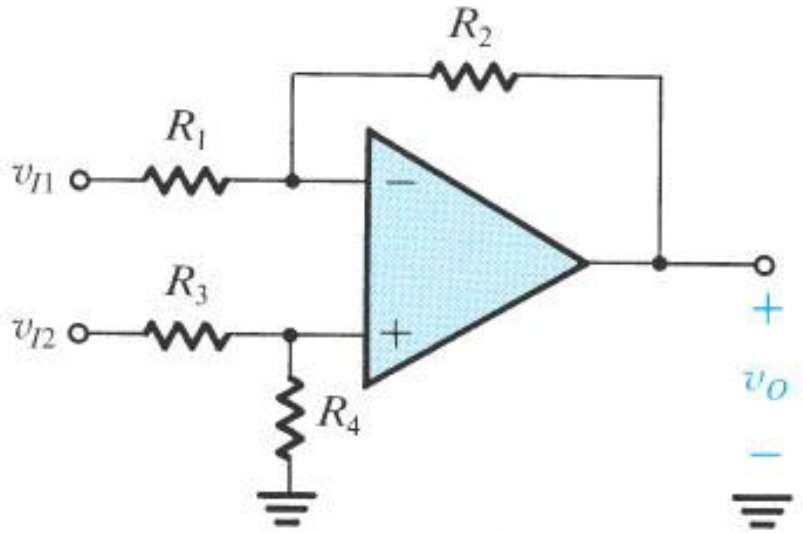
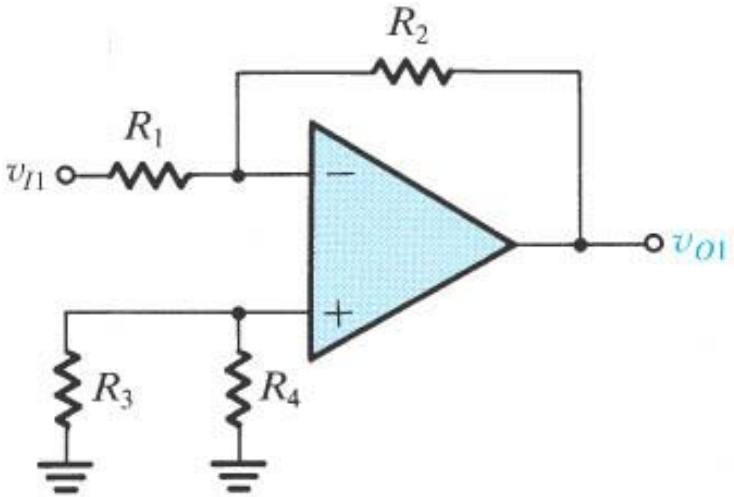


Figure 2.16 A difference amplifier.

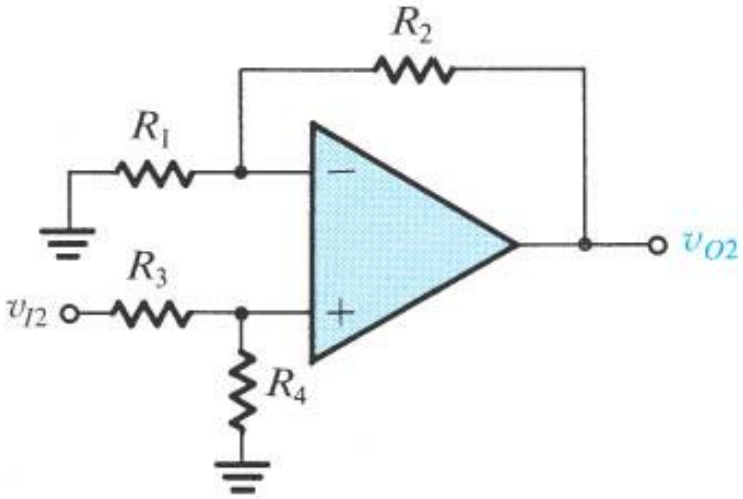
Teorema da Superposição



(a)

$$v_{o1} = -\frac{R_2}{R_1} v_{I1}$$

$$v_{o2} = \frac{R_4}{R_3 + R_4}\left(\frac{R_1 + R_2}{R_1}\right) v_{I2}$$

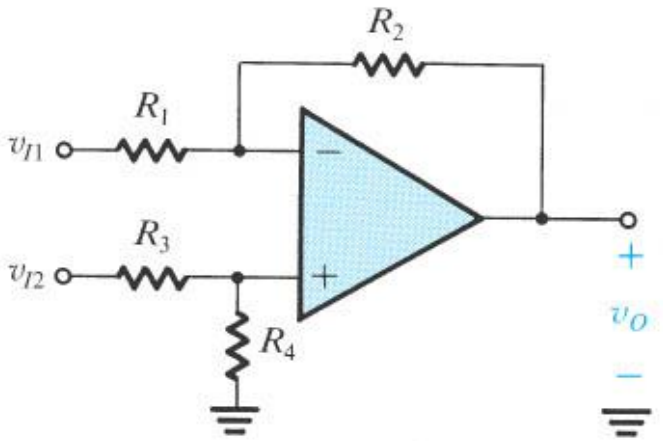


(b)

$$v_o = \frac{R_4}{R_3 + R_4}\left(\frac{R_1 + R_2}{R_1}\right) v_{I2} - \frac{R_2}{R_1} v_{I1}$$

Figure 2.17 Application of superposition to the analysis of the circuit of Fig. 2.16.

Amplificador de diferenças



$$v_o = \frac{R_4}{R_3 + R_4}\left(\frac{R_1 + R_2}{R_1}\right)v_{I2} - \frac{R_2}{R_1}v_{I1}$$

Se: $\dfrac{R_4}{R_3} = \dfrac{R_2}{R_1}$

$$v_o = \frac{R_2}{R_1}(v_{I2} - v_{I1})$$

Figure 2.16 A difference amplifier.

Amplificador de instrumentação

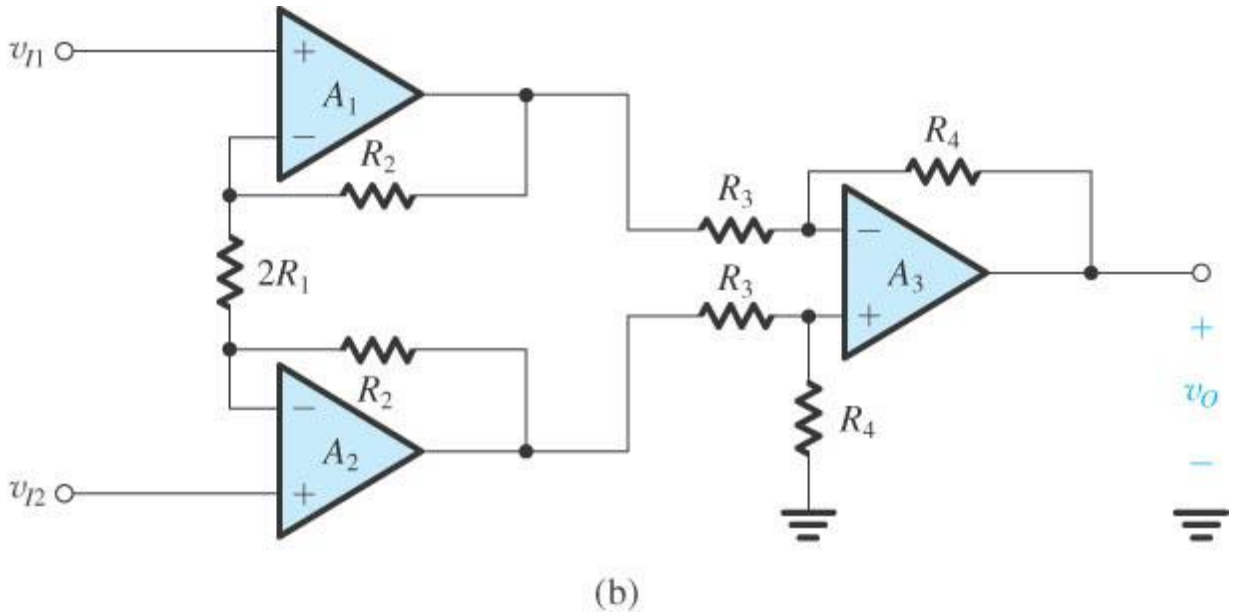
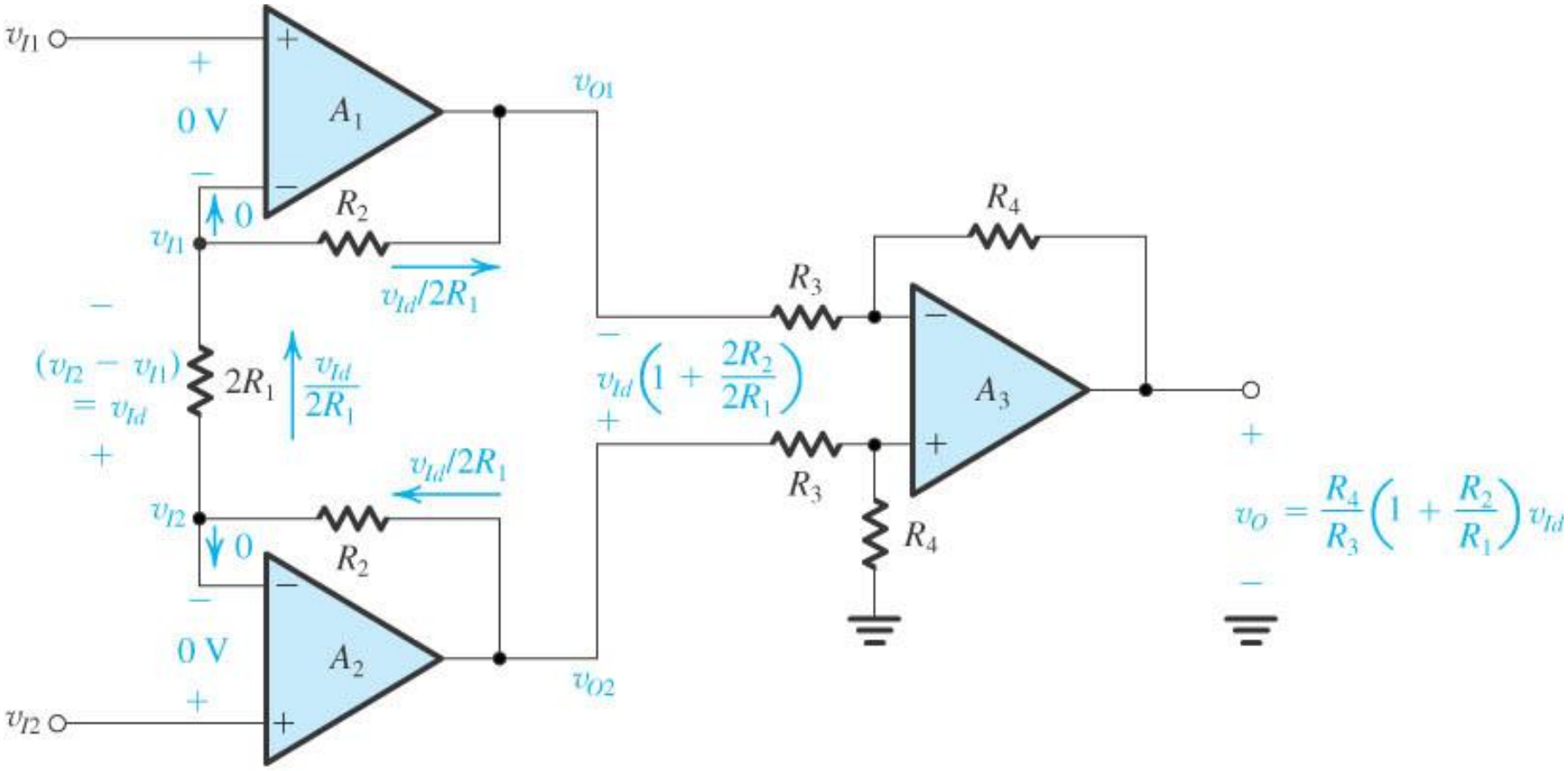


Figure 2.20 A popular circuit for an instrumentation amplifier: **(a)** Initial approach to the circuit; **(b)** The circuit in (**a**) with the connection between node X and ground removed and the two resistors R_1 and R_1 lumped together. This simple wiring change dramatically improves performance; **(c)** Analysis of the circuit in‘ **(b)** assuming ideal op amps.

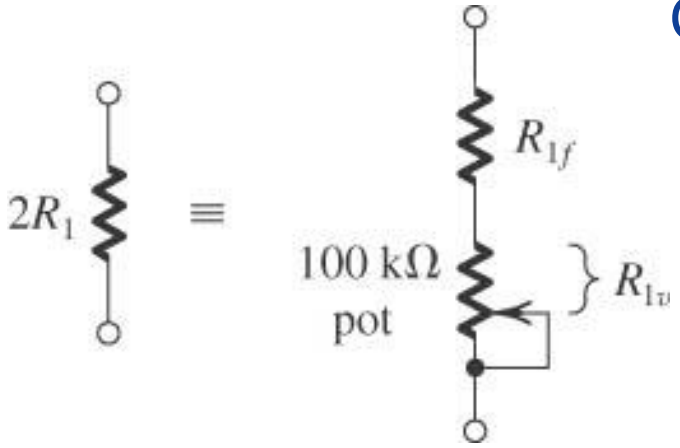
Amplificador de Instrumentação



(c)

Amplificador de Instrumentação

Projete o amplificador de instrumentação para que o ganho possa ser variado entre 2 e 1000 utilizando um potênciometro de 100 KΩ.



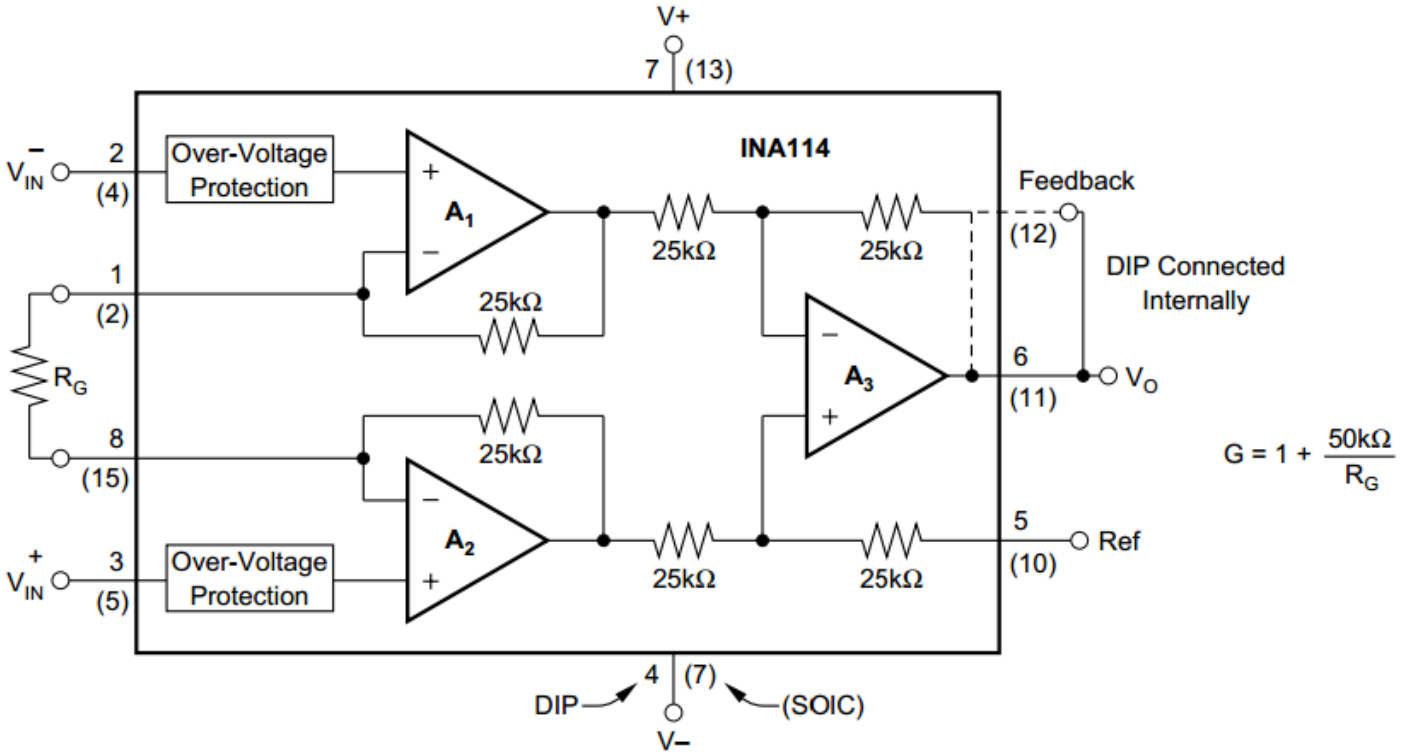
Ganho do primeiro estágio:

$$v_{o2} - v_{o1} = \left(1 + \frac{2R_2}{2R_1}\right) v_{id}$$

Figure 2.21 To make the gain of the circuit in Fig. 2.20(b) variable, $2R_1$ is implemented as the series combination of a fixed resistor R_{1f} and a variable resistor R_{1v}. Resistor R_{1f} ensures that the maximum available gain is limited.

Amplificador de Instrumentação – INA114

BURR - BROWN®



http://www.ti.com/lit/ds/sbos014/sbos014.pdf

Largura de faixa

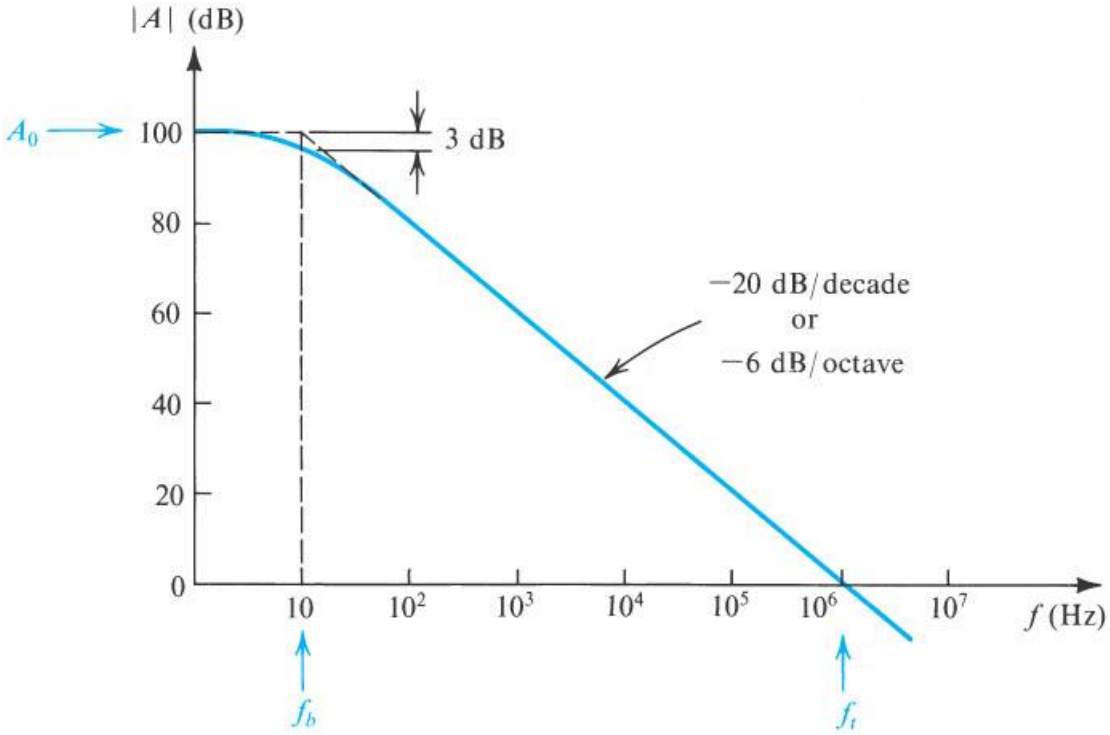
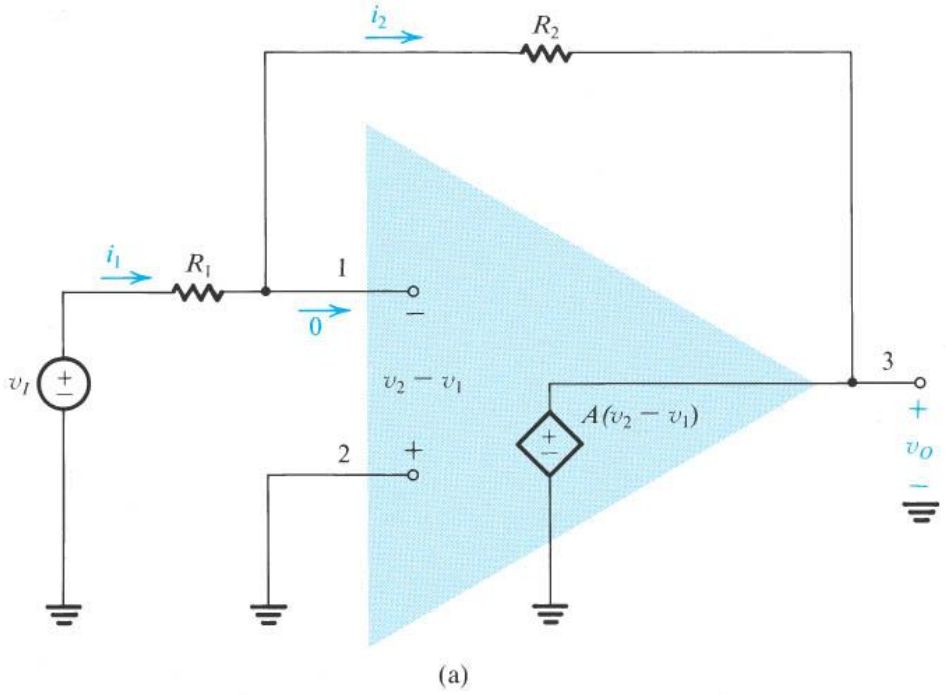


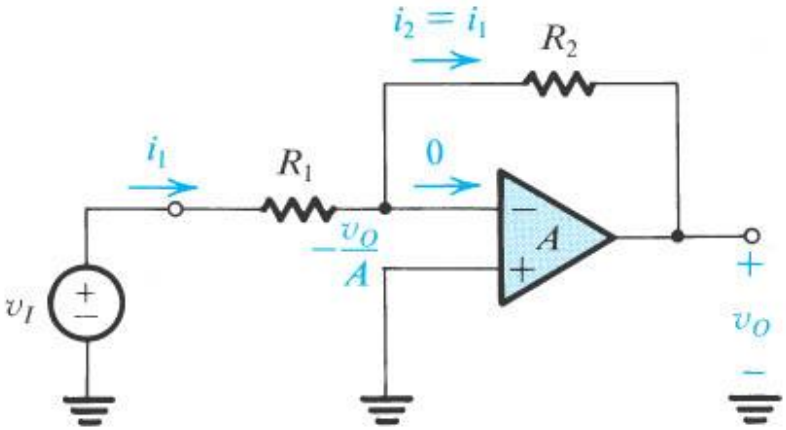
Figure 2.22 Open-loop gain of a typical general-purpose internally compensated op amp.

Considerando o ganho A finito



$$\frac{v_o}{v_i} = \frac{-R_2/R_1}{1+(1+R_2/R_1)/A}$$

$$(1+R_2/R_1) << A$$



Saturação da tensão de saída

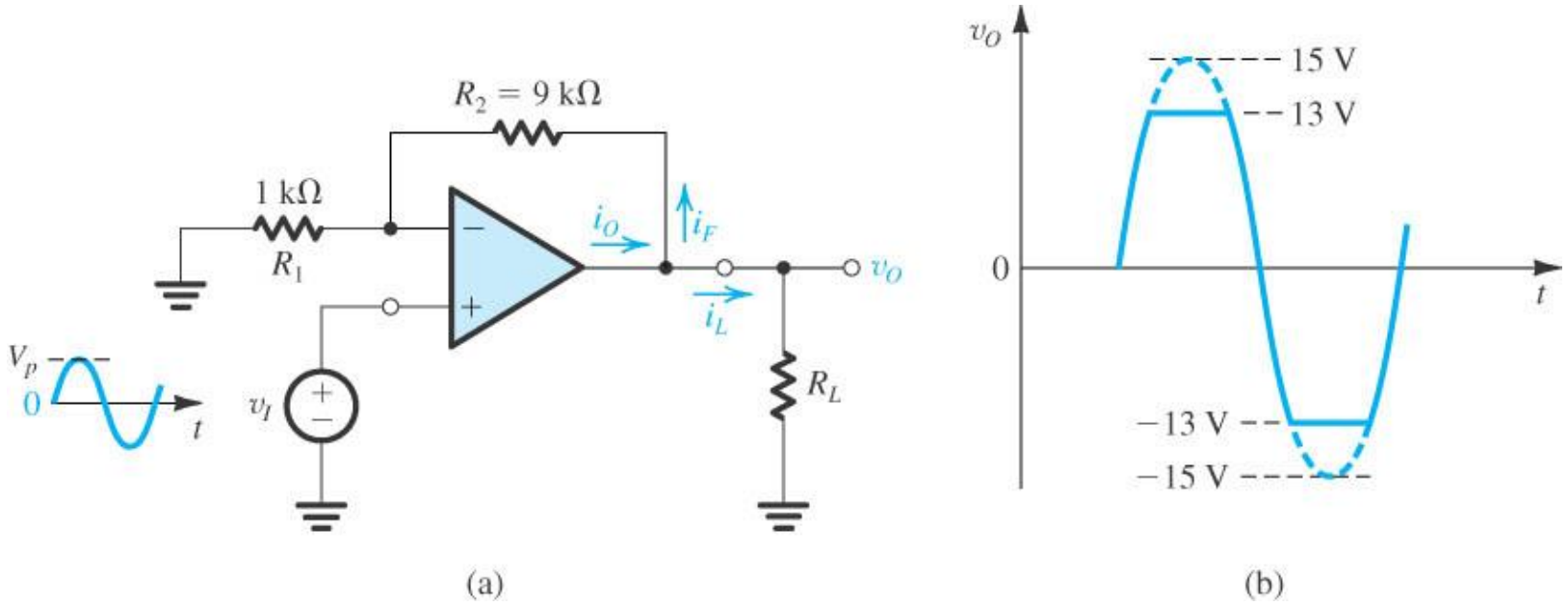
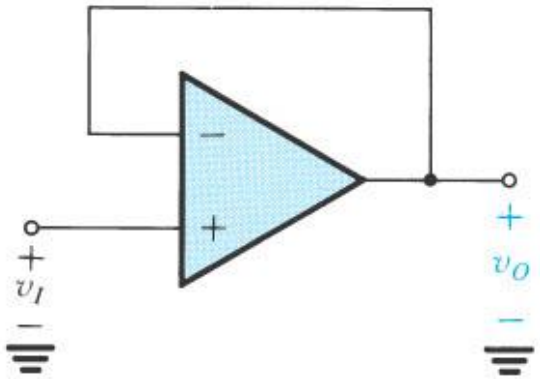


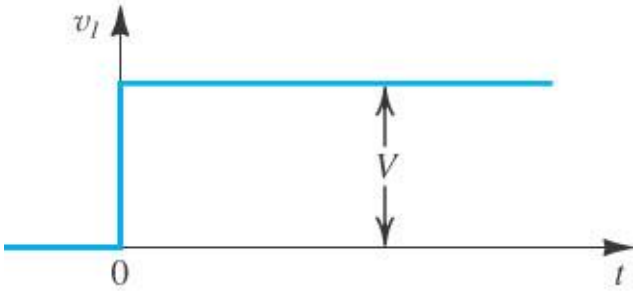
Figure 2.25 **(a)** A noninverting amplifier with a nominal gain of 10 V/V designed using an op amp that saturates at ±13-V output voltage and has ±20-mA output current limits. **(b)** When the input sine wave has a peak of 1.5 V, the output is clipped off at ±13 V.

Slew rate

É a máxima taxa de variação da tensão de saída de um A.O.

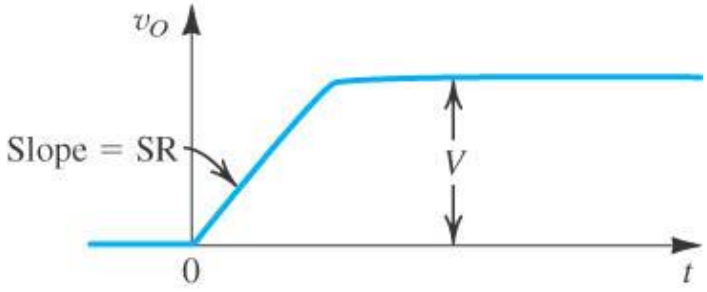


(a)

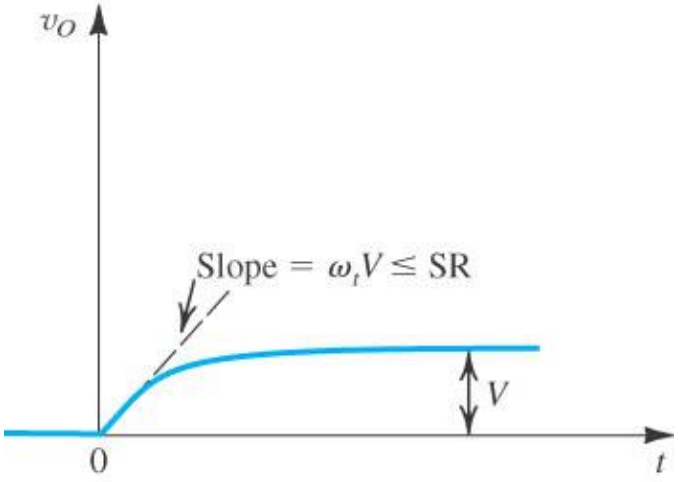


(b)

$$SR = \left.\frac{dv_o}{dt}\right|_{máx}$$



(c)



(d)

Full Power Bandwith

É a máxima frequência de uma senoide com amplitude máxima que pode ser amplificada sem distorção por um A.O. utilizado como buffer.

$$v_I = \hat{V}_i \sin wt$$

$$\frac{dv_I}{dt} = w\hat{V}_i \cos wt$$

$$w_M V_{o\,\max} = SR$$

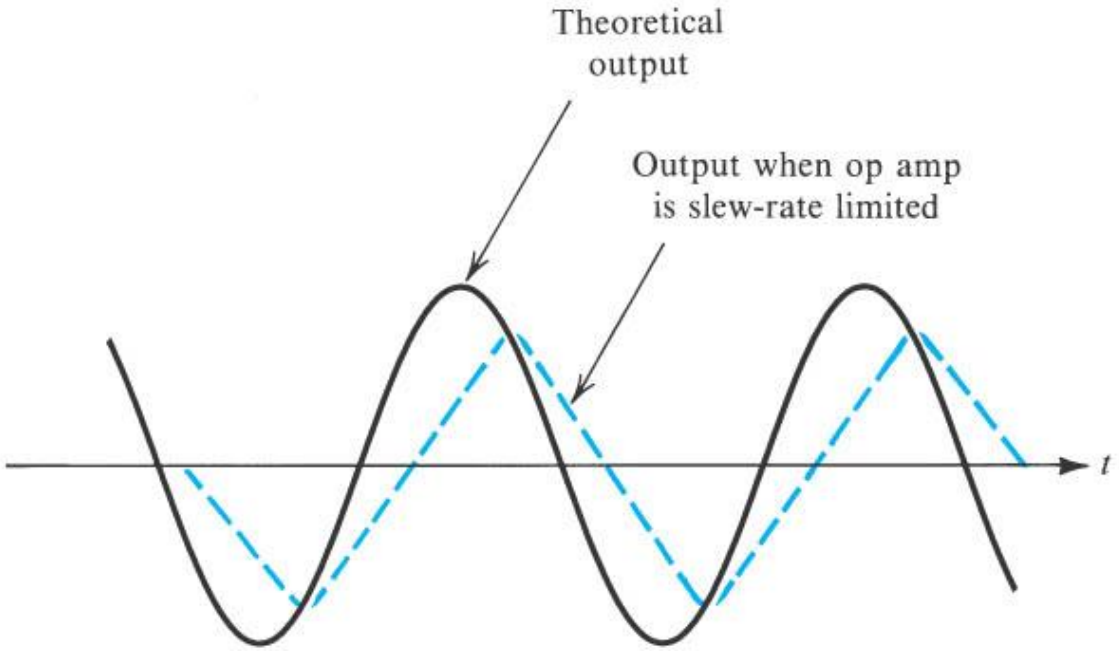


Figure 2.27 Effect of slew-rate limiting on output sinusoidal waveforms.

Imperfeições C.C. dos A.O's

1 – Tensão de Offset de entrada

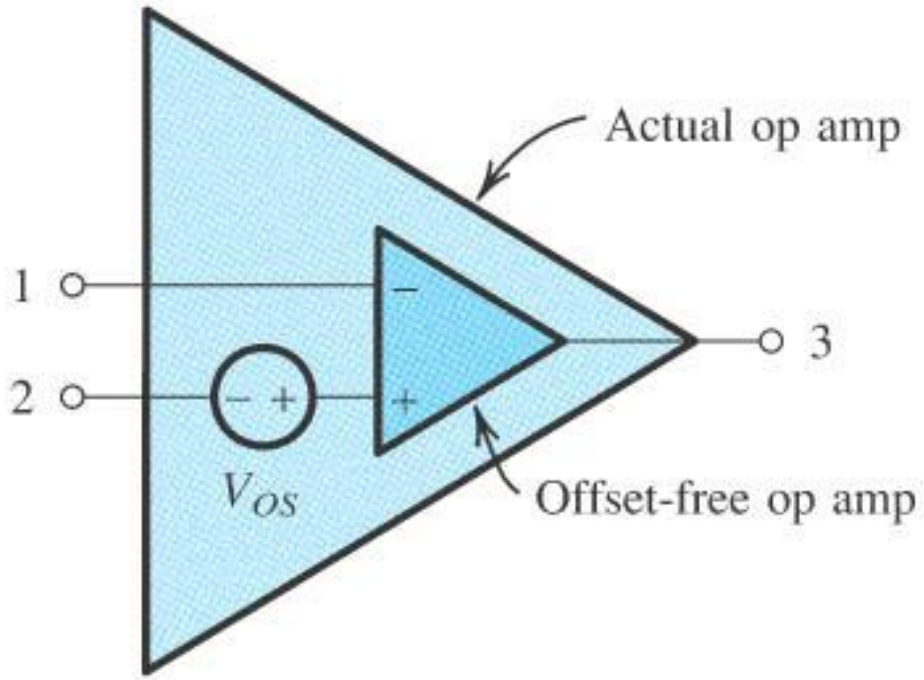


Figure 2.28 Circuit model for an op amp with input offset voltage V_{OS}.

Erro devido à tensão de offset de entrada

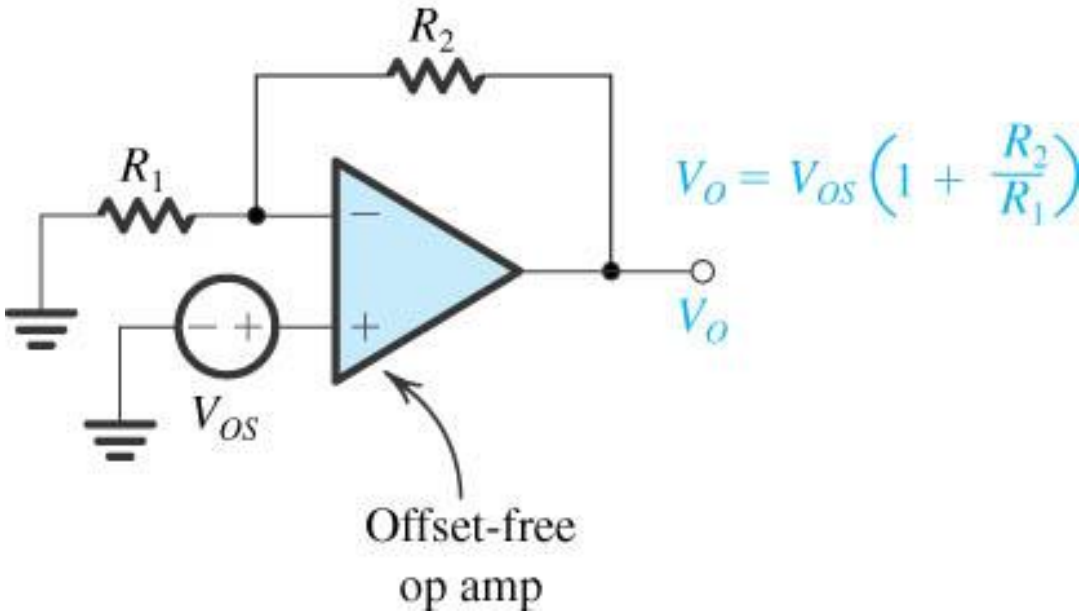


Figure 2.29 Evaluating the output dc offset voltage due to V_{OS} in a closed-loop amplifier.

Ajuste da tensão de Offset de entrada

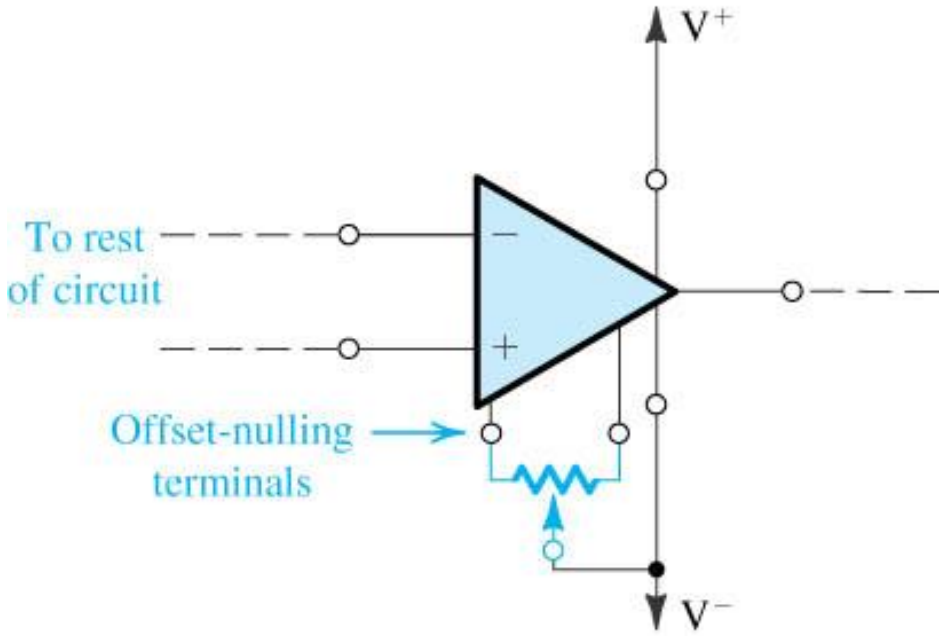


Figure 2.30 The output dc offset voltage of an op amp can be trimmed to zero by connecting a potentiometer to the two offset-nulling terminals. The wiper of the potentiometer is connected to the negative supply of the op amp.

Amplificador com acoplamento capacitivo

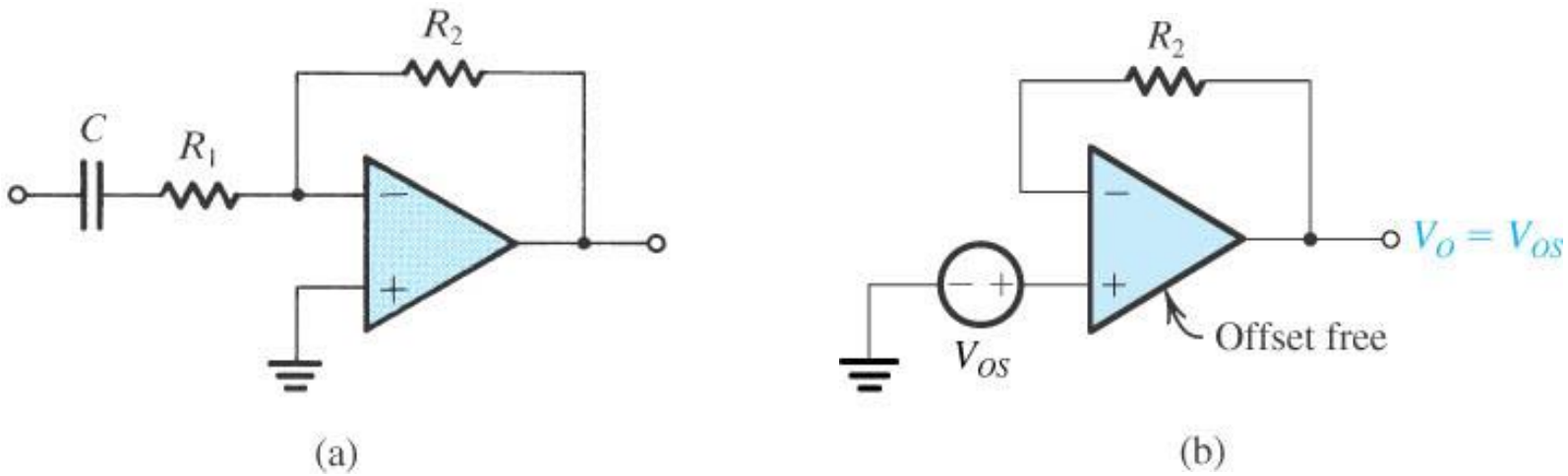
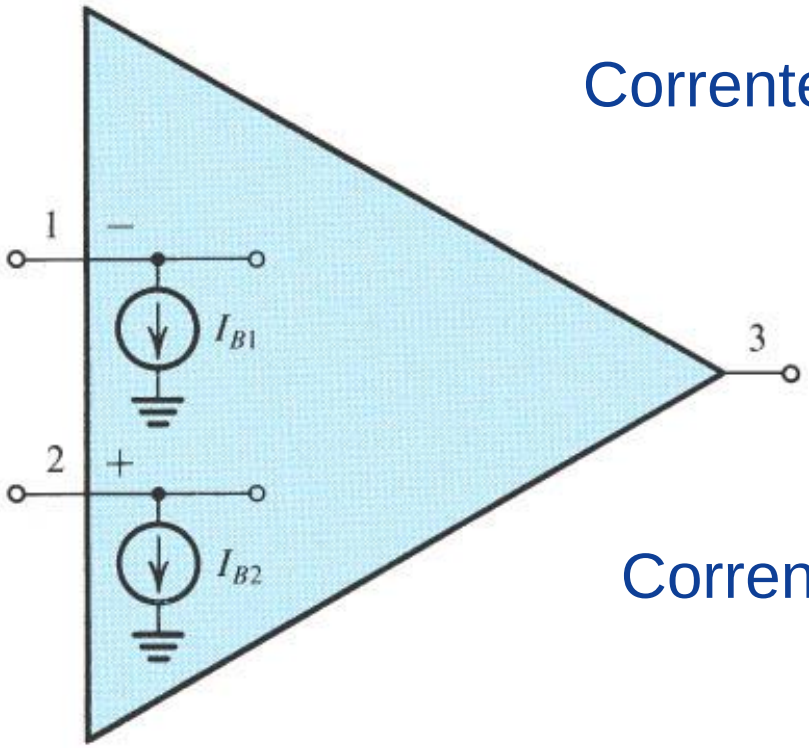


Figure 2.31 **(a)** A capacitively coupled inverting amplifier, and **(b)** the equivalent circuit for determining its dc output offset voltage V_O.

Corrente de polarização e corrente de offset



Corrente de polarização de entrada:

$$I_B = \frac{I_{B1} + I_{B2}}{2}$$

Corrente de offset de entrada:

$$I_{OS} = | I_{B1} - I_{B2} |$$

Figure 2.32 The op-amp input bias currents represented by two current sources I_{B1} and I_{B2}.

Erro devido à corrente de polarização

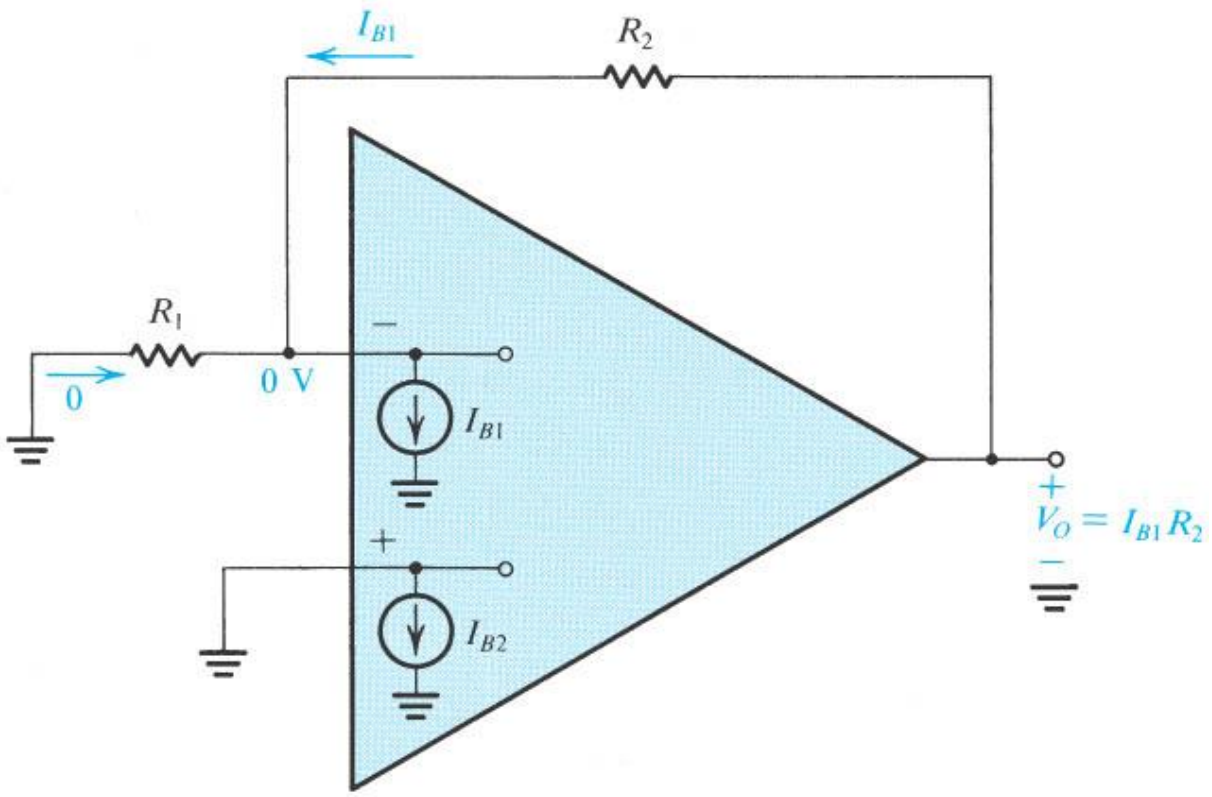
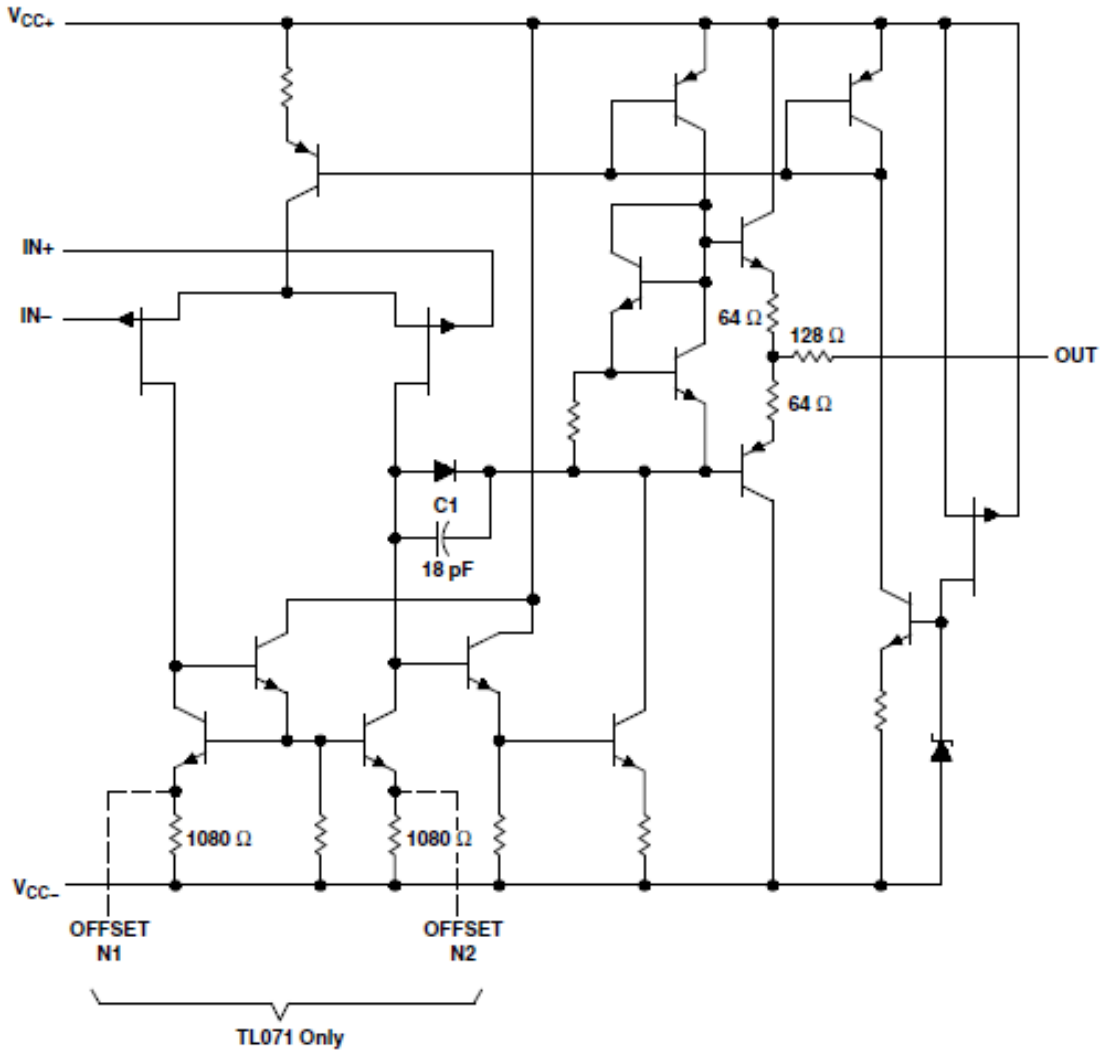


Figure 2.33 Analysis of the closed-loop amplifier, taking into account the input bias currents.

Características elétricas de Amp. Op



TL071, TL071A, TL071B, TL072
TL072A, TL072B, TL074, TL074A, TL074B
LOW-NOISE JFET-INPUT OPERATIONAL AMPLIFIERS

SLOS080J – SEPTEMBER 1979 – REVISED MARCH 2005

electrical characteristics, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

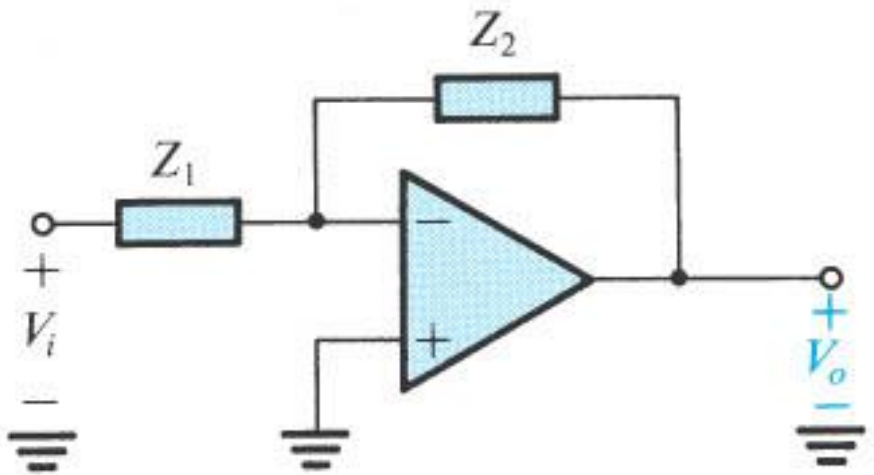
PARAMETER		TEST CONDITIONS†	T_A‡	TL071M TL072M			TL074M			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω	25°C		3	6		3	9	mV
			Full range			9			15	
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 0, R_S = 50 Ω	Full range		18			18		µV/°C
I_{IO}	Input offset current	V_O = 0	25°C		5	100		5	100	pA
			Full range			20			20	nA
I_{IB}	Input bias current‡	V_O = 0	25°C		65	200		65	200	pA
						50			50	nA
V_{ICR}	Common-mode input voltage range		25°C	±11	−12 to 15		±11	−12 to 15		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ	25°C	±12	±13.5		±12	±13.5		V
		R_L ≥ 10 kΩ	Full range	±12			±12			
		R_L ≥ 2 kΩ		±10			±10			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L ≥ 2 kΩ	25°C	35	200		35	200		V/mV
				15			15			
B_1	Unity-gain bandwidth	T_A = 25°C			3			3		MHz
r_i	Input resistance	T_A = 25°C			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω	25°C	80	86		80	86		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = ±9 V to ±15 V, V_O = 0, R_S = 50 Ω	25°C	80	86		80	86		dB
I_{CC}	Supply current (each amplifier)	V_O = 0, No load	25°C		1.4	2.5		1.4	2.5	mA
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 100	25°C		120			120		dB

† Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in Figure 4. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

‡ All characteristics are measured under open-loop conditions with zero common-mode voltage, unless otherwise specified. Full range is T_A = −55°C to 125°C.

PARAMETER		TEST CONDITIONS		TL07xM			ALL OTHERS			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_I = 10 V, C_L = 100 pF,	R_L = 2 kΩ, See Figure 1	5	13		8	13		V/μs

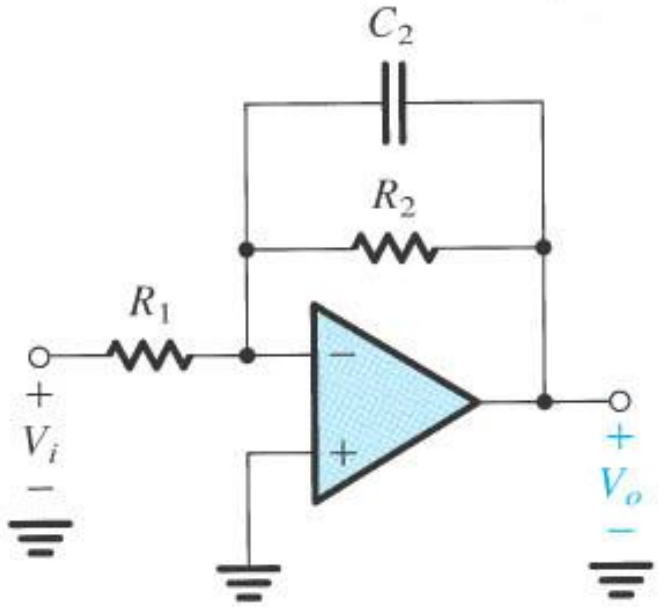
O amplificador inversor com impedâncias



$$\frac{V_o}{V_i} = -\frac{Z_2}{Z_1}$$

Figure 2.37 The inverting configuration with general impedances in the feedback and the feed-in paths.

Filtro passa baixas



$$V_0(s) = \frac{-R_2/R_1}{1+sC_2R_2}V_i(s)$$

$$V_0(jw) = \frac{-R_2/R_1}{1+jwC_2R_2}V_i(jw)$$

$$V_i(t) = V_i sen(wt)$$

$$w_0 = \frac{1}{C_2R_2}$$

Figure 2.38 Circuit for Example 2.6.

O integrado inversor

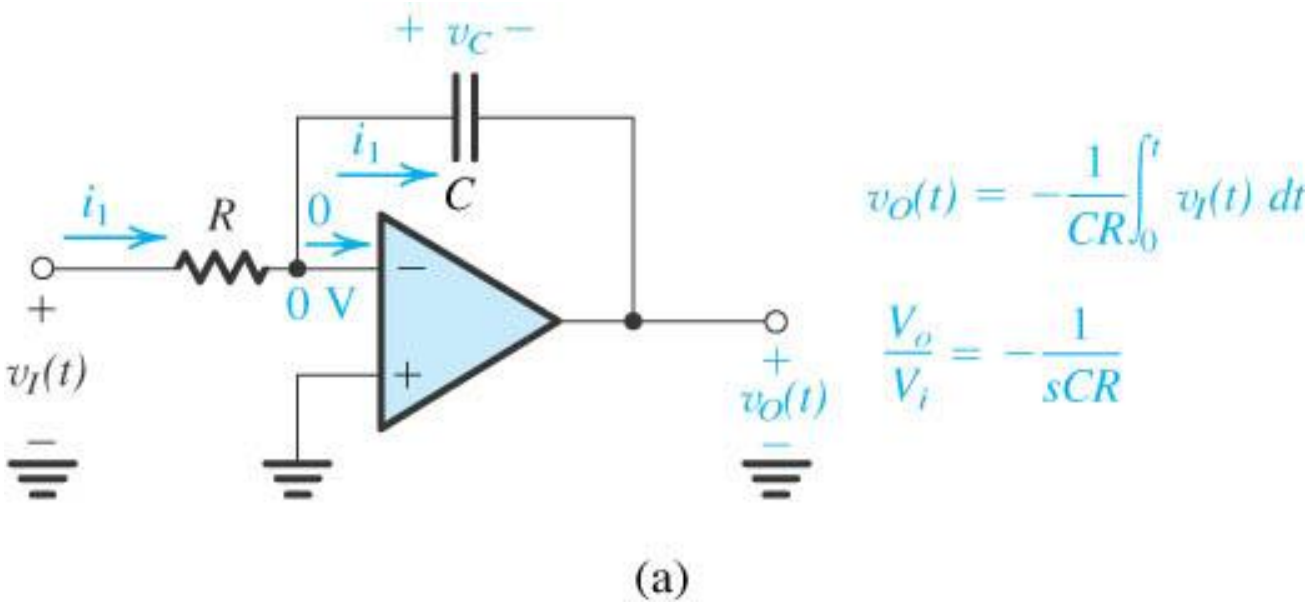


Figure 2.39 **(a)** The Miller or inverting integrator. **(b)** Frequency response of the integrator.

Circuito diferenciador

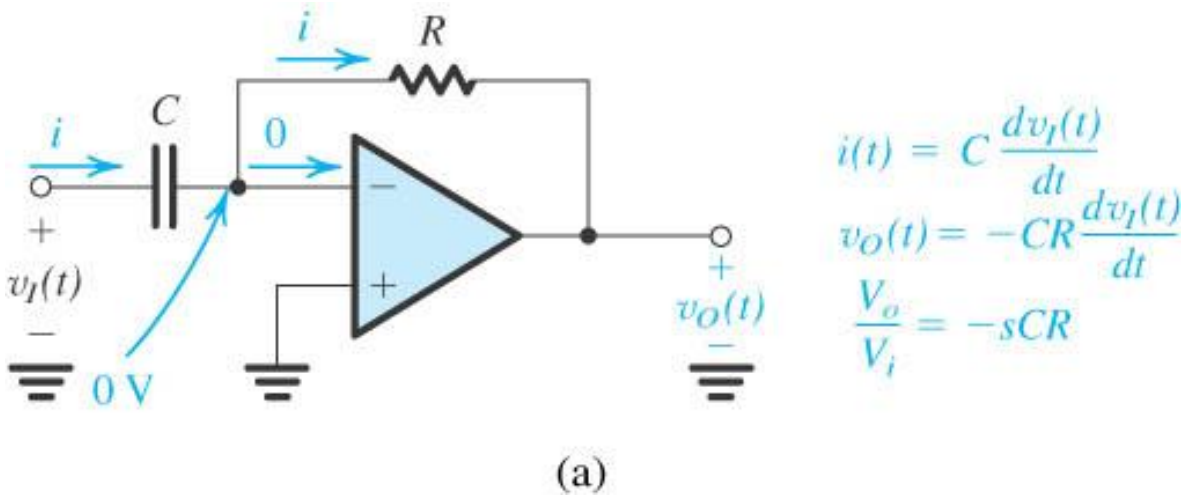
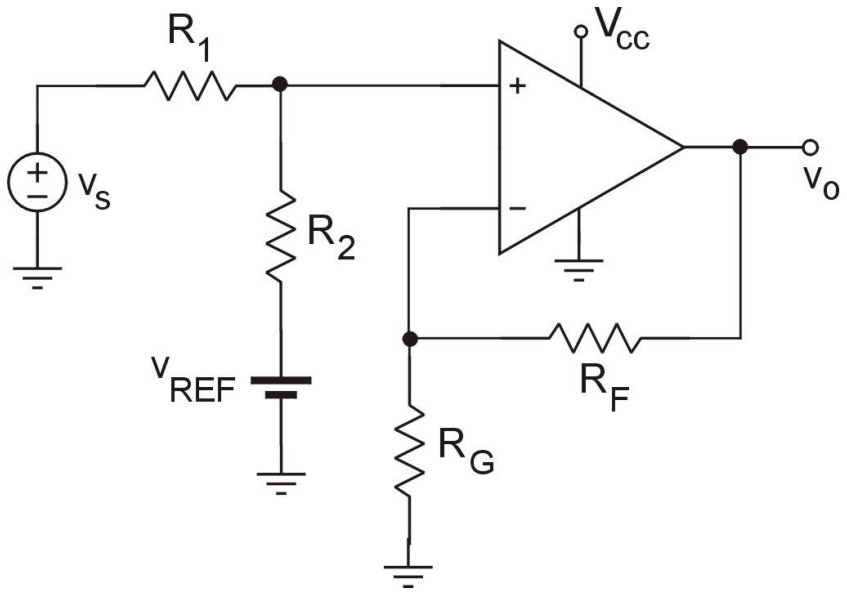


Figure 2.44 **(a)** A differentiator. **(b)** Frequency response of a differentiator with a time-constant *CR*.

Exemplo de circuitos

$$v_o = av_s + b$$

$$v_o = \frac{R_2}{R_1 + R_2}\left(1 + \frac{R_F}{R_G}\right)v_s + \frac{R_1}{R_1 + R_2}\left(1 + \frac{R_F}{R_G}\right)v_{REF}$$



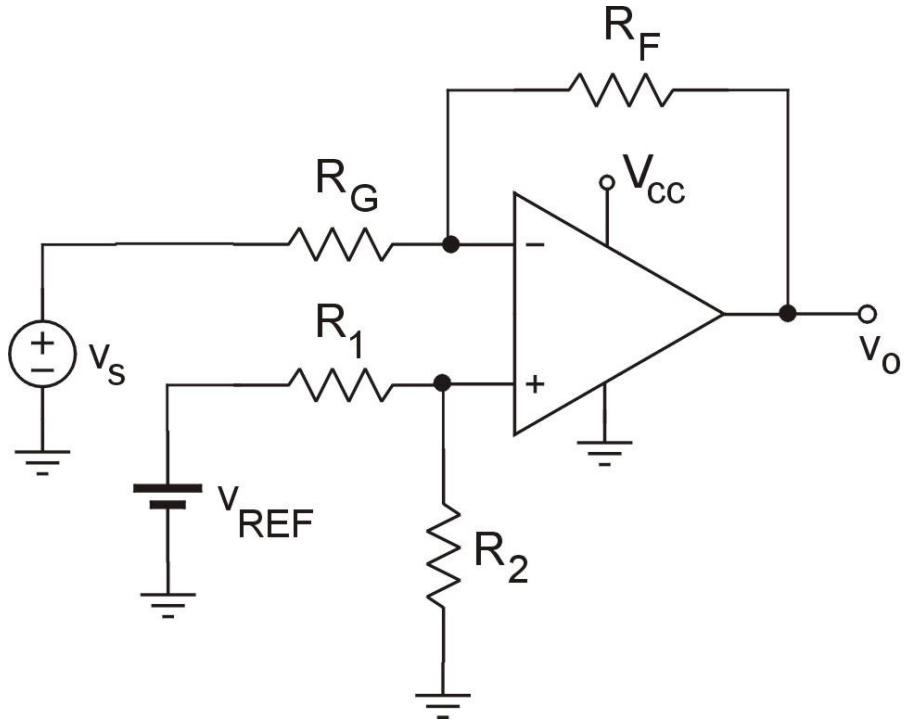
$$\begin{cases} a = \dfrac{R_2}{R_1 + R_2}\left(1 + \dfrac{R_F}{R_G}\right) \\ b = \dfrac{R_1}{R_1 + R_2}\left(1 + \dfrac{R_F}{R_G}\right)v_{REF} \end{cases}$$

Equação de projeto: $\dfrac{b}{a} = \dfrac{R_1}{R_2}v_{REF}$

Exemplo de circuitos

$$v_o = -av_s + b$$

$$v_o = -\frac{R_F}{R_G}v_s + \frac{R_2}{R_1 + R_2}\left(\frac{R_F + R_G}{R_G}\right)v_{REF}$$



$$\begin{cases} a = \dfrac{R_F}{R_G} \\ b = \dfrac{R_2}{R_1 + R_2}\left(\dfrac{R_F + R_G}{R_G}\right)v_{REF} \end{cases}$$

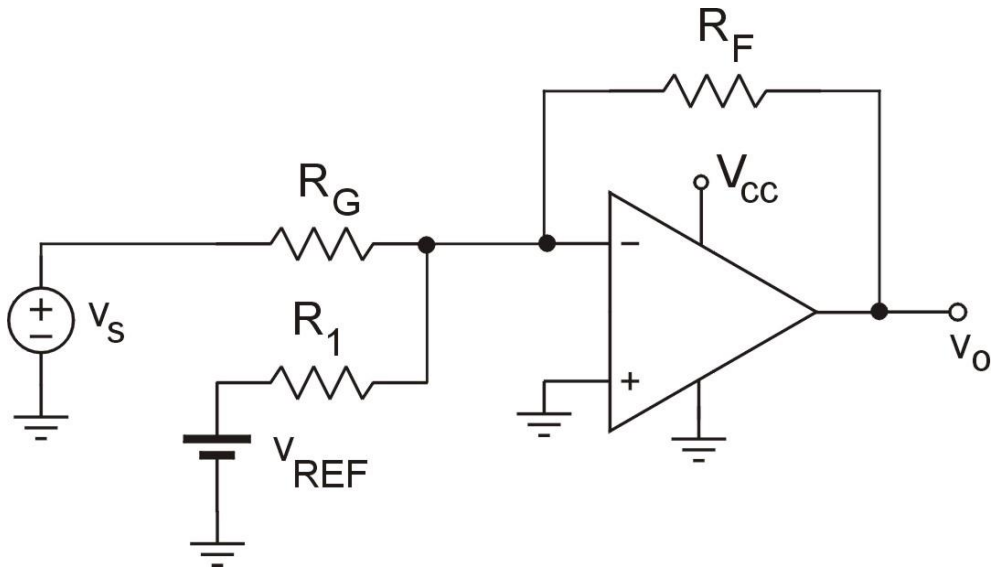
$$\frac{b}{(1-a)} = \frac{R_1}{R_1 + R_2}v_{REF}$$

Equação de projeto:

Exemplo de circuitos

$$v_o = -av_s - b$$

$$v_o = -\frac{R_F}{R_G}v_s - \frac{R_F}{R_1}v_{REF}$$



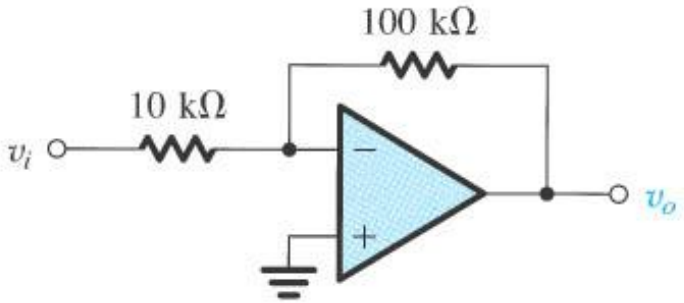
$$\begin{cases} a = \dfrac{R_F}{R_G} \\ b = -\dfrac{R_F}{R_1}v_{REF} \end{cases}$$

Equação de projeto:

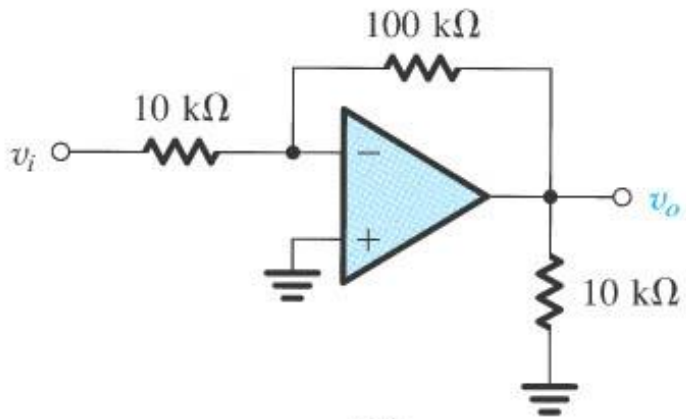
$$\frac{b}{a} = \frac{R_G}{R_1}v_{REF}$$

Problema 2.8

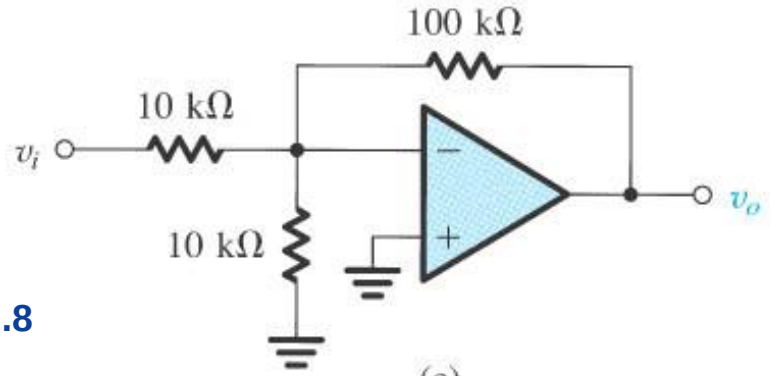
Determine o ganho v_o / v_i e a resistência de entrada R_{in} em cada circuito.



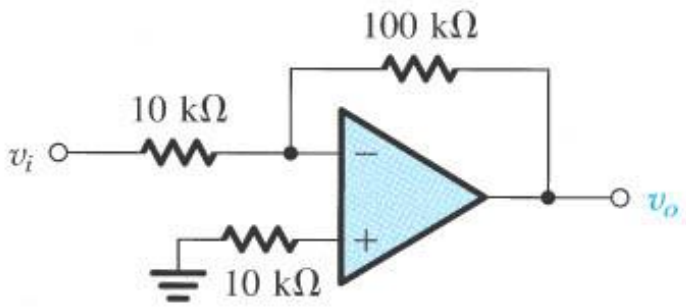
(a)



(b)



(c)



(d)

Figure P2.8

Problema 2.16

Encontre as correntes em todos em todos os ramos e as tensões em todos os nós do circuito. Como a corrente fornecida pelo A.O. é maior que a fornecida pela fonte de sinal, de onde vêm a corrente adicional?

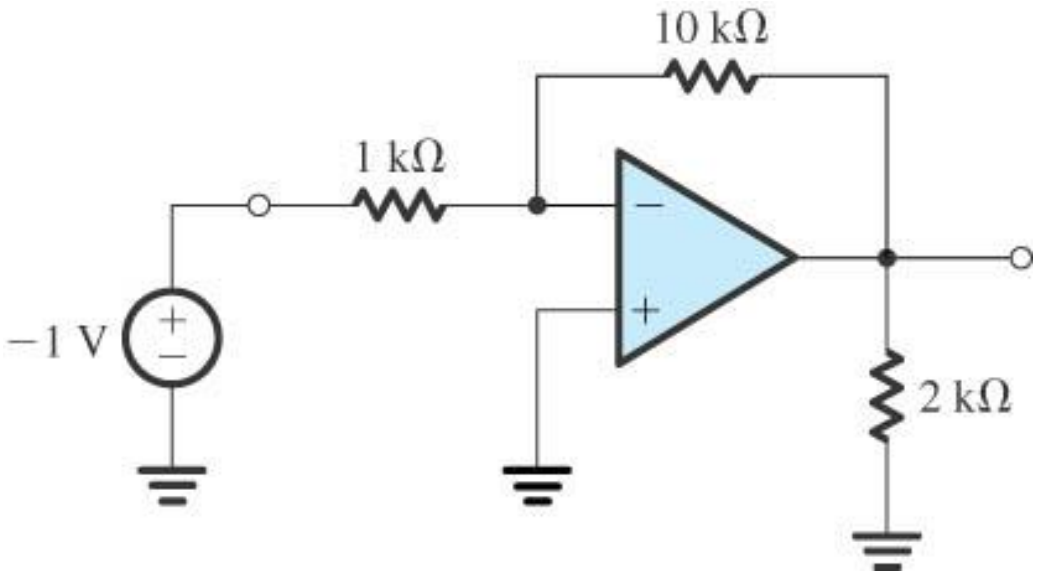


Figure P2.16

Problema 2.22

A tensão de saída é proporcional à corrente de entrada. Determine o ganho de transresistência e a resistência de entrada para os seguintes casos:

1. A é infinito.
2. A é finito.

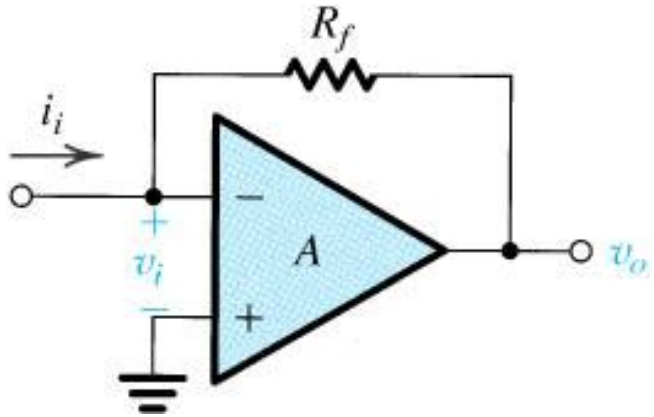


Figure P2.22

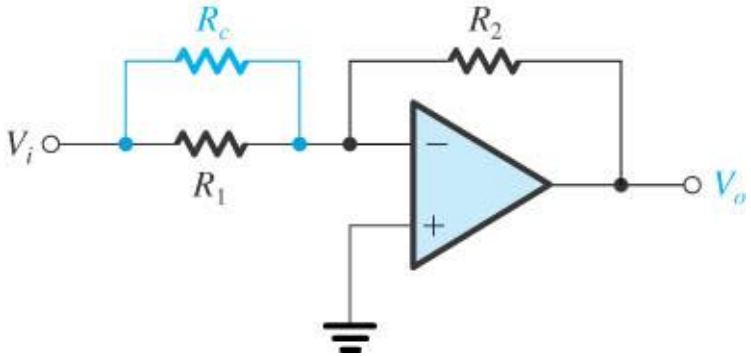


Figure P2.25

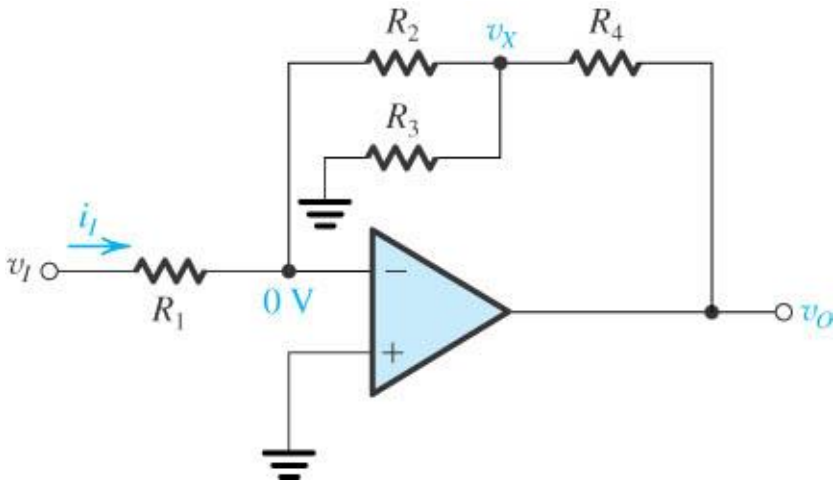


Figure P2.30

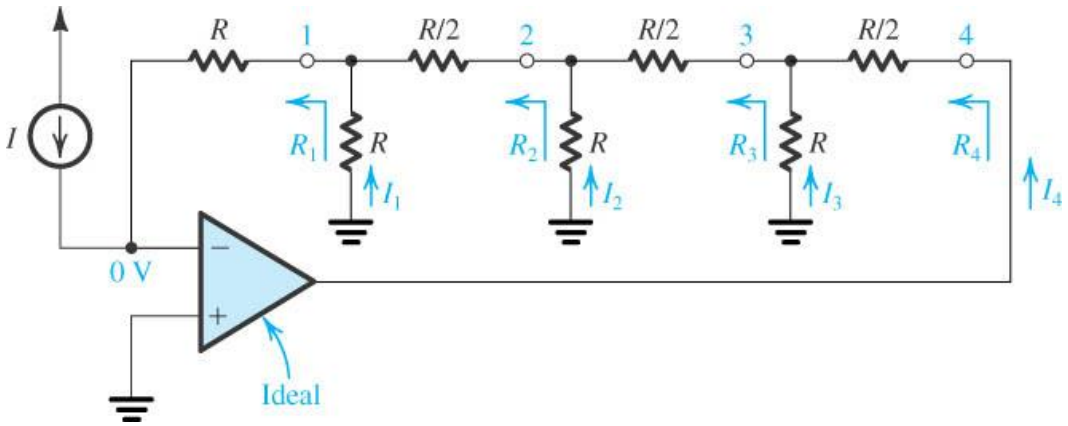


Figure P2.31

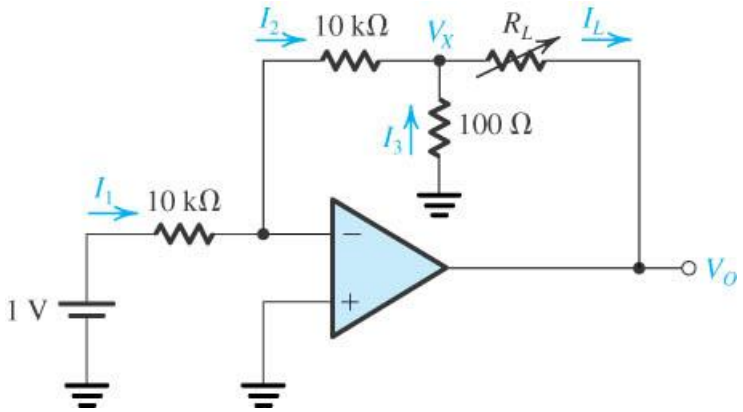


Figure P2.32

Problema 2.33

Projete o circuito da figura para implementar um amplificador de corrente com ganho i_L / i_I = 20A/A.

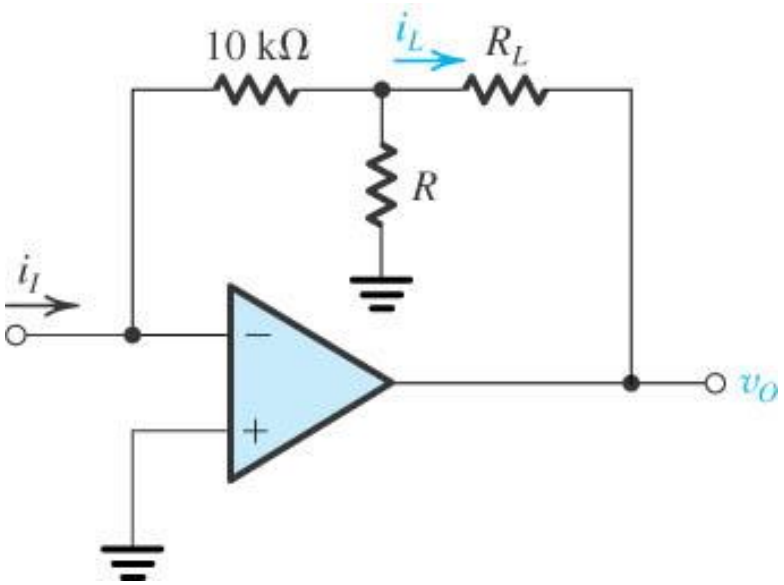


Figure P2.33

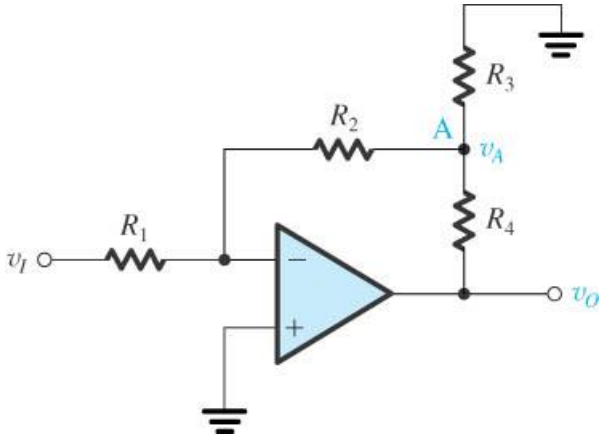


Figure P2.34

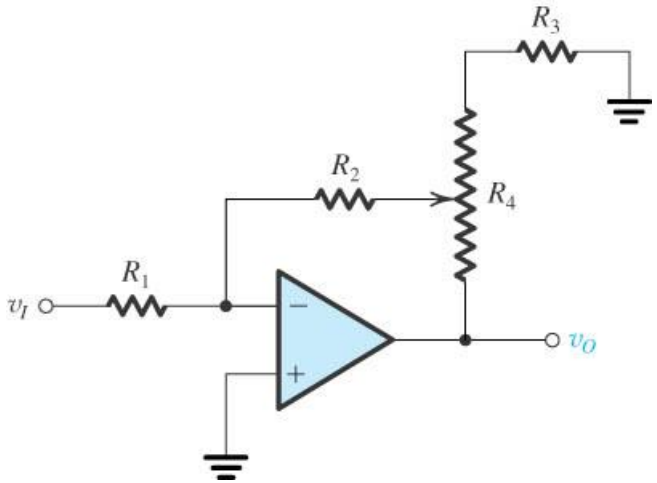


Figure P2.35

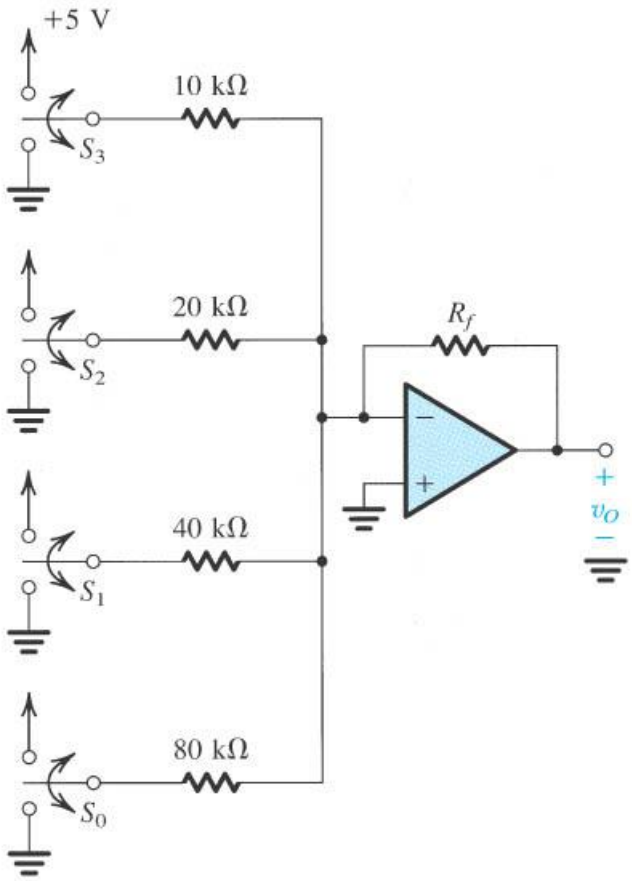


Figure P2.43

Problema 2.46

O circuito de um voltímetro analógico com alta resistência de entrada é mostrado na figura abaixo. O voltímetro mede a tensão V entre a entrada não inversora e terra. A deflexão máxima do medidor de bobina móvel ocorre para uma corrente de 100 μA. Calcule R de modo que o medidor de bobina móvel dê a leitura máxima quando V = 10 V. A resistência do medidor afeta a calibração do voltímetro?

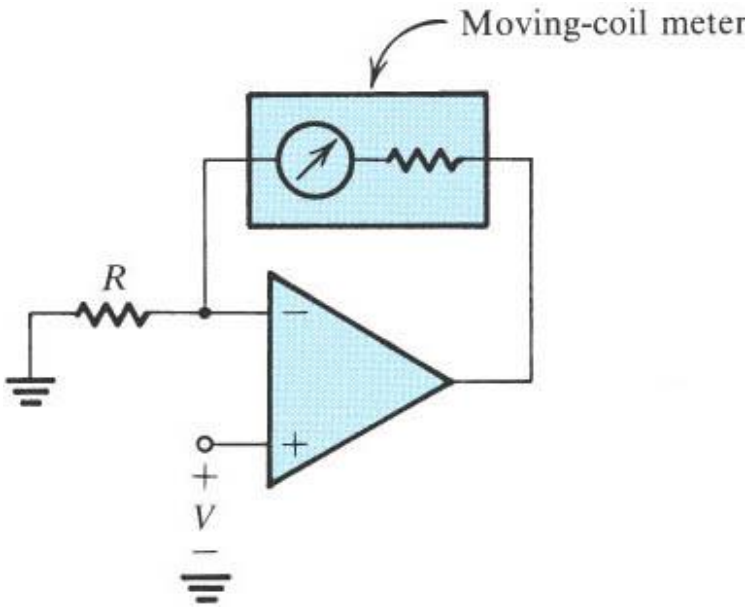


Figure P2.46

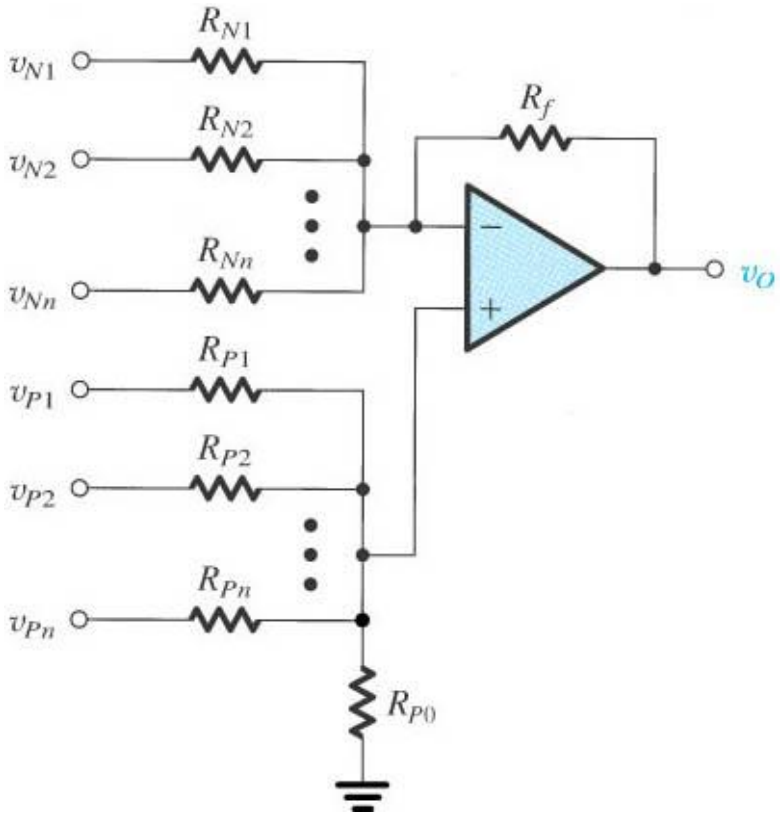


Figure P2.47

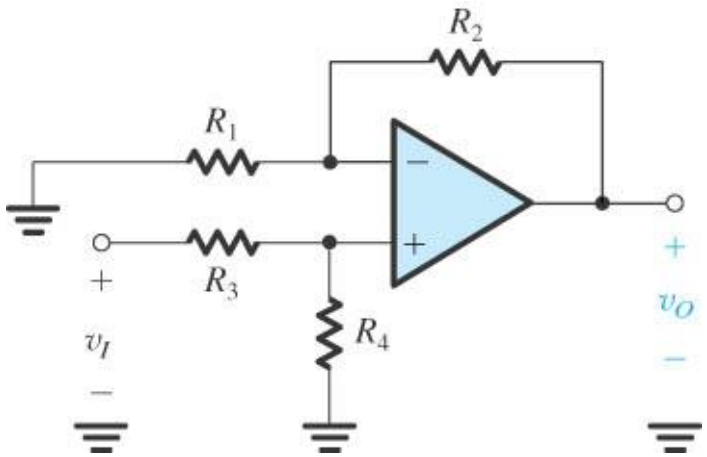


Figure P2.49

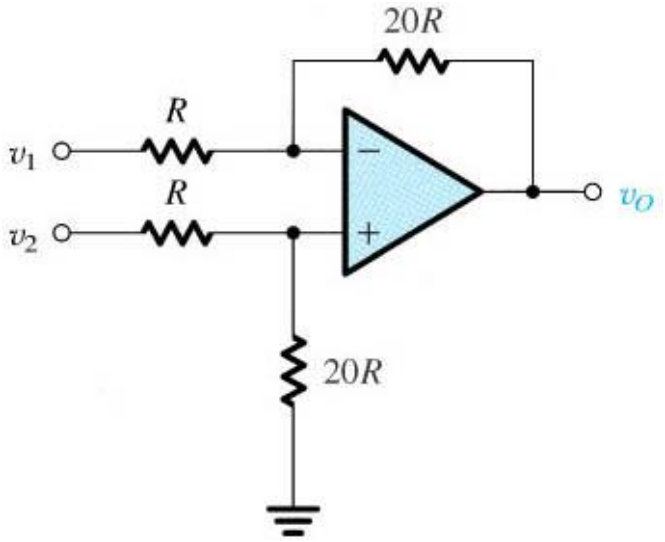


Figure P2.50

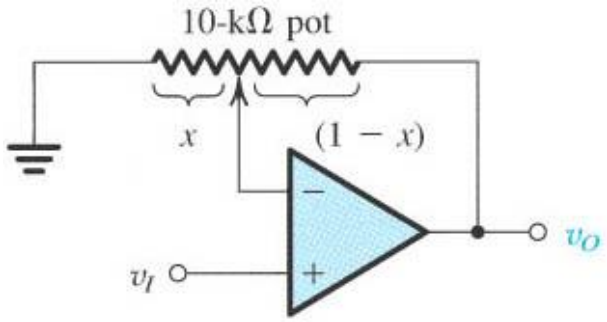


Figure P2.51

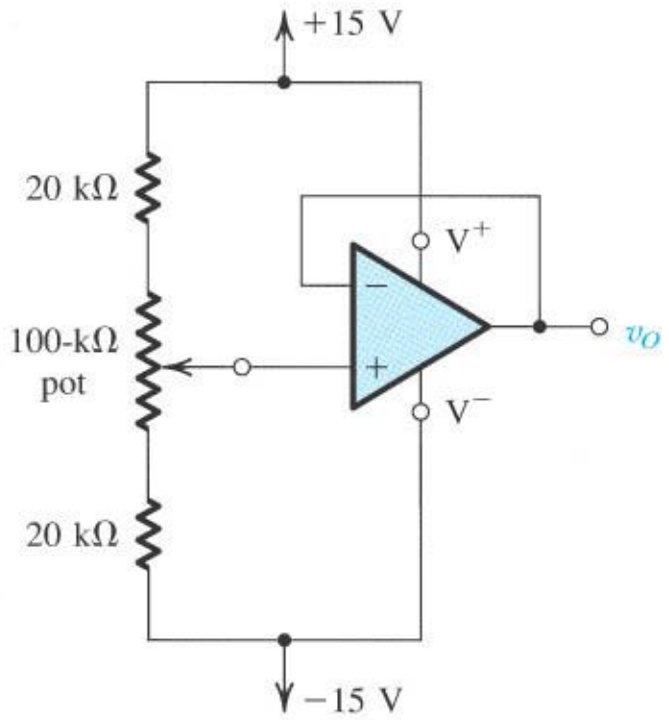


Figure P2.59

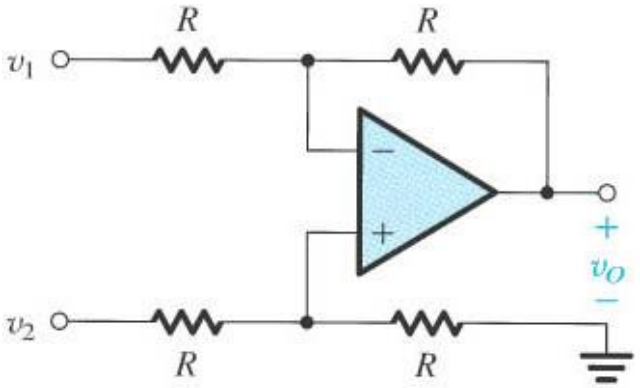


Figure P2.62

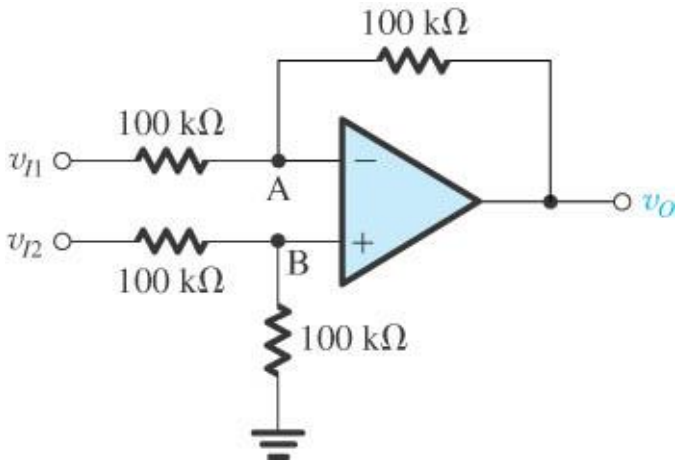


Figure P2.68

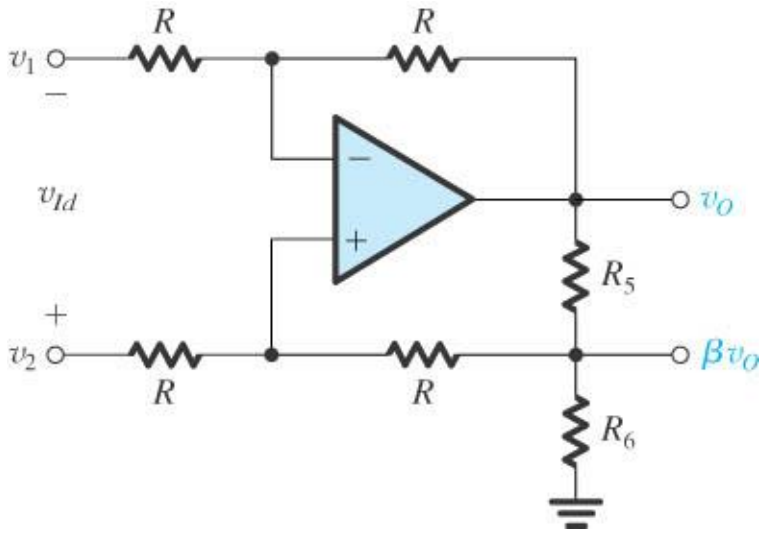


Figure P2.69

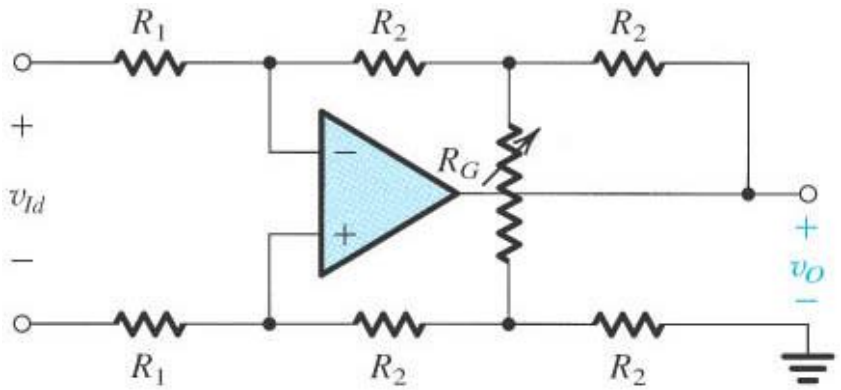


Figure P2.70

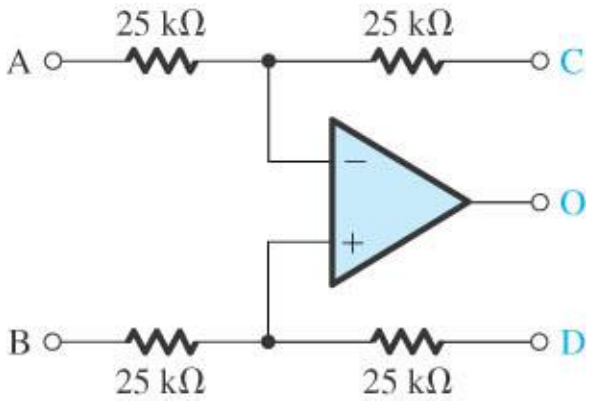


Figure P2.71

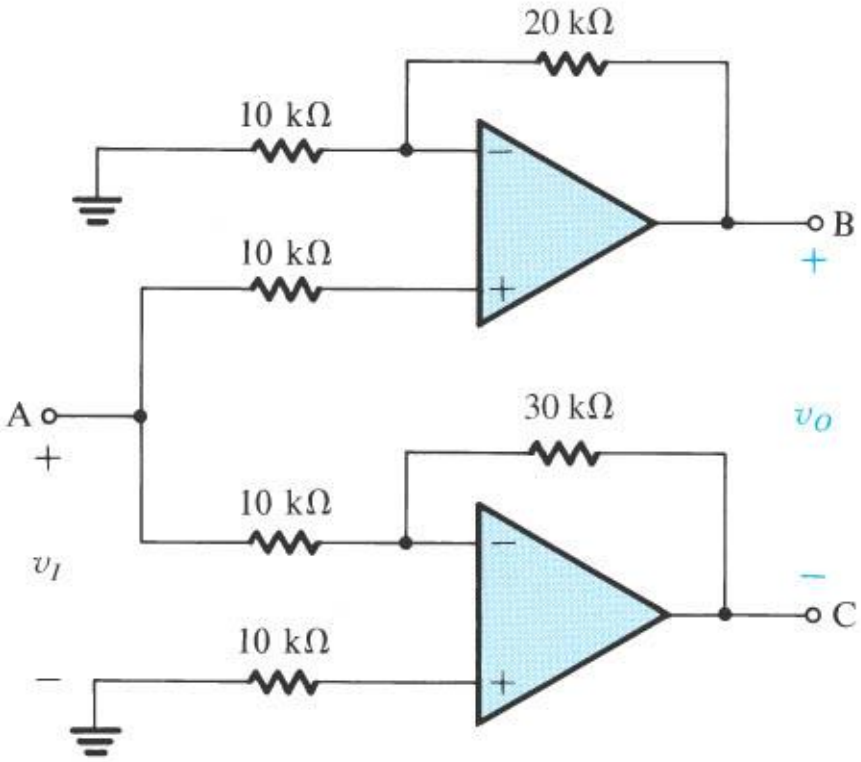


Figure P2.77

Problema 2.78

Os dois circuitos abaixo operam como conversores de tensão em corrente, ou seja, eles alimentam a impedância Z_L com uma corrente proporcional a v_I e independente do valor de Z_L. Determine as expressões i_o / v_I.

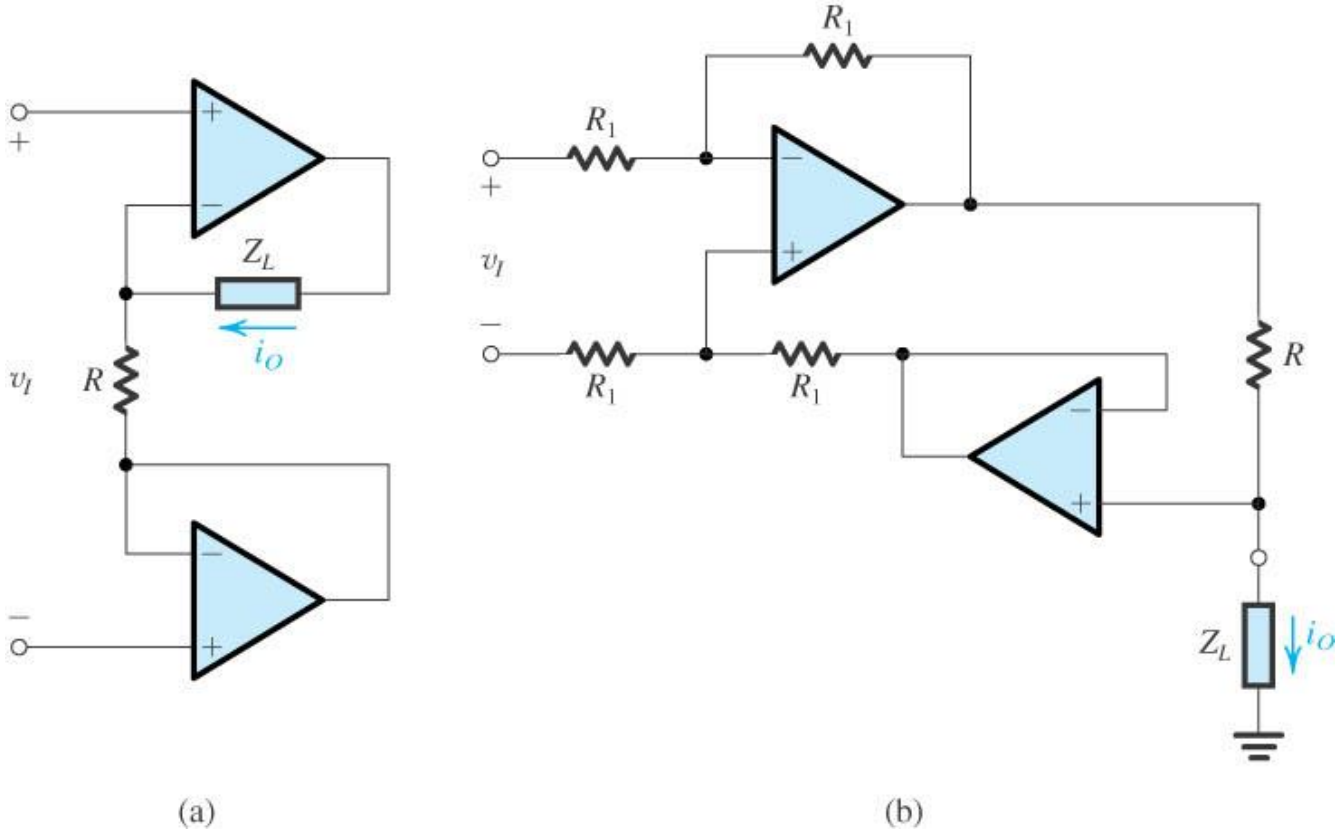


Figure P2.78

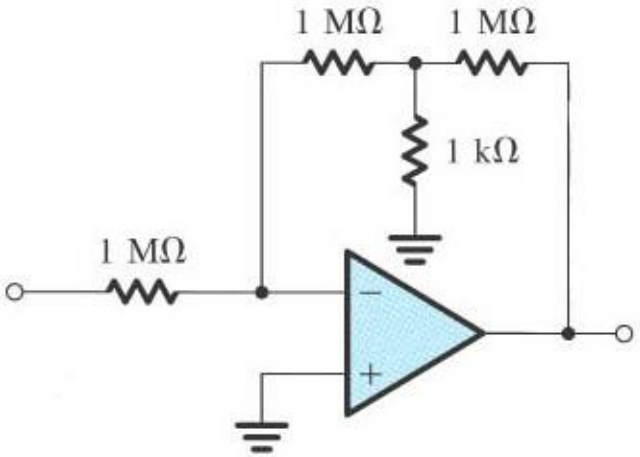


Figure P2.108

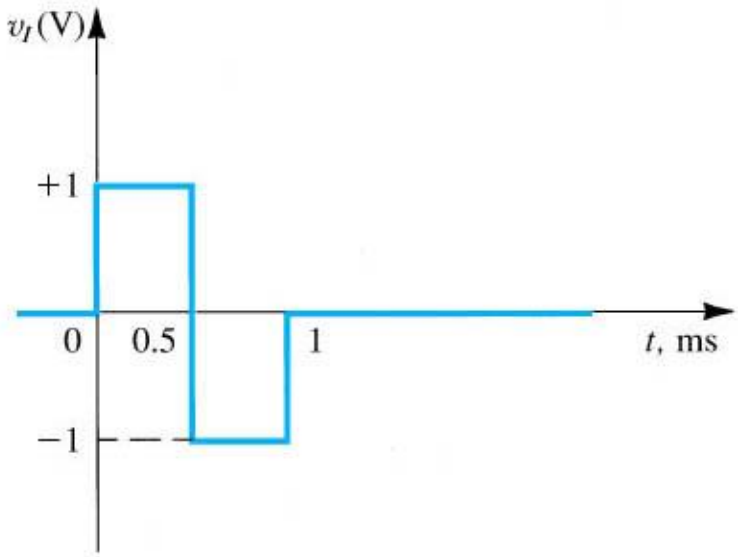


Figure P2.117

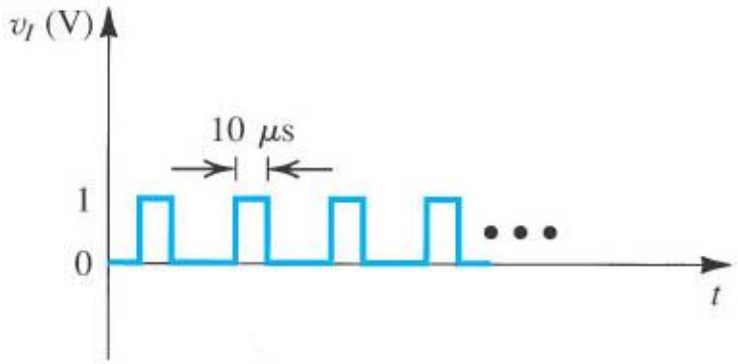


Figure P2.118

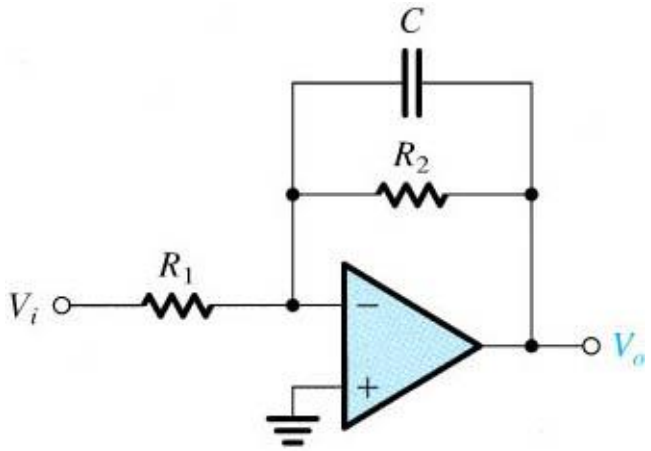


Figure P2.119

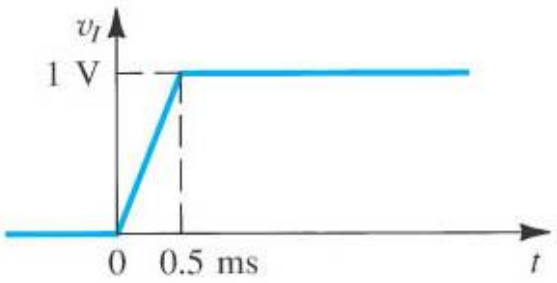


Figure P2.122

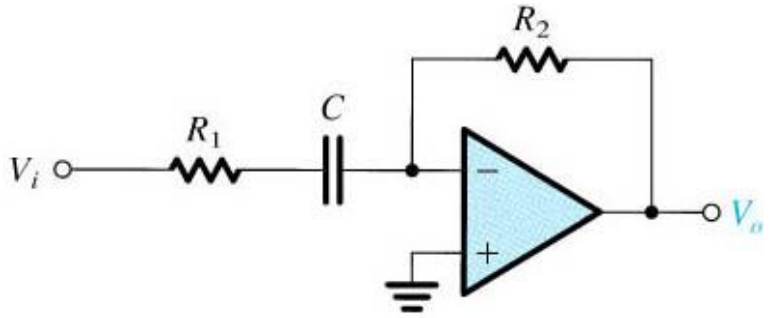


Figure P2.125

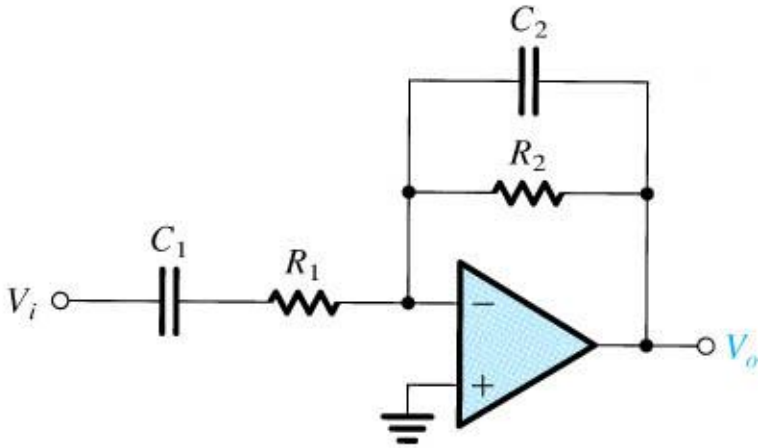


Figure P2.126