First Activity - Charts

The following experiments were executed 20 times each with a dynamic code in a i3-3110M CPU @ 2.40GHz. No cache cleaning techniques were used. The code and extracted raw data (in csv format) are attached to the zip file in which this file is located. Only for comparison purposes, naive approach (represented by "Normal" data) data was added to the files and used to better visualize the performance gain caused by Unrolling and Interchange techniques.

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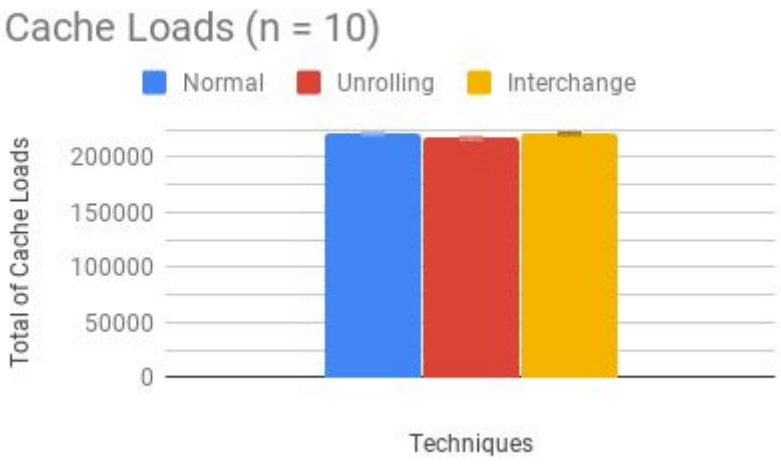
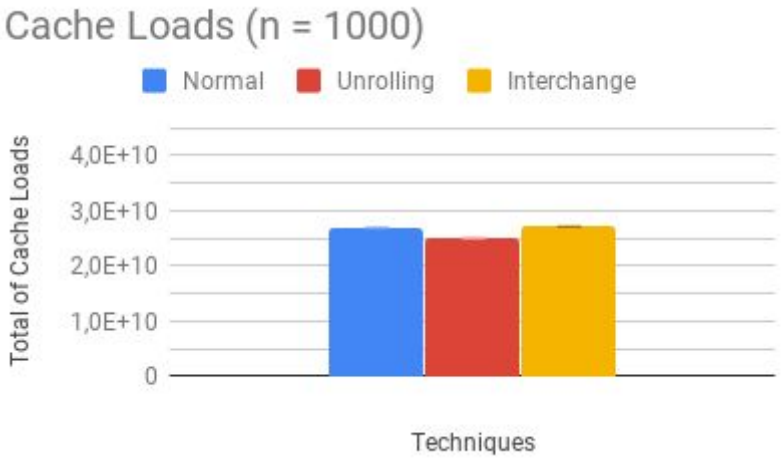
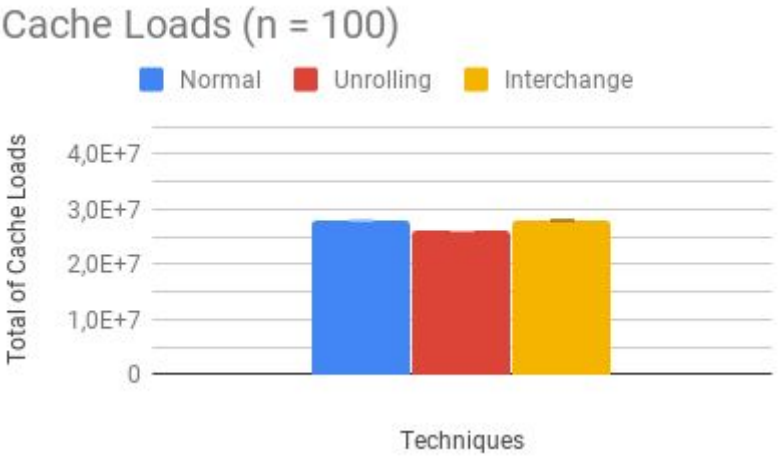
Results

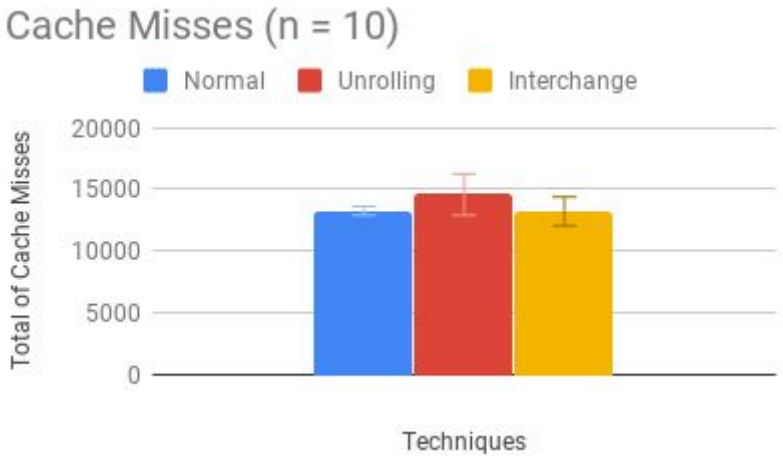
1. **Cache Load**







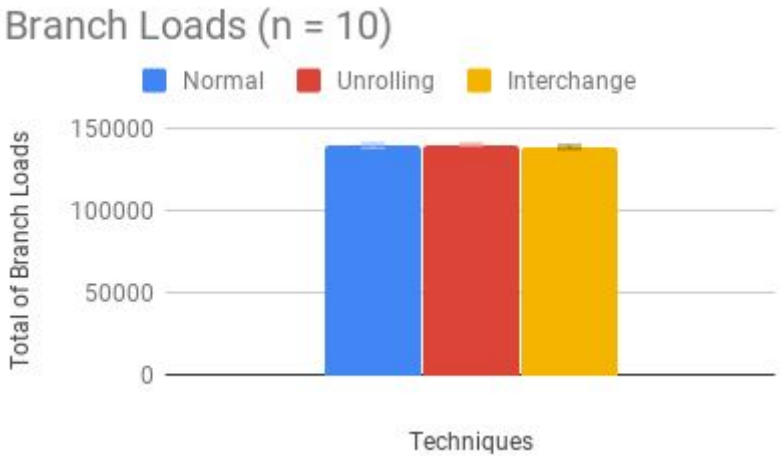
2. Cache Miss

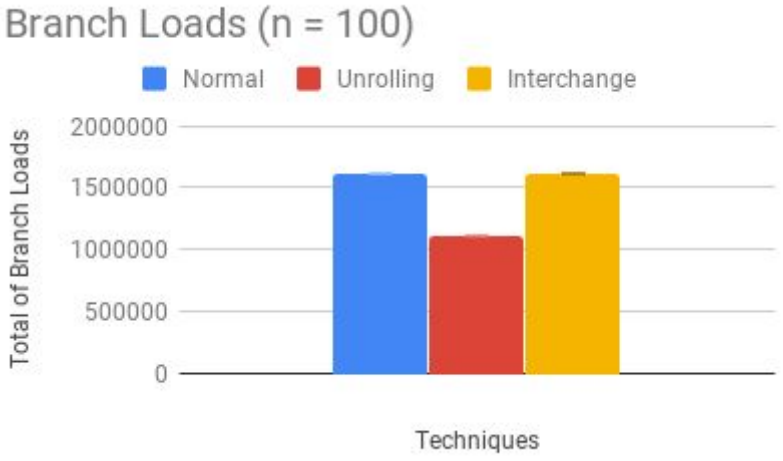

Cache Misses (n = 10)
Normal
Unrolling
Interchange
Total of Cache Misses
20000
15000
10000
5000
0
Techniques

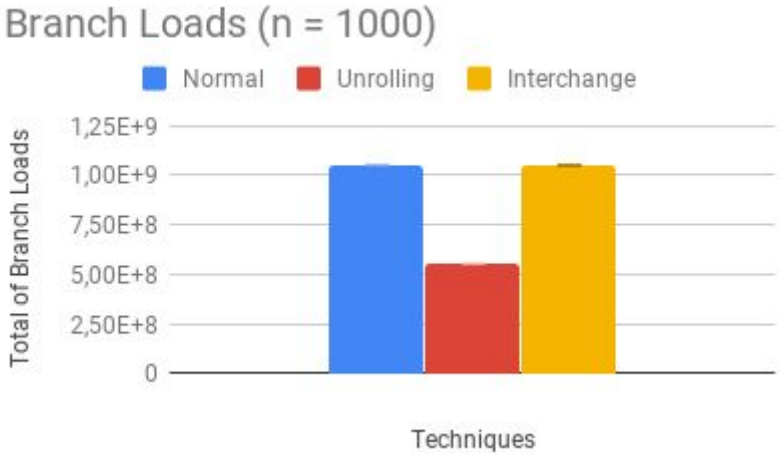

Cache Misses (n = 100)
Normal
Unrolling
Interchange
Total of Cache Misses
200000
150000
100000
50000
0
Techniques


Cache Misses (n = 1000)
Normal
Unrolling
Interchange
Total of Cache Misses
1,5E+9
1,0E+9
5,0E+8
0
Techniques

3. Branch Load







4. Branch Miss