ENCE461 Assignment 2 (version 2)

1 Introduction

This assignment is to be performed in pairs. It is a theoretical embedded systems design project where you are given an introduction to a problem and a set of requirements. This assignment can be done on computer or by hand, but calculations and reasoning must be included throughout the design process.

The objective of the embedded system is to measure the current distribution flowing through electrodes for the Joule Heating Log project, see Figure 1. The log heating system passes electrical current through segmented electrodes to heat a log through the Joule effect. Each electrode segment produces a small voltage proportional to the current passing through it. This needs to be amplified, digitised, and transmitted to a remote computer.

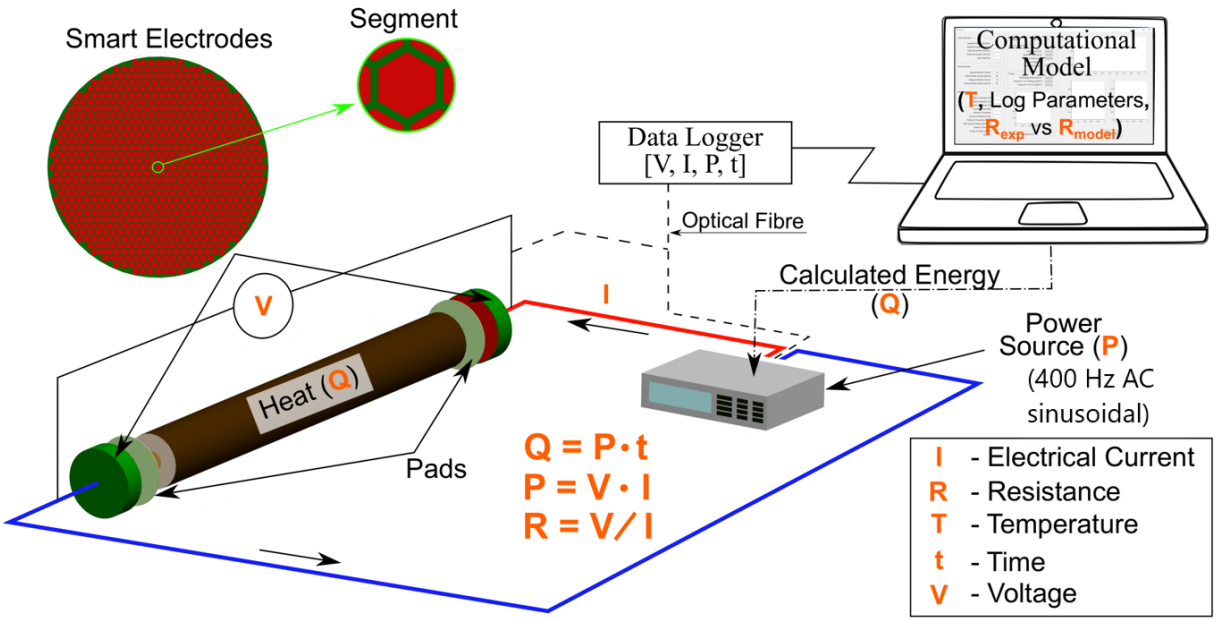

Figure 1: Overall system diagram for the Joule Heating Log project.

The system consists of a mother-board, 92 slave daughter-boards, and a master board, see Figure 3. The 500 × 500 mm mother-board has a hexagonal honeycomb pattern of 1015 electrode segments within a circle. A group of twelve electrode segments, see Figure 2, connects to a daughter-board plugged into the mother-board. Each daughter-board is identical, and at a minimum contains the following components:

- 12× opamp voltage amplifiers (gain 100), each with an enable input
- 1× microcontroller
- 1× 5 V linear regulator (each board is to be powered from 6 V)
- 1× rail splitter to provide 2.5 V reference for single-supply operation of the transimpedance amplifiers
- Connector to mother-board for input signals from the 12 electrode segments
- Connector to master board for power and communications

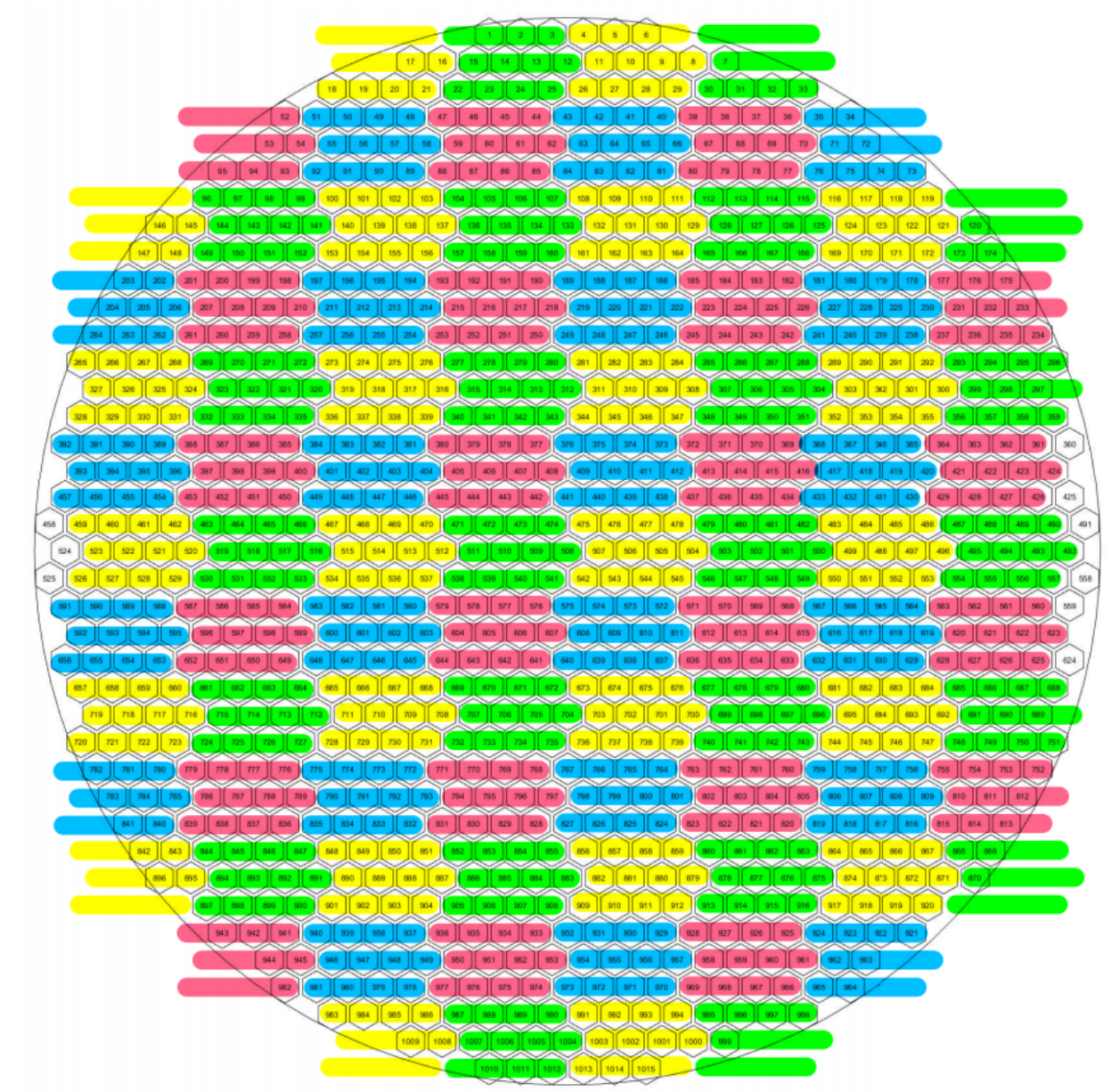

Figure 2: Each hexagon represents an individual electrode segment. A group of twelve connects to a daughterboard. The colours serve no purpose but to help distinguish the electrode segment grouping.

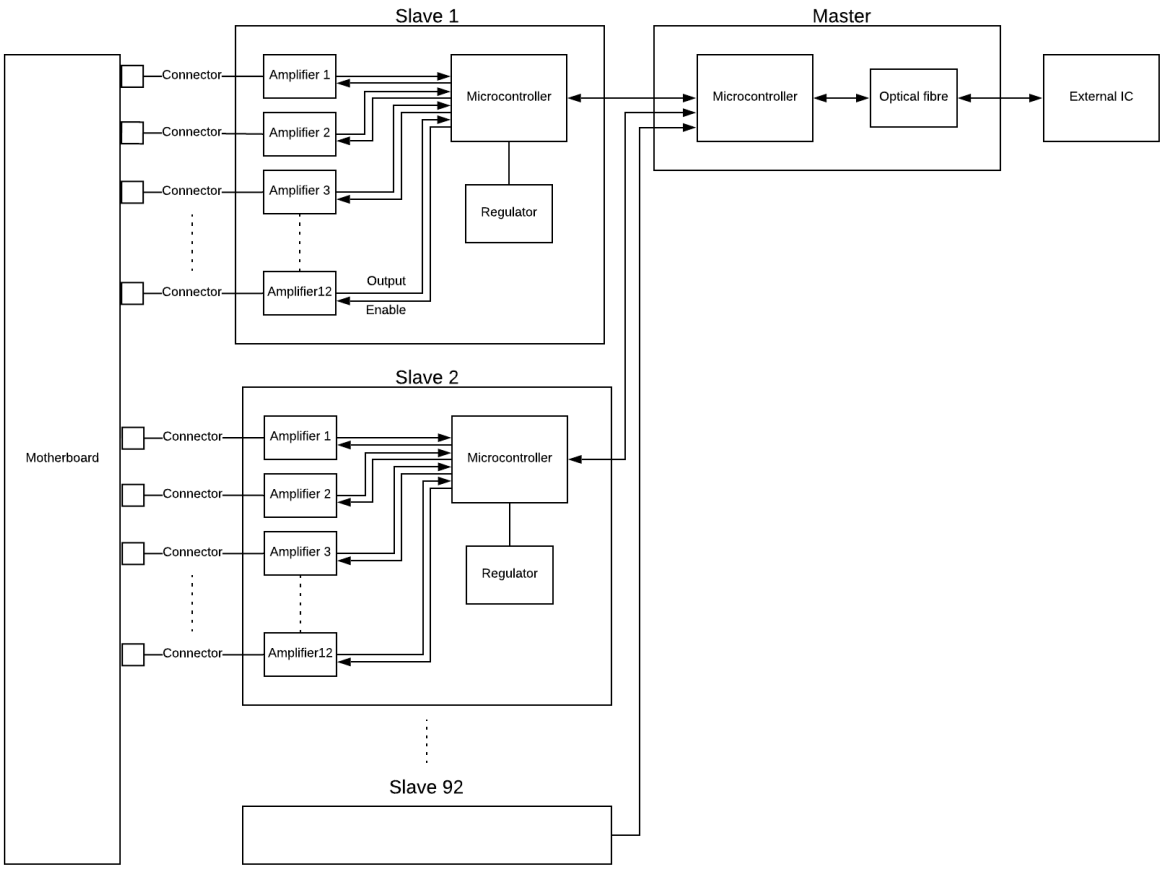

Figure 3: Simplified block diagram for the system. Here the slaves are the daughter-boards.

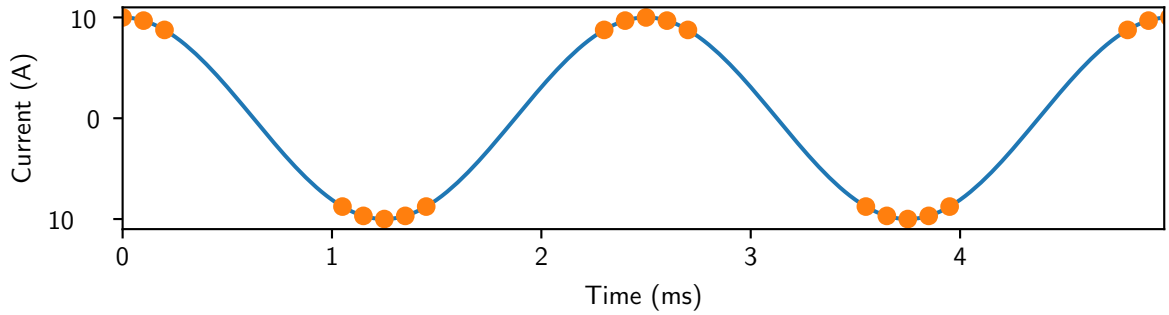

Figure 4: Sensor sampling for five sensors. The samples need to be taken near the peaks of the sinusoidal current waveform to maximise the signal to noise ratio. The sampling times are needed so that the amplitude of the sinewave can be estimated.

2 Operation

The goal of the system is to estimate the current distribution through the electrodes every 100 ms. The signal model for the measured current from a sensor is

$$x(t) = A\cos(2\pi f_0 t) + b + e(t), \tag{1}$$

where A is the unknown current amplitude, $f_0 = 400$ is the known excitation frequency, t is the measurement instant, b is an offset (assumed to be slowly varying), and $e(t)$ is the measurement noise. From this model the amplitude, A, can be estimated from two or more measurements, provided the sampling times are known. Ideally, the measurements should be taken near the peaks of the current waveform to maximise the signal to noise ratio, see Figure 4. Note, since the measurement times are required, each daughter-board needs to be synchronised to the voltage excitation.

The amplitude estimate is affected by measurement noise and timing uncertainty. The accuracy can be improved by averaging. For example, with a 400 Hz current waveform, there are 40 positive and 40 negative samples in the 100 ms measurement period.

3 System requirements

1. The system requires a mother-board, 92 slave daughter-boards, and a master board. You do not need to design the mother-board but must specify the daughter-board connector.
2. Each daughter-board has 12 opamp amplifiers (gain 100), where each opamp has an enable signal to save power.
3. The opamps require a 5 V logic signal to enable them.
4. The opamps produce a voltage between 0 and 5 V.
5. The opamps require a 5 V power supply plus a 2.5 V reference for single-supply operation. Assume each opamp takes 570 μA when disabled and 2.7 mA when enabled.
6. Each daughter-board is to be powered with 6 V.
7. Each daughter-board has a maximum width of 35 mm.
8. All components must be able to withstand ambient temperatures up to 105°C.
9. Each slave microcontroller requires at least 12 GPIO for enabling opamps, and at least 12 ADC channels to read the output voltage.
10. The selected microcontroller must achieve at least 12-bits of resolution for each channel.
11. The master and 92 slaves must be time-synced together, with an accuracy of at least 1 μs.

12. The slave and master microcontrollers must communicate. The master asks each slave for 12-bits of ADC data from each opamp, and the data from all channels must be collated every 100 ms. The communication system must be able to accommodate this and any extra required bits for error-detection, etc.
13. The microcontrollers must have a 32-bit core size.
14. The master must interface with an external IC using an optical fibre module (you do not have to select this external IC).
15. There are 92 daughter-boards, so the cost of each component used is crucial, and should be kept as low as possible.

4 Objectives

The objectives of this assignment are to:

1. Select master and slave microcontrollers to fit the requirements.
2. Select appropriate power-supply regulation.
3. Design an opamp amplifier with gain of 100. Assume that the source impedance $< 100\,\Omega$.
4. Select an appropriate communication protocol to interface between the master and slaves (not necessarily just one! Extra marks for a novel and appropriate design).
5. Select an appropriate optical communication module for the master.
6. Design a system to interlink the slaves and master to distribute power, data, and synchronisation.

5 Report

Each group needs to submit a report. This is to be a PDF with a 12-pt font or a tidily hand-written document. Clear hand-drawn sketches are acceptable without penalty. Verbosity will be penalised.

1. Describe your design, how it operates, and its pros and cons (**note, you must justify your choices**).
2. Sketch how all components are positioned on the daughter board (do not show tracks).
3. Describe layout considerations.
4. Create a bill of materials and include the cost of each component. Use `digikey.co.nz` or `mouser.co.nz` to find components.

Other aspects to consider:

1. How unique addresses are assigned to each board,
2. How the boards are programmed.
3. Communication protocols and their respective constraints.
4. Footprints of the chosen components.

Parts of the brief you do **NOT** need to look into:

1. Layout of the master microcontroller.
2. The external IC on the receiving end of the optical communication.