

# The Essence of Three-Phase PFC Rectifier Systems

Johann W. Kolar and Thomas Friedli  
 Power Electronic Systems Laboratory (PES), ETH Zurich  
 8092 Zurich, Switzerland, kolar@lem.ee.ethz.ch

**Abstract**—In this paper, three-phase PFC rectifier topologies with sinusoidal input currents and controlled output voltage are derived from known single-phase PFC rectifier systems and/or passive three-phase diode rectifiers. The systems are classified into hybrid and fully active PWM boost-type or buck-type rectifiers, and their functionality and basic control concepts are briefly described. This facilitates the understanding of the operating principle of three-phase PFC rectifiers starting from single-phase systems, and organizes and completes the knowledge base with a new hybrid three-phase buck-type PFC rectifier topology denominated as SWISS Rectifier. In addition, analytical formulas for calculating the current stresses on the power semiconductors of selected topologies are provided, and rectifier systems offering a high potential for industrial applications are comparatively evaluated concerning the semiconductor stresses, the loading and volume of the main passive components, and the DM and CM EMI noise level.

Finally, core topics of future research on three-phase PFC rectifier systems are discussed, such as the analysis of novel hybrid buck-type PFC rectifier topologies, the direct input current control of buck-type systems, the multi-objective optimization of PFC rectifier systems concerning efficiency and power density, and the investigation of the system performance sensitivity to semiconductor and passive components technology.

**Index Terms**—ac-dc converter, PWM rectifier, PFC rectifier, PFC, boost, buck, three-phase, single-phase, VIENNA Rectifier, SWISS Rectifier, overview, review.

## I. INTRODUCTION

The power electronics supply of high power electrical systems from the three-phase ac mains is usually carried out in two stages, i.e. the mains ac voltage is first converted into a dc voltage and then adapted to the load voltage level with a dc-dc converter with or without galvanic isolation (cf. Fig. 1). Often only one direction of power flow has to be provided; furthermore, coupling to the mains is typically implemented over only three conductors, i.e. without a neutral conductor.

In the simplest case, the rectification can be done by unidirectional three-phase diode rectifiers with capacitive smoothing of the output voltage and inductors on the ac or dc side (cf. Fig. 2). The low complexity and high robustness (no control, sensors, auxiliary supplies or EMI filtering) of this concept must, however, be weighed against the disadvantages of relatively high effects on the mains and an unregulated output voltage directly dependent on the mains voltage level.

The mains behavior of a power converter is characterized in general by the power factor  $\lambda$ , and/or the fundamental current-to-voltage displacement angle  $\Phi$ , and the total harmonic distortion of the input current,  $\text{THD}_i$ , which are related by the equation

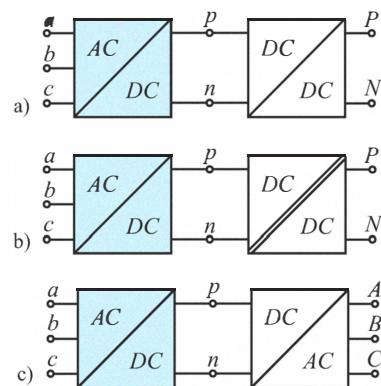
$$\lambda = \frac{1}{\sqrt{1 + \text{THD}_i^2}} \cos(\Phi). \quad (1)$$

The conduction state of the passive rectifiers shown in Figs. 2(a) and (b) is essentially determined by the mains line-to-line voltages, whereby only two diodes carry current at the same time, except the commutation intervals. This means that each diode of the positive and negative bridge halves carries current only for one third of the mains period, i.e. for  $120^\circ$ . Hence, the phase currents for

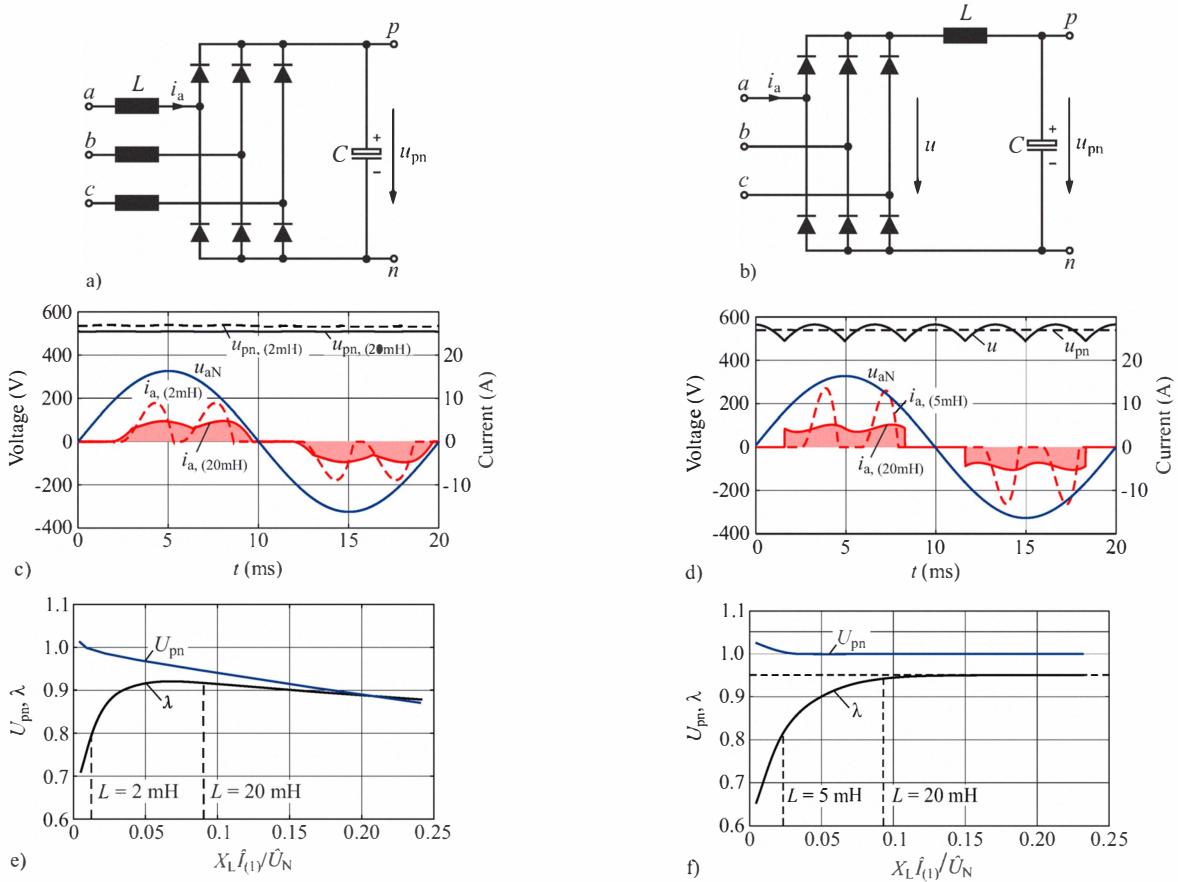
industrially applicable values of the smoothing inductance show  $60^\circ$ -wide intervals with zero current that result in a relatively high low-frequency harmonic content or a  $\text{THD}_i \approx 30\%$ . In order to avoid voltage distortions resulting from voltage drops across the inner (inductive) mains impedance or the excitation of resonances in the distribution grid a  $\text{THD}_i < 5\%$  at rated power is often required. For aircraft on-board power supplies, relatively high inner mains impedances exist and thus even stricter limits, i.e. a  $\text{THD}_i < 3\%$  (cf. DO160F, MIL-461E), have to be fulfilled. This mains current quality can be achieved only by means of active Power Factor Correction (PFC) rectifier systems.

It should be noted that for three-phase systems, the generally used designation *PFC Rectifier* is partly misleading, since passive rectifiers, for industrially used values of the smoothing inductance [ $X_L \hat{I}_{(1)} / \hat{U}_N = 0.05 \dots 0.15$  according to Figs. 2(e) and (f)], already exhibit a high power factor of  $\lambda = 0.9 \dots 0.95$  because of the low phase-shift of the power-forming mains current fundamental component and the associated phase voltage (cf. (1) for  $\cos(\Phi) = 1$  and  $\text{THD}_i \approx 30\%$ , [1], [2]). PFC rectifiers hence achieve with regard to the mains current (at rated operation) above all a reduction of the current harmonics but only a slight improvement in the power factor ( $\lambda > 0.99$  at the rated operating point is typically targeted).

A further important aspect of the use of active (PFC) rectifier systems is the possibility to control the output dc voltage to a constant value, independent of the actual mains voltage (Europe:  $U_{N,LL,\text{rms}} = 400\text{ V}$ ; USA, Japan:  $U_{N,LL,\text{rms}} = 200\text{ V}$ ,  $U_{N,LL,\text{rms}}$  denotes the rms value of the mains line-to-line voltage). A converter stage on the output side (cf. Fig. 1) can thus be dimensioned to a narrow voltage range. The mains voltage range must be considered only for the dimensioning of the rectifier stage (the delivery of a given rated power, e.g. at half of the input voltage, leads to a doubling of the input current that must be mastered by the power semiconductors,



**Fig. 1.** Block diagrams of typical converter configurations for supplying electrical loads from the three-phase ac mains. a) Three-phase ac-dc converter with non-isolated dc-dc converter (e.g. for the coupling of dc distribution systems to the three-phase mains or as a mains interface for high-power isolated loads, e.g. lighting systems). b) Three-phase ac-dc converter with isolated dc-dc converter (e.g. for telecom power supplies, welders, or induction heating systems). c) Three-phase ac-dc converter and three-phase dc-ac converter (inverter) without isolation (e.g. for variable speed drives).



**Fig. 2.** Passive three-phase diode rectification. a) Smoothing inductors  $L$  on the ac side. b) Smoothing inductor  $L$  on the dc side. c) and d) Corresponding input current waveforms. e) and f) Resultant global average value  $U_{pn}$  of the output voltage  $u_{pn}$  and power factor  $\lambda$  at the input. (Simulation parameters: rms line-to-line voltage  $U_{N,1l,\text{rms}} = 400\text{ V}$ , mains frequency  $f_N = 50\text{ Hz}$ , smoothing capacitance on the dc side  $C = 1\text{ mF}$ , and smoothing inductance  $L = [1\text{ mH} \dots 45\text{ mH}]$ .)

passive power components and the EMI filter) or a relatively high and well-defined voltage level is available for the generation of the output (load) voltage [cf. Fig. 1(c)].

The requirements placed on active PFC rectifier systems may thus be summarized as follows:

- sinusoidal input current according to regulations regarding the mains behavior of three-phase rectifier systems (EN 61000-3-2 if  $< 16\text{ A}$ , 61000-3-4 if  $> 16\text{ A}$ ); in industry, however, typically independent of the concrete application, a  $\text{THD}_i < 5\%$  is required (at the rated operating point);
- ohmic fundamental mains behavior ( $\cos(\Phi) > 0.99$ );
- regulated output voltage; depending on the required level of the output dc voltage relative to the mains voltage, a system with boost-, buck- or buck-boost-type characteristic has to be provided;
- mastering of a mains phase failure, i.e. for interruption or voltage collapse of one mains phase, continued operation at reduced power and unchanged sinusoidal current shape should be possible;
- unidirectional power flow, perhaps with (limited) capability of reactive power compensation. Often, because of the supply of a purely passive load (e.g. telecom power supply), only unidirectional energy conversion has to be provided or as for aircraft on-board power supplies, no feedback of energy into the mains is permitted;
- compliance with specifications regarding electromagnetic, especially conducted interference emissions by means of suitable EMI filtering.

The designation *three-phase PFC rectifier* chosen in this paper implies both sinusoidal mains current shaping and regulation of the dc output voltage. Here, it should be noted that an active harmonic filter [3] of lower rated power arranged in parallel to a passive rectifier system would also enable a sinusoidal mains current, but no regulation of the output voltage. Accordingly, because of the system-related advantage of a constant supply voltage of a load side converter, a PFC rectifier system is often preferred over active filtering despite the larger implementation effort, i.e. the conversion of the entire output power.

Parallel to the development of single-phase PFC rectifier circuits, numerous concepts for three-phase PFC rectifier systems have been proposed and analyzed over the last two decades. However, the topological relationships between the circuits and a comprehensive classification have received relatively little attention. Furthermore, the basic function of the circuits was typically treated by space vector calculation, analogous to three-phase drive systems, which is not immediately comprehensible on the basis of knowledge of dc power supply technology or single-phase PFC rectifier circuits.

The goal of the present work is hence to develop the concepts of three-phase PFC rectifiers, starting from known single-phase PFC rectifier systems, and to explain as clearly as possible their basic function and control, without reference to analysis techniques being specific to three-phase converter concepts. Details of the Pulse Width Modulation (PWM) and a detailed mathematical analysis are omitted, i.e. only the operating range of the systems is clarified with regard to output voltage and mains current phase angle. Furthermore, the dimensioning of the power semiconductors, the main passive components, and the EMI filter is briefly discussed.

To keep matters short, the considerations remain limited to unidirectional systems and here to those circuits that come into question with regard to implementation effort for industrial applications or have already found such applications. Numerous, only theoretically interesting circuit proposals of high complexity and/or high component loading are hence not considered. In particular, no circuits are discussed that fundamentally demand low frequency passive components e.g. dimensioned for sixfold mains frequency. Passive six- or twelve-pulse rectifier systems [5], and hybrid rectifier circuits with passive 3<sup>rd</sup> harmonic current injection networks [6], [7] are thus also not treated.

In the following, in **Section II**, a comprehensive classification of unidirectional three-phase rectifier systems is presented that for completeness also includes purely *passive* systems. For PFC rectifier circuits, a division is made between circuits that are fully active and hybrid, i.e. partially mains-commutated, and partially self-commutated systems. With regard to the basic structure, phase-modular and direct three-phase systems are distinguished and subsequently treated in more detail in **Section III** and **Section IV** with reference to selected examples. Apart from systems with boost-type characteristic, buck-type PFC rectifier systems are also discussed, which were not considered in [8], but will be of special interest in future in connection with the charging of electric vehicle batteries or the supply of dc distribution grids. The ordering and complementation of the knowledge base of three-phase buck-type PFC rectifier systems leads to a new hybrid circuit concept (SWISS Rectifier) that is characterized by low complexity of the power circuit and control, and thus of particular interest for industrial applications. In **Section V**, in the sense of support for the dimensioning of the circuits, the current stresses of the main circuit components are briefly summarized in the form of simple analytical expressions, and the Differential

Mode (DM) and Common Mode (CM) EMI filtering of the systems discussed. Finally, in **Section VI**, a comparative evaluation of selected boost-type and buck-type PFC rectifier systems is presented, which is intended as an aid for the choice of concepts in industrial development projects. In conclusion, in **Section VII**, with regard to future further increasing requirements on the efficiency and power density of the systems, and the further spreading of active mains interfaces, research subjects in the field of PFC rectifier circuits are identified.

## II. CLASSIFICATION OF UNIDIRECTIONAL THREE-PHASE RECTIFIER SYSTEMS

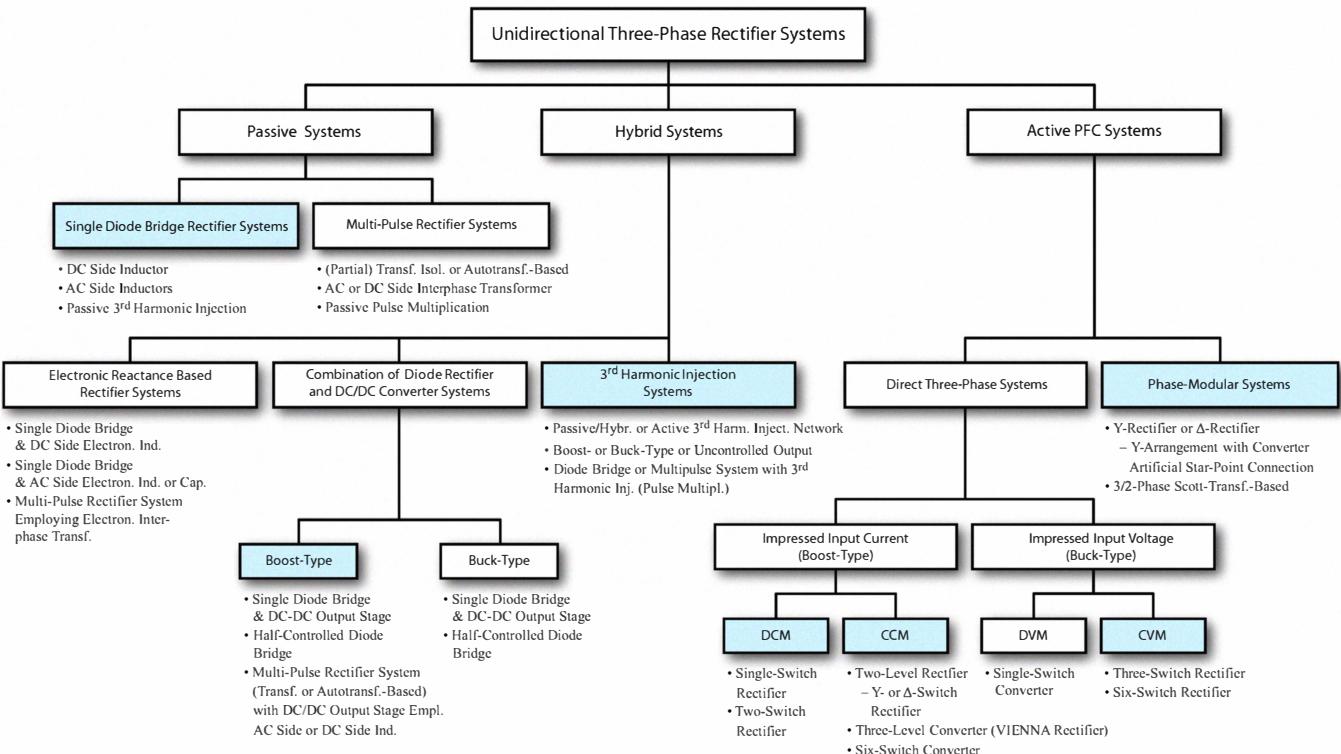
In **Fig. 3**, a classification of unidirectional three-phase rectifier circuits is shown that for completeness also includes purely *passive* systems which

- contain no turn-off power semiconductors, i.e.
- work purely mains-commutated, and
- employ low frequency, i.e. passive components for output voltage smoothing and mains current shaping and, where applicable, mains or auto-transformers for the phase-shift of several converter stages working in parallel or series (multi-pulse rectifier circuits).

Furthermore, since here only diode and not thyristor circuits are considered,

- there is no possibility of output voltage regulation.

An approximately sinusoidal mains current and/or partial elimination of low frequency harmonics in the input current is thus only obtainable with multi-pulse systems, i.e. for 12-, 18- or 36-pulse rectifier circuits. In industry, multi-pulse rectifiers, because of their low complexity and great robustness, are mainly used at high power ( $> 100 \text{ kW}$ ) as mains interfaces, where the supply is typically direct



from the medium voltage mains whose low inner impedance allows higher input current harmonics to be accepted.

The coupling and/or partial integration of a passive rectifier and of an active circuit part implemented with power semiconductors that can be actively switched off, leads to *hybrid rectifier circuits*.

These systems fundamentally allow a regulation of the output voltage and a sinusoidal control of the mains current; however, a limitation to voltage regulation is possible (e.g. in the case of a diode bridge with downstream dc–dc converter) or to sinusoidal current shaping (active-filter-type 3<sup>rd</sup> harmonic current injection, cf. Sec. IV or [9]–[14]). Furthermore, low frequency filter components of passive rectifier systems may be replaced/emulated by high-frequency PWM converters of relatively low rated power (Electronic Inductor [15], [16]), e.g. in the sense of an increase of the power density. With an ac side arrangement of these electronic reactances, via a change in the inductance or capacitance value in operation, a limited possibility of voltage regulation exists (Magnetic Energy Recovery Switch (MERS) concept [17], [18]).

3<sup>rd</sup> harmonic injection concepts form a major group of hybrid rectifier circuits. Here, current is injected by a passive or active injection network always into that phase which would not carry current in case of conventional diode bridge rectification. The current waveforms of the two other phases are shaped in such a way that as a result, sinusoidal current flows in all phases. The rectifier function of these systems is implemented by a diode bridge on the input side. The active network for current shaping, injection, and voltage regulation, arranged on the dc side, may thus be considered essentially as a dc–dc converter working on a time-varying (six-pulse) dc input voltage. The circuits are hence relatively simple, i.e. may be analyzed without specific knowledge of three-phase converter systems and exhibit relatively low complexity, also regarding control. The essential characteristics of hybrid rectifier circuits may thus be summarized as follows:

- mains-commutated (diode circuits) and force-commutated, circuit sections implemented with power semiconductors that can be actively switched off;
- low frequency and/or switching frequency passive components;
- output voltage regulation and/or sinusoidal mains current shaping by turn-off power semiconductors.

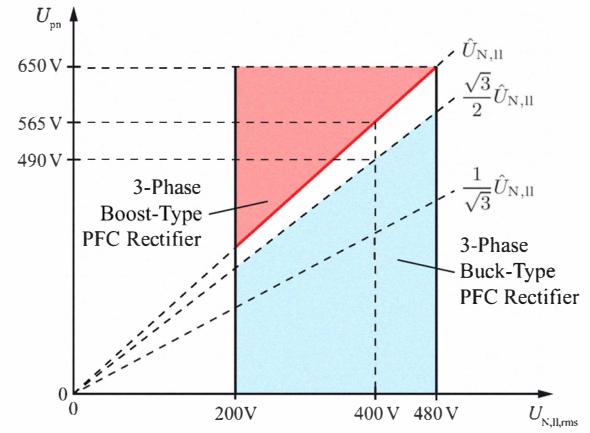
In the present work, only those hybrid rectifier circuits are considered which exhibit regulated output voltage and sinusoidal mains current, and exclusively switching frequency passive components.

Integration of turn-off power semiconductors into the bridge-legs of a passive system finally leads to *active PFC rectifier systems*. Essential features of these systems are:

- forced commutation (only for systems with impressed output current partly natural commutations occur, depending on the position of the switching instant in the mains period);
- exclusively switching frequency passive components;
- regulated output voltage.

As described in more detail in Sec. IV, these systems exhibit in general bridge topologies and here bridge-legs of same structure, i.e. *phase symmetry*, and a similar configuration of the power semiconductors in the positive (connected to the positive output voltage bus) and negative bridge halves, i.e. *bridge symmetry*.

Apart from these direct three-phase versions (cf. Fig. 3), however, an implementation is also possible via a combination of single-phase PFC rectifier systems in star(Y)- or delta( $\Delta$ )-connection [cf. Figs. 5(a) and (b)]. These phase-modular versions, however, lead to three individual dc output voltages, i.e. a single output voltage can only be formed via isolated dc–dc converters that are connected to the rectifier outputs. An advantage of the phase-modular version is



**Fig. 4.** Output voltage range of direct three-phase PFC rectifier systems with boost- or buck-type characteristic in dependence of the rms line-to-line mains voltage  $U_{N,ll,rms}$  (considered mains voltage range:  $U_{N,ll,rms} = 200 \text{ V} \dots 480 \text{ V}$ );  $\hat{U}_{N,ll}$  denotes the peak value of the line-to-line voltage. In addition, the lower output voltage limit of a single-phase boost-type PFC rectifier system ( $U_{pn} > 1/\sqrt{3}\hat{U}_{N,ll}$ ), connected between a mains phase and the mains neutral, is shown.

the possibility of realizing a three-phase system starting from existing already developed single-phase systems. However, it must be taken into account that with the star-connection a coupling of the phase system results. For the delta-connection, the high input voltage of the modules has to be considered, which is defined by the mains line-to-line voltage and not by the phase voltage.

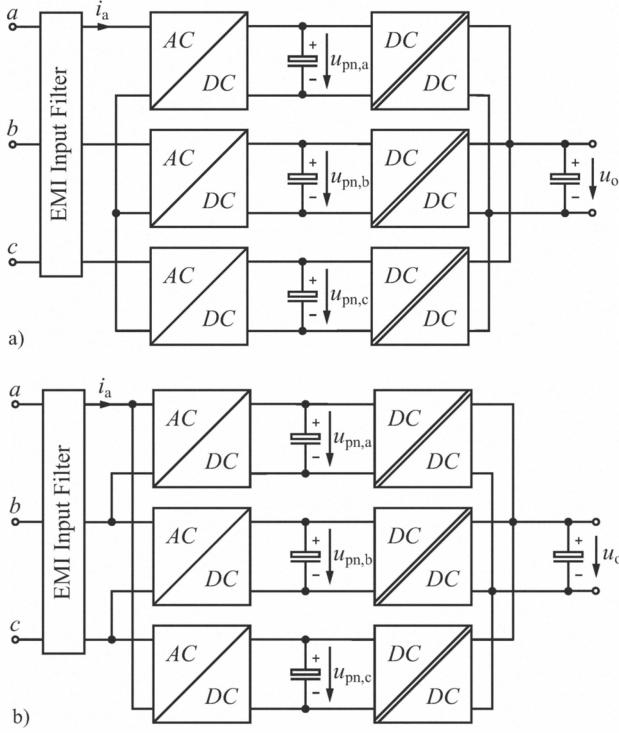
Apart from the topological distinction, a classification of the systems must also be carried out with regard to the available output voltage range, i.e. fundamentally into circuits with boost- or buck-type characteristic. As shown in Fig. 4, the lower or upper output voltage limits of the systems are defined by the mains line-to-line voltage. The voltage range, not covered by the two basic converter forms, is usually realized in industry by means of a downstream dc–dc converter with boost- or buck-type characteristic. Alternatively, a three-phase extension of buck-boost [19], Cuk- or SEPIC-converters [20] could be used. Because of the high complexity of the resulting circuit, however, this approach is only of theoretical interest and is hence not described in more detail.

With regard to phase-modular rectifiers, it must be pointed out that buck-type converter systems enable a current shaping only in a part of the mains period [21]. Hence, for sinusoidal mains current, a boost function must be provided which results in a lower limit of the output voltages of the modules.

Note: Systems with galvanic isolation of the output voltage are not treated in this paper. In many cases, isolation is achieved by a dc–dc output stage at high frequency, or is required directly at the supply of the systems for voltage adaptation, e.g. for connection to the medium voltage level. Alternatively, a transformer may be integrated directly into the rectifier structure. Such high frequency isolated three-phase ac–dc matrix converter concepts [22]–[24], however, are characterized by a relatively high complexity of the power circuit and modulation and hence are of limited importance for industrial applications.

### III. PHASE-MODULAR RECTIFIERS

Starting from the basic circuits of symmetrical three-phase loads, three-phase PFC rectifier systems can be implemented by star- or delta-connection of single-phase PFC rectifiers. The phase-modular systems thus formed will be termed in the following Y- or  $\Delta$ -rectifiers according to the circuit structure. The phase modules here may exhibit a conventional topology or could be implemented as bridgeless, i.e.



**Fig. 5.** Block diagram of phase-modular PFC rectifier systems [25]–[27]. **a)** Star(Y)-connection / Y-rectifier and **b)** delta( $\Delta$ )-connection /  $\Delta$ -rectifier with output side isolated dc–dc converters. Instead of a common EMI input filter for all phases as used for **a)** and **b)**, in terms of full modularity, also separate EMI filters could be implemented for each rectifier module.

dual-boost converters, or ac-switch converters (cf. **Fig. 11**). They may contain an EMI filter or advantageously, a three-phase EMI filter could be installed common to all phase systems.

#### A. Y-Rectifier

**Fig. 6** shows the circuit topology of a Y-rectifier with a bridgeless topology of the phase modules and an equivalent circuit of the ac side system part. If the EMI filter is three-phase (not shown in **Fig. 6**) and the star-point  $N'$  is not connected to an artificial star-point, which could be formed e.g. by filter capacitors, a switching frequency voltage  $u_{N'N}$  occurs between  $N'$  and the mains star-point  $N$ .

According to

$$\begin{aligned} L \frac{di_a}{dt} &= u_{aN} - (u_{\bar{a}N'} + u_{N'N}) \\ L \frac{di_b}{dt} &= u_{bN} - (u_{\bar{b}N'} + u_{N'N}) \\ L \frac{di_c}{dt} &= u_{cN} - (u_{\bar{c}N'} + u_{N'N}) \end{aligned} \quad (2)$$

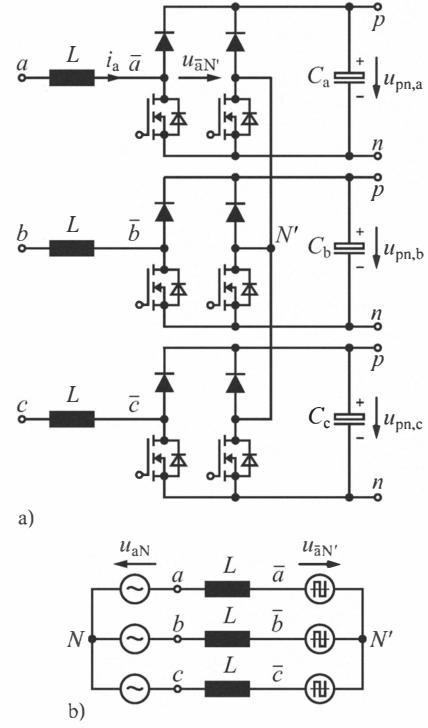
the impression of the ac currents is via the differences of the mains phase voltages and the voltages  $u_{\bar{i}N'}$  ( $i = a, b, c$ ) formed at the input of the rectifier stages, so that the star-point voltage  $u_{N'N}$  with consideration of

$$\frac{d}{dt} (i_a + i_b + i_c) = 0 \quad (3)$$

results in

$$u_{N'N} = -\frac{1}{3} (u_{\bar{a}N'} + u_{\bar{b}N'} + u_{\bar{c}N'}) . \quad (4)$$

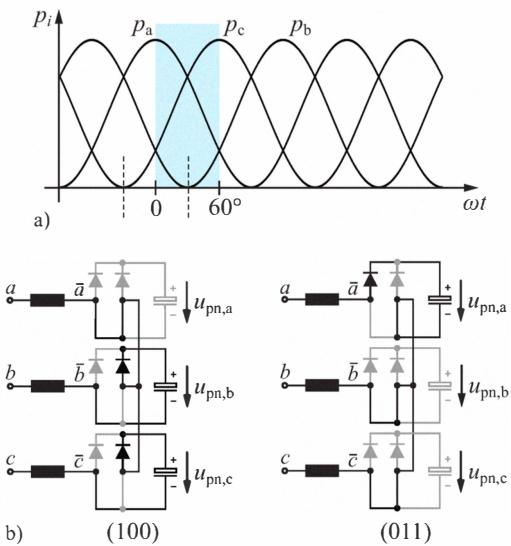
Therefore, with a free star-point  $N'$ , a part of the rectifier input voltage  $u_{\bar{i}N'}$  advantageously does not form a current ripple, so that the values of the boost inductance may be reduced compared to



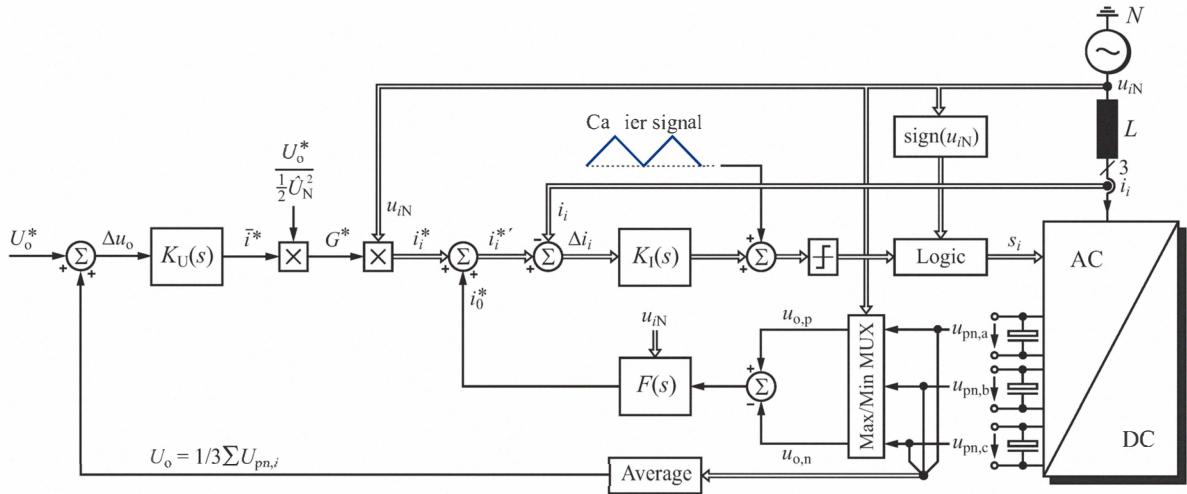
**Fig. 6.** **a)** Basic structure of the Y-rectifier. **b)** Equivalent circuit of the ac system part without the EMI input filter.

a fixed star-point for the same ripple amplitude. This advantage is gained at the expense of a CM voltage  $u_{N'N}$  of the modules, which requires an appropriate CM filter.

As clearly shown by **Fig. 6(b)** and with regard to the fundamental of the input voltage required for the impression of the input current, the same conditions are present for the phase modules as for single-phase PFC rectifiers supplied from a mains phase. Therefore, despite the high peak value of the line-to-line voltage of the European low-voltage grid ( $\hat{U}_{N,II} = 565$  V and/or  $U_{N,II,rms} = 400$  V), the output



**Fig. 7.** **a)** Time behavior of the instantaneous fundamental power of the phases of a Y-rectifier. **b)** Redundant switching states concerning the resulting variation of the phase currents for  $i_a > 0, i_b < 0, i_c < 0$  [valid within  $\varphi_N = (-30^\circ, +30^\circ)$ ], which can be used for balancing the dc output voltages  $u_{pn,a}, u_{pn,b}, u_{pn,c}$  of the phase modules.



**Fig. 8.** Structure of the Y-rectifier control: superimposed control of the average value of the dc output voltages  $u_{pn,a}$ ,  $u_{pn,b}$ ,  $u_{pn,c}$  of the phase modules with subordinate control of the phase currents and 2-out-of-3 balancing of the dc output voltages of the phase modules. Equal signal paths of all phases are represented by double lines. The dependence of the formation of the voltages  $u_{iN'}$  on the sign of the respective phase currents  $i_i$  is considered by an inversion of the switching signals for negative phase currents.

voltage of the phase modules can be selected e.g. at  $U_{pn,i} = 400$  V and/or the power transistors may be realized with 600 V superjunction power MOSFETs.

The control structure of the system is shown in **Fig. 8**. The reference conductance  $G^*$  is defined by the output voltage controller  $K_U(s)$ . Multiplication of  $G^*$  by the normalized mains phase voltages leads to the phase current reference values  $i_i^*$  to be set by the subordinate current controllers  $K_I(s)$ . With regard to the fundamental input current, the system thus behaves as a symmetrical ohmic load with resistances  $R = 1/G^*$  in star-connection. Accordingly, for asymmetrical mains, there occurs in a phase with lower voltage a lower current amplitude, or a reduced supply of power to the respective output. This must be considered for setting the reference value of a downstream dc–dc converter.

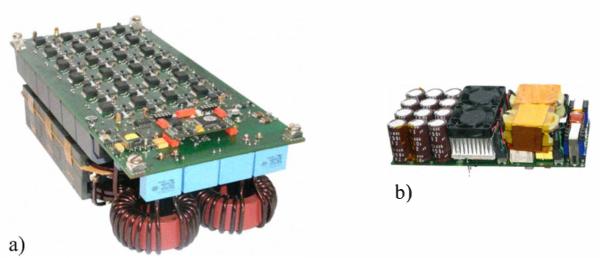
Because of the phase-modular structure, three output voltages are to be regulated. Therefore, the voltage control is split into two parts. On the one hand, the power drawn from the mains, i.e.  $G^*$  is defined from the average control error of the three output voltages  $u_{pn,i}$ . On the other hand, a balancing of the output voltages is implemented, whereby in each case only the phase with the highest positive and the highest negative voltage value is taken into account [25], [28], [29]. As shown in **Fig. 7**, only for these phases, e.g.  $a$  and  $c$ , a higher instantaneous output power flow is present and hence the possibility of changing the output voltage value. Dependent on the difference between  $U_{pn,a}$  and  $U_{pn,c}$ , an offset of the reference phase current values  $i_0^*$  is formed which, however, cannot be set by the phase current controllers because of the free star-point  $N'$ ,  $i_a + i_b + i_c = 0$  is unalterable. The phase currents thus keep their sinusoidal shape and the symmetry to the time axis. However, as could be shown by a more detailed analysis, for  $i_0^* > 0$ , the switching state (100) is mainly used instead of (011) for the formation of the voltages  $u_{iN'}$  required for current impression. Similarly, for  $i_0^* < 0$  increasingly (011) is employed instead of (100). Both switching states are redundant with respect to the voltage formation and result in equal voltages  $u_{\bar{a}\bar{b}}$ ,  $u_{\bar{b}\bar{c}}$ ,  $u_{\bar{c}\bar{a}}$ . However, for (100), primarily the output capacitor  $C_c$  is charged and for (011) the capacitor  $C_a$  and thus an equalization of  $U_{pn,a}$  and  $U_{pn,c}$  is enabled. For (100), power also flows to output  $u_{pn,b}$ , but because of the low instantaneous value of  $i_b$  in  $\varphi_N = \omega_N t = (0, 60^\circ)$  and/or the associated low output current, the output voltage  $u_{pn,b}$  is not significantly changed [29].

In connection with the balancing of the output voltages it should be pointed out that a symmetrical mains current system can be surprisingly also maintained for unequal distribution of the input power to the three outputs, i.e. is also possible for asymmetrically loaded outputs.

To summarize, the total power drawn from the three-phase mains is set by  $G^*$  and the distribution of the power to the phases is determined by  $i_0^*$ . Shifting the power between always only two phases has the advantage that the fulfillment of  $i_a + i_b + i_c = 0$  does not need to be specially observed since the third phase can always carry a resulting current. This procedure thus exhibits, compared to alternative concepts [27], a greater stability range and a significantly lower parameter sensitivity or greater robustness.

It should be emphasized that the balancing procedures described may be employed only in the case of a common EMI filter for all phases and/or for a free star-point  $N$ , which allows a variation of  $u_{NN'}$  with switching frequency. Here, the balancing of the output capacitor voltages and not a vanishing (low frequency) voltage difference of  $N'$  from the mains star-point  $N$  is of importance.

For employing individual EMI filters per module, on the other hand, only low frequency potential changes in  $N'$  can occur and the balancing of the phase units can be with reference to the star-point voltage [31]. Alternatively, and/or in addition to balancing,  $N'$  can also be connected to an artificial star-point that is formed by a transformer circuit of low zero sequence impedance and can be loaded with a zero sequence current component occurring in case



**Fig. 9.** Hardware demonstrator of a) an ultra-efficient Y-rectifier phase module (nominal efficiency  $\eta_{\text{nom}} > 99\%$ ) and b) of an ultra-compact Y-rectifier phase module (power density  $\rho > 5 \text{ kW/dm}^3 = 82 \text{ W/in}^3$ ). The nominal output power of both systems is 3.3 kW [30].

of asymmetry [32], [33]. The disadvantage of this concept, basically known from the star-point formation in electrical networks, however, lies in the requirement of an additional inductive component of relatively large volume and weight.

In **Fig. 9(a)**, the demonstrator of a highly compact version of a single-phase bridgeless PFC rectifier system [cf. **Fig. 11(b)**] is shown; **Fig. 9(b)** shows a highly efficient version of the same rectifier topology. Starting from these systems, Y-rectifiers with power densities of up to  $5\text{ kW/dm}^3$  or efficiencies of  $\eta > 99\%$  may be realized.

### B. $\Delta$ -Rectifier

For delta-connection of the PFC rectifier modules [cf. **Fig. 5(b)**], the subsystems are decoupled, in contrast to the star-connection (Y-rectifier). The control can therefore be carried out, individually for each subsystem, in the same way as for single-phase PFC rectifiers. Balancing of the modules with respect to power consumption is of advantage in the sense of symmetrical loading of the mains, but is not absolutely necessary. However, the line-to-line voltage of the mains appears at the input to the modules. Hence, a relatively high output voltage  $U_{pn,i} > \sqrt{2} U_{N,II,\text{rms}}$  (typ.  $U_{pn,i} = 700\text{ V} \dots 800\text{ V}$  for the European low-voltage mains, taking into account voltage tolerances) or a high blocking capability of the power semiconductors has to be provided. Alternatively, the semiconductor blocking voltage stress could be halved by means of a three-level topology. Also a buck converter could be placed in front of each boost converter stage, i.e. in each phase, a buck-boost converter with a common inductor could be implemented. This would allow the output voltage level of the individual modules to be chosen similar as for the Y-rectifier with  $400\text{ V}$  [34]. Then, only the transistors of the buck stage have to be designed for line-to-line voltages. However, an additional power transistor then lies in the current path, which leads to higher conduction losses.

At the input of the rectifier stages of the  $\Delta$ -rectifier modules, for a two-level implementation of the boost output stages, voltages

$$u_{ij} = s_{ij} \text{sign}(i_{ij}) \in (0, +U_{pn,i}, -U_{pn,i}) \quad (5)$$

( $s_{ij}$  designates the switching state of the power transistors  $S_{ij}$ ;  $i, j = \{a, b, c\}$ ) are formed that, apart from the switching state  $s_{ab} = s_{bc} = s_{ca} = 0$ , contain a switching frequency zero sequence voltage component  $u_0$ ,

$$\begin{aligned} u_{\bar{a}b} &= u'_{\bar{a}b} + u_0 \\ u_{\bar{b}c} &= u'_{\bar{b}c} + u_0 \\ u_{\bar{c}a} &= u'_{\bar{c}a} + u_0 . \end{aligned} \quad (6)$$

As can be immediately seen via a delta-star transformation for the formation of the phase currents  $i_i$ , only the voltages  $u'_{\bar{a}b}$ ,  $u'_{\bar{b}c}$ ,  $u'_{\bar{c}a}$ , and/or the equivalent star-point phase voltages

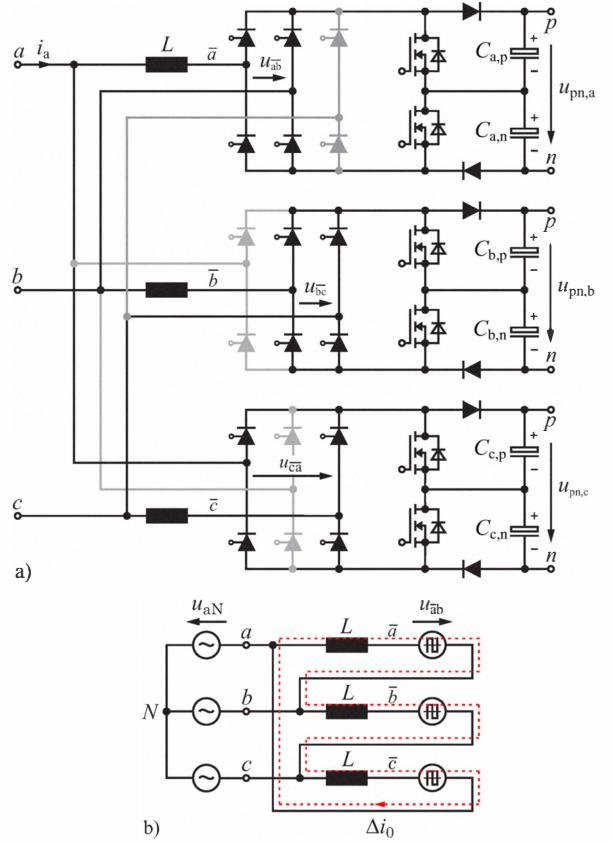
$$\begin{aligned} u'_{aN} &= \frac{1}{3} (u'_{\bar{a}b} - u'_{\bar{c}a}) \\ u'_{bN} &= \frac{1}{3} (u'_{\bar{b}c} - u'_{\bar{a}b}) \\ u'_{cN} &= \frac{1}{3} (u'_{\bar{c}a} - u'_{\bar{b}c}) \end{aligned} \quad (7)$$

with

$$u'_{\bar{a}b} + u'_{\bar{b}c} + u'_{\bar{c}a} = 0 \quad (8)$$

are effective. The zero sequence voltage component

$$u_0 = \frac{1}{3} (u_{\bar{a}b} + u_{\bar{b}c} + u_{\bar{c}a}) , \quad (9)$$



**Fig. 10.** a) Basic structure of the  $\Delta$ -rectifier, with thyristor bridges at the input of the modules to provide the nominal output power in case of phase loss; three-level boost stages are employed to reduce the voltage stress of the power semiconductors. b) Simplified ac side equivalent circuit with the zero sequence component  $\Delta i_0$  of the input current ripples of the modules.

thus drives only a switching-frequency current within the delta-circuit. This means that for a three-phase EMI filter, the modulation is best designed through suitable synchronization of the carrier signals of the modules such that  $u_0$  is maximized or a maximum fraction  $\Delta i_0$  of the switching-frequency input current ripple of the modules is held within the delta circuit [27], [35]. There then results a minimum ripple of the phase currents  $i_i$ , and the EMI filter effort is minimized. However, this advantage should be weighed against full modularity/independence of the subsystems (also regarding switching and modulation), that is obtainable only with the configuration of an individual EMI filter per module.

An essential advantage of the  $\Delta$ -rectifier is the availability of the full rated power even for a failure of one mains phase. For this purpose, the modules must be connected as in **Fig. 10(a)** via three-phase thyristor bridges to the mains, and the thyristor bridges, on interruption of a mains phase, are switched over to the two remaining phases (cf. [27], [34]). However, this concept is applicable only for a suitably high loading capacity of the remaining mains phases.

### C. Discussion

Phase-modular systems allow the knowledge on single-phase PFC rectifier systems to be exploited relatively directly and/or allow for the development of a three-phase PFC rectifier system with low effort. However, this advantage can be realized only with a fully modular structure, i.e. with the arrangement of an individual EMI filter per module, so that the modulation methods for the reduction of ripple in the phase currents described above cannot be used. However, in any

case, a balancing of the modules is required to assure a symmetrical loading of the mains. Here, the additional effort for measurement and signal processing required for the Y-rectifier should be noted.

Basically, due to the modular structure, three individual dc output voltages are formed that only with the aid of downstream isolated dc–dc converters can be employed for the supply of a single load. Furthermore, each module requires filtering of the power flow, which pulsates with twice the mains frequency, i.e. electrolytic capacitors of suitably high capacitance must be provided on the output side. On the other hand, the assurance of a mains-holdup to master the failure of a mains voltage half-cycle anyway requires a relatively high output capacitance. Furthermore, by division of the overall system into three subsystems, a compact construction is supported and the cooling of the power components is simplified.

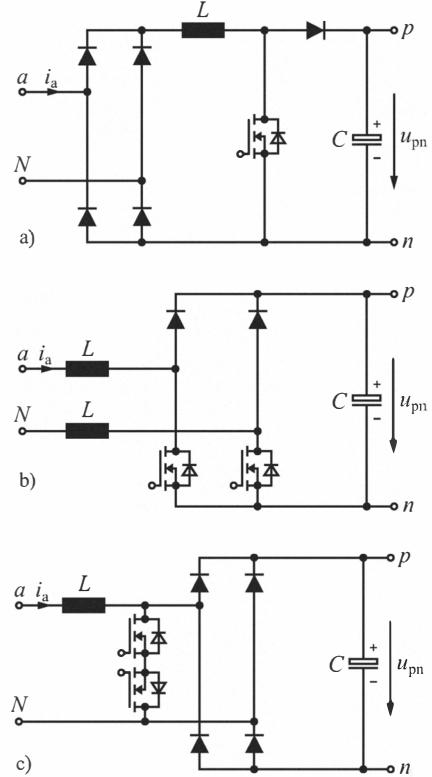
The essential advantage of the Y-rectifier is the lower voltage stress of the power semiconductors or the relatively low level of the output dc voltages. However, a. direct coupling of the phase modules is present, which especially for mastering of a phase failure requires a close co-ordination of the modules and finally a control circuit for the overall system. Hence, the advantage of modularity cannot be used for the control. Industrially, the system will thus probably remain of minor importance. In contrast, the modules of the  $\Delta$ -rectifier work in a decoupled manner, and via a relatively simple expansion of the circuit topology, the full rated power is available on phase failure. The disadvantage of the relatively high output voltage and/or required blocking voltage capability of the power semiconductors in the modules ought to be alleviated in future by the availability of 1200 V SiC power JFETs or SiC power MOSFETs. Then also an additional buck converter stage could be implemented for each module, which enables to maintain the output voltage level given by single-phase PFC systems and therewith the use of already developed dc–dc converter circuits. On the whole, then, an excellent potential for industrial application of this system can be discerned.

#### IV. DIRECT THREE-PHASE PWM RECTIFIER TOPOLOGIES

In the following, the topologies of important direct three-phase boost- and buck-type rectifier systems will be derived and briefly described with regard to their basic function and control. Boost systems will be developed by three-phase extension of known single-phase boost-type PFC circuits (cf. Fig. 11 and/or Fig. 26 in [30]); the circuit structures of the buck-type systems follow by extension of passive three-phase diode rectifiers with turn-off power semiconductors.

In general, the definition of three-phase converter topologies, should be under consideration of a high level of symmetry of the resulting circuit structure. Because of the identical nature of the phases of the supplying mains (pure ac voltages of same shape and amplitude), it is obvious to provide the same structure for the circuit branches connected to the phase terminals (phase symmetry). On the other hand, the symmetry of the positive and negative half-cycles of the ac input phase currents to be impressed by the rectifier system naturally leads to an identical arrangement of power semiconductors in the positive and the negative half of the phase-legs. In connection with the dc voltage to be formed, corresponding topologically to a positive and a negative output terminal, there thus results a three-phase bridge topology with symmetrical positive and negative bridge halves (bridge symmetry). For a dc–dc converter, connected to the rectifier output, this symmetry does not necessarily need to be maintained. Here, a decision could be made e.g. by analysis and comparison of the CM EMI emissions and the conduction losses of a symmetrical or asymmetrical topology.

It should be noted that rectifier systems which violate one or both symmetry requirements, e.g. with the aim of reducing the implementation effort, can also enable the impression of mains ac currents and



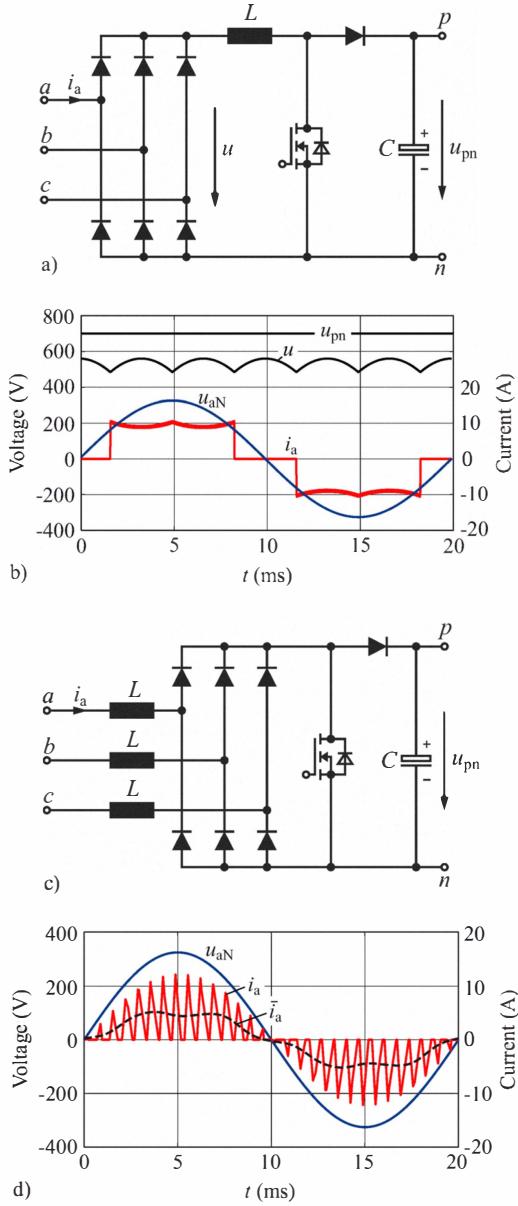
**Fig. 11.** Single-phase boost-type PFC rectifier systems; the three-phase extensions of the circuits leads to direct three-phase hybrid or active PFC rectifier systems with boost-type characteristic. a) Conventional PFC rectifier, b) bridgeless (dual-boost) PFC rectifier, and c) PFC rectifier with ac-switch.

the formation of a regulated output dc voltage. However, a sinusoidal shape of the phase currents is possibly not feasible (cf. Sec. IV-A2 for systems showing phase symmetry but no bridge symmetry), and/or the output voltage or the modulation range of the circuits is limited compared to symmetric structures. Furthermore, in general a more complex modulation results (cf. e.g. [36] as an example of a system with bridge symmetry but no phase symmetry). In addition, with missing phase or bridge symmetry, differing loadings of the individual power semiconductors occur. Asymmetrical circuits are hence treated within the scope of this work only as an intermediate step in the derivation of symmetrical circuits.

In the following for all circuits, i.e. also for systems employing power semiconductors with high blocking voltage stress (defined by the mains line-to-line voltage), power MOSFETs are shown as switching elements. This should point out the generally existing requirement of high switching frequency or high power density. An implementation of the power semiconductors would be possible with Si super-junction MOSFETs with a blocking voltage of 900 V [37] or in future with SiC JFETs (in a cascode configuration, [38]–[40]) or SiC MOSFETs [41]. Alternatively, 1200 V IGBTs, possibly with SiC freewheeling diodes could also be employed, however, with considerably lower switching frequency, due to the relatively high switch-off losses.

##### A. Boost-Type Systems

A three-phase extension of the conventional single-phase boost-type PFC rectifier [cf. Fig. 11(a)], i.e. the addition of a third bridge-leg to the input rectifier bridge, results in a hybrid rectifier structure shown in Fig. 12(a). The system enables a control of the output voltage, but the input current exhibits the characteristic block shape of passive diode rectification with  $\text{THD}_i \approx 30\%$  [cf. Fig. 12(b)].



**Fig. 12.** Three-phase extension of the single-phase system shown in Fig. 11(a). **a)** System structure and **b)** corresponding mains voltage and mains current if the dc-dc boost converter stage operates in Continuous Conduction Mode (CCM). **c)** System structure if the boost inductor is shifted to the ac side and divided over the phases. **d)** Corresponding mains voltage and current ( $\bar{i}_a$  refers to the local average value of the phase current  $i_a$ ) for operation of the system in Discontinuous Conduction Mode (DCM).

If the boost inductance is moved to the ac side and distributed over the phases [cf. Fig. 12(c)] and the mode of operation is changed to DCM at constant duty cycle of the power transistors, the switching frequency peak values of the discontinuous phase currents follow a sinusoidal envelope. However, as shown by more detailed analysis, low-frequency harmonics of the phase currents continue to occur [42]. A modulation of the transistor switch-on time with sixfold mains frequency [43], [44] and/or operation in Boundary Conduction Mode (BCM) also cannot completely eliminate the low-frequency current distortion, since the smallest phase current in each case always reaches zero prior to the other two phase currents and thus exhibits a zero current interval at switching frequency [42]. Accordingly, a relatively high current quality is only attainable for high voltage transfer ratios and/or a relatively short demagnetization time of the

inductors  $L$  compared to the transistor switch-on time, i.e. for output voltages  $U_{pn} > 1\text{ kV}$  when operating in the European low-voltage mains. Because of this limitation, and the high peak current loading of the power semiconductors and the large EMI filter effort, this circuit concept has not been successful in industry.

Fundamentally, it should also be noted here that for three-phase converter systems, because of the relatively high power, operation in CCM is clearly preferable. Accordingly, the phase-shifted operation of several DCM converter stages, which would be possible for the system shown in Fig. 12(c), [45], [46], and is frequently used for single-phase systems (for power levels up to typ. 1 kW) is of minor importance.

### 1) Hybrid 3<sup>rd</sup> Harmonic Current Injection PFC Rectifier:

An improvement in the input current quality of the circuit in Fig. 12(a) is only possible by extension of the controllability, i.e. by addition of a further power transistor (cf. Fig. 13). The currents in the positive and negative dc buses,  $i_+$  and  $i_-$ , can then be controlled independently and proportional to the two phase voltages involved in each case in the formation of the output voltage of the diode bridge. If the difference of  $i_+$  and  $i_-$  is then fed back via a current injection network (three four-quadrant switches, of which in each case only one is switched on) into the mains phase which would not carry current for simple diode rectification, a sinusoidal current shape can be assured for all mains phases as shown below [47].

Because of the symmetries of the supplying mains voltage system, the mathematical proof of the sinusoidal current shaping can be limited to a 60°-wide interval of the mains period with e.g.  $u_{aN} > u_{bN} > u_{cN}$ , for which the injection switch  $S_{bYb}$  (in general, the injection switch of the phase with the smallest absolute voltage value) is continuously switched on.

By suitable modulation of  $S_+$ , a current proportional to the mains phase voltage  $u_{aN}$  can then be impressed in  $L_+$  or in the conducting diode  $D_{a+}$ ,

$$i_+ = \bar{i}_a, \quad (10)$$

whereby for the local average, i.e. the fundamental frequency component

$$\bar{i}_a = G^* u_{aN} \quad (11)$$

has to apply. Correspondingly, by suitable modulation of  $S_-$ , a current

$$-i_- = \bar{i}_c \quad (12)$$

proportional to  $u_{cN}$  can be impressed in  $L_-$  or  $D_{c-}$  with

$$\bar{i}_c = G^* u_{cN}. \quad (13)$$

The fundamental frequency conductance  $G^*$ , determining the rectifier input and/or power, is thereby defined by the output voltage controller. The switching of  $S_+$  and  $S_-$  must not be carried out in a co-ordinated manner since freewheeling of  $i_+$  and/or  $i_-$  is always possible via the freewheeling diodes  $D_+$  and  $D_-$  or the diodes antiparallel to  $S_+$  and  $S_-$  and the injection switch  $S_{bYb}$ .

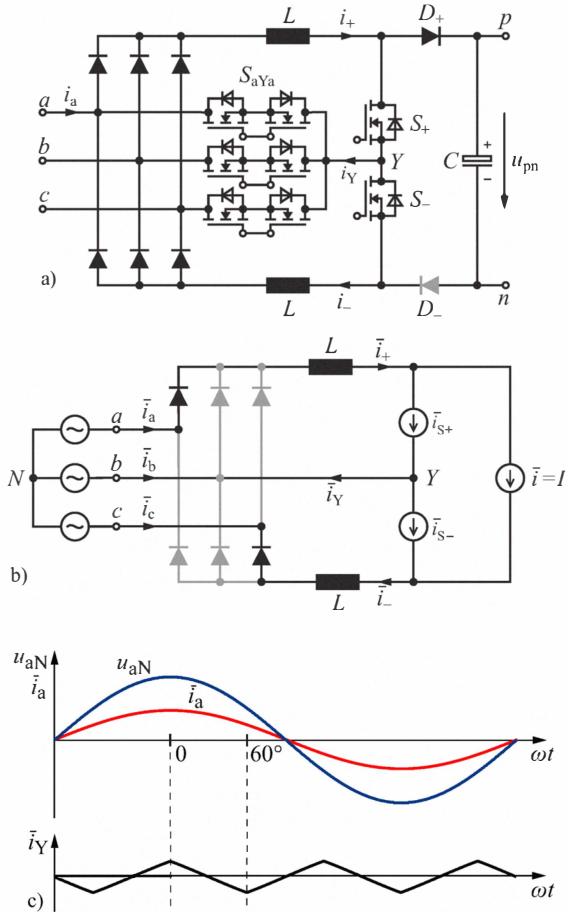
For the injection current  $i_Y$  follows by Kirchhoff's current law  $i_+ - i_- - i_Y = 0$  or  $i_a + i_c - i_Y = 0$ , and on consideration of  $i_b = -i_Y$  (injection switch  $S_{bYb}$  is switched on)

$$i_b = -(i_a + i_c) \quad \text{and} \quad \bar{i}_b = -(\bar{i}_a + \bar{i}_c). \quad (14)$$

With (11), (12) and  $u_{a0} + u_{b0} + u_{c0} = 0$  (symmetrical sinusoidal mains phase voltages) there then results

$$\bar{i}_b = -G^* (u_{aN} + u_{bN}) = G^* u_{bN}. \quad (15)$$

Accordingly, for all phases a current shape proportional to the corresponding mains phase voltage is achieved. (Equation (14) could also



**Fig. 13.** a) Basic structure of the hybrid 3<sup>rd</sup> harmonic current injection rectifier [47]. b) Local average equivalent circuit of the active system part for  $u_{aN} > u_{bN} > u_{cN}$ . c) Waveforms of the phase voltage  $u_{aN}$ , the corresponding phase current  $i_a$ , and the injected current  $\bar{i}_Y$ . It would be advantageous to add a second freewheeling diode  $D_-$  in the negative bus to minimize the switching frequency CM voltage variation of the output. However, this would result in increased conduction losses.

be stated directly with reference to the current sum  $i_a + i_b + i_c = 0$  forced to zero because of the free mains star-point N, but was derived here starting from the dc side in order to illustrate the function of the current injection.)

As would be clear from an analysis of further  $60^\circ$  sections of the mains period, the injection current  $i_Y$  exhibits threefold mains frequency. Thus, and in the sense of the classification chosen here, the rectifier system should be called *hybrid 3<sup>rd</sup> harmonic current injection PFC rectifier*.

The feedback and/or injection of current occurs in **Fig. 13** always into only one phase, which is selected by proper gating of the four-quadrant injection switches. Alternatively, the current injection could also be carried out by means of a purely passive injection network, e.g. a resonance network or a transformer circuit with low zero sequence impedance (cf. MINNESOTA Rectifier, [48]). However, it can then not be chosen in which phase a current is injected, but the feedback current can only be divided up into equal parts that are then injected into the phases. As shown in [4], a sinusoidal phase current waveform proportional to the mains voltage can also be attained therewith. However, the passive injection network shows a relatively large volume and weight. Furthermore, in comparison to the circuit in **Fig. 13(a)** a threefold amplitude of the injection current is required, so that the semiconductors of the converter stages that impress the

currents  $i_+$  and  $i_-$  must be dimensioned for a significantly higher current loading. Hence, considering the high power density often demanded in industry, an active current injection is clearly preferable.

With regard to the operating range of the system it must be stated that the output voltage must be selected significantly higher than the peak value of the line-to-line mains voltage, i.e. as  $U_{pn} > \sqrt{6} U_{N,1l,rms}$  as given in [49], p. 595, Sec. II-D. As shown above, ohmic fundamental mains behavior can be attained, but no phase displacement of the mains current relative to the mains voltage is possible. However, it has to be emphasized that the system allows a continuation of operation with sinusoidal current shape (at reduced power) on failure of a mains phase. All injection switches then have to be blocked and a simultaneous gating of  $S_+$  and  $S_-$  provided, so that the same conditions exist as for a single-phase PFC rectifier system operating on a mains line-to-line voltage.

#### Hybrid 3<sup>rd</sup> Harmonic Current Injection Active-Filter Rectifier:

Starting from **Fig. 13(a)** and following a circuit concept known from passive injection networks [11], [50], the two inductors  $L_+$  and  $L_-$  could be lumped together into a single inductor  $L_Y$  lying in the injection path. The resulting circuit structure is shown in **Fig. 14**, [13], [14]. The output diodes  $D_+$  and  $D_-$  can now be omitted, since a simultaneous switching on of the transistors  $S_+$  or  $S_-$  would lead to a short-circuiting of the mains, in contrast to **Fig. 13**, and is thus not allowed.

Accordingly, the system shows a relatively low implementation effort, however, at the expense of a missing output voltage control. As can be immediately seen from the absence of diodes  $D_+$  and  $D_-$ , the output voltage is now determined directly by the diode bridge and hence exhibits a six-pulse shape. However, as will be shown below, assuming a constant power load, the possibility of impressing sinusoidal mains phase currents remains. Thus the system does not provide the full functionality of an output voltage-regulated PFC rectifier, but the function of a passive rectifier with integrated active filter and hence should be called a *hybrid 3<sup>rd</sup> harmonic current injection active-filter rectifier*.

If a load with constant power consumption is supplied, there results a load current varying in antiphase to the six-pulse rectifier output voltage. As shown below, this leads to a sinusoidal shape of all mains phase currents after overlaying with the injection current.

Consider a  $60^\circ$  interval of the mains period with  $u_{aN} > u_{bN} > u_{cN}$  as in **Sec. IV-A1**. For the current to be injected into phase b

$$\bar{i}_Y = -\bar{i}_b = -G^* u_{bN} \quad (16)$$

applies. The mains frequency voltage drop across the inductor  $L_Y$  can in a first approximation be neglected for the formation of  $\bar{i}_Y$ ,

$$\bar{u}_{LY} = 0 . \quad (17)$$

Accordingly, we have for the voltage to be formed at the output of the bridge-leg

$$\bar{u}_{YN} = \bar{u}_{bN} . \quad (18)$$

If in any case one of the transistors  $S_+$  or  $S_-$  is switched on,  $\alpha_+ + \alpha_- = 1$  applies for the relative switch-on times or  $\alpha_- = 1 - \alpha_+$  and hence, for the voltage formation of the bridge-leg

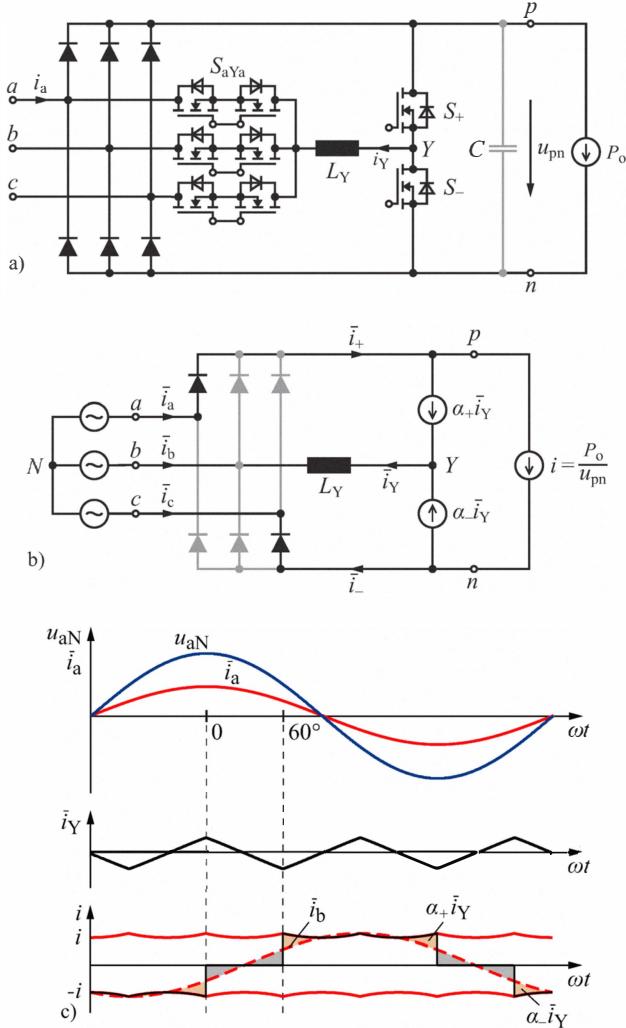
$$\bar{u}_{LY} = \alpha_+ u_{aN} + (1 - \alpha_+) u_{cN} = \alpha_+ u_{ac} + u_{cN} . \quad (19)$$

Correspondingly, there follows the duty cycle  $\alpha_+$  with (19) as

$$\alpha_+ = \frac{u_{bc}}{u_{ac}} \quad (20)$$

and thus for the current in  $S_+$

$$\bar{i}_{S+} = \alpha_+ i_Y = -\alpha_+ i_b = -\alpha_+ G^* u_{bN} = -G^* u_{bN} \frac{u_{bc}}{u_{ac}} . \quad (21)$$



**Fig. 14.** a) Hybrid 3<sup>rd</sup> harmonic current injection active filter rectifier according to [4], [14]. b) Local average equivalent circuit of the active part of the system for  $u_{aN} > u_{bN} > u_{cN}$ . c) Waveform of the phase voltage  $u_{aN}$ , the phase current  $\bar{i}_a$ , the injection current  $\bar{i}_Y$ , and the load current  $i = P_o/u_{pn}$  at a constant output power  $P_o$ .

Considering the fundamental input currents that have to be generated at the input

$$\begin{aligned}\bar{i}_a &= G^* u_{aN} \\ \bar{i}_b &= G^* u_{bN} , \\ \bar{i}_c &= G^* u_{cN}\end{aligned}\quad (22)$$

the low frequency component of the current consumption of the constant power load can be expressed via

$$i = \frac{P_o}{u_{ac}} = \frac{\bar{i}_a u_{ac} + \bar{i}_b u_{bc}}{u_{ac}} = G^* \frac{u_{aN} u_{ac} + u_{bN} u_{bc}}{u_{ac}} \quad (23)$$

$$= G^* \left( u_{aN} + u_{bN} \frac{u_{bc}}{u_{ac}} \right) . \quad (24)$$

For the resultant low frequency current component drawn from phase  $a$ , there then follows with (21)

$$\bar{i}_a = i - \bar{i}_{S+} = G^* u_{aN} \quad (25)$$

directly the desired (sinusoidal) waveform proportional to the mains voltage. Furthermore, there applies with (16), (25),

$$i_a + i_b + i_c = 0 , \quad (26)$$

and  $u_{aN} + u_{bN} + u_{cN} = 0$  for phase  $c$

$$\bar{i}_c = G^* u_{cN} , \quad (27)$$

so that the sinusoidal shape of all phase currents has been proved.

It must be emphasized that the circuit in Fig. 14(a) allows a sinusoidal regulation of the mains currents only in case a converter output stage, e.g. in the form of a dc-dc converter or a PWM inverter stage, is present that assures constant power consumption. The implementation effort of this concept should therefore be evaluated only with regard to the overall system.

Furthermore, it should be noted that the waveform of  $i$  required for the formation of a sinusoidal mains current only results if no smoothing capacitor (of higher capacitance) is connected between constant power load and rectifier stage. Load variations are thus passed on directly to the mains.

### 2) $\Delta$ -Switch Rectifier:

If the circuit in Fig. 11(c) is extended with a third bridge-leg and a delta-connection of four-quadrant switches is added with respect to the operating principle and the three-phase symmetry, there follows the topology in Fig. 15(a) of the  $\Delta$ -switch rectifier [51]–[53]. The four quadrant switches enable to influence the conduction state of the diode rectifier and thus to control the ac side voltage formation via pulse width modulation. The  $\Delta$ -switch rectifier is an active PFC rectifier circuit since the commutation of the diode bridge occurs, in contrast to the circuit in Fig. 13, at switching frequency.

Similar to single-phase PFC rectifier circuits, the voltage formed at the input of a rectifier bridge-leg, e.g.  $\bar{u}_{\bar{a}M'}$  ( $M'$  designates a virtual mid-point of the output voltage), depends on the switching state of the (entire) converter and on the direction of the phase current  $i_a$ . This does not represent a limitation since a current  $i_a$  in phase with the mains voltage  $u_{aN}$  has to be impressed. Neglecting the voltage drop across the input inductor  $u_{aN} \approx \bar{u}_{\bar{a}N}$  has to be ensured. Therewith,  $i_{\bar{a}} = G^* u_{aN}$  and  $\bar{u}_{\bar{a}N}$  always have the same polarity.

Except for a simultaneous switch on of all four-quadrant switches ( $s_{\bar{a}\bar{b}} = s_{\bar{b}\bar{c}} = s_{\bar{c}\bar{a}} = 1$ ), one phase terminal, e.g.  $\bar{a}$ , is always connected with the positive or negative output voltage bus,  $p$  or  $n$ . Accordingly, the circuit shows a two-level characteristic with regard to the voltage formation. As is immediately clear considering the diode rectification on the input side, the output voltage has to be selected according to

$$U_{pn} > \sqrt{2} U_{N, ll, rms} . \quad (28)$$

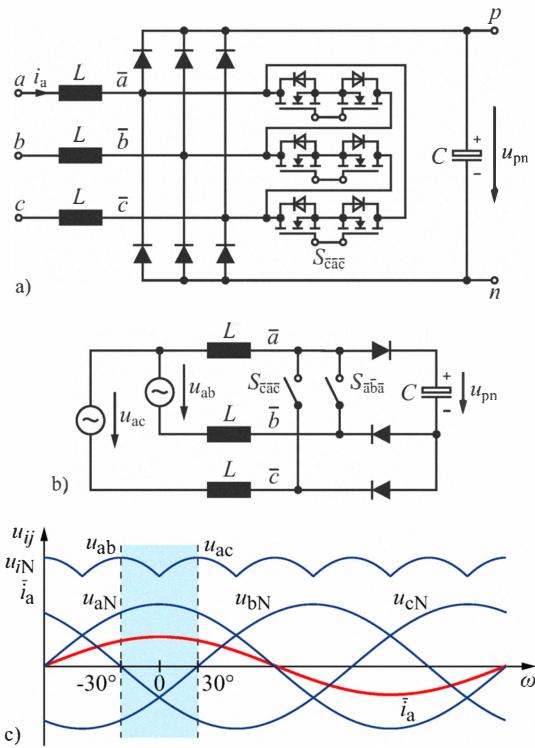
In case of a failure of a mains phase, the two four-quadrant switches associated to the phase that failed have to be permanently disabled. Then again a single-phase PFC rectifier circuit with an ac side switch is present, which operates however from a line-to-line voltage, but still allows a regulation of the output voltage and a sinusoidal impression of the mains currents.

It is interesting to understand that the operating range of the  $\Delta$ -switch rectifier is not restricted to ohmic fundamental mains behavior (as could be expected due to the diode rectifier) but allows the formation of current phase displacements in the angular interval

$$\Phi = (-30^\circ, +30^\circ) . \quad (29)$$

This can be clarified by a more detailed analysis of the conduction states of the system, which may be restricted to a  $60^\circ$  interval due to the symmetry of the three-phase mains system. The equivalent circuit of the active part of the  $\Delta$ -switch rectifier is shown in Fig. 15(b) for  $i_a > 0, i_b < 0, i_c < 0$ . It is assumed that only the four-quadrant switches connected to the phase with the largest absolute voltage value is switched [52].

For the impression of  $i_b$  and  $i_c$ ,  $S_{\bar{a}\bar{b}}$  and  $S_{\bar{a}\bar{c}}$  are switched such that  $\bar{u}_{\bar{a}\bar{c}}$  and  $\bar{u}_{\bar{a}\bar{b}}$  compensate the line-to-line voltages  $u_{ac} > 0$  and  $u_{ab} >$



**Fig. 15.** a) Circuit topology of the  $\Delta$ -switch rectifier [51]. Also a bridge configuration of six transistors with antiparallel diodes and short-circuited output terminals could be used instead of a delta-connection of four-quadrant switches. b) Equivalent circuit of the system for  $i_a > 0$ ,  $i_b < 0$ ,  $i_c < 0$ , i.e. for  $\varphi_N = (-30^\circ, +30^\circ)$ . c) Waveforms of the mains phase voltages, local average phase current  $\bar{i}_a$ , and sections of the line-to-line voltages.

0. The voltages  $\bar{u}_{\bar{a}\bar{c}}$  and  $\bar{u}_{\bar{a}\bar{b}}$  can be formed for the given polarities of the currents. However, as a result of the phase displacement between the phase quantities and the line-to-line quantities of  $\pm 30^\circ$  (compare e.g.  $u_{aN}$  and  $u_{ab}$  or  $u_{aN}$  and  $u_{ac}$ )  $u_{ac} > 0$  and  $u_{ab} > 0$  applies, not only for  $\varphi_N = (-30^\circ, 30^\circ)$  but also for  $\varphi_N = (-60^\circ, 60^\circ)$ . Therewith, the balance of the voltages  $u_{ac} \approx \bar{u}_{\bar{a}\bar{c}} > 0$  and  $u_{ab} \approx \bar{u}_{\bar{a}\bar{b}} > 0$  can be also achieved for phase voltages with a displacement of  $\pm 30^\circ$  against the phase current system.

It is advantageous to use the circuit in Fig. 16 for the control of the system. There, all phase currents are continuously controlled opposed to alternative control concepts [54]. The voltage reference values formed at the output of the phase current controllers are converted with a Y- $\Delta$  transformation into the effectively adjustable line-to-line voltage reference values

$$\begin{aligned} u_{\bar{a}\bar{b}}^* &= u_{\bar{a}N}^* - u_{\bar{b}N}^* \\ u_{\bar{b}\bar{c}}^* &= u_{\bar{b}N}^* - u_{\bar{c}N}^* . \\ u_{\bar{c}\bar{a}}^* &= u_{\bar{c}N}^* - u_{\bar{a}N}^* \end{aligned} \quad (30)$$

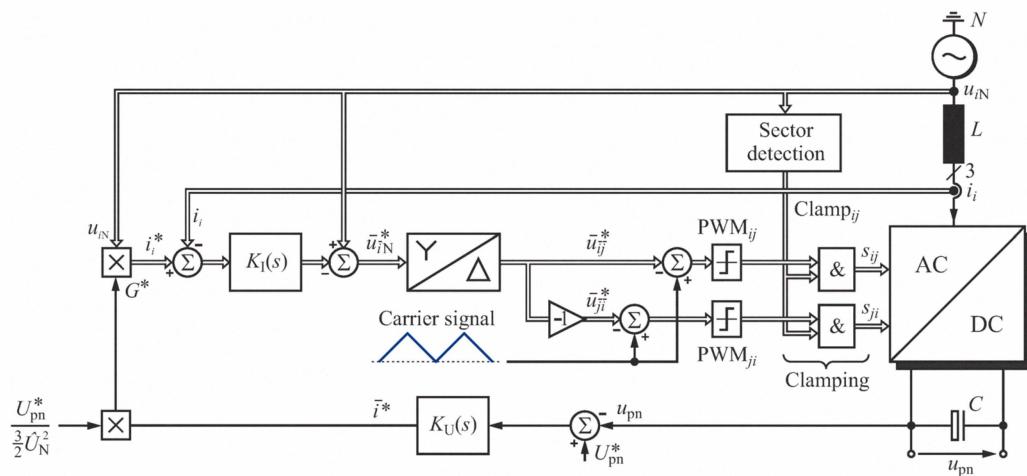
The polarity of the phase currents or phase voltages, i.e. the information of the actual  $60^\circ$  sector of the mains period has then to be considered for the control of the individual power transistors, however, no sector dependent switch-over of the entire control structure is required. This results in a higher input current quality as a switch-over of the control, potentially causes current distortions at the switching instants.

### 3) VIENNA Rectifier:

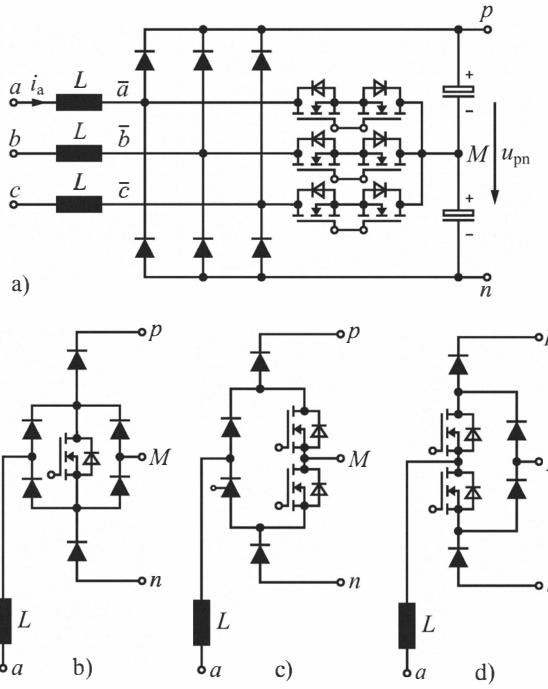
If the delta( $\Delta$ )-connection of the four-quadrant control switches of the  $\Delta$ -switch rectifier is replaced by a star-connection, and the star-point of the switch arrangement is connected to a capacitively formed mid-point  $M$  of the output voltage in terms of highest possible symmetry, an active three-level PWM rectifier system (cf. Fig. 17(a), [42], [55]), known as VIENNA Rectifier, results. Functionally equivalent alternative implementations of the bridge-leg structure with a lower blocking voltage stress of the power diodes are depicted in Figs. 17(b)-(d) [55]–[57].

As for the  $\Delta$ -switch rectifier, the ac side voltage formation of the system is again dependent on the sign of the phase currents. However, the rectifier phase input, e.g.  $\bar{a}$ , now can be also connected to the midpoint  $M$  of the output voltage besides the positive and the negative output voltage bus. Thus, three voltage levels are available for the formation of  $\bar{u}_{\bar{a}M}$ , which justifies the designation of the system as a three-level converter.

A major advantage of the three-level characteristic is that for the selection of the blocking voltage capability of the power transistor only half of the peak value of the line-to-line voltage and not the total value is relevant. Furthermore, as a result of the higher number of levels of  $\bar{u}_{aM}$ , the difference  $u_{aN} - u_{aN}$  remains limited to small values. Thus a smaller mains current fundamental ripple results [cf.



**Fig. 16.** Control scheme of the  $\Delta$ -switch rectifier with superimposed output voltage controller  $K_U(s)$  and subordinate input current controllers  $K_I(s)$  with feed-forward of the mains phase voltages  $u_{iN}$ . The rectifier input phase voltage reference values generated by the phase current controllers are converted into line-to-line voltage reference values by using a Y- $\Delta$ -transformation and then applied to the system by modulation of always only two of the four-quadrant switches  $S_{\bar{a}\bar{b}\bar{a}}, S_{\bar{b}\bar{c}\bar{b}}, S_{\bar{c}\bar{a}\bar{c}}$  [cf. Fig. 15(e)].



**Fig. 17.** a) Circuit topology of the original VIENNA Rectifier [42]. b-d) Alternative bridge-leg structures, whereas the bridge-leg variant b) requires only three transistors but shows higher conduction losses due to the series-connected diodes [55]; c) [56] is advantageous concerning precharging the output capacitor at start-up [55] (after the precharge interval the thyristor is gated, thus a parallel path with precharging resistor and series diode is bypassed); d) [57] allows a further reduction of the conduction losses compared to the topology in c).

(2)], and/or the value of the input (boost) inductances can be reduced. In addition, as a result of the lower switched voltage also a lower conducted EMI noise level is generated.

In analogy to the  $\Delta$ -switch rectifier,

$$U_{pn} > \sqrt{2} U_{N,1l,rms} \quad (31)$$

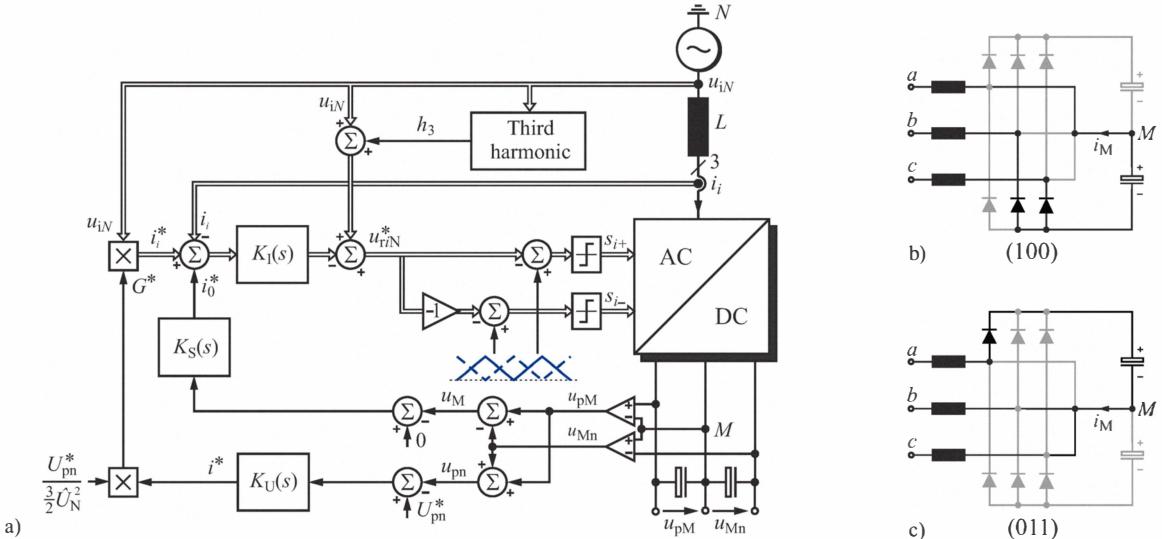
applies for the output voltage range of the system and

$$\Phi = (-30^\circ, +30^\circ) \quad (32)$$

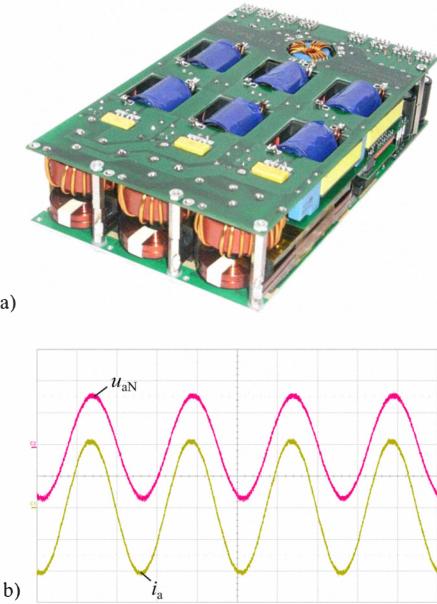
for the phase displacement range of the mains voltage and the mains current fundamental in case a high output voltage  $U_{pn} > 2\sqrt{2} U_{N,1l,rms}$  and a small boost inductance are assumed. The phase displacement range is increasingly reduced to pure ohmic mains behavior ( $\Phi = 0$ ) [53], [55] for lower output voltage values, i.e. for  $\sqrt{2} U_{N,1l,rms} < U_{pn} < 2\sqrt{2} U_{N,1l,rms}$ . Similar to the  $\Delta$ -switch rectifier in case of a phase loss, also the VIENNA Rectifier can still be operated at a reduced output power and at the same output voltage and with sinusoidal input currents in the remaining phases [58]–[60].

The control structure of the system is shown in **Fig. 18(a)** with a superimposed voltage controller, defining the reference value of the fundamental frequency conductance  $G^*$  and/or the power delivered to the output, and subordinate phase current controllers. Simple P-type controllers can be used if feed-forward of the mains voltages is applied. The balancing of the two partial output voltages, which is required due to the integration of the capacitive mid-point of the output voltage into the system function, can be implemented in a similar manner as shown for the Y-rectifier (cf. **Sec. III-A**), i.e. by adding an offset  $i_0^*$  of the phase current reference values. The reason for this is that the system, shown in **Figs. 18(b)** and **(c)** for  $i_a > 0$  and,  $i_b, i_c < 0$ , has redundant switching states (100) and (011) regarding the voltage formation on the ac side. A positive offset  $i_0^* > 0$  leads to an increase of the relative on-time of (100) compared with (011) and a negative offset  $i_0^* < 0$  to a relative decrease compared with (100). Correspondingly, mainly the lower or upper output capacitor is charged.

The output voltages of the system can be loaded asymmetrically, as was shown in the analysis in [61]. However, the admissible degree of asymmetry depends on the mains voltage level. High degrees of asymmetry are only possible for high output voltages.



**Fig. 18.** a) Basic structure of the control of the VIENNA Rectifier with superimposed control of the output voltages  $u_{pM}$ ,  $u_{Mn}$  and subordinate phase current control with feed-forward of the phase (mains) voltages. In order to increase the output voltage control range, a third harmonic of the mains frequency is superimposed to the mains voltage feed-forward signal [25]. The balancing of the two output voltages is achieved by adding an offset  $i_0^*$  to the phase current reference values. b) and c) Redundant switching states of the system (for  $i_a > 0$ ,  $i_b, i_c < 0$ ) that result in equal rectifier input line-to-line voltages and opposite signs of  $i_M$  and therefore facilitate a balancing of the output capacitor voltages without influence on the phase current shaping. (E.g. for  $i_0^* > 0$ , the relative on-time of the switching state (100) is increased and the on-time of the switching state (011) is reduced resulting in  $\bar{i}_M < 0$ ; correspondingly  $i_0^* < 0$  results in  $\bar{i}_M > 0$ . The switching state is represented by phase switching functions  $s_i$ , and/or  $(s_a, s_b, s_c)$ , where  $s_i = 1$  ( $i = \{a, b, c\}$ ) indicates that the corresponding four-quadrant switch is switched-on and  $s_i = 0$  that it is switched-off.



**Fig. 19.** a) Hardware demonstrator of a 10 kW VIENNA Rectifier. b) Measured phase current  $i_a$  ( $\text{THD}_i = 1.6\%$ ) and corresponding mains phase voltage  $u_{AN}$ . Operating parameters: mains rms line-to-line voltage  $U_{N,1l,\text{rms}} = 400 \text{ V}$ , mains frequency  $f_N = 800 \text{ Hz}$ , output voltage  $U_{pn} = 800 \text{ V}$ , switching frequency  $f_P = 250 \text{ kHz}$ . Scales: 200 V/div, 10 A/div, 0.5 ms/div.

A state-of-the-art hardware demonstrator of the VIENNA Rectifier is shown in **Fig. 19**. The switching frequency of the system is  $f_P = 250 \text{ kHz}$ . Such a high switching frequency, however, is only useful if an extremely low  $\text{THD}_i$  of the input currents has to be achieved at high mains frequencies (e.g. for More Electric Aircraft [53],  $f_N = 360 \text{ Hz} \dots 800 \text{ Hz}$ ). No advantage is given with regard to power density compared to a system with  $f_P = 72 \text{ kHz}$  for forced air cooling (cf. **Fig. 35**).

#### 4) Hybrid Half-Controlled / Active Full-Controlled Six-Switch PFC AC/DC Bridge Circuit:

If instead of the conventional single-phase PFC rectifier structure bridgeless (or dual-boost) converter topology in **Fig. 11(b)** is extended to three-phases, a half-controlled hybrid phase-symmetrical rectifier circuits shown in **Fig. 20(a)** results.

This circuit topology does not allow to impress a sinusoidal input current within the entire mains period because of the lack of bridge-symmetry. If, e.g. a  $60^\circ$  interval with  $u_{AN} > 0$  and  $u_{BN}, u_{CN} < 0$ , i.e. an angular interval  $\varphi_N = (-30^\circ, 30^\circ)$  of the mains period is considered [cf. **Fig. 21(a)**] and phase currents with identical signs as the corresponding mains phase voltage are assumed, only the switching-off of  $S_{\bar{a}n}$  would cause a commutation of  $i_a$  to  $D_{\bar{a}p}$ . In the phases  $b$  and  $c$ , the anti-parallel diodes  $D_{\bar{b}n}$  and  $D_{\bar{c}n}$  would remain conductive, independent of the switching state of the transistors  $S_{\bar{b}n}$  and  $S_{\bar{c}n}$ .

Therefore, sinusoidal current impression is possible only for those  $60^\circ$  intervals in which two mains phase voltages have a positive sign, thus when e.g.  $u_a, u_b > 0, u_c < 0$ , or  $i_{\bar{a}}, i_{\bar{b}} > 0, i_{\bar{c}} < 0$  applies [cf.  $\varphi_N = (30^\circ, 90^\circ)$ , **Fig. 21(c)**]. By switching on  $S_{\bar{n}\bar{a}}$  or  $S_{\bar{n}\bar{b}}$ ,  $\bar{a}$  or  $\bar{b}$  can then be connected to the negative output voltage bus  $n$  and  $i_a$  or  $i_b$  increased. At the switch-off of  $S_{\bar{N}\bar{a}}$  or  $S_{\bar{N}\bar{b}}$ , the corresponding freewheeling diode  $D_{\bar{a}p}$  or  $D_{\bar{b}p}$  becomes conducting. Thus, a positive potential is applied to  $\bar{a}$  or  $\bar{b}$ , and the corresponding phase currents are reduced. Therewith, either an increase or decrease of two phase currents and consequently a sinusoidal current waveform is achievable. The third phase current then also shows a sinusoidal shape as a result of  $i_a + i_b + i_c = 0$ .

In summary, a sinusoidal current shape can be achieved only in sections of the mains period. The function of the circuit is hence essentially limited to output voltage regulation, whereby by using the simple control procedure described in [62], at least a block-shaped current waveform, comparable to passive rectifiers, may be realized.

It should be noted that to simplify matters, all transistors could also be switched synchronously with a duty cycle constant over the mains period and the system operated in DCM. The input current shape would then be identical to that in **Fig. 12(d)**. As an advantage, lower conduction losses would occur but at the cost of a higher implementation effort.

Voltage regulation and sinusoidal current impression requires an extension of the circuit in **Fig. 20(a)** to bridge symmetry, i.e. the addition of three further transistors antiparallel to the freewheeling diodes of the positive bridge half. There then results the six-switch converter structure shown in **Fig. 20(b)**, which is employed e.g. for supplying of the voltage dc-link of variable speed drives.

Since for a switched on transistor the current in any case flows over this transistor or its antiparallel diode, the system allows, in each phase, a voltage formation independent of the current. At the input of each rectifier bridge-leg, a positive or a negative voltage may be generated referred to the virtual output voltage mid-point. Thus the bridge-legs exhibit a two-level characteristic and hence allow the impression of sinusoidal phase currents of any phase displacement relative to the mains voltage. In particular, the current may also be led in antiphase to the mains voltage, i.e. power may be fed back into the mains. This inverter operating mode is e.g. employed in variable speed ac machine drives to feed braking energy back into the mains, and represents the main energy flow direction for supplying an ac machine from a voltage dc-link.

With regard to the level of the output voltage,

$$U_{pn} > \sqrt{2} U_{N,1l,\text{rms}} \quad (33)$$

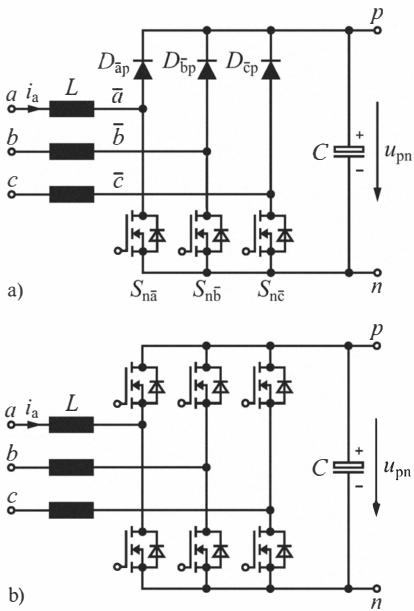
is required, the same as for the systems in **Fig. 15(a)** and **Fig. 17**. Furthermore, the system can deal with a mains phase failure, thus representing a mains interface that can be used in an extremely flexible manner. Hence the entire circuit structure is also commercially available as a power module (generally denominated as “sixpack” power module) and is widely used in industry.

It should be emphasized that the circuit has a relatively simple structure, despite the high functionality, i.e. in particular, the bidirectionality does not result in an increase in the number of switches compared with the unidirectional structures derived above. This becomes especially clear on using Reverse Conducting (RC)-IGBTs, which apart from the power transistor, also include the antiparallel freewheeling diode in one chip. The same applies (in future) e.g. for SiC JFETs (in cascode connection). The circuit is thus of particular interest, despite the limitation made here to unidirectional systems as the wide phase angle range may be exploited also in the purely rectifier mode, e.g. for reactive power compensation.

#### 5) Discussion:

According to **Sec. IV-A1**, the implementation of a three-phase boost-type PFC rectifier is possible with a current injection concept based on passive diode rectification or, according to **Sec. IV-A2–Sec. IV-A4**, by control of the conduction state of a diode bridge with turn-off power semiconductors, which allows a direct impression of sinusoidal ac currents.

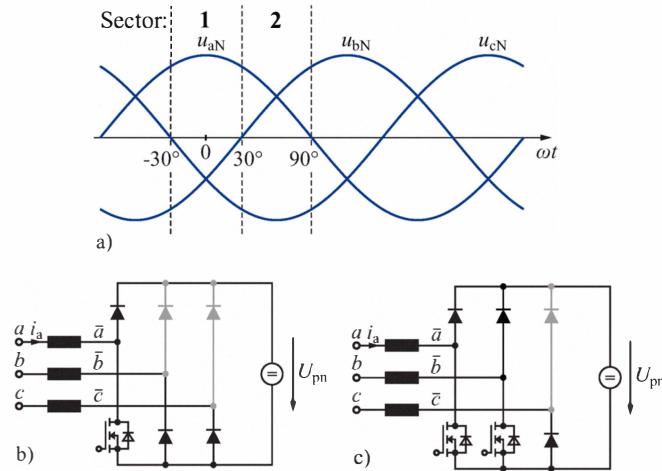
The direct ac current impression is preferable compared with the impression of two dc currents (in combination with a current injection into the third phase) for an industrial system as a switching at the sector borders, potentially causes distortions is not required. In addition, active rectifier systems are not limited to a purely ohmic fundamental mains behavior, therewith e.g. the capacitive reactive



**Fig. 20.** a) Half-controlled (hybrid) boost-type three-phase ac-dc bridge circuit. b) Full-controlled active three-phase ac-dc bridge circuit (bidirectional six-switch active PFC rectifier).

power of the EMI input filter can be (partly) compensated, or in general a higher flexibility for the current control is given.

Thus, for the comparative evaluation in **Sec. VI-C**, only the  $\Delta$ -switch rectifier, the VIENNA Rectifier and the (bidirectional) six-switch boost-type PFC rectifier are considered. The  $\Delta$ -switch rectifier could here be also omitted with regard to the system complexity. Given by its structure, however, the system cannot generate a short-circuit of the output voltage in case of a faulty control of the power transistors. Therewith, an advantage is given regarding the operational safety compared with the six-switch converter. The evaluation of the system furthermore is reasonable in terms of completeness of the analysis.



**Fig. 21.** a) Time behavior of the phase voltages within a mains period. b) Active part of the system for sector 1 (\$u\_{aN} > 0, u\_{bN}, u\_{cN} < 0\$) with the possibility of controlling only one phase current. c) Active part of the system for sector 2 (\$u\_{aN}, u\_{bN} > 0, u\_{cN} < 0\$) with the possibility of controlling two phase currents, i.e. all phase currents.

### B. Systems with Buck-Type Characteristic

As single-phase buck-type ac-dc converters do not enable to provide sinusoidal currents over the entire mains period [21], the derivation of buck-type PFC rectifier structures has to refer directly to three-phase diode rectifier circuits with dc side inductor [cf. **Fig. 2(b)**]. The diode bridge has to be extended with turn-off elements by considering phase- and bridge-symmetry requirements, such that the mains phases to be connected with the dc side can be arbitrarily selected. Alternatively, also a system based on the injection principle could be conceptualized with reference to **Sec. IV-A1**.

#### 1) Active Six-Switch Buck-Type PFC Rectifier:

A power transistor has to be added in series to each diode in the circuit shown in **Fig. 2(b)** to enable a full, i.e. a voltage-independent controllability of the power transfer. The resultant converter structure is shown in **Fig. 22(a)**, which is known from current dc-link converters used for drive systems [63]. The diode-transistor series-combinations represent here unidirectional, bipolar blocking switches, which can be also replaced by RC-IGBTs in terms of a reduction of the conduction losses. However, a limitation of the switching frequencies to relatively low values (in the range of 10 kHz) would then be required due to the relatively high switching losses [64].

If a transistor of the positive bridge half, e.g. transistor \$S\_{\bar{a}p}\$, and a transistor of the negative bridge half, e.g. \$S\_{n\bar{c}}\$, are switched on, the output inductor current \$I\$ is drawn from phase a and fed back into phase c,

$$\begin{aligned} i_a &= +I \\ i_b &= 0 \\ i_c &= -I \end{aligned} \quad (34)$$

[cf. **Fig. 22(b)**]. In addition, the line-to-line voltage \$u\_{ac}\$ is switched to the output, i.e. is used for the formation of the output voltage

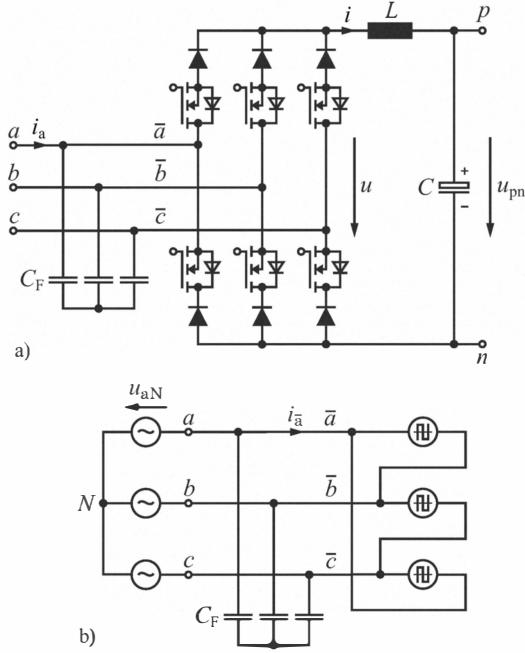
$$u_{pn} = u_{\bar{a}N} - u_{\bar{c}N} = u_{\bar{a}\bar{c}} = u_{ac}. \quad (35)$$

If solely both transistors of a bridge-leg are switched on, \$i\_a = i\_b = i\_c = 0\$ applies and \$u = 0\$, i.e. the system is in a freewheeling state. The conduction losses in the freewheeling state could be reduced by implementation of an explicit freewheeling diode.

By proper modulation, the output current \$i\$ can thus be distributed to the three phases in such a manner that after low-pass filtering of the pulse-width modulated discontinuous input currents \$i\_{\bar{a}}, i\_{\bar{b}}, i\_{\bar{c}}\$ sinusoidal mains currents result (in **Fig. 21(a)** only the filter capacitors \$C\_F\$ of the EMI filter on the mains side are shown). Furthermore, the output voltage, which is formed by low-pass filtering of \$u\$ with the output inductor \$L\$ and the output capacitor \$C\$, can be adjusted with the relative duration of the freewheeling state starting from zero to values

$$U_{pn} < \sqrt{\frac{3}{2}} U_{N,ll,rms}. \quad (36)$$

The limited output voltage range is explained by the fact that two line-to-line voltages have to be used in each pulse period for the formation of the output voltage in order to supply each mains phase with current. In order to maximize the achievable output voltage, here always the two largest voltages, e.g. \$u\_{\bar{a}\bar{c}}\$ and \$u\_{\bar{a}\bar{b}}\$ are selected (valid within a \$60^\circ\$ interval of the mains period \$\varphi\_N = (-30^\circ, +30^\circ)\$, cf. **Fig. 15(c)**). Both voltages have a phase displacement of \$60^\circ\$. Therefore, only voltage values \$u\_{\bar{a}\bar{c}} = u\_{\bar{a}\bar{b}} = \sqrt{3/2} U\_{N,ll,rms}\$ are available for the pulse period at the intersection of both voltages. Correspondingly, the output voltage range is defined by (36). The full controllability of the system generally allows an arbitrary phase



**Fig. 22.** a) Circuit topology of the active six-switch buck-type PFC rectifier. b) Equivalent circuit of ac part of the system. Note: if power transistors were only implemented in the positive or negative bridge half, a circuit analogous to Fig. 20(a) would result, which also would not allow for a sinusoidal current impression due to the limited controllability.

displacement between the mains current and the mains voltage of

$$\Phi = (-180^\circ, +180^\circ) . \quad (37)$$

However, with an increasing phase displacement  $\Phi$ , the line-to-line voltages switched to the output have lower instantaneous values, and/or

$$U_{pn} < \sqrt{\frac{3}{2}} U_{N,II,rms} \cos(\Phi) \quad (38)$$

applies. Correspondingly, e.g. for  $\Phi = 90^\circ$  follows  $U_{pn} = 0$ , as is immediately clear considering the power balance between the ac and the dc side. The output voltage range (36) is thus only valid for  $\Phi = 0$  and/or in order to ensure a wide output voltage range, the phase displacement  $\Phi$  has to be limited to small values [65].

Note: According to (37), for the circuit in **Fig. 22(a)**, the reversal of the power flow direction demands a change of the output voltage. A reversal of the power flow direction at the same polarity of the output is only possible by extension of the circuit structure with anti-parallel transistors to the diodes [66].

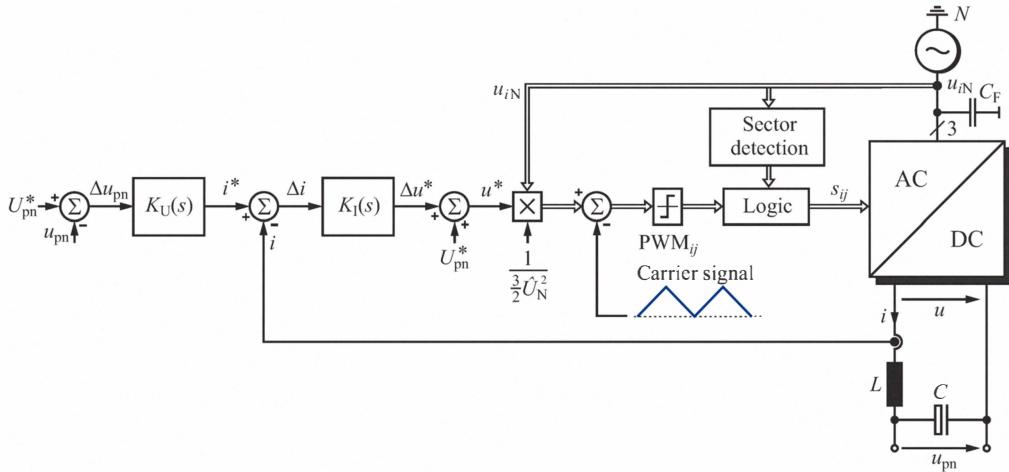
A superimposed output voltage controller with an underlying current controller is used for the system control (cf. **Fig. 23**), whereupon possibly active damping of the input filter has to be applied [67]. It has to be pointed out that opposed to boost-type PFC rectifiers the mains current is not directly impressed by the control, but is formed only by pulse width modulation without feedback from a controlled dc current. Accordingly, variations of the dc current, parasitic timing errors of the switching or distortions at borders of the  $60^\circ$  mains voltage sectors [68] are not immediately corrected. In the practical application, particularly at high mains frequencies, buck-type PFC systems therefore show a lower input current quality than boost-type PFC systems. First considerations of a direct mains current control, which could eliminate this disadvantage, can be found in [67].

A hardware demonstrator of the rectifier system is presented in **Fig. 24** [69]. The efficiency of the system, implemented with 900 V super-junction MOSFETs and SiC Schottky diodes ( $f_P = 18$  kHz) equals to 98.9% at the nominal operating point. This clearly shows, that with an appropriate semiconductor effort, despite the implementation of the switches as diode-transistor series connection, very high efficiencies are achievable.

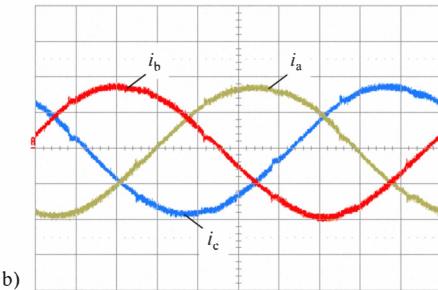
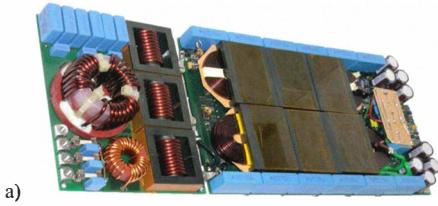
### 2) Active Three-Switch Buck-Type PFC Rectifier:

As an alternative to **Fig. 22**, the selection of the conducting phases is also possible with four-quadrant switches arranged on the ac side of the bridge rectifier. The four-quadrant switches can then be integrated into the bridge-leg structure as shown in **Figs. 25(a)–(c)**. The resulting three-switch buck-type PFC rectifier system is depicted in **Fig. 25(d)**.

Due to the reduction of the number of switches and/or higher number of diodes, higher conduction losses result. On the other hand, the installed chip area of the power transistors is better utilized. However, as a result of the lower number of switches, the controllability is limited compared with **Fig. 22**. There is not any more a possibility given for a reversal of the power flow direction, as can be immediately verified with **Fig. 25(a)**. Furthermore, only the current conducting bridge-legs but not directly the current conducting diodes are definable. The conduction state thus adjusts depending on the polarity of the voltages at the activated bridge-legs.



**Fig. 23.** Structure of the control of the active six-switch buck-type PFC rectifier with a superimposed output voltage controller  $K_U(s)$ . The output current controller  $K_I(s)$  with feed-forward of the output voltage  $U_{pn}^*$  defines the voltage at the output of the rectifier bridge. The modulation is performed such that output voltage of the rectifier is formed in each pulse period by segments of two line-to-line voltages and the dc current  $i$  is distributed to the input phases and sinusoidally modulated.



**Fig. 24.** a) Hardware demonstrator of a 6 kW active six-switch buck-type PFC rectifier. b) Time behavior of the phase currents within a mains period. Operating parameters: rms line-to-line voltage  $U_{N,ll,rms} = 400$  V, mains frequency  $f_N = 50$  Hz, dc output voltage  $U_{pn} = 400$  V, switching frequency  $f_P = 18$  kHz. The rectifier enables an extremely high nominal efficiency of  $\eta_{nom} = 98.9\%$  [69] although there are always four power semiconductor in the current path (two diode-MOSFET series connections). Scales: 5 A/div, 2 ms/div.

A restriction of the operating range to

$$\Phi = (-30^\circ, +30^\circ) \quad (39)$$

results, as is shown by a more detailed analysis, which however is of minor importance in view of the preferred ohmic operation as a consequence of (38). A figurative explanation of (39) is possible in a similar manner as for the boost-type  $\Delta$ -switch rectifier [cf. Fig. 15(c)] with the  $\pm 30^\circ$  phase displacement between the phase quantities and the line-to-line quantities, however, is not shown here for the sake of brevity. The output voltage range for  $\Phi = 0$  is still given by

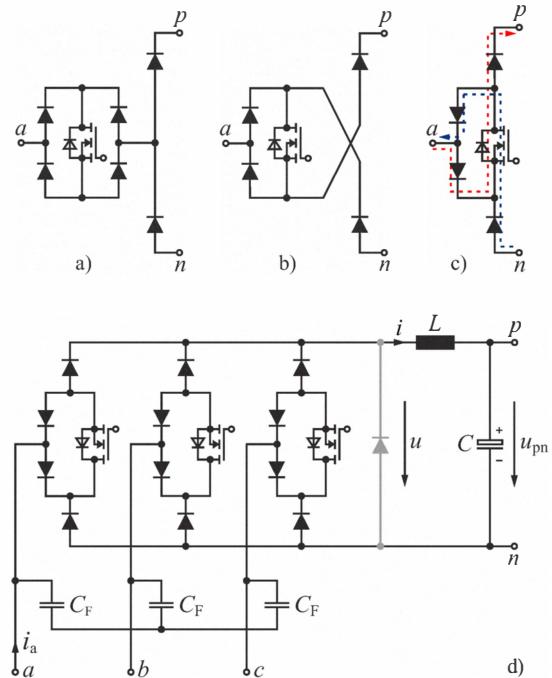
$$U_{pn} < \sqrt{\frac{3}{2}} U_{N,ll,rms}. \quad (40)$$

The control scheme depicted in Fig. 23 can be also applied to the three-switch system. The switching signals of the transistors then have to be generated by OR-connection of the switching signals of the power transistors of the respective bridge-legs of the six-switch buck-type PFC topology.

### 3) Hybrid Current Injection Buck-Type (SWISS) PFC Rectifier:

As an alternative to the direct control of the current formation of a three-phase diode bridge, a three-phase PFC rectifier can also be implemented, according to the concept of 3<sup>rd</sup> harmonic current injection described in Sec. IV-A1 for boost-type systems. Then, only the dc–dc boost converters of the circuit in Fig. 12 have to be replaced by buck converters. The resultant circuit is shown in Fig. 26(a). To the knowledge of the authors, this system has not yet been described in the literature, presumably due to the general focus in research on systems with boost-type characteristic. In the following, the circuit topology is thus designated as SWISS Rectifier [4], [70].

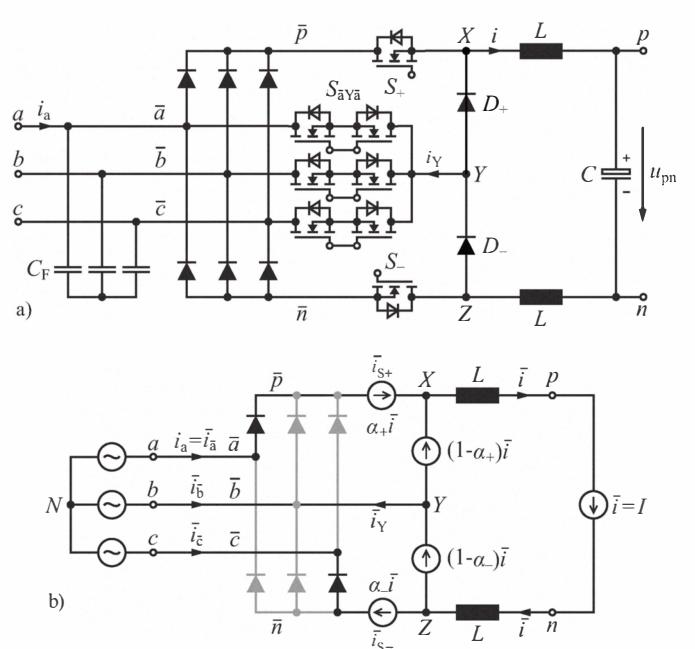
Contrary to the circuits according to Sec. IV-B1 and Sec. IV-B2, the rectifier diodes of the system are not commutated with switching frequency. Correspondingly, the conduction losses can be reduced by employing devices with a low forward voltage drop (and a higher reverse recovery time). As for the boost-type system, the current injection is performed again with four-quadrant switches into the phase with the currently smallest absolute voltage value. In this



**Fig. 25.** Derivation of the circuit topology of the active three-switch buck-type PFC rectifier. A four-quadrant switch is formed by a diode bridge and a dc side power transistor is inserted on the ac side in a). After merging series connected diodes and redrawing, the bridge-leg structure in c) results, and/or the three-phase circuit topology in d).

context, it should be mentioned that with a passive injection network, a current injection into all three phases is possible. Such a system was proposed in [12] and is, as described in Sec. IV-A1, also known for boost-type systems. However, in consideration of the large volume of the passive injection network and the higher injection current, this approach is not discussed further in this paper.

For the proof of the sinusoidal controllability of the mains currents,



**Fig. 26.** a) Basic structure of the SWISS Rectifier. b) Local average equivalent circuit of the active part of the system for  $u_{aN} > u_{bN} > u_{cN}$ .

again a  $60^\circ$  interval of the mains period with  $u_{aN} > u_{bN} > u_{cN}$  or  $\varphi_N = (0, 60^\circ)$  is considered. The active part of the circuit in this mains sector is depicted in **Fig. 26(b)**.

The rectifier system should represent a symmetric three-phase load of (fundamental) phase conductance  $G^*$  to the mains. Accordingly, the local average values of the (discontinuous) input currents may be written as

$$\begin{aligned}\bar{i}_{\bar{a}} &= G^* u_{aN} \\ \bar{i}_{\bar{b}} &= G^* u_{bN} \\ \bar{i}_{\bar{c}} &= G^* u_{cN}\end{aligned}\quad (41)$$

( $u_{iN} = u_{\bar{i}N}$ ). The reference output current  $I^*$ , to be impressed by the buck converter, is then given under the assumption of a symmetrical three-phase mains system by

$$I^* = \frac{3}{2} G^* \frac{\hat{U}_N^2}{U_{pn}} \quad (42)$$

( $\hat{U}_N$  designates the amplitude of the phase voltages,  $U_{pn}$  is the output voltage). An ideal output current controller and/or  $i = I = I^*$  is assumed for the further considerations. The currents in the phases  $a$  and  $c$  are impressed by a respective switching (PWM) of  $S_+$  and  $S_-$

$$\alpha_+ I = \bar{i}_{\bar{a}} \quad \alpha_- I = -\bar{i}_{\bar{c}} \quad (43)$$

whereby the duty cycles result with (41), (42), and (43) as

$$\alpha_+ I = \frac{2}{3} \frac{U_{pn}}{\hat{U}_N^2} u_{aN} \quad \alpha_- I = -\frac{2}{3} \frac{U_{pn}}{\hat{U}_N^2} u_{cN}. \quad (44)$$

Considering the partitioning of the current in the node  $Y$  and  $i_a + i_b + i_c = 0$  or  $\bar{i}_{\bar{a}} + \bar{i}_{\bar{b}} + \bar{i}_{\bar{c}} = 0$ , the injection current

$$\bar{i}_Y = (1 - \alpha_+) I - (1 - \alpha_-) I = \bar{i}_{\bar{a}} + \bar{i}_{\bar{c}} = -\bar{i}_{\bar{b}} \quad (45)$$

results. Thus, the correct current is injected into the third phase (here phase  $b$ ). For the formation of the output voltage,

$$\bar{u}_{xz} = \alpha_+ u_{aN} + (1 - \alpha_+) u_{bN} - (\alpha_- u_{cN} + (1 - \alpha_-) u_{bN}) \quad (46)$$

is relevant. After simplification, the output voltage may be written as

$$\bar{u}_{xz} = \alpha_+ u_{ab} - \alpha_- u_{cb}. \quad (47)$$

A multiplication of (47) with  $I$  results in

$$\bar{u}_{xz} I = \bar{i}_a u_{ab} + \bar{i}_c u_{cb} = \bar{p} = P, \quad (48)$$

the instantaneous power  $\bar{p}$ , which under the assumption of symmetrically loaded mains shows a constant value  $\bar{p} = P$ . Accordingly, at a constant current  $I$ , also a constant voltage  $\bar{u}_{xz}$  and thus due to  $\bar{u}_L = 0$  a constant output voltage  $\bar{u}_{pn} = U_{pn}$  is generated.

As the previous derivation shows, the operation of the system is limited to purely ohmic fundamental mains behavior,

$$\Phi = 0 \quad (49)$$

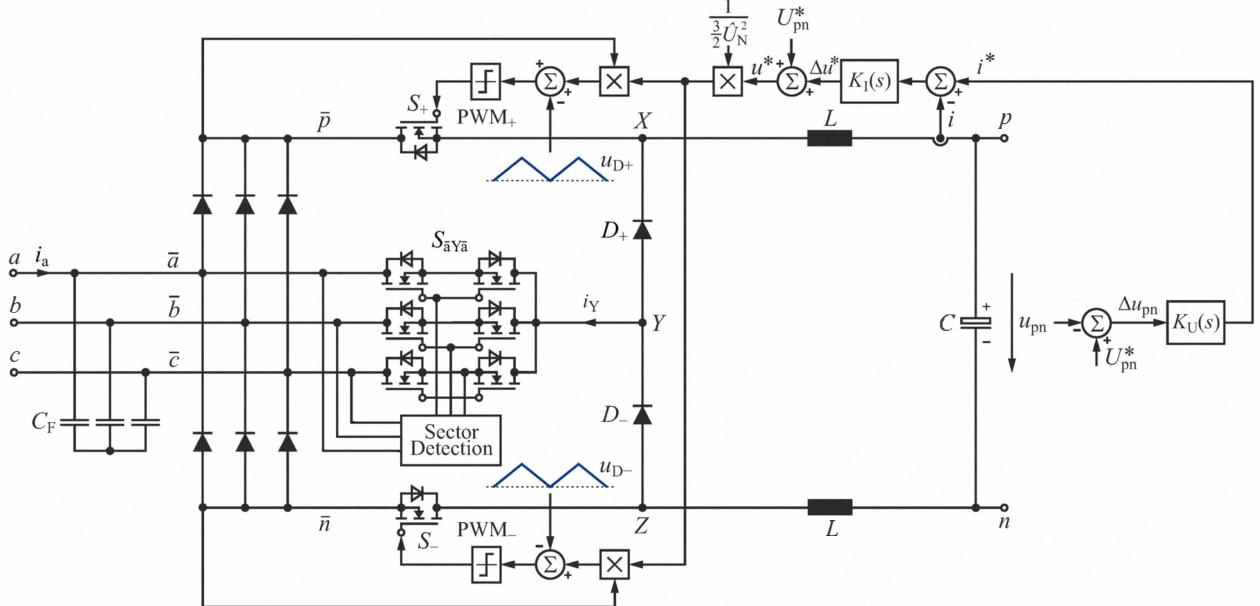
[cf. (41)]. The output voltage range is limited by the minimal value of the six-pulse diode bridge output voltage,

$$U_{pn} < \sqrt{\frac{3}{2}} U_{N,11,\text{rms}}, \quad (50)$$

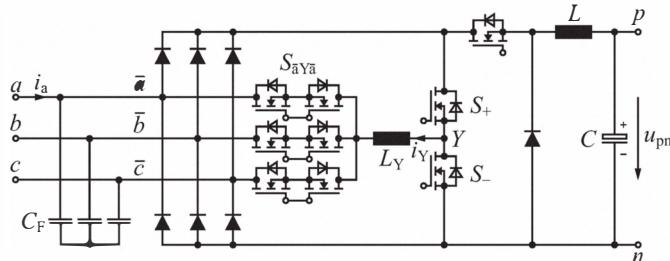
and therewith identical with the output voltage range for six-switch active buck-type PFC rectifier systems.

A possible implementation of the control circuit of the system, with a superimposed output voltage controller  $K_U(s)$  and a subordinate output current controller  $K_I(s)$  is shown in **Fig. 27**. Ultimately, with the output current controller the current forming voltage  $\bar{u}_{xz}$  is defined, where advantageously a feed-forward of the output voltage  $u_{pn}^* = U$  is applied. The adjustment of  $u_{xz}$  is obtained with an appropriate selection of the duty cycle of the pulse width modulation of the transistors  $S_+$  and  $S_-$  [cf. (43)]. There, the (normalized) voltages  $u_{pN}$  and  $u_{nN}$  are used as modulation functions according to (44) (cf. also **Fig. 27**).

The pulse width modulation of  $S_+$  and  $S_-$  can be implemented in phase or antiphase. The switching frequency ripple of  $i_Y$  is minimized for carrier signals  $u_{D+}$  and  $u_{D-}$  that are in phase. For carrier signals that are in opposite phase, a minimal output current ripple but a



**Fig. 27.** Control structure of the SWISS Rectifier with a superimposed output voltage controller  $K_U(s)$  and a subordinate output current controller  $K_I(s)$  with feed-forward of the output voltage. The voltage required to control the output current is formed through modulation of  $S_+$  and  $S_-$  such that in both conducting branches of the diode bridge a pulse width modulated current results. The local average value of this current is proportional to the corresponding mains phase voltage. A four-quadrant switch is switched on by the sector control and injecting always into the mains phase with the smallest absolute voltage value.



**Fig. 28.** Combination of an active-filter-type 3<sup>rd</sup> harmonic current injection rectifier and a dc–dc buck-type converter stage to an active buck-type PFC rectifier system. The system is characterized by a minimal number of power semiconductors in the main current path, and only a low-frequency variation of the output CM voltage. The dc–dc buck converter should be advantageously implemented as interleaved converter.

maximum ripple of  $i_Y$  results, which needs to be considered for the design of the filter capacitors  $C_F$  at the input.

It should be noted that a hybrid 3<sup>rd</sup> harmonic injection PFC rectifier circuit can also be built by combination of an active-filter-type 3<sup>rd</sup> harmonic injection rectifier and a simple dc–dc buck converter stage (cf. **Fig. 28**). The buck stage to be controlled e.g. for a constant output current or a constant output voltage then ensures, independent of the pulsation of the voltage  $u_{pn}$  with sixfold mains frequency, a constant output power. The advantage of this circuit topology is that only a single power transistor is lying in the main current path, i.e. in particular at high output voltages with a relatively short freewheeling interval, low conduction losses occur. In addition, the negative output voltage terminal is always connected to the mains via a diode of the lower bridge half of the diode rectifier. Therefore, no output CM voltage with switching frequency is generated. The implementation effort of the CM EMI filter can thus be reduced. Only the parasitic capacitors of the power semiconductors lead to high-frequency CM noise currents (cf. related consideration of boost-type PFC rectifier systems in [53]).

#### 4) Discussion:

The impression of the mains current of the considered buck-type PFC rectifier systems is obtained with so far known current control schemes always only in an indirect manner. Accordingly, contrary to the boost-type PFC rectifiers (cf. **Sec. IV-A5**), concepts based on the current injection principle and direct active systems can be considered as equivalent regarding the achievable input current quality.

Therefore, for the comparative evaluation in **Sec. VI-C**, both concepts, i.e. the six-switch buck-type PFC rectifier and the SWISS Rectifier, are considered. The three-switch buck-type PFC rectifier is omitted due to the higher conduction losses and the less uniform distribution of the semiconductor losses compared to the six-switch buck-type PFC rectifier.

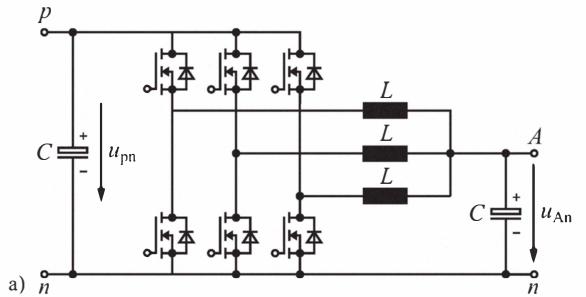
#### C. Systems with Boost-Type and Buck-Type Characteristic

As shown in **Fig. 4**, the output voltage range of boost-type PFC rectifiers is not immediately adjoining the output voltage range of buck-type systems. Voltages in the range

$$\sqrt{\frac{3}{2}} U_{N, ll, rms} < U_{pn} < \sqrt{2} U_{N, ll, rms} \quad (51)$$

can thus only be generated with a downstream dc–dc boost converter of the buck-type PFC rectifier or by combination of boost-type PFC rectifier and a dc–dc buck converter.

A possible implementation of such dc–dc converter system is shown in **Fig. 29**. The bidirectional, i.e. for boost and buck operation designed converter has an output power of 10 kW, allows a voltage



**Fig. 29.** a) Circuit topology of a (bidirectional) 6 kW Triangular Current Mode (TCM) Zero Voltage Switching (ZVS) buck dc–dc converter comprising three interleaved stages. b) Ultra-efficient and ultra-compact hardware demonstrator with a nominal efficiency of  $\eta = 99\%$  and a power density of  $\rho = 18.5 \text{ kW/dm}^3$ . Specifications: nominal input voltage  $U_{pn} = 350 \text{ V}$ , output voltage range  $U_{An} = 0 \text{ V} \dots 350 \text{ V}$ , rated output power  $P_2 = 10 \text{ kW}$ , switching frequency of each stage at rated output power  $f_P = 48 \text{ kHz}$ .

transfer from  $U_1 = 350 \text{ V}$  to  $U_2 = 0 \text{ V} \dots 350 \text{ V}$ , and comprises three interleaved subsystems. The discontinuous current mode operation of the subsystems with resonant switching transition and/or zero voltage switching [71] minimizes switching losses and allows the selection of a high switching frequency (at nominal operation) of  $f_P = 48 \text{ kHz}$ . Therewith, a very high efficiency of  $\eta = 99\%$  and a power density of  $\rho = 18.5 \text{ kW/dm}^3$  is achievable.

As an alternative to an explicit implementation of a dc–dc converter, a dc–dc boost converter stage could also be integrated into the output stage of a buck-type PFC system, whereby the output inductor could also be used as boost inductor [72], [73].

#### V. DIMENSIONING OF THE POWER SEMICONDUCTORS AND OF THE EMI FILTER

In the following, the current and voltage stresses of the systems in **Sec. IV-A5** and **Sec. IV-B4** are briefly summarized to assist a practical implementation of the circuit topologies described above. In addition, the basic structure of the EMI filter on the ac side is discussed with a focus on the CM filtering.

#### A. Dimensioning of the Power Semiconductors and Main Passive Components

The current stresses of the power semiconductors of a PFC rectifier systems are often determined for a defined operating point by simulation. Alternatively, a calculation can be also performed only analytically with good accuracy. Simple mathematical expressions then result, which are valid over the whole operating range (under the constraint of CCM) and thus provide an ideal basis for the analysis of the component stresses and/or the losses at different operating points or input and/or output voltages.

The starting point for the analytical calculations are the relative switch-on times of the power transistors which can be determined analytically for the whole mains period if the modulation method is known. The remaining parameter is the modulation index  $M$ , which

represents the ratio of the amplitude of the three-phase voltage or current system on the ac side and the dc output voltage, and/or the dc output current

$$M = \frac{\hat{U}_U}{\frac{1}{2}U_{pn}} \quad M = \frac{\hat{I}_U}{I} \quad (52)$$

$\hat{U}_U \approx \hat{U}_N$  represents the amplitude of the fundamental of the discontinuous phase voltage at the rectifier input of a boost-type system,  $\hat{I}_U$  is the amplitude of the fundamental of the discontinuous phase currents at the rectifier input of a buck-type system).

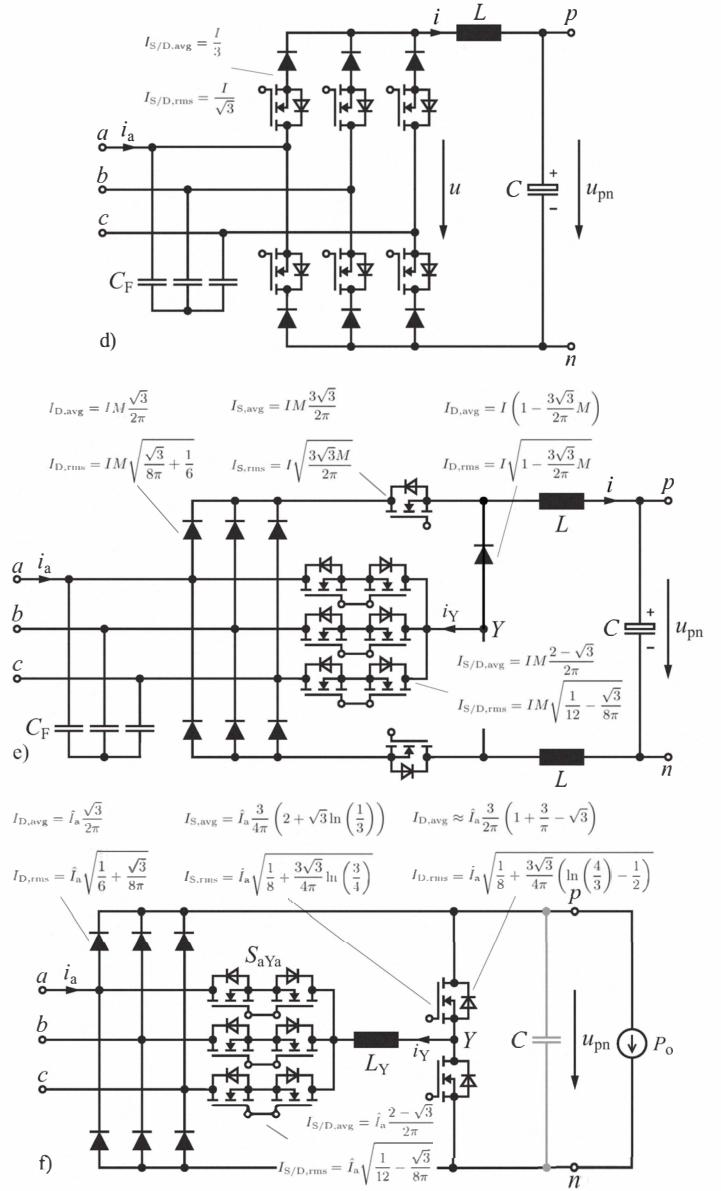
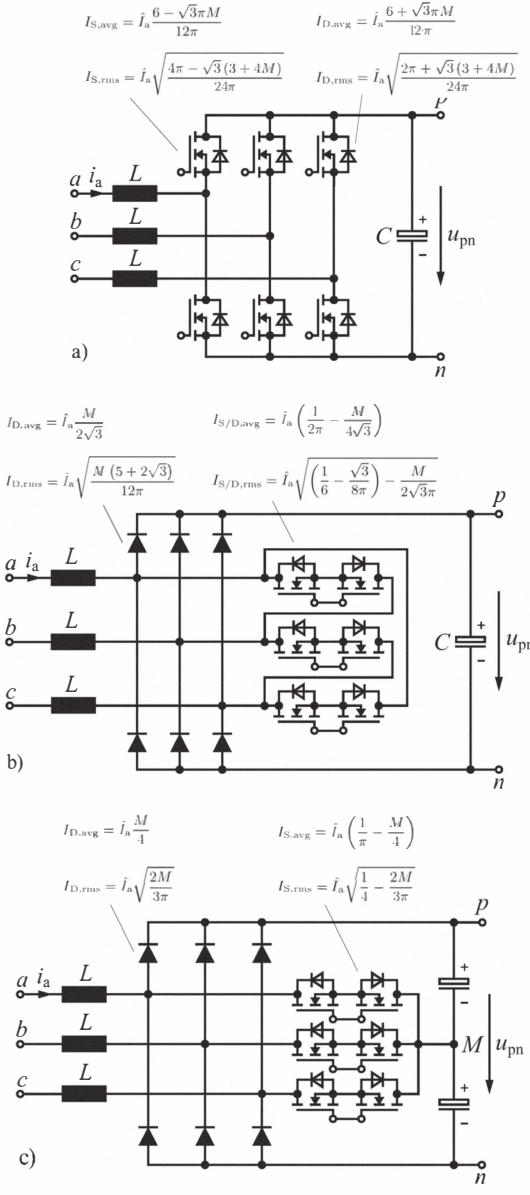
With the relative switch-on time (duty cycle) and the input current (for boost-type rectifiers), and/or the output current (for buck-type rectifiers), the instantaneous conduction states of the power semiconductors are defined, and the local average current values can be calculated by averaging over a pulse period. Based on that, the global average and root mean square (rms) values of the currents and

voltages of interest can be determined [74] by averaging over the mains period. The resultant equations for the individual topologies are compiled in **Fig. 30**.

### B. DM and CM EMI Filter

The input inductors of the boost-type PFC rectifier systems, discussed in **Sec. IV-A**, are to be considered as the first stage of a multi-stage EMI filter placed on the ac side similar to the input filter capacitors of the systems with buck-type characteristic. The conducted EMI noise is suppressed with this filter such that the standards of conducted noise are fulfilled in the frequency range of 150 kHz...30 MHz (e.g. CISPR 11). (Depending on the application, another EMI filter might be required on the dc side [75], [76], which however is not discussed here for the sake of brevity.)

Three-phase rectifier circuits inherently generate a CM voltage between the mid-point of the output voltage (the output voltage buses)



**Fig. 30.** Circuit topologies and current stresses of the main components of the power circuit of selected active boost- and buck-type PFC rectifier systems. **a)** Six-switch boost-type PFC rectifier (cf. **Fig. 20(b)**), **b)**  $\Delta$ -switch rectifier (cf. **Fig. 16**), **c)** VIENNA Rectifier (cf. **Fig. 18**), **d)** six-switch buck-type PFC rectifier (cf. **Fig. 21**), **e)** SWISS Rectifier (cf. **Fig. 25**), and **f)** active-filter-type 3<sup>rd</sup> harmonic current injection rectifier (cf. **Fig. 13**).

and ground. The CM voltage waveform for a passive diode rectifier circuit with inductors on the dc side is depicted in **Fig. 31(a)**. For active rectifier circuits, the CM voltage has a pulsed waveform [cf. **Figs. 31(b) and (c)**] thus, CM currents result due to the parasitic capacitances to ground.

For fully active boost-type PFC systems, e.g. for the VIENNA Rectifier, the CM voltage originates from the rectifier ac side phase voltages employed for the current impression that do not add to zero (except for the switching state  $s_{\bar{a}M} = s_{\bar{b}M} = s_{\bar{c}M} = 1$ ). Thus, as for the Y-rectifier, shown in **Sec. III-A**, a CM voltage

$$u_{MN} = -\frac{1}{3}(u_{\bar{a}M} + u_{\bar{b}M} + u_{\bar{c}M}) = u_{CM}, \quad (53)$$

is generated between the mid-point of the output voltage and the (grounded) mains star-point, which could contain a low-frequency component  $\bar{u}_{CM}$ , but contains in any case a switching frequency component  $u_{CM,\sim}$

$$u_{CM} = \bar{u}_{CM} + u_{CM,\sim} \quad (54)$$

(cf. for the VIENNA Rectifier also [53], Fig. 3.4 and Fig. 5.73). A filtering of  $u_{CM,\sim}$  can be achieved by connecting  $M$  via a capacitor  $C_{CM,M}$  to an artificial mains star-point  $N'$  (representing the ground potential), formed by a star-connection of filter capacitors  $C_F$  and insertion of a CM inductor  $L_{CM,1}$  in series to the boost inductors [cf. **Fig. 32(a)**]. A low-frequency variation of the potential of  $M$  is thus not prevented. In addition, contrary to a placement of CM filter capacitors to ground, ground currents are minimized. Additional CM filter stages have to be implemented on the mains side for the filtering of the noise currents that result from the parasitic capacitances of the power semiconductors to the heat sink [53].

For fully active buck-type PFC systems, within each pulse period two line-to-line voltages are switched to the rectifier output for the formation of the output voltage and for the distribution of the output current to the mains phases. This again leads to a CM voltage  $u_{CM,\sim}$  at switching frequency. (A CM voltage during the freewheeling interval can be avoided by symmetrical splitting of the output inductor to the positive and negative output bus). The concept described above for boost-type converters can advantageously also be used for the filtering of  $u_{CM,\sim}$  of buck-type systems [cf. **Fig. 32(b)**] where the CM inductance has to be inserted on the dc side.

For determining the switching frequency component of the DM voltage, which is relevant for the design of the DM filtering, for boost-type systems within each pulse period, the formation of the input current has to be considered. E.g. for phase  $a$

$$L \frac{di_a}{dt} = u_{aN} - (u_{\bar{a}M} + u_{CM}) = u_{aN} - u_{\bar{a}N} \quad (55)$$

$$= u_{aN} - \bar{u}_{aN} - u_{\bar{a}N,\sim} \quad (56)$$

applies. The phase current consists of a fundamental and a switching frequency component

$$i_a = \bar{i}_a + i_{a,\sim}, \quad (57)$$

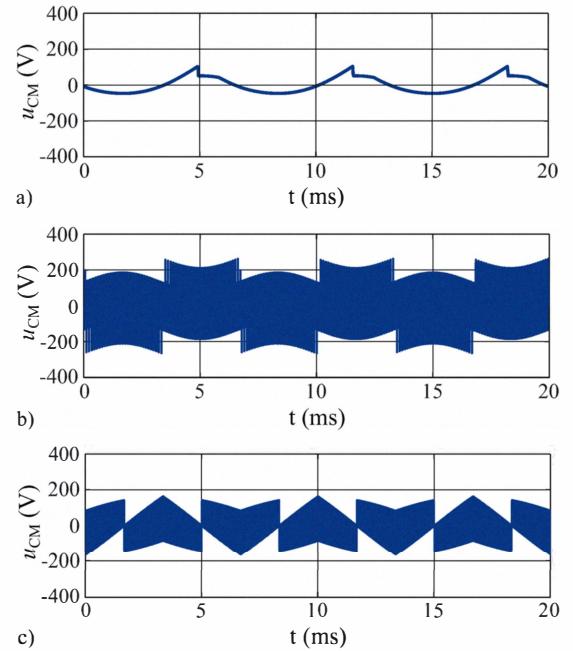
where the fundamental component  $\bar{i}_a$  is formed according to

$$L \frac{d\bar{i}_a}{dt} = u_{aN} - \bar{u}_{aN} \quad (58)$$

and the voltage to be suppressed by the DM filtering is

$$L \frac{di_{a,\sim}}{dt} = u_{\bar{a}N,\sim} = u_{DM,\sim}. \quad (59)$$

The filtering of  $u_{DM,\sim}$  (each phase shows an equal spectral composition of the related DM voltage) is performed with the boost inductors and with ac side capacitors  $C_{DM,1}$  between the phases, whereby typically two filter stages are required [cf. **Fig. 32(a)**]. Additionally,



**Fig. 31.** CM voltage at the output of three-phase rectifier systems referenced to the grounded star-point of the mains. a) Passive diode rectifier with smoothing inductor on the dc side [cf. **Fig. 2(b)**]. b) VIENNA Rectifier [cf. **Fig. 18(a)**]. c) Six-switch buck-type PFC rectifier [cf. **Fig. 22(a)**].

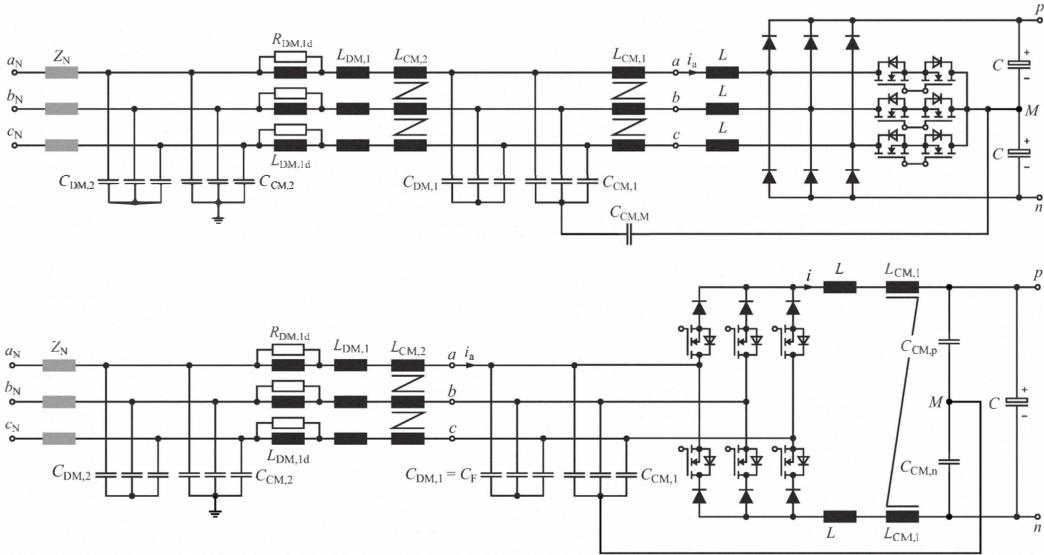
damping elements for reducing the resonance peaks [77] in respect of the control stability of the system have to be added, which also prevent the excitation of the filter by harmonics of the mains voltage.

For buck-type systems, the DM noise is generated by the pulsating input currents at switching frequency and is attenuated by the input filter capacitors  $C_F$  and the ac side filter inductors  $L_{DM,1}$  and an additional input filter stage.

Regarding the volume of the EMI filter, it has to be noted that, e.g. for boost converter systems, a constant voltage is decomposed into its spectral components by the pulse width modulation, i.e. into a mains-frequency fundamental component and harmonic components grouped around multiples of the switching frequency with sidebands. Only the fundamental frequency is used for the impression of the phase current, i.e. the switching frequency harmonics must be suppressed with an appropriate EMI (input) filter. The harmonic components, i.e. ultimately the difference between the constant output voltage  $U_{pn}$  and the actual low-frequency voltage component to be formed, e.g.  $\bar{u}_{aN}$ , show similar rms values. Considering in addition that the EMI input filter has to conduct the input current of the converter, a significant fraction of the total converter volume is expected to be determined by the EMI input filter. This is confirmed by implemented systems, where the volume of the EMI filter (including the boost inductors or buck input filter capacitors) typically represents 30% to 50% of the total converter volume (cf. **Fig. 20**). Here, it should be pointed out that the required filter attenuation can be calculated analytically in a simple manner by determining the spectral decomposition of the rectifier input voltage into a fundamental and a total noise voltage [78]–[80].

## VI. COMPARATIVE EVALUATION

In the foregoing sections, boost- and buck-type PFC rectifier systems suitable for industrial application have been identified and briefly discussed. In the following, a comparative evaluation of selected circuit concepts with regard to efficiency, volume, and



**Fig. 32.** Example of the EMI filter structure of a) an active boost-type PFC rectifier system [VIENNA Rectifier, cf. Fig. 18(a)] and of b) an active six-switch buck-type PFC rectifier [cf. Fig. 21]. Commercial EMI input filters typically employ filter capacitors at the input (mains) side. Accordingly, an additional filter stage is formed by the inner mains impedance  $Z_N$ , which could be deliberately increased to limit the short-circuit current. Fuses, over-voltage protection devices, bleeding resistors, and precharging circuitry are not shown. (Remark: Optionally, the CM capacitors could also be combined with the DM capacitor stages, i.e. by adding a Y-capacitor between the star-point of the DM capacitors and ground.)

implementation effort, and therewith finally implementation costs is provided to highlight the advantages and disadvantages of the individual systems and to facilitate the selection of a circuit topology for a specific application.

The performance indices used for the evaluation (cf. Sec. VI-A) are calculated using the same specifications for each system:

- Rated output power  $P_o = 10\text{ kW}$ ;
- Line-to-line mains voltage  $U_{N,1l,\text{rms}} = 400\text{ V}$ ;
- Output voltage  $U_o = 700\text{ V}$  (boost-type systems),  $U_o = 400\text{ V}$  (buck-type systems);
- Power transistors: 1200 V SiC JFETs (Infineon/SiCED, in cascode configuration, i.e. with normally-off characteristic);
- Power diodes: 1200 V SiC Schottky diodes (Infineon, ThinQ2, commutation/freewheeling diodes), 1200 V Si EmCon4 diodes (Infineon, rectifier diodes of the SWISS Rectifier);
- Switching frequency:  $f_P = 48\text{ kHz}$ ;
- Thermal conditions: average junction temperature of the semiconductors  $T_{J,\text{avg}} = 125^\circ\text{C}$ , heat sink temperature  $T_S = 85^\circ\text{C}$ , ambient temperature  $T_A = 45^\circ\text{C}$ ;
- DC output capacitors: aluminum electrolytic capacitors (B43501-series, EPCOS), 400 V capacitors for boost-type systems (two in series), 500 V capacitors for buck-type systems, designed for a mean time-to-failure of 50'000 h regarding the rms current loading and an assumed maximum capacitor temperature of  $65^\circ\text{C}$ ;
- AC filter capacitors (buck-type systems): foil capacitors (MKP, 305 V ac, X2, B3277x-series, EPCOS).

The rated output power of 10 kW represents a typical value for three-phase power supplies. The power transistors are implemented with SiC JFETs. This allows the use of the same transistor technology for all systems under investigation as the boost-type PFC rectifier systems feature two- or three-level characteristic, which requires a minimum blocking capability of 700 V or 350 V. Furthermore, in combination with SiC Schottky freewheeling diodes, a relatively high switching frequency of  $f_P = 48\text{ kHz}$  is enabled which represents a reasonable compromise for both converter types. (For the six-switch boost-type PFC rectifier systems the internal body diodes of the JFETs are used instead of explicit freewheeling diodes.)

Alternatively, the three-level converter (VIENNA Rectifier) could also be implemented with Si super-junction MOSFETs and the two-level converter with 1200 V IGBTs, which however would only allow a maximum switching frequency of  $f_P \approx 20\text{ kHz}$ . In addition, the SiC JFETs can be also applied for the buck-type rectifier systems, which have a similar blocking voltage requirement for the power semiconductors as the two-level boost-type systems. Only for the SWISS Rectifier, the diode rectifier at the input is implemented with low on-state voltage drop Si diodes instead of SiC Schottky diodes in order to achieve a high efficiency.

The chip area of the semiconductors is designed based on a thermal model of a typical semiconductor package (EconoPACK, Infineon, [79]) and a heat sink temperature of  $T_S = 85^\circ\text{C}$  such that an average junction temperature of  $T_{J,\text{avg}} = 125^\circ\text{C}$  results. For determining the semiconductor losses, the conduction characteristics (on resistance or diode forward characteristic) and the switching losses are considered with reference to data sheet values and results of experimental measurements on commercial components [79]. Thus, an equal usage of all semiconductors is ensured. In addition, the semiconductor design ensures that the amplitude of the junction temperature ripple (with mains frequency) remains limited to values that guarantee a mean time-to-failure of 50'000 h considering typical cycles-to-failure rates [81] that is equivalent to the dimensioning of the electrolytic capacitors.

It is worth noting that the relatively high equal junction temperature of all power semiconductors leads to relatively high semiconductor conduction losses due to the selected unipolar devices. In order to achieve a higher efficiency, semiconductor devices with a higher current rating, i.e. a larger chip area, could be used, and a lower junction temperature could be selected.

#### A. Definition of the Performance Indices

In order to provide a universally valid quantification of the converter performances, normalized performance indices are employed, which are independent of the actual system dimensioning. Thereby, the output power  $P_o$  and the load current  $I_o$  are used as reference values.

With reference to [8], the fictitious total apparent power and the normalized conduction and switching power loss are used for the characterization of the semiconductor expenditure.

### 1) Total Transistor and Diode VA Rating:

Total Transistor VA Rating

$$\mu_S^{-1} = \frac{\sum_n u_{S,\max,n} i_{S,\max,n}}{P_o}; \quad (60)$$

Total Diode VA Rating

$$\mu_D^{-1} = \frac{\sum_n u_{D,\max,n} i_{D,\max,n}}{P_o} \quad (61)$$

( $u_{S,\max,n}$  and  $u_{D,\max,n}$  refer to the maximum blocking voltage stress without considering switching overvoltages,  $i_{S,\max,n}$  and  $i_{D,\max,n}$  to the peak current value of the  $n$ -th device;  $\mu_S$  and  $\mu_D$  were defined in [8] for the assessment of the transistor and diode utilization.)

### 2) Relative Total Conduction Losses:

Relative Total Transistor Conduction Losses

$$\tau_C = \frac{\sum_n I_{S,\text{rms},n}}{I_o}; \quad (62)$$

Relative Total Diode Conduction Losses

$$\delta_C = \frac{\sum_n I_{D,\text{rms},n}}{I_o}. \quad (63)$$

As mentioned above, for the transistors (SiC JFETs) and diodes, the semiconductor chip area is scaled with the current loading and/or the power loss such that a constant (average) junction temperature of all power semiconductors is given. Correspondingly, the conduction losses of the transistors only increase linearly and not quadratically with the current loading.

### 3) Relative Total Transistor and Diode Switching Losses:

$$\tau_P = \frac{\sum_n P_{S,P,n}}{P_o} \quad (64)$$

$$\delta_P = \frac{\sum_n P_{D,P,n}}{P_o} \quad (65)$$

The switching losses are calculated based on experimentally verified switching loss measurement data [79] and are approximated linearly as a function of the switched voltage and the switched current for a junction temperature of  $T_J = 125^\circ\text{C}$ .

### 4) Relative Boxed Volume of the Inductors and Capacitors:

Regarding the passive components for the boost-type rectifier systems only the boxed volume of the boost inductors (iron power cores) and the output capacitors (electrolytic capacitors) and for the buck-type rectifier systems only the boxed volume of the output inductors (same core material as used for boost inductors) and of the ac side filter capacitors  $C_F = C_{DM,1}$  (MKP X2 foil capacitors) are considered.

$$\text{Inductors} \quad \rho_L^{-1} = \frac{\sum_i V_{L,i}}{P_o} \quad (66)$$

$$\text{Capacitors} \quad \rho_C^{-1} = \frac{\sum_i V_{C,i}}{P_o} \quad (67)$$

### 5) Conducted Differential and Common Mode Noise:

The assessment of the conducted EMI noise behavior and/or of the required filter effort to meet the EMC standards is performed for the boost-type systems based on the Differential Mode (DM) component  $u_{DM}$  and the Common Mode (CM) component  $u_{CM}$  of the noise voltage at the rectifier input

$$u_{\text{noise}} = u_{DM,\sim} + u_{CM,\sim}. \quad (68)$$

Thereby, in terms of a simplification [78], for the DM noise voltage  $u_{DM}$  the total voltage, forming the boost inductor current ripple

component of a phase current may then be written as (shown e.g. for input phase  $a$ )

$$u_{DM,a,\sim,\text{rms}} = \sqrt{u_{aN,\text{rms}}^2 - u_{aN,\text{rms}}^2} = u_{DM,\sim,\text{rms}}. \quad (69)$$

The Common Mode (CM) voltage is given by

$$u_{CM} = -\frac{1}{3}(u_{aM} + u_{bM} + u_{eM}) \quad (70)$$

(cf. (4), where  $M$  designates the (fictitious) mid-point of the output voltage. Analogous to (69), the CM noise voltage relevant for the filter design can then be approximately calculated by subtracting the low frequency component  $\bar{u}_{CM}$

$$u_{CM,\sim,\text{rms}} = \sqrt{u_{CM,\text{rms}}^2 - \bar{u}_{CM,\text{rms}}^2}. \quad (71)$$

For the buck-type PFC system the CM voltage can be calculated as

$$u_{CM} = \frac{1}{2}(u_{pN} + u_{nN}), \quad (72)$$

and the switching frequency component again according to (71). Instead of  $u_{DM,\sim}$  [cf. (59)], here, the rms value of the switching frequency components of the discontinuous input currents

$$i_{DM,a,\sim,\text{rms}} = \sqrt{i_{a,\text{rms}}^2 - \bar{i}_{a,\text{rms}}^2}. \quad (73)$$

(shown for input phase  $a$ ) is used for the assessment of the DM filter attenuation requirement. A voltage noise level could be calculated by multiplication with  $R = 50\Omega$ , the input resistance of a typical EMI test receiver.

### 6) Efficiency:

The efficiency of the systems is characterized by the relative losses

$$\frac{P_L}{P_o} = \frac{P_N - P_o}{P_o} = \frac{1}{\eta} - 1 = \frac{1 - \eta}{\eta} \approx 1 - \eta, \quad (74)$$

where in addition to the semiconductor losses and main power components also a power consumption of  $P_{aux} = 30\text{W}$  for the auxiliary supply (control circuitry, gate drives, fans) is considered.

### 7) Volume of the Cooling System:

With the relative losses  $(1 - \eta)$  and the Cooling System Performance Index [82]

$$CSPI = \frac{G_{th,S-A}}{V_S} \quad (75)$$

( $G_{th,S-A}$  designates the required thermal conductance ( $\text{W}/\text{K}$ ) between the surface of the heat sink and the ambient) and a given admissible temperature difference  $\Delta T_{S-A}$  the volume of the forced air cooled heat sink can be calculated to [83]

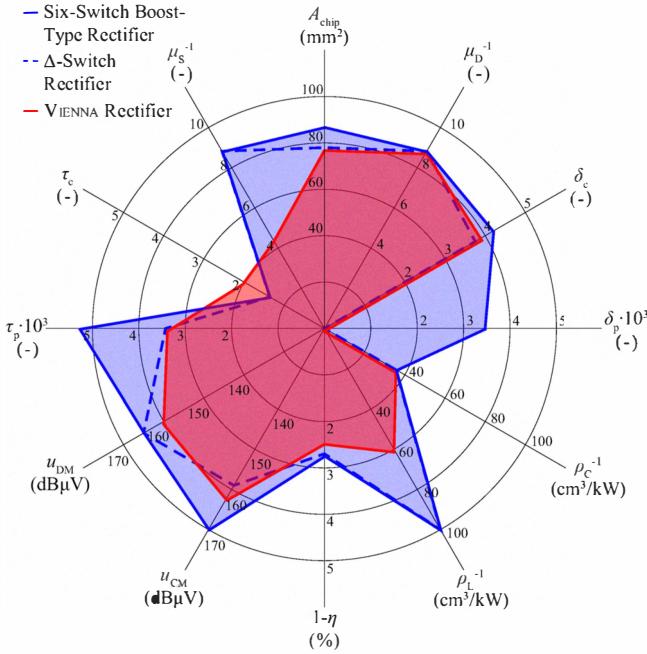
$$V_S = \frac{G_{th,S-A}}{CSPI} = \frac{P_L}{\Delta T_{S-A} CSPI} \approx \frac{P_o}{\Delta T_{S-a} CSPI} (1 - \eta). \quad (76)$$

Commercial heat sink profiles have a typical  $CSPI = 5 \dots 7 \text{W}/(\text{K dm}^3)$ , with optimized heat sink profiles a  $CSPI = 12 \dots 15 \text{W}/(\text{K dm}^3)$  is achievable.

### B. Comparison of the Six-Switch Boost Rectifier, the $\Delta$ -Switch Rectifier, and the VIENNA Rectifier

In Fig. 33, a performance comparison of the six-switch boost PFC rectifier, the  $\Delta$ -switch rectifier, and the VIENNA Rectifier is shown based on the performance indicies defined in Sec. VI-A. The representation is chosen such that for high performance only a small area is covered.

All systems require a similar total chip area, show approximately equal relative losses, approximately the same DM and CM conducted EMI noise levels, and allow for continuous operation in case of a mains phase loss. The main advantage of the three-level characteristic of the VIENNA Rectifier is the significantly lower volume of the



**Fig. 33.** Comparative evaluation of two alternative active boost-type PFC rectifier systems, i.e. the six-switch rectifier according to Fig. 20(b) and the VIENNA Rectifier according to Fig. 17(a). The characteristic of the  $\Delta$ -switch rectifier is shown by a dashed line.

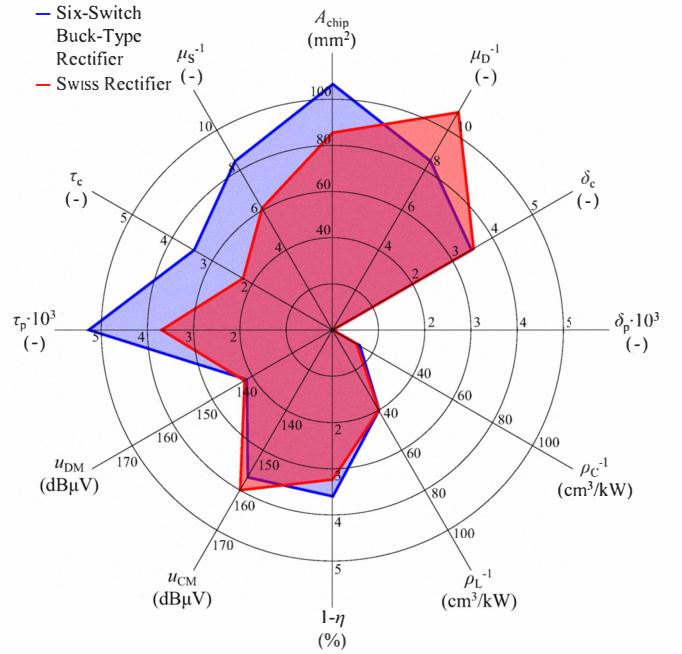
boost inductors compared with the two-level topologies. Only a small difference between the individual systems is given regarding the volume of the output capacitor as the two- and three-level converters have similar rms values of the capacitor currents and in any case a series connection of two electrolytic capacitors is required because of the output voltage of  $U_{\text{pn}} = 700$  V. The center tap for the VIENNA Rectifier thus is inherently available.

In summary, the six-switch converter is characterized by a very simple structure of the power circuit and the VIENNA Rectifier by a relatively small overall volume or a high power density. In addition, for the VIENNA Rectifier (as well as for the  $\Delta$ -switch rectifier) a short circuit of the dc-bus through a faulty control of a power transistor is not possible and for both topologies, power transistors with relatively slow parasitic anti-parallel body diodes can be used.

The use of the  $\Delta$ -switch rectifier, which is relatively complex with regard to the circuit structure and modulation, can be only justified when a three-level topology does not provide significant advantages due to a low mains voltage or if an unidirectional topology is required that prevents energy feedback into the mains by its hardware structure and not only by control. Power supplies in aircraft could serve as an example here.

#### C. Comparison of the Active Six-Switch Buck-Type PFC Rectifier and the SWISS Rectifier

In Fig. 34, a conventional six-switch buck-type PFC rectifier according to Fig. 22(a) and a SWISS Rectifier according to Fig. 26 are compared. Both systems show, with respect to the total chip area requirements, the volume of passive components, the efficiency, and the conducted EMI noise, only very little differences. An increase in efficiency of the six-switch structure would be easily possible by using an explicit freewheeling diode across the dc link. For the SWISS Rectifier, a reduction of the number of power semiconductors can be achieved through modification of the circuit topology according to Fig. 28. In addition, the mains commutated injection switches could be implemented with RC-IGBTs with a low forward voltage drop as an alternative to the SiC JFETs.



**Fig. 34.** Comparative evaluation of two alternative buck-type PFC rectifier systems, i.e. of the active six-switch rectifier according to Fig. 22(e) and the hybrid SWISS Rectifier according to Fig. 26.

In summary, the main advantage of the SWISS Rectifier is not seen in a higher performance but in a dc-dc converter like circuit structure. Accordingly, basic knowledge of the function of a passive diode rectifier of the input stage of the system is sufficient to implement a three-phase PFC rectifier with sinusoidal input current and a controlled output voltage. In particular, no space vector based modulation scheme, which is frequently applied to three-phase converters and typically leads to difficulties when dealing the first time with three-phase systems, has to be implemented.

## VII. CONCLUSIONS

As shown in this paper, a three-phase PFC rectifier functionality can be implemented besides a phase-modular approach with

- 1) direct control of the conduction state of a three-phase rectifier through integrated power transistors or parallel control branches with active power semiconductors, i.e. as an active rectifier or
- 2) by shaping the output currents of a three-phase diode rectifier on the dc side and feedback/injection of the current difference always in that phase which would not conduct current for conventional passive diode rectification, i.e. as a hybrid rectifier with 3<sup>rd</sup> harmonic current injection.

Following these basic concepts, direct three-phase rectifier circuits with boost- or buck-type characteristic are realizable. These circuits advantageously have a bridge topology (at the input) with bridge-legs of identical structure and thus feature an overall bridge symmetry.

For both circuit categories, over the last two decades, a variety of circuit topologies have been proposed. However, in the opinion of the authors, from the category of the boost-type rectifier systems, only the conventional (bidirectional) six-switch converter and the VIENNA Rectifier and from the systems with buck-type characteristic only again the six-switch structure and the SWISS Rectifier, proposed in this paper, are of interest for industrial application. Compared to these four topologies, other circuit concepts show a (significantly) higher complexity of the power and/or the control circuit, or have high component stresses at a lower complexity and a limited operating

range with regard to output voltage range and/or current-to-voltage phase displacement angle at the input. This is of particular importance when operating at unbalanced mains systems or in case of failure of a mains phase.

The selected circuit topologies enable very high efficiencies as a result of the excellent conduction and switching characteristics of modern Si and SiC power semiconductors. Soft-switching concepts are thus not necessary and would also not be accepted by industry due to the increase in complexity resulting from the auxiliary circuit branches with additional losses and due to the typically complex state sequence within a switching period. In general, in industry only circuit topologies are practicable that are well understood not only by the inventors but also by a sufficiently large number of engineers.

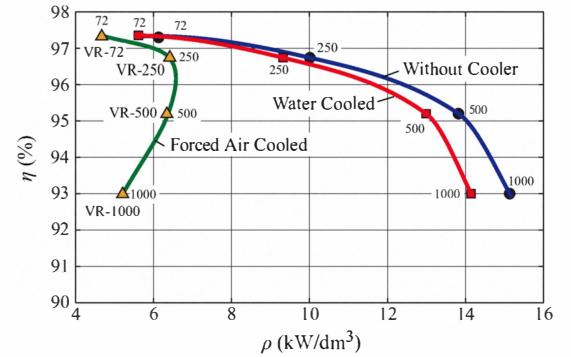
In terms of system complexity, it should be noted that the restriction to unidirectional power flow does not allow a reduction e.g. a halving of the number of active semiconductors or a simpler control scheme. The reason is that ultimately also unidirectional structures have to conduct phase currents of both directions and to generate voltages with both polarities. Only for three-level converters, a clear advantage of unidirectional converters (VIENNA Rectifier) is given compared with bidirectional converters; for the unidirectional system six transistors (with anti-parallel diodes) and six diodes are required, whereas the implementation of a topologically similar bidirectional T-type three-level converter system [84] requires twelve transistors (with anti-parallel diodes).

The main three-phase PWM rectifier circuit topologies, except the SWISS Rectifier, have been already theoretically investigated and experimentally verified in the literature. Therefore, for further academic research, mainly the following relatively narrow topics remain:

- Direct mains (input) current control of buck-type PFC rectifier circuits. [For these systems typically only the output voltage and the output current is directly controlled and/or the mains current is not explicitly included in a feedback loop; thus, particularly for high mains frequencies (800 Hz), current distortions can occur at the intersections of the line-to-line voltages.]
- Parallel operation of a higher number (more than two) converter systems. (High output power levels are often implemented by parallel connection of multiple low-power modules where circulating currents could occur in between the systems.)
- Stability of distributed converter systems. (The constant power characteristic of PFC rectifiers results in a negative differential input impedance, which can lead to instability in combination with the EMI input filter or the inner mains impedance and/or with other converters [85].)

In addition to these topics, especially the multi-objective optimization of converter systems represents a wide and interesting field of research. When developing an industrial systems, besides a defined efficiency and power density, mainly a cost target has to be met, and a certain lifetime has to be guaranteed, i.e. multiple performance indices have to be simultaneously considered. It is therefore essential to understand the mutual dependence of the performance indices in the course of the design, e.g. the trade-off between power density  $\rho$  ( $\text{kW}/\text{dm}^3$ ) and efficiency  $\eta$  (%).

The achievable performance limit (Pareto-Front), i.e. when all degrees of freedom are optimally used, can be determined based on a mathematical model of the system behavior and the design process with a multi-objective optimization (cf. [30], Fig. 26). The influence of individual design parameters, e.g. the switching frequency, can then be immediately identified and/or the necessary parameters for a target performance can be directly calculated. **Fig. 35** shows, as an example, the  $\eta$ - $\rho$ -Pareto-Front based on data of hardware demonstrators of the VIENNA Rectifier with different switching frequencies.



**Fig. 35.**  $\eta$ - $\rho$ -Pareto-Front based on hardware demonstrators of 10kW VIENNA Rectifier systems (the parameter is the switching frequency). The best compromise between the efficiency and the volume determining technologies was identified during the design process for each system. A switching frequency of  $f_P \leq 250$  kHz is recommended for an industrial implementation based on the current state-of-the-art as it leads to a relatively high power density ( $\rho = 6.4 \text{ kW}/\text{dm}^3$ ) and still a high nominal efficiency ( $\eta_{\text{nom}} = 96.7\%$ ), and guarantees a high input current quality also for high mains frequencies as e.g. in More Electric Aircraft (MEA) applications [cf. **Fig. 20(b)**].

Starting from  $f_P = 73$  kHz, an increase in the switching frequency leads, due to the increase of the switching losses and therewith an increase in the heat sink volume, to a reduction of the power density, which cannot be compensated by the possible reduction of the EMI filter. A higher switching frequency, e.g.  $f_P = 250$  kHz is therefore only sensible, if a low distortion of the input current THD<sub>i</sub> must be guaranteed at high mains frequencies as e.g. for MEA applications with  $f_N = 360 \dots 800$  Hz.

The  $\eta$ - $\rho$ -Pareto-Front, besides for the specification of the design parameters, can be also advantageously used for a comparison of alternative circuit concepts, e.g. in the course of an industrial development process. Each circuit topology is then characterized by the associated performance limit and thus the difference in performance and the suitability of a concept to meet the target performance is immediately visible.

However, in order to obtain a complete picture, also the relation between  $\eta$  and  $\rho$  and the relative costs  $\sigma$  ( $\text{kW}/\$$ ), i.e. also the  $\eta$ - $\sigma$ - and  $\rho$ - $\sigma$ -Pareto-Fronts should be considered. Furthermore, the impact of new technologies, e.g. the replacement of Si by SiC/GaN power semiconductors on the system performance could be analyzed using the Pareto-Front. The resulting shift of the performance limits then directly shows the possibility of improving a selected concept and the resulting costs can be immediately determined (cf. [30], Fig. 26).

Such analysis so far only has been performed only for single-phase systems [8], and is therefore seen as a focus of future academic research in the field of three-phase PWM rectifier systems and as a key topic in power electronics in general.

#### ACKNOWLEDGMENT

The authors would like to thank Dr. Michael Hartmann for providing figures and data of the VIENNA Rectifier and the  $\Delta$ -switch rectifier from his Ph.D. thesis [53] and Dr. Johann Miniboeck for providing data of the VR-73 VIENNA Rectifier and the bidirectional TCM ZVS dc–dc converter hardware demonstrator.

#### REFERENCES

- [1] P. Walther, "A new rectifier system high efficient, high dense, modular, quick to install and superior for service," in *Proc. 15th Int. Telecom. Energy Conf. INTELEC '93*, vol. 2, Sep. 27–30, 1993, pp. 247–250.
- [2] A. Pietkiewicz and D. Tollik, "Cost/performance considerations for 1-phase input current shapers," in *Proc. 16th Int. Telecom. Energy Conf. INTELEC '94*, Apr. 11–15, 1994, pp. 165–170.

- [3] A. Kuperman, U. Levy, J. Goren, A. Zafranski, and A. Savernin, "High power Li-ion battery charger for electric vehicle," in *Proc. 7th Int. Compatibility and Power Electronics Conf.-Workshop CPE '11*, Jun. 1–3, 2011, pp. 342–347.
- [4] J. W. Kolar, T. Friedli, and M. Hartmann, "Three-phase PFC rectifier and ac-ac converter systems – Part I, Tutorial," in *presented at 26th IEEE Applied Power Electronics Conf. and Exposition APEC '11*. presented at 26th IEEE Applied Power Electronics Conf. and Exposition APEC '11, Mar. 6–10, 2011.
- [5] D. A. Paice, *Power Electronics Converter Harmonics: Multipulse Methods for Clean Power*. John Wiley & Sons, 1999.
- [6] P. Pejovic, *Three-Phase Diode Rectifiers with Low Harmonics*. Springer Science+Business Media, 2007.
- [7] T. Sakkos, V. Sarv, and J. Soojärvi, "Optimum diode-switched active filters for power factor correction of single- and three-phase diode rectifiers with capacitive smoothing," in *Proc. 7th European Conf. on Power Electron. and Appl. EPE '97*, Sep. 8–10, 1997, pp. 870–875.
- [8] J. W. Kolar and H. Ertl, "Status of the techniques of three-phase rectifier systems with low effects on the mains," in *Proc. 21st Int. Telecom. Energy Conf. INTELEC '99*, Jun. 6–9, 1999, pp. 14–1 1–16.
- [9] M. Rastogi, R. Naik, and N. Mohan, "Optimization of a novel dc-link current modulated interface with 3-phase utility systems to minimize line current harmonics," in *Proc. 23d IEEE Power Electronics Specialists Conf. PESC '92*, Jun. 29–Jul. 3, 1992, pp. 162–167.
- [10] R. Naik, M. Rastogi, N. Mohan, R. Nilssen, and C. P. Henze, "A magnetic device current injection in a three-phase sinusoidal-current utility interface," in *Proc. 28th IEEE Industry Applications Society Annual Meeting IAS '93*, Oct. 2–8, 1993, pp. 926–930.
- [11] S. Kim, P. Enjeti, D. Rendusara, and I. J. Pitel, "A new method to improve THD and reduce harmonics generated by a three phase diode rectifier type utility interface," in *Proc. 29th IEEE Industry Applications Society Annual Meeting IAS '94*, Oct. 2–6, 1994, pp. 1071–1077.
- [12] Y. Nishida, Y. Ohgoe, M. Nakaoka, and A. Maeda, "A simple three-phase boost-mode PFC rectifier," in *Proc. 31th IEEE Industry Applications Society Annual Meeting IAS '96*, vol. 2, Oct. 6–10, 1996, pp. 1056–1061.
- [13] H. Yoo and S.-K. Sul, "A novel approach to reduce line harmonic current for a three-phase diode rectifier-fed electrolytic capacitor-less inverter," in *Proc. 24th IEEE Applied Power Electronics Conf. and Exposition APEC '09*, Feb. 15–19, 2009, pp. 1897–1903.
- [14] ——, "A new circuit design and control to reduce input harmonic current for a three-phase ac machine drive system having a very small dc-link capacitor," in *Proc. 25th IEEE Applied Power Electronics Conf. and Exposition APEC '10*, Feb. 21–25, 2010, pp. 611–618.
- [15] H. Ertl and J. W. Kolar, "A constant output current three-phase diode bridge rectifier employing a novel "electronic smoothing inductor"," *IEEE Trans. Ind. Electron.*, vol. 52, no. 2, pp. 454–461, Apr. 2005.
- [16] K. Mino, M. L. Heldwein, and J. W. Kolar, "Ultra compact three-phase rectifier with electronic smoothing inductor," in *Proc. 20th IEEE Applied Power Electronics Conf. and Exposition APEC '05*, vol. 1, Mar. 6–8, 2005, pp. 522–528.
- [17] T. Takaku, G. Homma, T. Isober, S. Igarashi, Y. Uchida, and R. Shimada, "Improved wind power conversion system using magnetic energy recovery switch (MERS)," in *Proc. 40th IEEE Industry Applications Society Annual Meeting IAS '05*, vol. 3, Oct. 2–6, 2005, pp. 2007–2012.
- [18] J. A. Wiik, F. D. Widjaya, T. Isobe, T. Kitahara, and R. Shimada, "Series connected power flow control using magnetic energy recovery switch (MERS)," in *Proc. IEEE/IEEJ Power Conversion Conf. PCC '07*, Apr. 2–5, 2007, pp. 983–990.
- [19] K. D. Ngo, "Topology and analysis in PWM inversion, rectification, and cyclconversion," Ph.D. dissertation, California Institute of Technology, 1984.
- [20] J. W. Kolar, H. Sree, U. Drozenik, N. Mohan, and F. C. Zach, "A novel three-phase three-switch three-level high power factor SEPIC-type ac-to-dc converter," in *Proc. 12th Applied Power Electronics Conf. and Exposition APEC '97*, vol. 2, Feb. 23–27, 1997, pp. 657–665.
- [21] L. Huber, L. Gang, and M. M. Jovanovic, "Design-oriented analysis and performance evaluation of buck PFC front-end," in *Proc. 24th IEEE Applied Power Electronics Conf. and Exposition APEC '09*, Feb. 15–19, 2009, pp. 1170–1176.
- [22] V. Vlatkovic, D. Borojevic, and F. C. Lee, "A zero-voltage switched, three-phase isolated PWM buck rectifier," *IEEE Trans. Power Electron.*, vol. 10, no. 2, pp. 148–157, 1995.
- [23] J. W. Kolar, U. Drozenik, and F. C. Zach, "VIENNA Rectifier II – a novel single-stage high-frequency isolated three-phase PWM rectifier system," in *Proc. 13th IEEE Applied Power Electronics Conf. and Exposition APEC '98*, vol. 1, Feb. 15–19, 1998, pp. 23–33.
- [24] D. S. Greff and I. Barbi, "A single-stage high-frequency isolated three-phase ac/dc converter," in *Proc. 32nd IEEE Industrial Electronics Society Conf. IECON '10*, Nov. 6–10, 2006, pp. 2648–2653.
- [25] J. Miniboeck, R. Greul, and J. W. Kolar, "Evaluation of a delta-connection of three single-phase unity power factor rectifier modules ( $\Delta$ -rectifier) in comparison to a direct three-phase rectifier realization," in *Proc. 23rd Int. Telecom. Energy Conf. INTELEC '01*, Oct. 14–18, 2001, pp. 446–454.
- [26] R. Greul, S. D. Round, and J. W. Kolar, "Analysis and control of a three-phase, unity power factor Y-Rectifier," *IEEE Trans. Power Electron.*, vol. 22, no. 5, pp. 1900–1911, Sep. 2007.
- [27] R. Greul, "Modulare Dreiphasen Pulsgleichrichtersysteme," Ph.D. dissertation, no. 16370, ETH Zurich, 2005.
- [28] J. W. Kolar, "Vorrichtung zur Regelung der Phasenzwischenkreisspannungen einer Sternschaltung einphasiger Pulsgleichrichtersysteme in Analogie zu Dreiphasen-Dreipunkt-Pulsgleichrichtersystemen," Swiss Patent, 2009.
- [29] J. Biela, U. Drozenik, F. Krenn, J. Miniboeck, and J. W. Kolar, "Novel three-phase Y-rectifier cyclic 2-out-of-3 dc output voltage balancing," in *Proc. 29th Int. Telecom. Energy Conf. INTELEC '07*, Sep. 30 – Oct. 4, 2007, pp. 677–685.
- [30] J. W. Kolar, J. Biela, and J. Miniboeck, "Exploring the Pareto front of multi-objective single-phase PFC rectifier design optimization – 99.2% efficiency vs. 7 kW/dm<sup>3</sup> power density," in *Proc. 6th IEEE Int. Power Electronics and Motion Control Conf. IPMEC '09*, May 17–20, 2009, pp. 1–21.
- [31] D. Chapman, D. James, and C. J. Tuck, "A high density 48V 200A rectifier with power factor correction – an engineering overview," in *Proc. 15th Int. Telecom. Energy Conf. INTELEC '93*, vol. 1, Sep. 27–30, 1993, pp. 118–125.
- [32] M. Karlsson, C. Thoren, and T. Wolpert, "A novel approach to the design of three-phase ac/dc power converters with unity power factor," in *Proc. 21st Int. Telecom. Energy Conf. INTELEC '99*, Jun. 6–9, 1999, pp. 5–1–5–7.
- [33] ——, "Practical considerations concerning a novel 6 kW three-phase ac/dc power converter with unity power factor," in *Proc. 22nd Int. Telecom. Energy Conf. INTELEC '00*, Sep. 10–14, 2000, pp. 28–33.
- [34] R. Ridley, S. Kern, and B. Fulz, "Analysis and design of a wide input range power factor correction circuit for three-phase applications," in *Proc. 8th Applied Power Electronics Conf. and Exposition APEC '93*, Mar. 7–11, 1993, pp. 299–305.
- [35] J. W. Kolar, U. Drozenik, J. Miniboeck, and H. Ertl, "A new concept for minimizing high-frequency common-mode EMI of three-phase PWM rectifier systems keeping high utilization of the output voltage," in *Proc. 15th IEEE Applied Power Electronics Conf. and Exposition APEC '00*, vol. 1, Feb. 6–10, 2000, pp. 519–527.
- [36] R. Grinberg, F. Canales, and M. Paakkinnen, "Comparison study of full-bridge and reduced switch count three-phase voltage source inverters," in *Proc. 7th Int. Compatibility and Power Electronics Conf.-Workshop CPE '11*, Jun. 1–3, 2011, pp. 270–275.
- [37] Infineon, *CoolMOS C3 900 V – First 900V high voltage power MOSFET using charge compensation principle*, 2008.
- [38] B. Weis, M. Braun, and P. Friedrichs, "Turn-off and short circuit behaviour of 4H SiC JFETs," in *Proc. 36th Industry Applications Society Annual Meeting IAS '01*, vol. 1, Sep. 30 – Oct. 4, 2001, pp. 365–369.
- [39] T. Friedli, S. D. Round, and J. W. Kolar, "A 100kHz SiC Sparse Matrix Converter," in *Proc. 38th IEEE Power Electronics Specialists Conf. PESC '07*, Jun. 17–21, 2007, pp. 2148–2154.
- [40] D. Aggeler, J. Biela, and J. W. Kolar, "Controllable du/dt behaviour of the SiC MOSFET/JFET cascode – an alternative hard commutated switch for telecom applications," in *Proc. 25th IEEE Applied Power Electronics Conf. and Exposition APEC '10*, Feb. 21–25, 2010, pp. 1584–1590.
- [41] B. Hull, M. Das, F. Husna, R. Callanan, A. Agarwal, and J. Palmour, "20 A, 1200 V 4H-SiC DMOSFETs for energy conversion systems," in *Proc. 1st IEEE Energy Conversion Congress and Exposition ECCE '09*, Sep. 20–24, 2009, pp. 112–119.
- [42] J. W. Kolar, H. Ertl, and F. C. Zach, "Space vector-based analytical analysis of the input current distortion of a three-phase discontinuous-mode boost rectifier system," in *Proc. 24th IEEE Power Electronics Specialists Conf. PESC '93*, Jun. 20–24, 1993, pp. 696–703.
- [43] J. Sun and H. Grotstollen, "Averaged modeling and analysis of resonant converters," in *Proc. 24th IEEE Power Electronics Specialists Conf. PESC '93*, Jun. 20–24, 1993, pp. 707–713.
- [44] Q. Huang and F. C. Lee, "Harmonic reduction in a single-switch, three-phase boost rectifier with high order harmonic injected PWM," in *Proc.*

- [27th IEEE Power Electronics Specialists Conf. PESC '96, vol. 2, Jun. 23–27, 1996, pp. 1266–1271.]
- [45] D. J. Perreault and J. G. Kassakian, “Design and evaluation of a cellular rectifier system with distributed control,” in *Proc. PESC 98 Record Power Electronics Specialists Conf. 29th Annual IEEE*, vol. 1, May 17–22, 1998, pp. 790–797.
- [46] P. Barbosa, F. Canales, J.-C. Crebier, and F. C. Lee, “Interleaved three-phase boost rectifiers operated in the discontinuous conduction mode: analysis, design considerations and experimentation,” *IEEE Trans. Power Electron.*, vol. 16, no. 5, pp. 724–734, 2001.
- [47] J. C. Salmon, “Comparative evaluation of circuit topologies for 1-phase and 3-phase boost rectifiers operated with a low current distortion,” in *Proc. Canadian Conf. Electrical and Computer Engineering*, Sep. 25–28, 1994, pp. 30–33.
- [48] R. Naik, M. Rastogi, and N. Mohan, “Third-harmonic modulated power electronics interface with 3-phase utility to provide a regulated dc output and to minimize line-current harmonics,” in *Proc. IEEE Annual Industry Applications Society Annual Meeting IAS '92*, 1992, pp. 689–694.
- [49] J. C. Salmon, “Operating a three-phase diode rectifier with a low-input current distortion using a series-connected dual boost converter,” *IEEE Trans. Power Electron.*, vol. 11, no. 4, pp. 592–603, Jul. 1996.
- [50] S. Kim, P. Enjeti, P. Packebush, and I. Pitel, “A new approach to improve power factor and reduce harmonics in a three phase diode rectifier type utility interface,” in *Proc. 28th IEEE Industry Applications Society Annual Meeting IAS '93*, Oct. 2–8, 1993, pp. 993–1000.
- [51] J. W. Kolar, J. Ertl, and F. C. Zach, “Realization consideration for unidirectional three-phase PWM rectifier systems with low effects on the mains,” in *Proc. 6th Europ. Power Electronics Motion Control Conf. PEMC '1990*, vol. 2, Oct. 1–3, 1990, pp. 560–565.
- [52] M. Hartmann, J. Miniboeck, and J. W. Kolar, “A three-phase delta switch rectifier for more electric aircraft applications employing a novel PWM current control concept,” in *Proc. 24th IEEE Applied Power Electronics Conf. and Exposition APEC '09*, Feb. 15–19, 2009, pp. 1633–1640.
- [53] M. Hartmann, “Ultra-compact and ultra-efficient three-phase PWM rectifier systems for more electric aircraft,” Ph.D. dissertation, no. 19755, ETH Zurich, 2011.
- [54] N. Noor, J. Ewanchuk, and J. Salmon, “PWM current controllers for a family of 3-switch utility rectifier topologies,” in *Proc. Canadian Conf. Electrical and Computer Engineering CCECE '07*, Apr. 22–26, 2007, pp. 1141–1144.
- [55] J. W. Kolar and F. C. Zach, “A novel three-phase three-switch three-level pwm rectifier,” in *Proc. 28th Power Conversion Conference, PCIM '94*, Jun. 28–30, 1994, pp. 125–138.
- [56] Y. Zhao, Y. Li, and T. A. Lipo, “Force commutated three level boost type rectifier,” in *Proc. 28th IEEE Industry Applications Society Annual Meeting IAS '93*, Oct. 2–8, 1993, pp. 771–777.
- [57] M. L. Heldwein, S. A. Mussa, and I. Barbi, “Three-phase multilevel PWM rectifiers based on conventional bidirectional converters,” *IEEE Trans. Power Electron.*, vol. 25, no. 3, pp. 545–549, Mar. 2010.
- [58] F. Stögerer, J. Minibock, and J. W. Kolar, “Implementation of a novel control concept for reliable operation of a VIENNA Rectifier under heavily unbalanced mains voltage conditions,” in *Proc. 34nd IEEE Power Electronics Specialists Conf. PESC '01*, vol. 3, Jun. 17–21, 2001, pp. 1333–1338.
- [59] J. Minibock, F. Stögerer, and J. W. Kolar, “A novel concept for mains voltage proportional input current shaping of a VIENNA Rectifier eliminating controller multipliers, Part I – Basic theoretical considerations and experimental verification,” in *Proc. 16th IEEE Applied Power Electronics Conf. and Exposition APEC '01*, vol. 1, Mar. 4–8, 2001, pp. 582–586.
- [60] F. Stögerer, J. Minibock, and J. W. Kolar, “A novel concept for mains voltage proportional input current shaping of a VIENNA Rectifier eliminating controller multipliers, Part II – Operation for heavily unbalanced mains phase voltages and in wide input voltage range,” in *Proc. 16th IEEE Applied Power Electronics Conf. and Exposition APEC '01*, vol. 1, Mar. 4–8, 2001, pp. 587–591.
- [61] J. W. Kolar, U. Drofenik, and F. C. Zach, “Current handling capability of the neutral point of a three-phase/switch/level boost-type PWM (VIENNA) Rectifier,” in *Proc. 27th IEEE Power Electronics Specialists Conf. PESC '96*, vol. 2, Jun. 23–27, 1996, pp. 1329–1336.
- [62] D. Krahenbuhl, C. Zwyssig, K. Bitterli, M. Imhof, and J. W. Kolar, “Evaluation of ultra-compact rectifiers for low power, high-speed, permanent-magnet generators,” in *Proc. 35th IEEE Industrial Electronics Society Conf. IECON '09*, Nov. 3–5, 2009, pp. 448–455.
- [63] T. Friedli, S. D. Round, D. Hassler, and J. W. Kolar, “Design and performance of a 200 kHz All-SiC JFET current source converter,” in *Proc. 43rd IEEE Industry Applications Society Annual Meeting IAS '08*, Oct. 5–9, 2008, pp. 1–8.
- [64] F. Schafmeister, “Indirekte Sparse Matrix Konverter,” Ph.D. dissertation, no. 17428, ETH Zurich, 2007.
- [65] J. W. Kolar, T. Friedli, and M. Hartmann, “Three-phase PFC rectifier and ac-ac converter systems – Part II, Tutorial,” in *presented at 26th IEEE Applied Power Electronics Conf. and Exposition APEC '11*, Mar. 6–10, 2011.
- [66] T. C. Green, M. H. Taha, N. A. Rahim, and B. W. Williams, “Three-phase step-down reversible ac-dc power converter,” *IEEE Trans. Power Electron.*, vol. 12, no. 2, pp. 319–324, Mar. 1997.
- [67] T. Nussbaumer, G. Gong, M. L. Heldwein, and J. W. Kolar, “Control-oriented modeling and robust control of a three-phase buck+boost PWM rectifier (VRX-4),” in *Proc. 40th IEEE Industry Applications Society Annual Meeting IAS '05*, vol. 1, Oct. 2–6, 2005, pp. 169–176.
- [68] T. Nussbaumer and J. W. Kolar, “Advanced modulation scheme for three-phase three-switch buck-type PWM rectifier preventing mains current distortion originating from sliding input filter capacitor voltage intersections,” in *Proc. 34th IEEE Power Electronics Specialist Conf. PESC '03*, vol. 3, Jun. 15–19, 2003, pp. 1086–1091.
- [69] A. Stupar, T. Friedli, J. Miniboeck, M. Schweizer, and J. W. Kolar, “Towards a 99% efficient three-phase buck-type PFC rectifier for 400 V dc distribution systems,” in *Proc. 26th IEEE Applied Power Electronics Conf. and Exposition APEC '11*, Mar. 6–10, 2011, pp. 505–512.
- [70] M. Hartmann, T. Friedli, and J. W. Kolar, “Three-phase unity power factor mains interfaces of high power EV battery charging systems,” in *Power Electronics for Charging Electric Vehicles ECPE Workshop*, Mar. 21–22, 2011.
- [71] C. Marxgut, J. Biela, and J. W. Kolar, “Interleaved triangular current mode (TCM) resonant transition, single-phase PFC rectifier with high efficiency and high power density,” in *Proc. IEEE Int. Power Electronics Conf. IPEC '10*, Jun. 21–24, 2010, pp. 1725–1732.
- [72] J. W. Kolar, “Netzrückwirkungssarmes Dreiphasen-Stromzwischenkreis-Pulsgleichrichtersystem mit weitem Stellbereich der Ausgangsspannung,” Worldwide Patent WO 01/50583 A1, 2001.
- [73] T. Nussbaumer, K. Mino, and J. W. Kolar, “Design and comparative evaluation of three-phase buck-boost and boost-buck unity power factor PWM rectifier systems for supplying variable dc voltage link converters,” in *Proc. 10th European Power Quality Conf. PCIM '04*, May 25–27, 2004, pp. 126–135.
- [74] J. W. Kolar, H. Ertl, and F. C. Zach, “Analysis of the duality of three phase PWM converters with dc voltage link and dc current link,” in *Proc. 24th IEEE Industry Applications Society Annual Meeting IAS '89*, Oct. 1–5, 1989, pp. 724–737.
- [75] M. Alfayyoumi, A. H. Nayfeh, and D. Borojevic, “Input filter interactions in dc-dc switching regulators,” in *Proc. 30th IEEE Power Electronics Specialists Conf. PESC '99*, vol. 2, Jun. 27–Jul. 1, 1999, pp. 926–932.
- [76] F. Luo, X. Zhang, D. Borojevic, P. Mattevelli, J. Xue, F. Wang, and N. Gazel, “On discussion of ac and dc side EMI filters design for conducted noise suppression in dc-fed three phase motor drive system,” in *Proc. 26th IEEE Applied Power Electronics Conf. and Exposition APEC '11*, Mar. 6–11, 2011, pp. 667–672.
- [77] R. W. Erickson, “Optimal single resistor damping of input filters,” in *Proc. 14th Applied Power Electronics Conf. and Exposition APEC '99*, vol. 2, Mar. 14–18, 1999, pp. 1073–1079.
- [78] K. Ragg, T. Nussbaumer, and J. W. Kolar, “Guideline for a simplified differential-mode EMI filter design,” *IEEE Trans. Ind. Electron.*, vol. 57, no. 3, pp. 1031–1040, Mar. 2010.
- [79] T. Friedli, “Comparative evaluation of Si and SiC three-phase ac/ac converter systems,” Ph.D. dissertation, no. 19194, ETH Zurich, 2010.
- [80] M. L. Heldwein, “EMC filtering of three-phase PWM converters,” Ph.D. dissertation, no. 17554, ETH Zurich, 2007.
- [81] Infineon, *Power Cycling Capability for Modules*, 2011, rev. 4.
- [82] U. Drofenik and J. W. Kolar, “Analyzing the theoretical limits of forced air-cooling by employing advanced composite materials with thermal conductivities > 400 W/mK,” in *Proc. 4th Int. Conf. on Integrated Power Electronic Systems CIPS '06*, Jun. 7–9, 2006, pp. 323–328.
- [83] ———, “Sub-optimum design of a forced air cooled heat sink for simple manufacturing,” in *Proc. 4th IEEE/IEEJ Power Conversion Conf. PCC '07*, Apr. 2–5, 2007, pp. 1189–1194.
- [84] M. Schweizer, I. Lizama, T. Friedli, and J. W. Kolar, “Comparison of the chip area usage of 2-level and 3-level voltage source converter topologies,” in *Proc. 36th IEEE Industrial Electronics Society Conf. IECON '10*, Nov. 7–11, 2010, pp. 391–396.
- [85] M. Schweizer and J. W. Kolar, “Shifting input filter resonances – An intelligent converter behavior for maintaining system stability,” in *Proc. IEEE/IEEJ Int. Power Electronics Conf. IPEC '10*, Jun. 21–24, 2010, pp. 906–913.