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The Essence of Three-Phase PFC Rectifier Systems - Part II

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***Abstract*—The second part of the essence of three-phase PFC Rectifier Systems is dedicated to a comparative evaluation of four active three-phase PFC rectifiers that are of interest for industrial application: the active six-switch boost-type PFC rectifier, the VIENNA Rectifier (VR), the active six-switch buck-type PFC rectifier, and the SWISS Rectifier. Typical dynamic feed-back control structures of the considered topologies are shown, and analytical equations for calculating the current stresses of the power semiconductors are provided. In addition, EMI filtering is discussed. The rectifier systems are assessed and compared based on simple and demonstrative performance indices such as the semiconductor stresses, the required semiconductor chip area, the volume of the main passive components, the DM and CM conducted EMI noise levels, and the efficiency. Two implementation variants, a more advanced one using SiC JFETs and SiC Schottky diodes and one using Si IGBTs and SiC Schottky diodes, are considered. The comparison is extended with selected examples of hardware demonstrators of VR systems that are optimized for efficiency and/or power density. This allows to determine the tradeoff between efficiency and power density and to quantify a typical efficiency versus power density limit (Pareto-Front) for practical three-phase PFC rectifier systems using standard printed circuit board interconnection technology.**

***Index Terms*—Ac–dc converter, boost, buck, comparison, evaluation, PFC rectifier, PFC, PWM rectifier, rectifier, three-phase, SWISS rectifier, VIENNA rectifier.**

I. INTRODUCTION

NUMEROUS concepts for three-phase Power Factor Corrected (PFC) rectifier systems have been proposed and analyzed over the last decades. In Part I of this paper (cf. [1]), three-phase PFC rectifier topologies are derived from known single-phase systems and passive three-phase diode rectifiers. The individual topologies are classified into passive, hybrid, and active PFC rectifier systems, and their basic functionality and operating principle are briefly described. Criteria for the selection of suitable three-phase PFC rectifier topologies are determined, which can be summarized as follows: sinusoidal input currents (typically a $\mathrm{THD_i} < 5\%$ is required) ohmic fundamental mains behavior, controlled dc output voltage that can be lower or higher than the amplitude of the line-to-line input voltage, single-stage power conversion, no galvanic isolation, unidirectional power flow possibly with (limited) capability of reactive power compensation, simple circuit topology that features "phase symmetry" and/or "bridge symmetry" (according to [1, p. 4]), simple modulation and control schemes, possibility to achieve high efficiency and/or high power density, and use in industry or potential for future industrial application.

No circuit topologies are considered that fundamentally demand low frequency passive components, e.g., dimensioned for sixfold mains frequency, passive multipulse transformer rectifier systems, or hybrid rectifier circuits with passive third harmonic current injection network as they can hardly meet the aforementioned requirements in terms of high power density and control also partly. Direct single-stage (matrix-converter-based) rectifier systems or soft-switching topologies are also not investigated as they typically require (more) complex modulation and control schemes to guarantee safe operation and/or additional hardware, e.g., in auxiliary branches to enable soft commutation, compared with hard-commutated, pulse-width-modulated active PFC rectifier systems.

Apart from PFC rectifiers with boost-type characteristic, also buck-type PFC rectifier systems are discussed in order to consider circuit topologies that can provide a controlled output voltage between 0 and $\sqrt{3}/2 \approx 86.6\%$ of the amplitude of the line-to-line input voltage for sinusoidal modulation. Buck-type PFC rectifier systems are expected to provide an option in future for the supply of dc distribution grids or possibly also for the charging of electric vehicle batteries. The complementation and classification of the knowledge base of three-phase buck-type PFC rectifier systems led to a novel hybrid circuit concept, i.e., the SWISS Rectifier, that is characterized by a low complexity of the power circuit and control and is, therefore, also evaluated in this paper.

As a result of the first part of this paper, four active PFC rectifier topologies were identified which meet the aforementioned requirements and are comparatively evaluated in this paper (Part II). The respective circuit topologies are shown in Fig. 1: the active six-switch boost-type PFC rectifier ([cf. Fig. 1(a)], Section IV-A4 in [1]) and the VIENNA Rectifier (VR) ([cf. Fig. 1(b)], Section IV-A3 in [1]) from the category of boost-type rectifier systems. The active six-switch buck-type PFC rectifier ([cf. Fig. 1(c)], Section IV-B1 in [1]) and the SWISS Rectifier ([cf. Fig. 1(d)], Section IV-B3 in [1]) are selected from the category of buck-type rectifier systems. The active six-switch boost-type PFC rectifier enables bidirectional power

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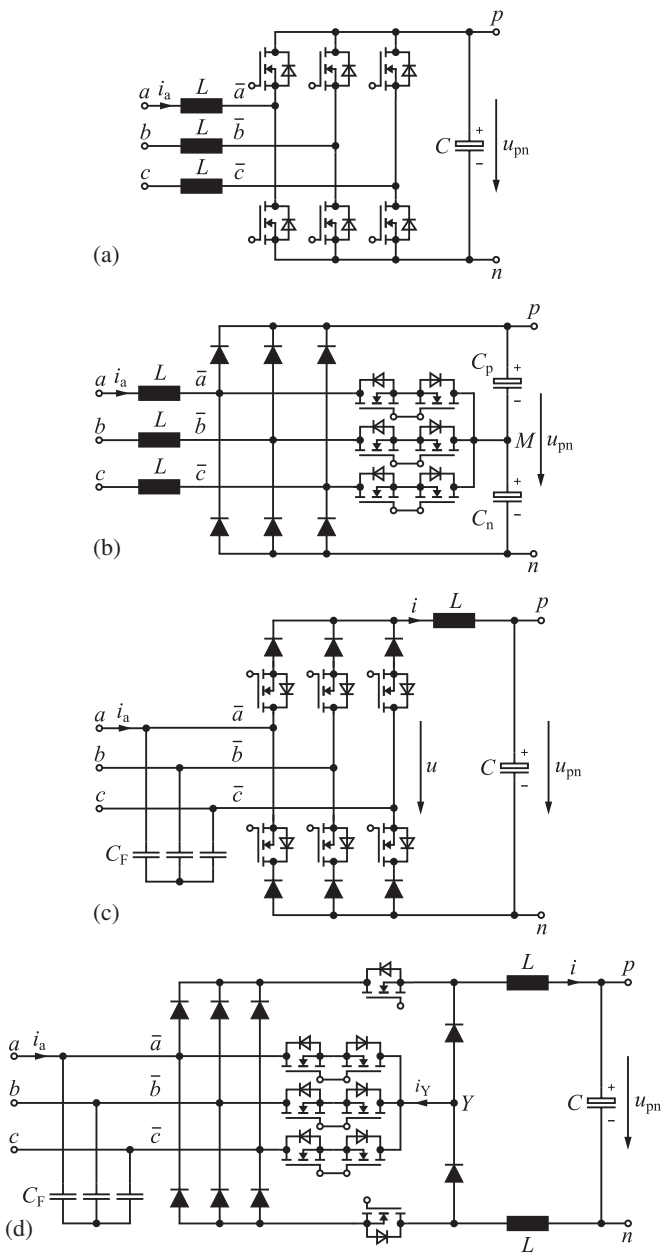


Fig. 1. Circuit topologies of the four considered three-phase active boost- and buck-type PFC rectifier systems. (a) Six-switch boost-type PFC rectifier (bidirectional power flow), (b) VIENNA Rectifier (unidirectional power flow), (c) six-switch buck-type PFC rectifier (bidirectional power flow, if the polarity of the dc output voltage $u_{\rm pn}$ can be inverted), and (d) SWISS Rectifier (unidirectional power flow).

flow, whereas the active six-switch buck-type PFC rectifier provides bidirectional power flow capability only if the polarity of the output voltage $u_{\rm pn}$ can be inverted. The other two rectifier topologies allow only for unidirectional power flow. It should be noted that regarding complexity, the restriction to unidirectional power flow does not necessarily lead to a reduction of the number of the active semiconductors or a simpler modulation and control since unidirectional structures also have to conduct phase currents of both directions and generate input voltages of the switching stage with both polarities. A clear advantage of unidirectional converters regarding complexity compared with bidirectional converters is only given for three-level converters (e.g., the VR).

In this paper, also for systems employing power semiconductors with high blocking voltage stress (defined by the mains line-to-line voltage or a dc-link voltage even higher than the mains line-to-line), power MOSFETs are shown as switching elements in the circuit schematics. This should highlight the generally existing requirement of high switching frequency or high power density.

Section II briefly describes the basic control structures of the selected boost- and buck-type PFC rectifier systems, and thus provides an extension to Part I of this paper which describes the basic properties and function of three-phase rectifiers. In Section III, in the sense of providing support for the dimensioning of the circuits, the current stresses of the power semiconductor components are briefly summarized in the form of simple analytical expressions, and the Differential Mode (DM) and Common Mode (CM) EMI filtering of the rectifier systems are discussed. Section IV is dedicated to the main topic of this paper and presents a comparative evaluation of the selected boost-type and buck-type PFC rectifier systems. State-of-the-art SiC JFET power transistors and SiC Schottky diodes are used for the evaluation and compared with a more standard implementation using Si IGBT devices with SiC Schottky diodes. Performance indices are identified for this purpose that enable a demonstrative and simple rectifier system assessment, which is intended to serve as an aid for the choice of circuit concepts in industrial development projects. In order to conclude this comparison, key performance figures such as the achieved efficiency η and power density ρ of implemented VR hardware demonstrators with a switching frequency range from 72 kHz to 1 MHz are identified. This allows to determine the tradeoff between efficiency and power density and to quantify a typical efficiency versus power density limit (η-ρ-Pareto Front) for practical three-phase PFC rectifier systems using standard multilayer printed circuit board assembly technology. Finally, in Section V, a compilation of the key findings is given, the achievable performance limits are discussed, and the core topics of future research on three-phase PFC rectifier systems are briefly discussed.

II. THREE-PHASE PFC RECTIFIER CONTROL

The first part of this paper [1] describes the basic function and modulation of three-phase PFC rectifier systems. In order to complete the overview, typical control structures of the four considered active boost- and buck-type rectifier systems are shown, and their main control properties are briefly discussed. Thereby, only cascaded feed-back control schemes using conventional Pulse Width Modulation (PWM) are considered. Space vector-based control or nonlinear control schemes [2]–[4] are not discussed for the sake of brevity and since PFC rectifier systems often have to operate at phase loss, i.e., if only two phases are available. Under this operating condition, phase-oriented PWM-based control [5] is more appropriate (less complex) than space vector-based control, opposed to, e.g., ac drives, where space vector control schemes enable a consistent mathematical description from the inverter stage to the motor shaft.

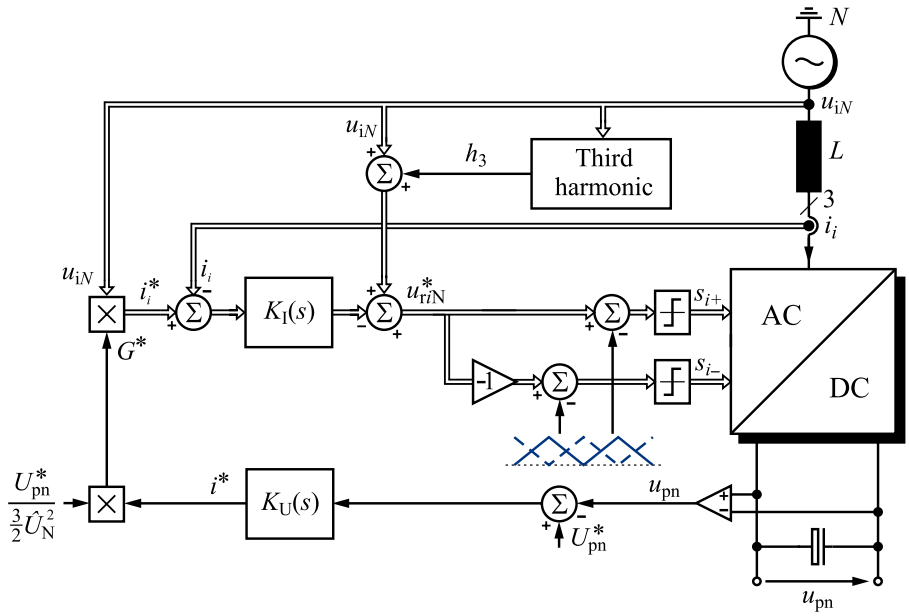


Fig. 2. Control structure of the active six-switch boost-type PFC rectifier with superimposed control of the output voltage $u_{\rm pn}$ and subordinate phase current control with feed-forward of the mains phase voltages. In order to increase the output voltage control range, a third harmonic is superimposed to the mains voltage feed-forward signal.

A. Six-Switch Boost-Type PFC Rectifier

A typical control structure of a six-switch boost-type PFC rectifier is given in Fig. 2. It consists of a superimposed voltage controller, often implemented as a PI-type controller, defining the reference value of the fundamental frequency conductance G^* and/or the power delivered to the output, and subordinate phase current controllers. Simple P-type current controllers can be used if feed-forward of the mains voltages is applied. In order to increase the output voltage control range, a voltage component with three times the mains frequency (third harmonic) is added to the mains voltage feed-forward signal.

B. VIENNA *Rectifier*

The control structure of the VR is shown in Fig. 3(a) with a superimposed voltage controller, defining the reference value of the fundamental frequency conductance G^* and/or the power delivered to the output, and subordinate phase current controllers similar to the control structure shown for the six-switch boost-type PFC rectifier. In order to increase the output voltage control range, again a third harmonic is superimposed to the mains voltage feed-forward signal [6].

The balancing of the two partial output voltages, which is required due to the integration of the capacitive midpoint of the output voltage into the system function, can be implemented by adding an offset i_0^* to the phase current reference values. As shown in Figs. 3(b) and (c), for the input phase currents $i_a > 0$ and $i_b, i_c < 0$, redundant switching states $(1\,0\,0)$ and $(0\,1\,1)$ regarding the voltage formation on the ac side occur. (The switching state is represented by phase switching functions s_i, and/or (s_a,s_b,s_c), where $s_i = 1$ $(i = \{a, b, c\})$ indicates that the corresponding four-quadrant switch is switched on and $s_i = 0$ indicates that it is switched off.) A positive offset $i_0^* > 0$ leads to an increase of the relative ON-time of switching state $(1\,0\,0)$ compared with state $(0\,1\,1)$ and a negative offset $i_0^* < 0$ to a relative decrease compared with state $(1\,0\,0)$. Correspondingly, mainly the lower or upper output capacitor is charged, and thus the two output voltages $u_{\rm pM}$ and $u_{\rm Mn}$ can be balanced.

C. Six-Switch Buck-Type PFC Rectifier

Similar to the boost-type rectifier systems, a superimposed output voltage controller with an underlying current controller according to Fig. 4 can be used for the control of the buck-type PFC rectifier, whereupon possibly active damping of the input filter has to be applied [7]–[9]. The output voltage controller is typically implemented as a PI-type controller, whereas for the current controller a P-type controller is sufficient if an output voltage feed-forward is provided ($U^*_{\rm pn}$ in Fig. 4).

It has to be pointed out that opposed to boost-type PFC rectifiers, the mains current is not directly impressed by the control, but is formed only by PWM without feed-back from a controlled dc current. Accordingly, variations of the dc current, parasitic timing errors of the switching or distortions at borders of the 60° mains voltage sectors [10] are not immediately corrected. In practical applications, particularly at high mains frequencies, buck-type PFC systems, therefore, show a lower input current quality than boost-type PFC systems. First considerations of a direct mains current control, which could eliminate this disadvantage, can be found in [8] and [11].

In contrast to the considered boost-type PFC rectifier systems, the buck-type PFC rectifier could be operated in open-loop control mode due to its buck-type (LC output filter-type) control characteristic. In this operating mode, the output voltage and current control loops (feed-back of the measurements of $u_{\rm pn}$ and i in Fig. 4) are omitted, and a constant output voltage reference value $U^*_{\rm pn}$ is provided for u^*. The buck-type PFC rectifier

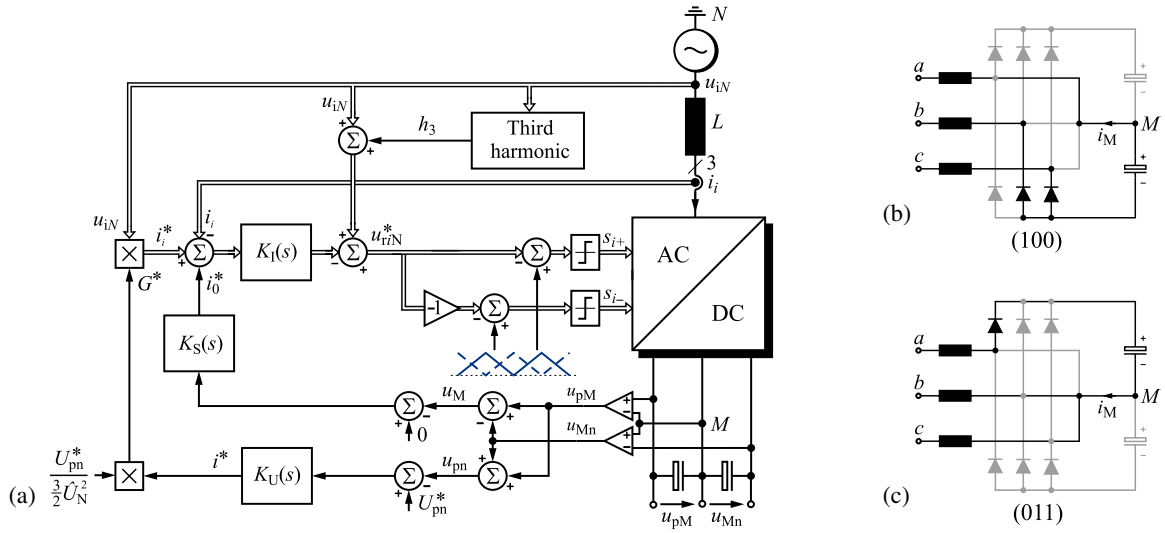


Fig. 3. (a) Basic control structure of the VIENNA Rectifier with superimposed control of the output voltages u_{pM} and u_{Mn}, and subordinate phase current control with feed-forward of the mains phase voltages. The balancing of the two output voltages is achieved by adding an offset i_0^* to the phase current reference values. (b) and (c) Redundant switching states of the system (for $i_a > 0, i_b, i_c < 0$) that result in equal rectifier input line-to-line voltages and opposite directions of i_{M} and, therefore, facilitate a balancing of the output capacitor voltages without influence on the phase current shaping. For example, for $i_0^* > 0$, the relative ON-time of the switching state (1 0 0) is increased and the ON-time of the switching state (0 1 1) is reduced resulting in $\bar{i}_{\mathrm{M}} < 0$; correspondingly $i_0^* < 0$ results in $\bar{i}_{\mathrm{M}} > 0$. (The direction of the arrow of i_{M} in (b) and (c) indicates the positive current direction and does not necessarily correspond to the actual current flow direction.) The switching state is represented by phase switching functions s_i, and/or (s_a,s_b,s_c), where $s_i = 1$ ($i = \{a, b, c\}$) indicates that the corresponding four-quadrant switch is switched on and $s_{\mathrm{i}} = 0$ indicates that it is switched off.

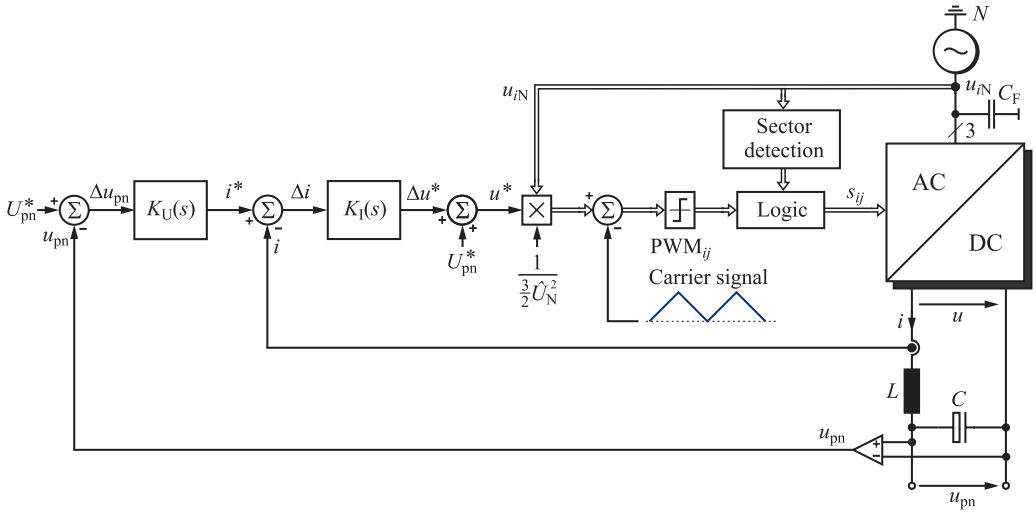


Fig. 4. Control structure of the active six-switch buck-type PFC rectifier with a superimposed output voltage controller $K_{\mathrm{U}}(s)$. The output current controller $K_{\mathrm{I}}(s)$ with feed-forward of the output voltage reference value U_{pn}^* defines the voltage at the output of the rectifier bridge. The modulation is performed such that the output voltage of the rectifier is formed in each pulse period by segments of two line-to-line voltages, and/or the dc current i is distributed to the input phases, i.e. sinusoidally modulated.

is then operated at a constant modulation index and generates a non-controlled dc output voltage.

D. SWISS *Rectifier*

A possible implementation of the control scheme of the SWISS Rectifier with a superimposed PI-type output voltage controller $K_{\mathrm{U}}(s)$ and a subordinate P-type output current controller $K_{\mathrm{I}}(s)$ is shown in Fig. 5. Ultimately, with the output current controller, the current forming voltage $\bar{u}_{\mathrm{XZ}}$ is defined, where advantageously a feed-forward of the output voltage $u_{\mathrm{pn}}^* = U$ is applied. The adjustment of u_{XZ} is obtained with an appropriate selection of the duty cycles of the transistors S_+ and S_- (cf. [1, eq. (43)]). The (normalized) voltages $u_{\bar{\mathrm{p}}\mathrm{N}}$ and $u_{\bar{\mathrm{n}}\mathrm{N}}$ are used as modulation functions according to in [1 eq. (44)], where N refers to the star-point of the mains input voltages (cf. also Fig. 5). The SWISS Rectifier could be also operated in an open-loop control mode with a constant reference voltage value U_{pn}^* (cf. Fig. 5) similar to the six-switch buck-type PFC rectifier.

The PWM of the transistors S_+ and S_- can be implemented using carrier signals $u_{\mathrm{D}+}$ and $u_{\mathrm{D}-}$ that are in phase or in antiphase (phase displacement of 180°). For the further considerations, carriers without a phase displacement are assumed as

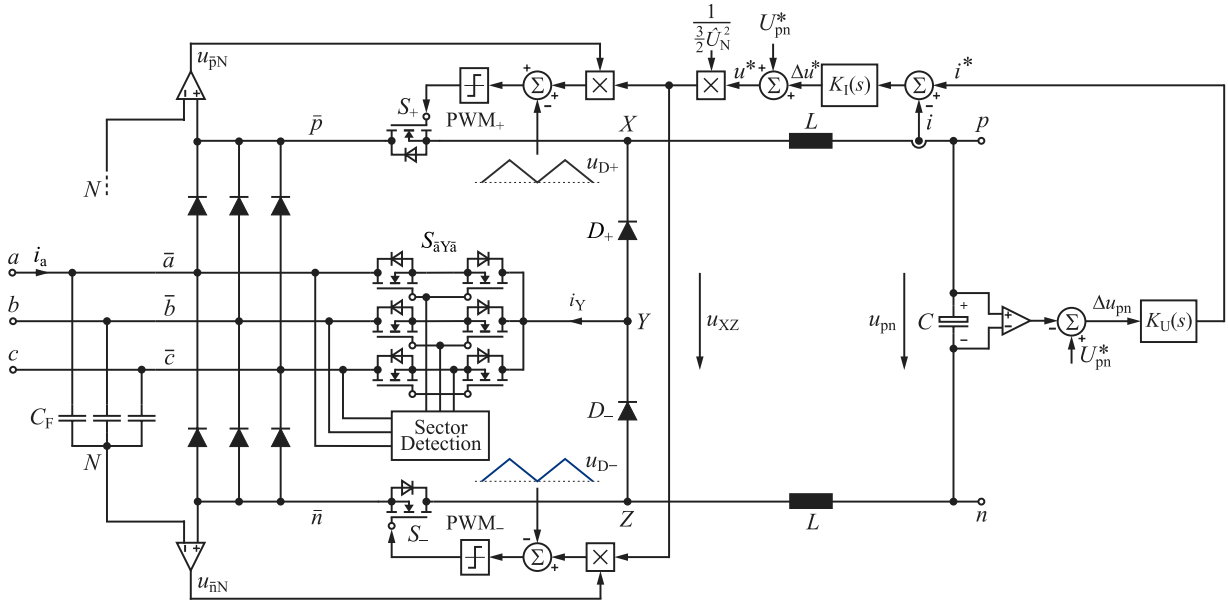


Fig. 5. Control structure of the SWISS Rectifier with a superimposed output voltage controller $K_U(s)$ and a subordinate output current controller $K_I(s)$ with feed-forward of the output voltage reference value. The voltage required to control the output current is formed through modulation of S_+ and S_- such that in both conducting branches of the diode bridge pulse-width-modulated currents result. The local average value of these currents is proportional to the corresponding mains phase voltages. A four-quadrant switch is switched on by the sector detection and is always connected to the mains phase with the smallest absolute voltage value and injects the current i_Y into this phase.

this leads to a lower current ripple of the current i_Y which is injected into the mains phases and thus also to a lower input current ripple (cf. also [1, Sec. IV-B3, p. 19]).

E. Discussion

The overview of the control structures shows that the control concepts and complexity of the four considered active PFC rectifier topologies are comparable. The VR provides the highest degree of freedom in modulation due to its three-level characteristic. The control of the VR is, however, well investigated [12]–[14].

It should be noted again that the mains current of the buck-type systems is not directly impressed by the control opposed to the boost-type systems, but is formed only by PWM without any feed-back from the controlled dc current. In addition, the buck-type systems can be operated in an open-loop control mode and do not need any precharging circuits for startup in contrast to the boost-type systems.

III. DIMENSIONING AID FOR THE POWER SEMICONDUCTORS AND THE EMI FILTER

In the following, the average and rms current stresses of the semiconductors of the four considered rectifier systems are briefly summarized to assist a practical design and implementation. In addition, the basic structure of the EMI filter on the ac side is discussed with a focus on the CM filtering.

A. Power Semiconductor Stresses

The current stresses of the power semiconductors of a PFC rectifier systems are often determined for a defined operating point by simulation. Alternatively, a calculation can also be performed, only analytically with good accuracy. This results in simple mathematical expressions, which are valid over the whole operating range, under the constraint of Continuous Conduction Mode (CCM), and thus provide an ideal basis for the analysis of the component stresses and/or the losses at different operating points or different mains input and/or output voltages.

The starting point for the analytical calculations is the relative ON-times of the power transistors which can be determined analytically for the whole mains period if the modulation method is known. The remaining parameter is the modulation index M, which represents the ratio of the amplitude of the three-phase voltage or current system on the ac side and the dc output voltage and/or the dc output current

$$M = \frac{\hat{U}_U}{\frac{1}{2}U_{pn}} \qquad M = \frac{\hat{I}_U}{I} \tag{1}$$

($\hat{U}_U \approx \hat{U}_N$ represents the amplitude of the fundamental of the discontinuous phase voltage at the boost-type rectifier input, $\hat{U}_N$ the amplitude of the grid voltage, and U_{pn} the average dc output voltage of a boost-type system. $\hat{I}_U$ is the amplitude of the fundamental of the discontinuous phase currents at the buck-type rectifier input and I the average dc output current of a buck-type system).

With the relative ON-time (duty cycle) and the input current (for boost-type rectifiers), and/or the output current (for buck-type rectifiers), the instantaneous conduction states of the power semiconductors are defined, and the local average current values can be calculated by averaging over a pulse period. Based on that, the global average and root mean square (rms) values of the currents and voltages of interest can be determined [15] by averaging over the mains period. The resultant equations for the individual topologies are compiled in Fig. 6. All four considered

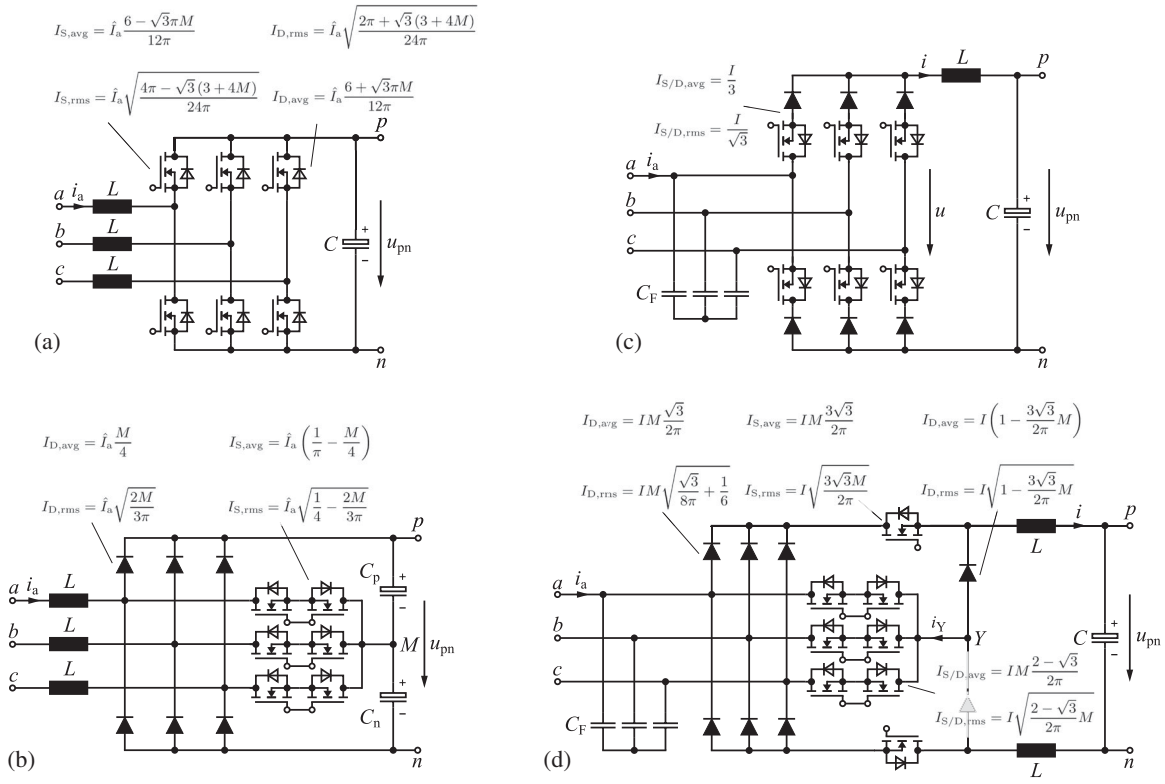


Fig. 6. Circuit topologies with average and rms current stresses of the power semiconductors of the selected active boost- and buck-type PFC rectifier systems evaluated for unity power factor and power flow from the mains to the dc side (purely ohmic mains behavior and rectifier operation). (a) Six-switch boost-type PFC rectifier, (b) VIENNA Rectifier, (c) six-switch buck-type PFC rectifier, and (d) SWISS Rectifier.

topologies were implemented as hardware prototypes to investigate their operating behavior and to validate and/or parameterize the derived models [16]–[19]. In addition, SiC semiconductor loss characterizations were performed with dedicated loss measurement setups and converter prototypes. A summary of the main loss data can be found in [20].

B. DM and CM EMI Filter

The input inductors of the boost-type PFC rectifier systems are to be considered as the first stage of a multistage EMI filter placed on the ac side similar to the input filter capacitors of the systems with buck-type characteristic. The conducted EMI noise is suppressed with this filter such that the standards concerning conducted noise are fulfilled in the frequency range of 150 kHz–30 MHz (e.g., CISPR 11). Depending on the application, another EMI filter might be required on the dc side [21]–[23], which is, however, not discussed here for the sake of brevity.

Three-phase rectifier circuits inherently generate a CM voltage between the midpoint of the output voltage (the output voltage buses) and ground. The CM voltage waveform for a passive diode rectifier circuit with inductors on the dc side is depicted in Fig. 7(a). For active rectifier circuits, the CM voltage has a pulsed waveform [cf. Figs. 7(b) and (c)]; thus, CM currents result due to the parasitic capacitances to the ground.

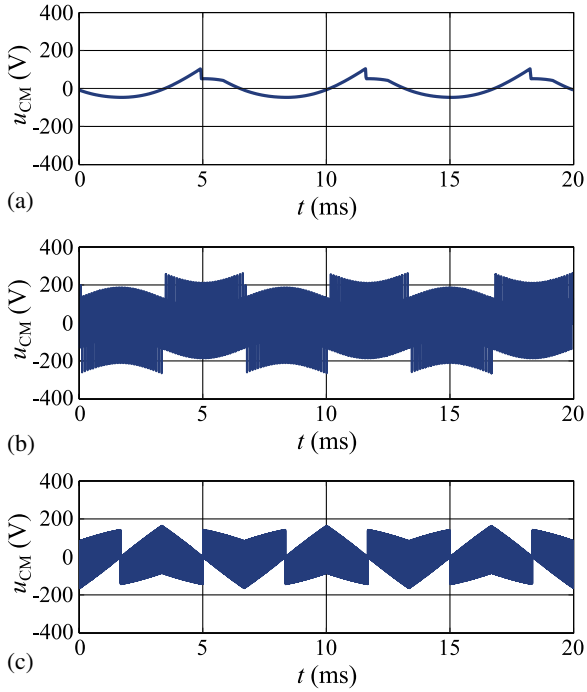


Fig. 7. CM voltage at the output of three-phase rectifier systems referenced to the grounded star-point of the mains. (a) Passive diode rectifier with smoothing inductor on the dc side [cf. [1, Fig. 2(b)]]. (b) VIENNA Rectifier [cf. Fig. 1(b)]. (c) Six-switch buck-type PFC rectifier [cf. Fig. 1(c)].

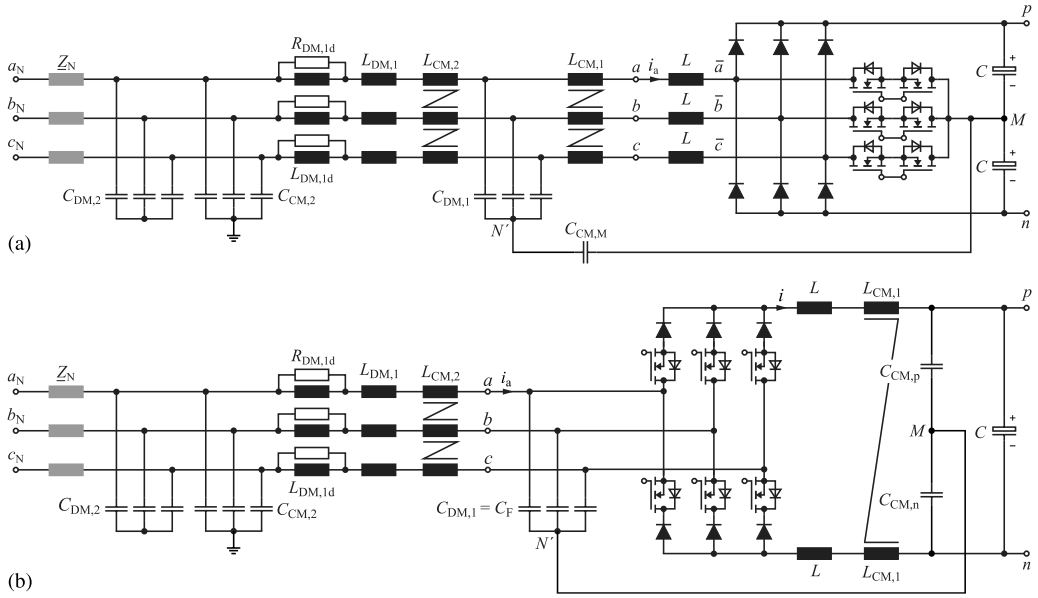


Fig. 8. Example of the EMI filter structure of (a) an active boost-type PFC rectifier system [VIENNA Rectifier, cf. Fig. 1(b)] and (b) an active six-switch buck-type PFC rectifier [cf. Fig. 1(c)]. Commercial EMI input filters typically employ filter capacitors at the input (mains) side. Accordingly, an additional filter stage is formed by the inner mains impedance $\underline{Z}_N$, which could be deliberately increased to limit the short-circuit current. Fuses, over-voltage protection devices, bleeding resistors, and precharging circuitry are not shown.

For fully active boost-type PFC systems, e.g., the VR, the CM voltage originates from the rectifier ac-side phase voltages employed for the current impression that do not add to zero except for the switching state $s_{\bar{a}M} = s_{\bar{b}M} = s_{\bar{c}M} = 1$. ($s_{\bar{a}M} = s_{\bar{b}M} = s_{\bar{c}M} = 1$ means that the rectifier inputs $\bar{a}, \bar{b}, \bar{c}$ [cf. Fig. 8(a)] are connected to the midpoint M of the output voltage. $u_{\bar{i}M}$ for $i = \{\bar{a}, \bar{b}, \bar{c}\}$ represents the voltage between the rectifier inputs $\bar{a}, \bar{b}, \bar{c}$ and the midpoint M.) Thus, a CM voltage

$$u_{MN} = -\frac{1}{3}\left(u_{\bar{a}M} + u_{\bar{b}M} + u_{\bar{c}M}\right) = u_{CM} \tag{2}$$

is generated between the midpoint M of the output voltage and the (grounded) mains star-point N, which could contain a low-frequency component $\bar{u}_{CM}$, but contains in any case a switching frequency component $u_{CM,\sim}$

$$u_{CM} = \bar{u}_{CM} + u_{CM,\sim} \tag{3}$$

(for the VR see [24, Figs. 3.4 and 5.73]). A filtering of $u_{CM,\sim}$ can be achieved by connecting M via a capacitor $C_{CM,M}$ to an artificial mains star-point N' (representing the ground potential), formed by a star-connection of filter capacitors C_F and insertion of a CM inductor $L_{CM,1}$ in series to the boost inductors L [cf. Fig. 8(a)]. A low-frequency variation of the potential of M is, thus, not prevented. In addition, contrary to a placement of CM filter capacitors to ground, ground currents are minimized. However, additional CM filter stages have to be implemented on the mains side for the filtering of the noise currents that result from the parasitic capacitances of the power semiconductors to the heat sink [17]. A detailed description of the CM modeling and the estimation of the parasitic capacitances of the power semiconductors to the heat sink is shown as an example for the VR in [24].

For fully active buck-type PFC systems, within each pulse period, two line-to-line voltages are switched to the rectifier output for the formation of the output voltage and for the distribution of the dc output current to the mains phases. This again leads to a CM voltage $u_{CM,\sim}$ at the switching frequency. (A CM voltage during the freewheeling interval can be avoided by symmetric splitting of the output inductor to the positive and negative output bus.) The concept described previously for boost-type converters can also advantageously be used for the filtering of $u_{CM,\sim}$ of buck-type systems [cf. Fig. 8(b)] where the CM inductor has to be inserted on the dc side.

For determining the switching frequency component of the DM voltage $u_{DM,\sim}$, which is relevant for the design of the DM filtering, for boost-type systems within each pulse period, the formation of the input current has to be considered. For example, for phase a of the the six-switch boost-type PFC rectifier with a boost inductance L

$$L\frac{di_a}{dt} = u_{aN} - \left(u_{\bar{a}M} + u_{CM}\right) = u_{aN} - u_{\bar{a}N} \tag{4}$$

$$= u_{aN} - \bar{u}_{\bar{a}N} - u_{\bar{a}N,\sim} \tag{5}$$

applies. u_{aN} represents the phase voltage between the rectifier input terminal a (on the grid side of the boost inductor) and the (grounded) mains star-point N and $u_{\bar{a}N}$ the voltage between the rectifier input $\bar{a}$ (on the rectifier side of the boost inductor) and the star-point N. Applying the same consideration as for the aforementioned analysis of the CM voltage, $u_{\bar{a}N}$ is separated in a low-frequency component $\bar{u}_{\bar{a}N}$ and a switching frequency component $u_{\bar{a}N,\sim}$. Consequently, the phase current i_a can also be written as a superposition of a fundamental $\bar{i}_a$ and a switching frequency component $i_{a,\sim}$

$$i_a = \bar{i}_a + i_{a,\sim}, \tag{6}$$

where the fundamental component $\bar{i}_{\mathrm{a}}$ is formed using (4) and (5) according to

$$L\frac{d\bar{i}_{\mathrm{a}}}{dt} = u_{\mathrm{aN}} - \bar{u}_{\bar{\mathrm{a}}\mathrm{N}} \ . \tag{7}$$

The switching frequency DM voltage component $u_{\mathrm{DM},\sim}$ to be suppressed by the DM filtering then equals

$$L\frac{di_{\mathrm{a},\sim}}{dt} = u_{\bar{\mathrm{a}}\mathrm{N},\sim} = u_{\mathrm{DM},\sim} \ . \tag{8}$$

The filtering of $u_{\mathrm{DM},\sim}$ (each phase shows an equal spectral composition of the related DM voltage if a symmetrical EMI filter is assumed and if parasitic couplings are neglected) is performed with the boost inductors and with ac-side capacitors $C_{\mathrm{DM},1}$ between the phases, whereby typically, two filter stages are required [cf. Fig. 8(a)]. Additionally, damping elements for reducing the resonance peaks [25], [26] in respect of the control stability of the system have to be added, which also prevent the excitation of the filter by harmonics of the mains voltage.

For buck-type systems, the DM noise is generated by the pulsating input currents at switching frequency and is attenuated by the input filter capacitors C_F and the ac-side filter inductors $L_{\mathrm{DM},1}$ and an additional input filter stage [cf. Fig. 8(b)].

Regarding the volume of the EMI filter, it has to be noted that, e.g., for boost converter systems, a constant voltage is decomposed into its spectral components by the pulse width modulation, i.e., into a mains-frequency fundamental component and harmonic components grouped around multiples of the switching frequency with sidebands. Only the fundamental frequency is used for the impression of the phase current, i.e., the switching frequency harmonics must be suppressed with an appropriate EMI (input) filter. The harmonic components, i.e., ultimately the difference between the constant output voltage U_{pn} and the actual low-frequency voltage component to be formed, e.g., $\bar{u}_{\bar{\mathrm{a}}\mathrm{N}}$, show similar rms values. Considering in addition that the EMI input filter has to conduct the input current of the converter, a significant fraction of the total converter volume is expected to be determined by the EMI input filter. This is confirmed by implemented systems, where the volume of the EMI filter (including the boost inductors or buck input filter capacitors) typically represents 30% of the total converter volume (cf. Figs. 11, 12, and Table II). Here, it should be pointed out that the required filter attenuation can be calculated analytically in a simple manner by decomposition of the rectifier input voltage into a fundamental and a total high frequency noise voltage [20], [24], [27], [28].

IV. Comparative Evaluation

In the first part of this paper [1] and in the foregoing sections, the main features of the four considered active boost- and buck-type PFC rectifier systems suitable for industrial application have been identified and briefly discussed. In the following, a comparative evaluation of these circuit topologies with regard to efficiency, volume, and implementation effort is provided to highlight the advantages and disadvantages of the individual systems and to facilitate the selection of an adequate circuit topology for a specific application.

A. Rectifier System Specifications

The four selected active boost- and buck-type three-phase PFC rectifier topologies are compared using the same specifications for each system with a rated output power of $P_{\mathrm{o}} = 10$ kW and a line-to-line mains voltage of $U_{\mathrm{N,ll,rms}} = 400$ V at a mains frequency of $f_{\mathrm{N}} = 50$ Hz. The rated output power of 10 kW represents a typical value for three-phase power supplies. For the boost-type systems, i.e., the active six-switch boost-type PFC rectifier and the VR, a rated output voltage of $U_{\mathrm{o}} = 700$ V is considered, whereas for the buck-type systems, i.e., the active six-switch buck-type PFC rectifier and the SWISS Rectifier, a rated output voltage of $U_{\mathrm{o}} = 400$ V is assumed.

Two different semiconductor implementation variants are investigated, an advanced one using 1200-V SiC JFETs and 1200-V SiC Schottky diodes with a switching frequency of $f_{\mathrm{P}} = 48$ kHz and a more standard one using 1200- and 600/650-V Si IGBTs and SiC Schottky diodes with a switching frequency of $f_{\mathrm{P}} = 24$ kHz.

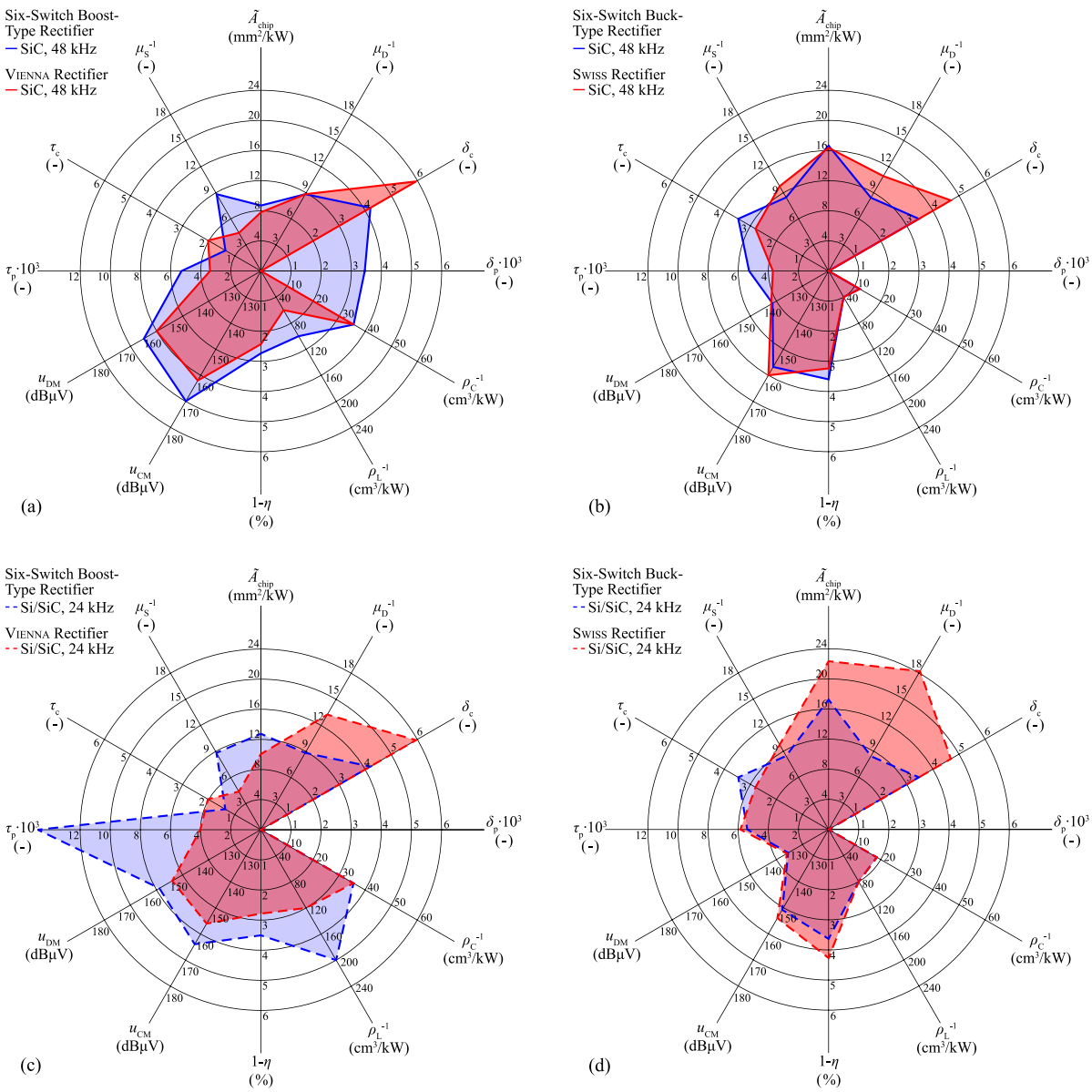
The PFC rectifier systems are designed for an ambient temperature of $T_{\mathrm{a}} = 45\,^{\circ}\mathrm{C}$. The average junction temperature of the semiconductors is defined by proper design to $T_{\mathrm{j,avg}} = 125\,^{\circ}\mathrm{C}$ for a heat sink temperature of $T_{\mathrm{s}} = 85\,^{\circ}\mathrm{C}$. The thermal design should ensure a lifetime of at least 50 000 h (approx. six years of continuous operation).

B. Modeling Approach

1) Power Semiconductors: In the semiconductor variant with SiC JFETs, whenever possible, the internal body diodes of the JFETs are used. This means that SiC Schottky diodes are only implemented for the six hard-commutated rectifier diodes at the input of the VR [cf. Fig. 6(b)], the six commutation diodes of the active six-switch buck-type PFC rectifier [cf. Fig. 6(c)], and the two freewheeling diodes of the SWISS Rectifier [cf. Fig. 6(d)] that are connected to the node Y. (For the active six-switch boost-type PFC rectifier [cf. Fig. 6(a)], the internal body diodes of the JFETs are used instead of explicit freewheeling diodes.) The diode rectifier switching losses at the input of the SWISS Rectifier are low since the two transistors in the positive and negative dc bus are switching the current. Thus, the six rectifier diodes at the input are implemented with Si diodes with a lower on-state voltage drop than SiC Schottky diodes in order to enable a high efficiency.

For the semiconductor variant with Si IGBTs and SiC Schottky diodes, 1200-V IGBTs are used except for the VR where 600/650-V IGBTs and SiC Schottky diodes are chosen for the bidirectional switches. 1200-V SiC Schottky diodes are used for all commutation/freewheeling diodes apart from the six rectifier diodes at the input of the SWISS Rectifier, where Si diodes are implemented also for the semiconductor variant with SiC JFETs [cf. Fig. 9(b)]. The considered power semiconductor devices are listed as follows:

1) 1200-V SiC JFETs, SiCED/Infineon (in cascode configuration, i.e. with normally-off characteristic);
2) 1200/650-V Si Trench&FieldStop IGBTs 4, Infineon;
3) 1200/600-V SiC Schottky barrier diodes, ThinQ2, Infineon, and



$\tilde{A}_{chip}$	Relative total semiconductor chip area	δ_c	Relative total diode rms rating	ρ_C^{-1}	Relative boxed capacitor volume
μ_S^{-1}	Relative total transistor VA rating	τ_p	Relative total transistor switching losses	1-η	Relative losses
μ_D^{-1}	Relative total diode VA rating	δ_p	Relative total diode switching losses	u_{DM}	Conducted differential mode noise
τ_c	Relative total transistor rms rating	ρ_L^{-1}	Relative boxed inductor volume	u_{CM}	Conducted common mode noise

Fig. 9. Comparative evaluation of (a) and (c) two alternative active boost-type PFC rectifier systems, i.e., the six-switch rectifier and the Vienna Rectifier, and (b) and (d) two alternative active buck-type PFC rectifier systems, i.e., the active six-switch rectifier and the Swiss Rectifier. The characteristics are shown for an implementation with SiC JFETs and SiC Schottky diodes at a switching frequency of 48 kHz [cf. (a) and (b)] and an implementation with Si IGBTs and SiC Schottky diodes at a switching frequency of 24 kHz [cf. (c) and (d)]. The fractions of the Si and SiC chip areas are as follows: (a) six-switch boost-type rectifier: $\tilde{A}_{\mathrm{chip,Si}} = 0$ mm²/kW and $\tilde{A}_{\mathrm{chip,SiC}} = 8.7$ mm²/kW, Vienna Rectifier: $\tilde{A}_{\mathrm{chip,Si}} = 0$ mm²/kW and $\tilde{A}_{\mathrm{chip,SiC}} = 7.8$ mm²/kW; (b) six-switch buck-type rectifier: $\tilde{A}_{\mathrm{chip,Si}} = 0$ mm²/kW and $\tilde{A}_{\mathrm{chip,SiC}} = 16.7$ mm²/kW, Swiss Rectifier: $\tilde{A}_{\mathrm{chip,Si}} = 3.6$ mm²/kW and $\tilde{A}_{\mathrm{chip,SiC}} = 13.0$ mm²/kW; (c) six-switch boost-type rectifier: $\tilde{A}_{\mathrm{chip,Si}} = 8.7$ mm²/kW and $\tilde{A}_{\mathrm{chip,SiC}} = 4.1$ mm²/kW, Vienna Rectifier: $\tilde{A}_{\mathrm{chip,Si}} = 4.7$ mm²/kW and $\tilde{A}_{\mathrm{chip,SiC}} = 5.3$ mm²/kW; (d) six-switch buck-type rectifier: $\tilde{A}_{\mathrm{chip,Si}} = 11.4$ mm²/kW and $\tilde{A}_{\mathrm{chip,SiC}} = 5.9$ mm²/kW, Swiss Rectifier: $\tilde{A}_{\mathrm{chip,Si}} = 18.6$ mm²/kW and $\tilde{A}_{\mathrm{chip,SiC}} = 3.8$ mm²/kW.

4) 1200-V Si EmCon4 diodes, Infineon.

Alternatively, the (three-level) VR could also be implemented with 600/650-V Si super-junction MOSFETs and with modified power circuit topologies, which is used for the hardware demonstrators in Section IV-F.

The chip area of the semiconductors is designed based on a thermal model of a typical semiconductor package (EconoPACK, Infineon, [20]) and a heat sink temperature of $T_s = 85\,^{\circ}\mathrm{C}$ such that an average junction temperature of $T_{j,avg} = 125\,^{\circ}\mathrm{C}$ results. Thus, an equal usage of all semiconductors is obtained. (The relationship between the semiconductor

chip area, the thermal impedance between the semiconductor junction and the heat sink, and the semiconductor losses can be summarized as follows: the larger the chip area, the lower are the thermal impedance and the conduction losses but the higher are the switching losses for a given switched current.) Both, conduction and switching losses are considered for determining the semiconductor losses. The required semiconductor loss and chip size data of the power devices are determined based on an analysis of power module data sheets, manufacturer data, and experimentally determined switching loss energies. The extracted data are related to a set of voltage, current, chip area, and temperature dependent semiconductor loss equations (cf. [20], Section IV, [16], [29]).

It is worth noting that the relatively high equal junction temperature of all power semiconductors leads to relatively high semiconductor conduction losses due to the selected devices (cf. also [30]). In order to achieve a higher efficiency, semiconductor devices with a higher current rating, i.e., a larger chip area, could be used, and/or a lower junction temperature could be selected.

2) Passive Components: In this comparison, only the main passive components of the individual rectifier topologies are considered; that are the dc output capacitors, the three ac boost inductors of the boost-type PFC rectifiers [cf. Fig. 8(a), inductors labeled with L], and the three ac filter capacitors and the two dc output inductors of the buck-type PFC rectifiers [cf. Fig. 8(b), capacitors labeled with C_{F} and inductors labeled with L].

The dc output capacitors are implemented with aluminum electrolytic capacitors. A series connection of two 400-V capacitors (B43501-series, EPCOS) is considered for the boost-type systems, whereas for the buck-type systems, 500-V capacitors (B43501-series, EPCOS) are selected. The capacitors are designed for a mean time-to-failure of 50 000 h regarding the rms current loading and an assumed maximum capacitor temperature of 65 °C. For the ac filter capacitors of the buck-type rectifiers, X2 foil capacitors (B3277x-series, EPCOS) are used.

Toroidal powder core inductors are considered for the ac boost inductors and dc output inductors. They provide a good compromise between the achievable inductance per volume and ac and dc magnetization properties and allow for simple and cost effective manufacturing. The inductance of the boost inductors of the boost-type rectifiers is designed such that the maximum peak-to-peak current ripple at the switching frequency is limited to 20% of the fundamental nominal input current amplitude. In analogy to the boost inductors, the inductance of the output inductors of the buck-type rectifiers is selected such that the maximum peak-to-peak current ripple at the switching frequency is limited to 20% of the nominal average dc output current. The dc output inductor of the six-switch buck-type PFC rectifier could be split into two identical inductors with half of the inductance of the single inductor as shown in Fig. 8(b) to enable a symmetric CM impedance. In this calculation, only a single dc output inductor is considered since the resultant CM impedance is mainly dominated by the CM inductor and the total inductor volume increases with split inductors. The same inductor design and powder core alloy (Magnetics) are used for all inductors. A detailed description of the inductor modeling and the main inductor parameters is given in [29, Section. III-B].

3) Cooling: Forced air-cooling with an aluminum heat sink is considered for the power semiconductors. The capacitors are passively surface cooled, and the inductors are placed in the air flow of the heat sink.

C. Definition of the Performance Indices

Normalized performance indices are employed, which are independent of the actual system dimensioning, in order to provide a universally valid quantification of the converter performances. Thereby, the output power P_{o} and the load current I_{o} are used as reference values.

The relative total required semiconductor chip area and, with reference to [31], the normalized conduction and switching power losses are used for the characterization of the semiconductor expenditure.

1) Relative Total Semiconductor Chip Area: The relative total Si or SiC semiconductor chip area of the transistors and diodes is calculated according to

$$\tilde{A}_{\mathrm{chip}} = \frac{\sum_n A_{\mathrm{Si/SiC,S},n} + \sum_n A_{\mathrm{Si/SiC,D},n}}{P_{\mathrm{o}}} \tag{9}$$

where $A_{\mathrm{Si/SiC,S},n}$ represents the Si/SiC chip area of the nth power transistor and $A_{\mathrm{Si/SiC,D},n}$ the Si/SiC chip area of the nth power diode. As mentioned previously, for the transistors and diodes, the semiconductor chip area is scaled with the current loading and/or the power loss such that a constant (average) junction temperature $T_{j,\mathrm{avg}} = 125\,^{\circ}\mathrm{C}$ of all power semiconductors is given. (The relative total semiconductor chip area should be considered as a means for comparison and not as a fixed value for a certain circuit topology as it strongly depends on the semiconductor and power module design constraints.)

2) Relative Total Transistor and Diode VA Rating: Relative total transistor VA rating

$$\mu_{\mathrm{S}}^{-1} = \frac{\sum_n u_{\mathrm{S,max},n}\, i_{\mathrm{S,max},n}}{P_{\mathrm{o}}}\,. \tag{10}$$

Relative total diode VA rating

$$\mu_{\mathrm{D}}^{-1} = \frac{\sum_n u_{\mathrm{D,max},n}\, i_{\mathrm{D,max},n}}{P_{\mathrm{o}}}. \tag{11}$$

($u_{\mathrm{S,max},n}$ and $u_{\mathrm{D,max},n}$ refer to the maximum blocking voltage stress without considering switching overvoltages, $i_{\mathrm{S,max},n}$ and $i_{\mathrm{D,max},n}$ refer to the peak current value of the nth device; μ_{S} and μ_{D} are used for the assessment of the transistor and diode utilization (cf. [31]).)

3) Relative Total RMS Current Rating: Relative total transistor RMS current rating

$$\tau_{\mathrm{C}} = \frac{\sum_n I_{\mathrm{S,rms},n}}{I_{\mathrm{o}}}\,. \tag{12}$$

Relative total diode RMS current rating

$$\delta_{\mathrm{C}} = \frac{\sum_n I_{\mathrm{D,rms},n}}{I_{\mathrm{o}}} \tag{13}$$

where $I_{\mathrm{S,rms},n}$ and $I_{\mathrm{D,rms},n}$ correspond to the transistor and diode rms value of the nth device. A linear dependence on $I_{\mathrm{S,rms}}$ and $I_{\mathrm{D,rms}}$ is used for this performance index. The motivation for using this relationship is based on the linear dependence of the conduction losses and the rms current of unipolar transistors under given thermal constraints, which is described in more detail in Appendix A. (The conduction losses of the unipolar transistors are still calculated using the ON-state resistance and the square of the transistor rms current, whereas the conduction characteristics of the bipolar devices are approximated by a constant forward voltage drop and a differential resistance and thus, the conduction losses are determined based on the average and the square of the rms device currents.)

It should be noted that currents flowing from the drain to the source terminal of the MOSFET symbols, cf. Fig. 6, are accounted as transistor currents independent on whether the actual switching device is implemented as a JFET with an antiparallel body diode or as an IGBT with an antiparallel SiC Schottky freewheeling diode. Correspondingly, currents flowing from the source to the drain terminal of the MOSFET symbols are considered as diode currents.

4) Relative Total Transistor and Diode Switching Losses: The relative total transistor switching losses are defined as

$$\tau_{\mathrm{P}} = \frac{\sum_n P_{\mathrm{S,P},n}}{P_{\mathrm{o}}}. \tag{14}$$

The relative total diode switching losses are calculated according to

$$\delta_{\mathrm{P}} = \frac{\sum_n P_{\mathrm{D,P},n}}{P_{\mathrm{o}}}, \tag{15}$$

where $P_{\mathrm{S,P},n}$ and $P_{\mathrm{D,P},n}$ represent the nth transistor and diode switching losses, and P_{o} is the rectifier output power.

5) Relative Boxed Volume of the Inductors and Capacitors: Regarding the passive components for the boost-type rectifier systems, only the relative boxed volume of the boost inductors (iron powder cores) and of the output capacitors (electrolytic capacitors) and for the buck-type rectifier systems, only the boxed volume of the output inductors (same core material as used for boost inductors) and of the ac-side filter capacitors $C_{\mathrm{F}} = C_{\mathrm{DM},1}$ (foil capacitors) is considered. $V_{\mathrm{L,i}}$ is the boxed volume of the ith inductor and $V_{\mathrm{C,i}}$ the boxed volume of the ith capacitor

$$\text{Inductors} \qquad \rho_{\mathrm{L}}^{-1} = \frac{\sum_i V_{\mathrm{L,i}}}{P_{\mathrm{o}}} \tag{16}$$

$$\text{Capacitors} \qquad \rho_{\mathrm{C}}^{-1} = \frac{\sum_i V_{\mathrm{C,i}}}{P_{\mathrm{o}}}\ . \tag{17}$$

Accordingly, ρ_{L}^{-1} corresponds to the relative boxed volume of the inductors and ρ_{C}^{-1} to the relative boxed volume of the capacitors.

6) Conducted Differential and Common Mode Noise: The assessment of the conducted EMI noise behavior and/or of the required filtering effort to meet the EMC standards is performed for the boost-type systems based on the DM component u_{DM}, and the CM component u_{CM} of the noise voltage at the rectifier input

$$u_{\mathrm{noise}} = u_{\mathrm{DM},\sim} + u_{\mathrm{CM},\sim}\ . \tag{18}$$

Thereby, in terms of a simplification [28], for the DM noise voltage u_{DM} the total voltage, forming the boost inductor current ripple component of a phase current can be written as (shown, e.g., for input phase a)

$$u_{\mathrm{DM,a},\sim,\mathrm{rms}} = \sqrt{u_{\mathrm{\bar{a}N,rms}}^2 - u_{\mathrm{aN,rms}}^2} = u_{\mathrm{DM},\sim,\mathrm{rms}}\ . \tag{19}$$

The CM voltage is defined according to (2), cf. in [1, eq. (4)], where M designates the (fictitious) midpoint of the output voltage. Analogous to (19), the CM noise voltage relevant for the filter design can then be approximately calculated by subtracting the low frequency component $\bar{u}_{\mathrm{CM}}$

$$u_{\mathrm{CM},\sim,\mathrm{rms}} = \sqrt{u_{\mathrm{CM,rms}}^2 - \bar{u}_{\mathrm{CM,rms}}^2}\ . \tag{20}$$

For the buck-type PFC system, the CM voltage can be calculated as

$$u_{\mathrm{CM}} = \frac{1}{2}\left(u_{\mathrm{pN}} + u_{\mathrm{nN}}\right) \tag{21}$$

and the switching frequency component $u_{\mathrm{CM},\sim}$ again according to (20), where u_{pN} represents the voltage between the positive dc-link rail and the (mains) star-point N and u_{nN} the voltage between the negative dc-link rail and N. Instead of $u_{\mathrm{DM},\sim}$ [cf. (8)], here, the rms value of the switching frequency components of the discontinuous input currents

$$i_{\mathrm{DM,a},\sim,\mathrm{rms}} = \sqrt{i_{\mathrm{a,rms}}^2 - \bar{i}_{\mathrm{a,rms}}^2} \tag{22}$$

(shown for input phase a) is used for the assessment of the DM filter attenuation requirement. A voltage noise level can be calculated by multiplication with $R = 50\,\Omega$ [28], the input resistance of a typical EMI test receiver.

7) Efficiency: The efficiency η of the systems is characterized by the relative losses

$$\frac{P_{\mathrm{L}}}{P_{\mathrm{o}}} = \frac{P_{\mathrm{N}} - P_{\mathrm{o}}}{P_{\mathrm{o}}} = \frac{1}{\eta} - 1 = \frac{1-\eta}{\eta} \approx 1 - \eta \tag{23}$$

where in addition to the semiconductor losses and main power components also a power consumption of $P_{\mathrm{aux}} = 30\,\mathrm{W}$ for the auxiliary supply (control circuitry, gate drives, fans) is considered in the total losses P_{L}. P_{N} represents the power at the rectifier input on the mains side and P_{o} the rectifier output power.

8) Volume of the Cooling System: With the relative losses $(1-\eta)$ and the Cooling System Performance Index (CSPI) [32]

$$\mathrm{CSPI} = \frac{G_{\mathrm{th,s-a}}}{V_{\mathrm{s}}} \tag{24}$$

($G_{\mathrm{th,s-a}}$ designates the required thermal conductance (W/K) between the surface of the heat sink and the ambient) and a given admissible temperature difference $\Delta T_{\mathrm{s-a}}$, the volume V_{s} of the forced air-cooled heat sink can be calculated to

$$V_{\mathrm{s}} = \frac{G_{\mathrm{th,s-a}}}{\mathrm{CSPI}} = \frac{P_{\mathrm{L}}}{\Delta T_{\mathrm{s-a}}\mathrm{CSPI}} \approx \frac{P_{\mathrm{o}}}{\Delta T_{\mathrm{s-a}}\mathrm{CSPI}}\left(1-\eta\right)\ . \tag{25}$$

Commercial aluminum heat sink profiles have a typical CSPI $=$ $5 \ldots 7\,\mathrm{W}/(\mathrm{K\,dm^3})$, with optimized heat sink profiles a CSPI $=$

$12 \ldots 17.5\,\mathrm{W/(K\,dm^3)}$ is achievable [32], [33]. In the following, a CSPI $= 12\,\mathrm{W/(K\,dm^3)}$ is assumed.

D. Comparison of the Six-Switch Boost-Type Rectifier and the VIENNA Rectifier

In Figs. 9(a) and (c), the performance comparison of the six-switch boost-type PFC rectifier [cf. Fig. 1(a)] and the VR [cf. Fig. 1(b)] is shown based on the performance indices defined in Section IV-C. The representation is chosen such that for higher performance, a smaller area is covered.

The two boost-type rectifier systems require a similar total semiconductor chip area $\tilde{A}_{\mathrm{chip}}$ and show approximately equal relative total losses $(1-\eta)$ for the implementation variant with SiC JFETs and SiC Schottky diodes and a switching frequency of 48 kHz. The semiconductor switching losses τ_{p} of the six-switch boost-type PFC rectifier increase approximately by a factor of 2.5 for the implementation with Si IGBTs and SiC Schottky diodes and a switching frequency of 24 kHz compared with the 48 kHz SiC JFET implementation. Thus, also the required total chip area $\tilde{A}_{\mathrm{chip}}$ rises for the implementation of the six-switch boost-type rectifier with Si IGBTs and SiC Schottky diodes under the given thermal constraints for the semiconductors. The increase of switching losses τ_{p} is less pronounced in the VR with Si IGBTs and SiC Schottky diodes since the commutation voltage of the transistors is half of the commutation voltage of the six-switch boost rectifier and 650-V IGBTs can be used for the VR instead of 1200-V IGBTs. As a result, the relative total losses $(1-\eta)$ of the VR are 20% lower than the losses of the six-switch boost-type rectifier for the implementation variant with Si IGBTs and SiC Schottky diodes. Both systems show approximately the same DM and CM conducted EMI noise levels (u_{DM} and u_{CM}), and allow for continuous operation in case of a mains phase loss. The main advantage of the three-level characteristic of the VR is the significantly lower volume of the boost inductors compared with the two-level topologies, which can be seen by comparing the relative inductor volumes ρ_{L}^{-1} for the rectifier systems with a switching frequency of 24 kHz. Only a small difference between the individual systems is given regarding the volume of the output capacitors ρ_{C}^{-1} as the two- and three-level converters have similar rms values of the capacitor currents, and in any case, a series connection of two electrolytic capacitors is required due to the output voltage of $U_{\mathrm{pn}} = 700$ V. The center tap in the dc-link of the VR thus is inherently available.

In summary, the six-switch rectifier is characterized by a very simple structure of the power circuit and the VR by a relatively small overall volume or a high power density. In addition, for the VR, a short circuit of the dc-link through a faulty control of a power transistor is not possible and power transistors with relatively slow parasitic antiparallel body diodes can be used.

E. Comparison of the Active Six-Switch Buck-Type PFC Rectifier and the SWISS Rectifier

In Figs. 9(b) and (d), a conventional six-switch buck-type PFC rectifier [cf. Fig. 1(c)] and a SWISS Rectifier [cf. Fig. 1(d)] are compared. The same performance indices and representation is chosen as for the comparison of the boost-type rectifier systems, i.e., for higher performance, a smaller area is covered.

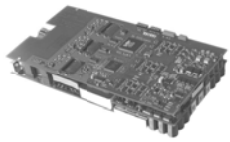
Both systems show, with respect to the total semiconductor chip area requirement $\tilde{A}_{\mathrm{chip}}$, the volumes of passive components ρ_{L}^{-1} and ρ_{C}^{-1}, the relative total losses $(1-\eta)$, and the conducted EMI noise u_{DM} and u_{CM}, only very little differences for the implementation variant with SiC JFETs and SiC Schottky diodes and a switching frequency of $48\,\mathrm{kHz}$. However, for the implementation with Si IGBTs and SiC Schottky diodes and a switching frequency of 24 kHz, the semiconductor switching losses of the SWISS Rectifier increase approximately by a factor of 1.5 compared with the SiC JFET implementation, whereas the switching losses τ_{p} for the six-switch buck-type rectifier only slightly increase. In addition, the total required chip area $\tilde{A}_{\mathrm{chip}}$ for the SWISS Rectifier variant with Si IGBTs and SiC Schottky significantly rises compared to the implementation with SiC JFETs and SiC Schottky diodes contrary to the required chip area of the six-switch buck-type rectifier, which remains approximately the same for both implementation variants. The reason for this behavior can be explained by the different commutation voltages of the six-switch buck-type rectifier and the SWISS Rectifier. The commutation voltage of the transistors in the six-switch buck rectifier is low, and thus, the total semiconductor losses are dominated by the conduction losses due to the impressed dc current. The replacement of the SiC JFETs showing low switching losses by Si IGBTs with higher switching losses in the six-switch buck-type rectifier only slightly affects the resultant switching losses. In the SWISS Rectifier, the switching losses are concentrated in the two transistors in the positive and negative bus with a higher commutation voltage compared to the six-switch buck-type rectifier. Replacing the SiC JFETs by Si IGBTs, therefore, leads to significantly higher switching losses and requires a larger transistor chip area to meet the thermal constraints. The total semiconductor area of the SWISS Rectifier is further increased by the implementation of the bidirectional injection switches and diodes by Si IGBTs and SiC Schottky diodes. Thus, for the implementation variant with Si IGBTs and SiC Schottky diodes, the relative total losses $(1-\eta)$ of the six-switch buck-type PFC rectifier are 1.2 times lower compared to the SWISS Rectifier.

An increase in efficiency of the six-switch structure would be easily possible by using an explicit freewheeling diode across the dc link. For the SWISS Rectifier, a reduction of the number of power semiconductors can be achieved through modification of the circuit topology according to Fig. 25 in [1]. In addition, the mains commutated injection switches could be implemented with an antiparallel connection of Reverse Blocking IGBTs or with Reverse Conducting IGBTs that are optimized for soft-switching applications and a low forward voltage drop as an alternative to conventional IGBTs or SiC JFETs.

In summary, the main advantage of the SWISS Rectifier is not seen in a higher performance but in a dc–dc converter like circuit structure. Accordingly, basic knowledge of the function of a passive diode rectifier of the input stage of the system is sufficient to implement a three-phase PFC rectifier with sinusoidal input current and a controlled output voltage. In particular, no space vector-based modulation scheme has to be

TABLE I
CONSTRUCTED VR PROTOTYPES WITH AN OUTPUT POWER LEVEL OF $P_{\mathrm{o}} = 10$ KW USING DIFFERENT SWITCHING FREQUENCIES






VR72	VR250	VR500	VR1000
$f_{\mathrm{P}} = 72\,\mathrm{kHz}$ $\rho = 6\,\mathrm{kW/dm^3}$ $\eta = 97.3\,\%$	$f_{\mathrm{P}} = 250\,\mathrm{kHz}$ $\rho = 10\,\mathrm{kW/dm^3}$ $\eta = 96.7\,\%$	$f_{\mathrm{P}} = 500\,\mathrm{kHz}$ $\rho = 13.8\,\mathrm{kW/dm^3}$ $\eta = 95.2\,\%$	$f_{\mathrm{P}} = 1\,\mathrm{MHz}$ $\rho = 15.1\,\mathrm{kW/dm^3}$ $\eta = 93\,\%$

implemented, which is frequently applied to three-phase converters and typically leads to difficulties when dealing the first time with three-phase systems. In terms of number of semiconductor devices and total semiconductor chip area for an implementation with IGBTs and SiC Schottky diodes, the six-switch buck-type rectifier is the preferred solution as it only requires six transistor and six diode chips compared to eight transistor and fourteen diode chips for the SWISS Rectifier.

F. Derivation of the η-ρ Pareto Front Using Constructed VIENNA *Rectifier Systems*

In the following, a Pareto Front considering the performance indices efficiency η and power density ρ is derived which is based on the data taken from constructed VR systems. Several rectifier systems with a power level of 10 kW and different switching frequencies between 72 kHz and 1 MHz have been built. The derived curve is, therefore, based on effectively constructed systems and not on theoretical calculations, which may differ from the practically implemented systems.

During the design of each considered rectifier system, the focus was laid on a high power density and the component selection/arrangement was done according to this requirement. The volume of the EMI filter, boost inductor, etc., can subsequently be analyzed using the data of the constructed systems which allows to give a statement on the practically achievable power density. The resulting power densities may, however, not be the highest possible ones for the corresponding switching frequencies and topology but serve as good values for comparison.

An overview on the constructed VR systems is given in Table I. The system VR72, with a switching frequency of 72 kHz, is forced air cooled and shows a power density of 6 kW/dm^3 (without cooling system). The rectifier system VR250, employing a switching frequency of 250 kHz, with its power density of 10 kW/dm^3 and an efficiency of 96.7% is a good tradeoff between power density and efficiency.

The rectifier system VR500, using a switching frequency of 500 kHz, is water cooled and represents an intermediate step during the exploration of the maximum possible power density. The constructed rectifier system VR1000 with a switching frequency of $f_{\mathrm{P}} = 1$ MHz shows the highest power density and detailed information can be found in [13], [17], and [24].

A breakdown of the particular volumes of the rectifier systems is given in Table II where boxed volumes are used for the functional elements of the system. This means that all parts include some air between the components. The proportion marked with "Air" is the remaining space between the boxed volumes of the specific elements. The boxed volumes fit more or less "seamlessly" together for the VR1000 rectifier system and the proportion "Air" is therefore not used for this prototype.

The measured efficiencies of the single rectifier systems at $U_{\mathrm{N,ll,rms}} = 400$ V, $f_{\mathrm{N}} = 50$ Hz, $U_{\mathrm{pn}} = 800$ V, and $P_{\mathrm{o}} = 10$ kW, are depicted in Fig. 10. The efficiency decreases approximately linearly with increasing switching frequency, and an efficiency of 93% can be read for $f_{\mathrm{P}} = 1$ MHz, whereas an efficiency of 97.3% is achieved for $f_{\mathrm{P}} = 72$ kHz. All systems use 600/650-V CoolMOS devices from Infineon. (Different power semiconductors are used for the VR prototypes compared to the selected semiconductors for the comparison performed in the previous section. However, the switching performance of the 600/650-V CoolMOS transistors is comparable with the switching performance of the considered SiC JFETs.) The reduction in efficiency is a result of the switching losses which increase linearly with the switching frequency. The extrapolated linear approximation, shown in Fig. 10, may be a too pessimistic estimation for low switching frequencies, where the conduction losses exceed the switching losses. This is, however, not further considered here.

The volumes of the corresponding boost inductors are given in Fig. 11. All inductors are designed for a peak current value of 27 A. According to Fig. 11, this volume decreases continuously for higher frequencies. A high-frequency material (Micrometals -8) must be used for a switching frequency of 1 MHz in order to avoid high core losses. The size of the inductor is larger than the one of a system using a material with higher permeability due to the considerably reduced permeability of this material. Another limitation can be found in the minimum required copper area of the winding as the rms current of the inductor remains constant, i.e. does not scale with the switching frequency.

Next, the volumes of the EMI filters are inspected, and the corresponding volumes are plotted in Fig. 12 as a function of

TABLE II
BREAKDOWN OF PARTICULAR VOLUMES AND CALCULATED POWER DENSITIES OF THE CONSTRUCTED VR PROTOTYPES USING EITHER AN OPTIMIZED FORCED AIR COOLING SYSTEM WITH A CSPI $= 12$ K/(Wdm^3) OR WATER COOLING

	VR72	**VR250**	**VR500**	**VR1000**
Semiconductors	$0.059\,\mathrm{dm}^3$	$0.042\,\mathrm{dm}^3$	$0.038\,\mathrm{dm}^3$	$0.038\,\mathrm{dm}^3$
Output capacitor	$0.255\,\mathrm{dm}^3$	$0.174\,\mathrm{dm}^3$	$0.07\,\mathrm{dm}^3$	$0.07\,\mathrm{dm}^3$
Boost inductors	$0.285\,\mathrm{dm}^3$	$0.223\,\mathrm{dm}^3$	$0.117\,\mathrm{dm}^3$	$0.08\,\mathrm{dm}^3$
EMI filter	$0.612\,\mathrm{dm}^3$	$0.403\,\mathrm{dm}^3$	$0.345\,\mathrm{dm}^3$	$0.34\,\mathrm{dm}^3$
Auxiliary supply	$0.104\,\mathrm{dm}^3$	$0.019\,\mathrm{dm}^3$	$0.053\,\mathrm{dm}^3$	$0.053\,\mathrm{dm}^3$
Gate drive	$0.074\,\mathrm{dm}^3$	$0.045\,\mathrm{dm}^3$	$0.047\,\mathrm{dm}^3$	$0.047\,\mathrm{dm}^3$
Control	$0.059\,\mathrm{dm}^3$	$0.053\,\mathrm{dm}^3$	$0.032\,\mathrm{dm}^3$	$0.032\,\mathrm{dm}^3$
Air	$0.22\,\mathrm{dm}^3$	$0.039\,\mathrm{dm}^3$	$0.021\,\mathrm{dm}^3$	–
Total volume	$1.67\,\mathrm{dm}^3$	$0.998\,\mathrm{dm}^3$	$0.723\,\mathrm{dm}^3$	$0.66\,\mathrm{dm}^3$
Power density (No cooler)	$6\,\mathrm{kW/dm}^3$	$10\,\mathrm{kW/dm}^3$	$13.8\,\mathrm{kW/dm}^3$	$15.1\,\mathrm{kW/dm}^3$
Forced air cooling				
Heat sink	$0.45\,\mathrm{dm}^3$	$0.55\,\mathrm{dm}^3$	$0.8\,\mathrm{dm}^3$	$1.17\,\mathrm{dm}^3$
Total volume	$2.12\,\mathrm{dm}^3$	$1.55\,\mathrm{dm}^3$	$1.52\,\mathrm{dm}^3$	$1.83\,\mathrm{dm}^3$
Power density	$4.7\,\mathrm{kW/dm}^3$	$6.5\,\mathrm{kW/dm}^3$	$6.6\,\mathrm{kW/dm}^3$	$5.5\,\mathrm{kW/dm}^3$
Water cooling				
Heat sink	$0.092\,\mathrm{dm}^3$	$0.074\,\mathrm{dm}^3$	$0.046\,\mathrm{dm}^3$	$0.046\,\mathrm{dm}^3$
Total volume	$1.77\,\mathrm{dm}^3$	$1.07\,\mathrm{dm}^3$	$0.77\,\mathrm{dm}^3$	$0.71\,\mathrm{dm}^3$
Power density	$5.7\,\mathrm{kW/dm}^3$	$9.3\,\mathrm{kW/dm}^3$	$13\,\mathrm{kW/dm}^3$	$14.1\,\mathrm{kW/dm}^3$

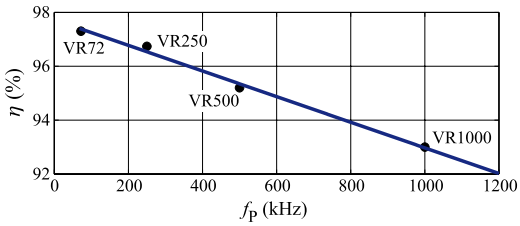


Fig. 10. Measured efficiencies η of the constructed rectifier systems as a function of the switching frequency f_P.

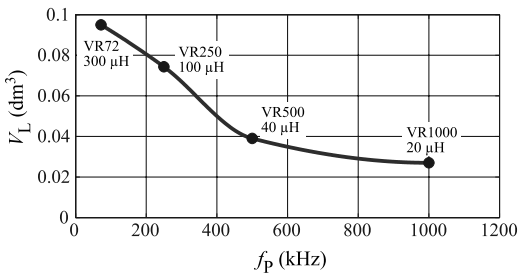


Fig. 11. Boxed volumes of the constructed boost inductors V_L for the implemented 10 kW rectifier systems as a function of the switching frequency f_P.

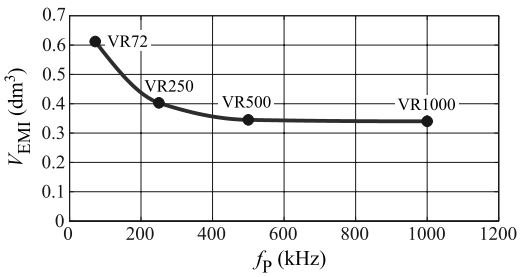


Fig. 12. EMI filter volumes V_{EMI} of the implemented 10 kW rectifier systems as a function of the switching frequency f_P.

the switching frequency. It is obvious that an increase of the switching frequency from 500 kHz to 1 MHz does not result in a significant volume reduction of the EMI filter. The reason can again be found on one hand in the lack of a suitable magnetic material. On the other hand, two small fans are inserted in the VR1000 rectifier system in order to improve the cooling of the inductors operating at their thermal limits. These fans require the reduced space that is obtained by the increase of switching frequency. An additional limitation is the lower emission limit of the EMI standard (CISPR 11) for lower frequencies which demands a higher attenuation for a switching frequency of 500 kHz or 1 MHz. An increase to such high switching frequencies is, therefore, from the EMI filter point of view, not beneficial.

Using the volumes listed in Table II, the power densities of the rectifier systems can be calculated, and the results are given in Fig. 13. Two of the systems are forced air cooled (VR72 and VR250), and the other two systems use a water cooler (VR500 and VR1000). The volumes of the constructed systems are, therefore, not directly comparable. Due to the limited volume reduction of the EMI filter, for switching frequencies above 500 kHz, also the power density saturates. A maximal power density of 15.1 kW/dm^3 is achieved for $f_P = 1$ MHz if the heat sink is not considered. A practically implemented system,

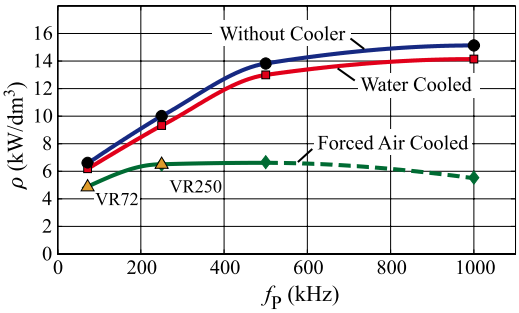


Fig. 13. Achieved power densities ρ of the constructed rectifier systems without cooler, water cooled, and forced air cooled assuming a CSPI of 12 K/(W dm^3) as a function of the switching frequency f_P. (The volume of the heat exchanger and the pump of the water cooled systems VR500 and VR1000 are not considered in this plot.) The achieved power densities of the implemented air-cooled rectifier systems VR72 and VR250 are shown with orange triangles.

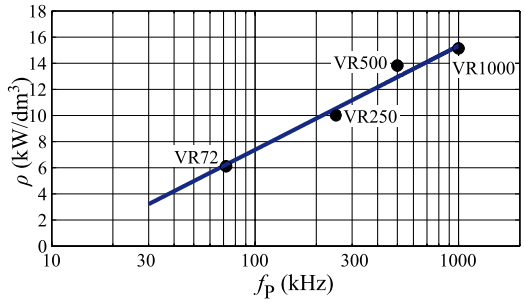


Fig. 14. Power densities ρ of the constructed VIENNA Rectifier ystems as a function of the switching frequency f_P.

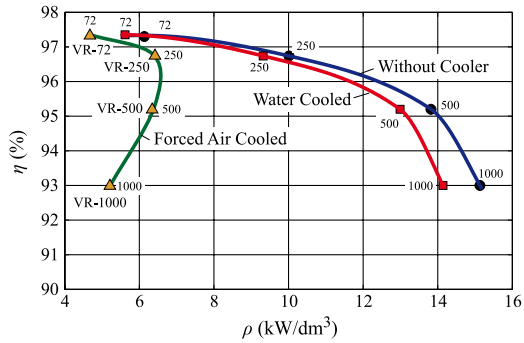


Fig. 15. Efficiency-power density η-ρ-Pareto curves of the VR topology. Pareto curves without a cooler, using forced air cooling with CSPI = 12 K/(W dm^3), and using a properly designed water cooler are given. Switching frequencies (in kHz) are marked in the particular curves. The resultant power densities of the implemented rectifier systems are shown with orange triangles.

however, requires a heat sink, and its volume must be included in the power density as the switching losses and, therefore, also the cooling demand increases with increasing switching frequency. The calculated power densities including a water cooler are plotted in Fig. 13 as well. The same power board (same type of semiconductors, semiconductor packages, and same arrangement) is used in the rectifier systems VR500 and VR1000. A water cooler is designed for the rectifier system VR1000 which shows an area equivalent to the area of the power semiconductors and a thickness of 11 mm. Please note, that the size of the remaining cooling system such as pump, heat exchanger, etc., is not considered. The VR1000 shows considerably higher semiconductor power losses than the system VR500, and the cooling system is designed accordingly. It is, therefore, also able to dissipate the smaller power losses of the system VR500. The size of the water cooler itself cannot be reduced for the VR500 as the same power board with the same semiconductor packages is used although the system VR500 shows considerably smaller power losses.

The rectifier systems VR72 and VR250 are originally air cooled, and in order to be able to compare the four rectifier systems, a water cooler with the same thickness and an area equivalent to the total footprint of the power semiconductor is assumed for the originally forced-air-cooled rectifier systems VR72 and VR250. In total, the rectifier system VR1000 results in a remarkable power density of 14.1 kW/dm^3, but it is worth noting that even for $f_P = 72$ kHz, a power density of 6.5 kW/dm^3 can be achieved.

The question arises how the VR system performs if forced air cooling is used. An optimized forced air cooled heat sink with a CSPI of 12 K/(W dm^3) is assumed. Using (26), the volume of the heat sink V_s can be determined. A heat sink temperature of $T_s = 75\,^\circ$C, and an ambient temperature of $T_a = 25\,^\circ$C are assumed. The total power densities including the heat sink are given in Fig. 13. The power density is now considerably reduced and a maximal value of 6.5 kW/dm^3 can be read at a switching frequency of approximately 350 kHz. It has to be stated that due to limitations with heat spreading, a switching frequency of 1 MHz cannot be implemented using forced air cooling. Only a dashed power density curve is hence plotted in Fig. 13 in order to illustrate this limitation. In addition, the power densities of the practically implemented air-cooled rectifier systems VR72 and VR250 are shown (orange triangles). The cooling system of these rectifiers show a CSPI below 12 K/(W dm^3) and a reduced power density is, therefore, obtained.

If the power densities are plotted using a logarithmic scale for f_P as shown in Fig. 14, the improvement of power density as a function of switching frequency can directly be read. A straight line is, therefore, fitted into the achieved power densities plotted in the logarithmic scale. According to Fig. 14, the power density could be improved by a factor of 1.88 (≈ 2) if the switching frequency is increased by a factor of 10. This experimentally proves the expected gain in power density by increasing the switching frequency based on implemented hardware prototypes, which was previously estimated in [34].

The resulting η-ρ-Pareto Fronts are given in Fig. 15 where corresponding switching frequencies (in kHz) are marked in the curves. Starting from $f_P = 72$ kHz, an increase in the switching frequency leads, due to the increase of the switching losses and therewith an increase in the heat sink volume, to a reduction of the power density, which cannot be compensated by the possible reduction of the EMI filter. A higher switching frequency, e.g., $f_P = 250$ kHz is, therefore, only sensible, if a low distortion of the input current must be guaranteed at high mains frequencies as, e.g., for More Electric Aircraft (MEA) applications [35] with $f_N = 360$–800 Hz.

The best compromise between the efficiency and the volume determining technologies was identified during the design process for each system. A switching frequency of $f_{\mathrm{P}} \leq 250$ kHz is recommended for an industrial implementation based on the current state-of-the-art as it leads to a relatively high power density ($\rho = 5.2$ kW/dm^3) and still a high nominal efficiency ($\eta_{\mathrm{nom}} = 96.7\%$), and guarantees a high input current quality also for high mains frequencies.

V. Conclusion

A comparative evaluation of two boost-type and two buck-type three-phase PFC rectifiers has been performed and substantiated with selected examples of hardware demonstrators of VR systems to investigate the achievable efficiency η versus power density ρ limit (η-ρ-Pareto-Front) for practical three-phase PFC rectifier systems.

The comparison results of the boost-type systems reveal that the six-switch boost-type PFC rectifier and the VR show similar overall performance. The six-switch boost-type rectifier features a very simple circuit topology and control, whereas the VR is characterized by a relatively small overall volume or a high power density as it requires approximately only half of the inductance for the boost inductors compared to the six-switch rectifier. Opposed to the six-switch rectifier, the VR enables a high efficiency at elevated switching frequencies with Si (standard) $600/650$-V IGBTs or MOSFETs and SiC Schottky diodes as a result of its three-level characteristic and does not require advanced 1200-V SiC power transistors (e.g., SiC JFETs) to lower the switching losses.

The comparison results of the buck-type systems show, in a similar manner as for the boost-type systems, comparable overall performance between the six-switch buck-type PFC rectifier and the Swiss Rectifier. In terms of total semiconductor chip area and number of semiconductor devices for an implementation with IGBTs and SiC Schottky diodes, the six-switch rectifier is the favorite topology. The main advantage of the Swiss Rectifier is not seen in a higher performance but in a dc–dc converter like circuit structure and very simple modulation. In addition, the Swiss Rectifier provides inherently a free-wheeling path for the dc output current, which is impressed in the output inductors, whereas for the buck-type PFC rectifier, an additional diode between the positive p and negative n dc bus has to be added to enable the same functionality. Mainly the Swiss Rectifier benefits from the use of SiC power transistors to reduce semiconductor losses in the two switches in the positive and negative bus.

Under the given design constraints, the two boost-type PFC rectifier systems require in general a lower semiconductor area but a larger volume for the passive components, generate a higher DM and CM noise, and allow for a higher efficiency compared to the two buck-type PFC rectifier systems.

The investigation of the performance figures of the VR hardware demonstrators indicates a switching frequency limit of $f_{\mathrm{P}} \leq 250$ kHz for an industrial system using standard printed circuit board interconnection technology to achieve a good compromise between efficiency and power density. A higher switching frequency is only sensible if a low input current distortion must be ensured at high mains frequencies (e.g., for More Electric Aircraft applications with $f_{\mathrm{N}} = 360$–800 Hz). The efficiency versus power density analysis of the implemented VR systems further demonstrates that an increase of the switching frequency by a factor of ten improves the power density approximately by a factor of two.

When developing industrial converter systems, besides a defined efficiency and power density, mainly a cost target has to be met, and a certain lifetime has to be guaranteed, i.e., multiple performance indices have to be simultaneously considered. It is, therefore, essential to understand the mutual dependence of the performance indices in the course of the design, e.g., the tradeoff between power density ρ (kW/dm^3) and efficiency η (%). In order to obtain a complete picture, also the relation between η and ρ and the relative costs σ (kW/$), i.e., also the η-σ- and ρ-σ-Pareto Fronts should be considered. Such analysis so far has been only rarely performed and is, therefore, seen as a focus of future academic research in the field of three-phase PWM rectifier systems and as a key topic in power electronics in general.

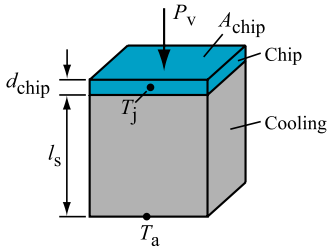


Fig. 16. Simplified model of a unipolar transistor including cooling conditions (thermal constraints, T_{a} and T_{j}) used to derive the relation between the conduction losses and the rms current flowing through the device. Considering also the thermal condition, i.e., a scaling of the chip such that the junction temperature remains at $T_{\mathrm{j}} = T_{\mathrm{j,max}}$, the conduction losses can be modeled linearly remains to the rms current $P_{\mathrm{v}} \propto I_{\mathrm{rms}}$ flowing through the device.

Appendix A
Relationship Between Chip Area and RMS Current Under Thermal Constraints

In Section IV-C, a linear dependence on the transistor and diode rms currents is used for the performance indices τ_{C} and δ_{C}. In the following, the reason for this unintuitive approach is discussed, which is justified by the relation of the conduction losses and the rms current of unipolar transistors (MOSFET, JFET) under defined thermal constraints.

The considered model of a transistor is given in Fig. 16. The chip has the area A_{chip}, the thickness d_{chip}, and for this simplified model, a constant temperature T_{j} is assumed in the whole chip. The chip is mounted on a heat sink with equal footprint as the chip and with the thickness l_{s}.

Considering the ambient temperature T_{a} the temperature difference $\Delta T_{\mathrm{j-a}} = T_{\mathrm{j}} - T_{\mathrm{a}}$ can be calculated. The maximum junction temperature T_{j} is limited to $T_{\mathrm{j-a,max}}$ which results in a maximum value $\Delta T_{\mathrm{j-a,max}}$ for a defined ambient temperature. Using the definition of the thermal resistance, which represents

the entire thermal resistance from the ambient to the junction

$$R_{\mathrm{th}} = \frac{l_{\mathrm{s}}}{\gamma A_{\mathrm{chip}}} \tag{26}$$

the maximum temperature difference between junction and ambient can be calculated as

$$\Delta T_{\mathrm{j-a,max}} = P_{\mathrm{v}} R_{\mathrm{th}} \tag{27}$$

where P_{v} are the total conduction losses of the chip. As can be seen in (26), the thermal resistance R_{th} is inversely proportional to the chip area A_{chip}. This results in a minimum required chip area of

$$A_{\mathrm{chip,min}} = \frac{l_{\mathrm{s}}}{\gamma \Delta T_{\mathrm{j-a,max}}} P_{\mathrm{v}}. \tag{28}$$

According to (28), $A_{\mathrm{chip,min}}$ is directly proportional to the conduction losses of the chip.

On the other hand, the conduction losses of the chip can be calculated using the resistive behavior of the channel

$$P_{\mathrm{v}} = I_{\mathrm{rms}}^2 \frac{d_{\mathrm{chip}}}{\sigma A_{\mathrm{chip}}}. \tag{29}$$

Combining (28) and (29) results in

$$A_{\mathrm{chip,min}} = \frac{l_{\mathrm{s}}}{\gamma \Delta T_{\mathrm{j-a,max}}} I_{\mathrm{rms}}^2 \frac{d_{\mathrm{chip}}}{\sigma A_{\mathrm{chip,min}}} \tag{30}$$

which after some simplification and grouping finally yields to

$$A_{\mathrm{chip,min}} = \sqrt{\frac{l_{\mathrm{s}} d_{\mathrm{chip}}}{\gamma \sigma \Delta T_{\mathrm{j-a,max}}}} I_{\mathrm{rms}}. \tag{31}$$

The minimum chip area $A_{\mathrm{chip,min}}$ is thus directly proportional to I_{rms} of the device if the maximum temperature difference between the junction and ambient is constant $T_{\mathrm{j-a,max}} = \mathrm{const}$. As according to (28), also the power losses are directly proportional to the chip area, and thus also P_{v} is directly proportional to I_{rms}

$$P_{\mathrm{v}} \propto A_{\mathrm{chip,min}} \propto I_{\mathrm{rms}} \tag{32}$$

if the cooling system limitations are considered. The power losses itself are indeed proportional to the square of I_{rms}^2. If however, the cooling system is considered operating at its particular limits, which may be the case in an optimization and/or the chip area is adapted depending on the occurring losses, a linear behavior can be used to model the conduction losses of an unipolar transistor.

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