Novel Protection Strategy for Current Interruptions in IGBT Current Source Inverters

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Abstract— **A novel protection strategy against dc link overvoltages in IGBT current source inverters caused by current interruptions is presented. The proposed concept consists of two steps - a fast passive voltage clamp and actively turned on freewheeling paths across the dc link terminals. To implement this strategy, an electronic circuit was developed and successfully tested. The protection circuit is completely independent from normal inverter operation, has no effect on the CSI behaviour and can be realized at low cost.**

I. INTRODUCTION

Power converters of the current source type (CSI) are commercially used for many years. The inherent ability for regenerative operation with only a total of 12 reverse blocking power devices and the sinusoidal input and output currents make CSIs very interesting especially in high-power application, where symmetrically blocking GTOs could be used.

CSIs using IGBT switches are still not widely spread, because up to now no market damands as well as no reverse blocking IGBT with an appropriate switching characteristic exist. The required additional series diode to every IGBT doubles the number of power semiconductors compared to GTO CSIs and makes IGBT CSIs unattractive compared to VSIs (voltage source inverters), although a CSI has notable advantages (regenerative operation, much better EMC).

Besides the number of required power semiconductors, it has some other drawbacks. One is the constraint, that as long as the dc link inductor carries current, the conductance in the loop consisting of four IGBTs and four diodes must never be lost. Otherwise, e.g. if a diode, switch, driver or modulation fault occurs, the inductor back emf produces a high overvoltage. This acts on the semiconductor switches and may destroy them.

In GTO CSIs such current interruptions are not a critical problem, because GTOs commonly use dv/dt snubbers and also show an inherent overvoltage protection mechanism. If their breakdown voltage is exceeded, they automatically fire again and start conducting with the normal forward voltage. In a CSI, the energy stored in the dc link inductor will then be dissipated without exceeding the SOA (safe operating area) of the GTO.

This does not apply for IGBTs. In the case of a current interruption, the voltage across the switch will rise to the breakdown voltage and remain at this level causing excessive heat. Without protective measures, the IGBT will be destroyed within only a few microseconds. A chain reaction with a complete bridge destruction may result.

To avoid this, a suitable protection method has to be found. The fact of self-protection in GTO CSIs and the less spread of IGBT CSIs may be the reason, why only sparse informations could be found in literature about CSI overvoltage protection [1].

In this paper, after giving a general overview of CSI operation (II) and explaining the appearance of overvoltages caused by current interruptions (III), the characteristics of conventional voltage limiting devices are described and their usability for CSI protection is discussed (IV). To fully protect the semiconductor switches against dc link overvoltages, a novel strategy is presented and an electronic circuit is developed to implement the new concept (V). The paper closes with measurement results, that show the efficiency of the protection hardware (VI).

II. OPERATION OF A CSI

Fig. 1 shows the basic circuit of a three phase IGBT current source inverter consisting of two bridges with a total of 12 reverse-blocking switches (IGBT with series diode). Both bridges commonly operate in pwm mode using various modulation and control techniques depending on the required switching frequency and dynamic response time of the drive.

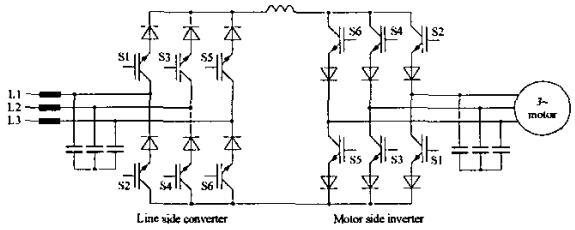

Fig. 1. Basic circuit of a CSI drive

It is common for all modulation schemes, that always four switches must conduct to provide a continuous path for the dc link current. This may flow in the dc link only (shorted bridge legs) or through lines and/or motor phases. Capacitors across the input and output terminals ensure, that the currents in the mains or motor inductances can decay, if the related bridge leg was actively turned off and the current has commutated to another leg.

It should be mentioned but not further described here, that the capacitors across the input and output terminals are only dimensioned to store the energy of the mains or motor inductances during normal CSI operation, what means, that a continuous pulsing of the CSI is assumed. Otherwise, e.g.

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after the complete bridge is turned off ("pulse off"), it is not ensured, that the voltages across the filter capacitors remain symmetric, which could cause the voltage across one or more capacitors and/or switches to exceed their maximum ratings. These fault situations are analyzed in details in [2].

In the present paper, the focus is on current interruptions in the dc link. Their impact on the mains and motor side is not further discussed.

III. DC Link Current Interruptions in a CSI

A. Characteristics of the dc link current path in IGBT CSIs

The dc link of a CSI is highly inductive. Besides parasitic effects (IGBT, diode, inductor capacitance), there is no capacitive element in the dc link, that could limit the voltage slope in the case of a current interruption. Especially there is no inherent freewheeling path, as it could be found in a VSI. In IGBT CSIs there is also no voltage limiting device like in GTO CSIs. A GTO would automatically be turned on, if its breakdown voltage is exceeded, whereas an IGBT remains at the breakdown voltage comparable to MOSFETs.

As the IGBTs are not dimensioned to withstand the high momentary power dissipation in the case of such an overvoltage for more than some microseconds, whereas the dc link current needs a much longer time to become zero, a protection circuit is required, that provides a current path as long as the dc link current is greater than zero. It must also ensure a conductance high enough to limit the voltage to a level below the maximum rating of the switches even at nominal dc link current.

In the following it will first be described what happens, when one of the switches, that should be on, loses its conductance and interrupts the dc link current. This may be caused by a switch, driver, modulation or power supply failure.

B. Effect of a dc link current interruption

Fig. 2 shows the equivalent circuit diagram of the dc link.

The voltage source $v_{d,m}$ is an equivalent for the mean value of the voltage applied to the dc link by the motor side inverter.

$S_{1,3,5}$ should represent the switch currently conducting in the top half bridge of the line converter, $S_{2,4,6}$ is the conducting switch of the bottom half bridge. C_{filter} represents the filter capacitor across the input terminals, whose voltage is currently switched to the dc link. During normal CSI operation with constant dc link current, the mean values of the line and the motor side dc link voltage are equal.

C_{Ld} stands for the parasitic capacitance of the dc link inductor referenced to the bottom dc link terminal. C_{oes} is the sum of all applicable output capacitances of the switches (IGBTs and diodes), also referenced to the bottom dc link terminal.

Fig. 2 also shows a SPICE simulation plot of a dc link current interruption using typical values of a 22 kW CSI drive working at a 400 V grid voltage. The values of the interesting elements are shown in table I.

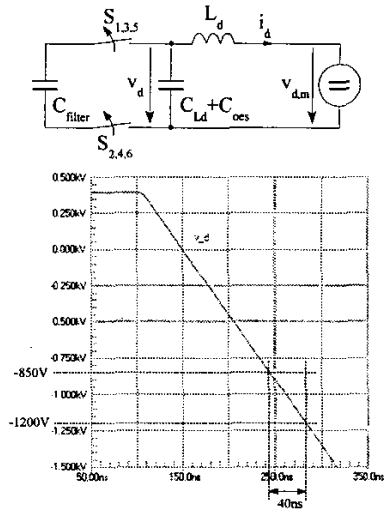

Fig. 2. Dc link voltage slope after interrupting the inductor current

TABLE I
ELEMENT VALUES OF THE 22 KW EXAMPLE DRIVE

C_{Ld}	5 nF
C_{oes}	400 pF
L_d	30 mH
$I_{d,nom}$	45 A
$V_{IGBT,max}$	1200 V

The current interruption occurs at time $t_1 = 100$ ns, when one of the conducting switches fails or is unintentionally turned off. The motor side dc link voltage at this point of time should be approx. 400 V.

It can be seen in fig. 2, that the line side dc link voltage starts to fall from its initial value of 400 V with a slope only limited by the parasitic capacitances according to equation (1). Using the values in table I as an example a slope of approx. 8.3 kV/µs results.

$$\frac{dv_d}{dt} = \frac{1}{C_{Ld} + C_{oes}} i_d \qquad (1)$$

The levels printed in fig. 2 at 1200 V and 850 V should represent the IGBT breakdown voltage and the voltage, from which on an overvoltage condition could first be detected. The latter is calculated according to (2) out of the maximum rectified grid voltage, grid tolerances (10 %), the max. allowed commutation overvoltage v_{co} (e.g. 150 V; depends on the parasitic inductances in the commutation path and the IGBT switching speed) and tolerances in the overvoltage detection circuit (e.g. 10 %).

$$v_{min} \approx \left(\sqrt{2} v_{grid}\left(1 + tol_{grid}\right) + v_{co}\right)\left(1 + tol_{detect}\right) \qquad (2)$$

For the 22 kW test drive a minimum detection voltage of 850 V is calculated.

It does not make sense to set the detection limit lower than calculated in (2), because all voltage levels up to v_{min}

could be reached during normal CSI operation and the protection must be inactive then.

It is now interesting, how fast the protection circuit has to become active to ensure a dc link voltage below the switch breakdown voltage. In fig. 2 a time of about 40 ns can be grafically extracted. It can also be easily calculated using the voltage difference between the two levels and the calculated slope using equation (1).

What is also required to develop a protection strategy is the maximum momentary power and the total amount of energy to dissipate.

The momentary power can be calculated according to (3) out of the maximum clamping voltage (e.g. equal to the IGBT breakdown voltage) and the maximum dc link current.

$$p_{max} = v_{clamp} i_{d,max} \tag{3}$$

Using $v_{clamp} = 1200$ V and $i_{d,max} = i_{d,nom} = 45$ A for the 22 kW CSI, a peak momentary power dissipation of 54 kW results.

$$e_{max} = \frac{1}{2} L_d i_{d,max}^2 \tag{4}$$

The total energy to dissipate is equal to the dc link inductor energy (4), which is 30 J for the test drive.

Knowing these values allows an estimation, if the used bridge IGBTs are capable of dissipating this energy without being damaged. But this consideration is superfluous, because IGBTs are not rated for an operation in the avalanche region, so under all circumstances it has to be ensured by external circuitry, that the breakdown voltage is never exceeded.

IV. Conventional Overvoltage Protection Strategies

The greatest problem for protection of an IGBT CSI is the very short time available to react on an overvoltage condition in the dc link as shown in the previous chapter (fig. 2). There are currently no obtainable protection devices, that can be actively turned on within this time. In the following an overview of conventional currently employed passive voltage limiting devices/strategies is presented and their suitability for CSI protection is discussed.

A. Voltage limiting discretes (varistors / zener diodes)

Varistors and zener diodes are commercially available with various breakdown voltages, are quite fast and show a high energy absorption capability in relation to device volume, which surely is one criteria for an appropriate device for CSI protection.

Unfortunately varistors and zener diodes have a quite flat v/i-characteristic, which would require the use of very large devices. Only then they would be able to reliably block below the minimum detection voltage (eq. 2) and at the same time limit the overvoltage at maximum dc link current below the IGBT breakdown voltage.

B. Active clamping

Active clamping [3] of the turned off switches could also provide the required response time and compared to varistors, much steeper v/i characteristics can be attained.

However for active clamping it is required to equip all 12 bridge IGBTs with clamping circuits and protection also only works, if the switches are all still operative. If a defective IGBT is the cause of the overvoltage, the protection would fail.

Another drawback of clamping is the fact, that an immediate pulse off of the whole inverter, which makes sense in several other failure situations [2], would not be possible any longer. This is because during clamping the current will still flow through the clamped switches and may be distributed to the line and motor side filter capacitors. This could cause an unsymmetric charge, resulting in line/motor side overvoltages and/or overcurrents.

Furthermore the high peak losses in the clamped IGBTs (totally 54 kW in the above example with 1200 V clamping voltage) cause extreme stress on the devices, which they typically cannot withstand. The transient thermal response of economically dimensioned IGBTs commonly allow clamping at this high power rate only for a maximum of some 10 µs. This time would never be long enough to dissipate the dc link inductor energy.

The calculated 30 J in the above example of the 22 kW drive would require clamping at 1200 V for about 1.1 ms with a mean value for the power dissipation of 27 kW (half the peak power). The transient thermal impedance of the used 75 A IGBT (BSM75GB120D) is published in the datasheet for a 1 ms pulse with a value of 0.01 K/W. According to equation (5), a rise in junction temperature of about 270 K results, which will inevitably destroy the IGBT.

$$\Delta T_j = Z_{th}(t_{pulse}) \cdot \bar{P}_d = Z_{th}(t_{pulse}) \cdot v_{clamp} \cdot \bar{i}_d \tag{5}$$

C. Breakover diodes

Breakover diodes (BOD) are devices, that operate in a non conducting off-state, until the breakover voltage is applied to its terminals. The BOD will then start conducting with a rather low forward voltage, comparable to a parasitically fired thyristor or GTO, and will remain in this on-state until the current is reduced below the minimum holding current of the BOD.

The static behaviour of breakover diodes is ideal for CSI protection, because the low forward voltage allows the inductor energy to be safely dissipated without producing such excessive heat as if the voltage is clamped at a high level. And if the inductor current becomes zero, the BOD automatically turns off again.

The main disadvantage, which prevents breakover diodes from being used for protection in IGBT CSIs, is their poor dynamic behaviour, especially the maximum rate of voltage rise that may be applied to the BOD. If this slope is exceeded, the BOD could accidentally turn on even if the breakover voltage is not reached already.

Typical BODs allow voltage slopes of about 1000 V/µs. They are well suited for thyristor protection, but due to the short voltage rise and fall times in IGBT circuits (10 kV/µs or more), they are not applicable for IGBT protection.

V. Novel Protection Strategy for CSI Dc Link Current Interruptions

The overview in the last section shows, that all currently available limiting devices are not a perfect solution for CSI protection. For this reason a novel two-step strategy was developed that provides both, an appropriate response time for voltage limitation and a safe dissipation of the inductor energy.

To handle dc link current interruptions in a fast switching IGBT CSI, a combination of passive and active protection mechanisms is proposed.

A. Basic two-step protection concept

The basic concept of the new protection strategy consists of two steps:

1) Fast and "hard" voltage limitation

As there are no devices available, that could be turned on within the required response time and conduct the full dc link current, the CSI is equipped with an ultra fast passive clamping circuit, that can dissipate the momentary peak power for at least the time, a freewheeling path needs to become active (500 ns up to 2 µs). At the same time, the clamping circuit is able to limit the voltage at full dc link current below the maximum rating of the IGBTs ("hard" limitation).

For this limitation, devices with a steep v/i characteristic are required. MOSFETs working in the avalanche breakdown [3] are proposed for this purpose.

2) Extra (actively turned on) freewheeling path across the dc link terminals

Immediately after an overvoltage situation is detected, the 6 switches of the related bridge should be pulsed off and an extra freewheeling path across the dc link terminals must be opened. This is held on, until the inductor energy becomes zero. Compared to clamping of the dc link voltage at a high voltage level this reduces the momentary power dissipation at the expense of a longer time to get the inductor current to zero. As the CSI has to be powered down anyway in such a fault situation, time is not an important factor.

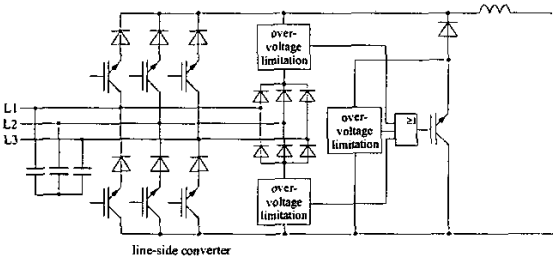

Fig. 3. CSI with overvoltage protection circuit against dc link interruptions (shown is only line side)

Fig. 3 shows the CSI with the proposed detection/protection circuits for the line side converter. It applies to the motor side inverter accordingly.

B. Overvoltage detection and limitation circuit

For detection and limitation of an overvoltage, a chain out of medium voltage MOSFETs (100 V ... 400 V) working in the avalanche breakdown is proposed (fig. 4).

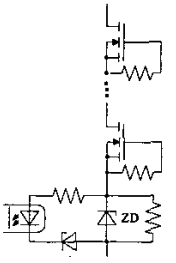

Fig. 4. MOSFET chain for voltage limitation

MOSFETs are best suited for this application because they have a much steeper breakdown v/i-characteristic compared to other available voltage limiting devices like zener diodes or varistors [3] [4]. As the historically known latch-up problems have also been overcome with modern MOSFETs, the maximum junction temperature would be the only limiting criteria for the size of the applicable MOSFETs [5].

The rise in junction temperature can easily be calculated by equation (5) using the single-pulse dynamic thermal response of the MOSFET (published in the datasheet) and the power dissipation during clamping.

In the example of the 22 kW CSI drive, a chain of four IRF640 MOSFETs (200 V, TO220 case) was used without any cooling. The devices are able to conduct the nominal current of 45 A at 250 V clamping voltage for about 10 µs, what is long enough to turn the freewheeling path on.

The clamping chain could be also used for overvoltage detection and triggering of the freewheeling IGBT driver. Therefore, in the developed circuit the clamping current also flows through a low voltage zener-diode (ZD in fig. 4; e.g. 16 V) in series to the MOSFET chain. The provided voltage drop can be used for directly driving the sender diode of an optocoupler, that works as trigger element for the freewheeling IGBT driver. It should be noted that due to the high voltage slope between the sender and receiver side, care must be taken when selecting an appropriate optocoupler. A coupler with a common mode transient immunity of at least 10 kV/µs must be used in the considered CSI.

The resistor in parallel to ZD is required, because the zener diode in series to the MOSFET chain is dynamically the bottom element of a capacitive voltage divider. The voltage drop across ZD is determined by the relationship of the parasitic capacitances of MOSFETs and zener diode, which could under certain conditions (unfavourable ratio of MOSFET and zener diode capacitances) cause the zener voltage do be reached, even if the voltage applied to the

total chain is well below the limiting level. The capacitively injected current caused by the regular voltage slope in the dc link (e.g. during commutation events), could hereby be high enough to trigger the optocoupler. To avoid this, the dynamic (and static) impedance of the zener diode is reduced by a low ohmic parallel resistor (e.g. 10 Ohms), which absorbs almost the complete injected current.

C. *Overvoltage distribution across the switches*

As shown in fig. 3, the limitation/detection circuit is required six times in a CSI. The reason is, that the voltages across the top half bridge, the bottom half bridge and the dc link terminals must be limited individually for the line and motor side bridge. This will be explained on the basis of the three possible interruption cases for the line side converter, which are the failure of

- one switch in the top half bridge (S_1, S_3 or S_5)
- one switch in the bottom half bridge (S_2, S_4 or S_6)
- one switch simultaneously in both the top and the bottom half bridge.

The switch and voltage naming is illustrated in fig. 5.

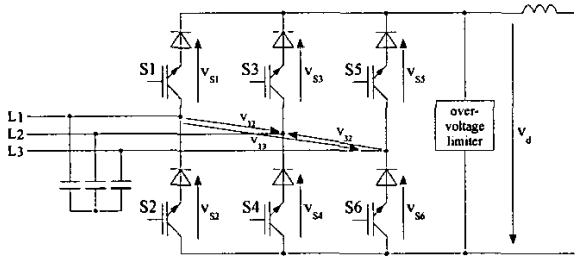

Fig. 5. Line side power circuit with only a v_d limiter

1) Interruption in one of the conducting switches of the top half bridge (e.g. driver or IGBT failure)

If the conducting switch of the top half bridge loses conductance, the top dc link terminal is isolated from the mains, whereas the bottom dc link terminal is still connected to the potential of one of the mains phases.

The voltages across the three IGBTs of the top half bridge could now be calculated as sum out of the dc link voltage v_d and the momentary line-to-line voltage between the phase connected to the conducting switch of the bottom half bridge and the related IGBT in the top half bridge.

Assuming S4 is still on, the voltages across S1, S3 and S5 could be calculated according to equations (6).

$$\begin{aligned} v_{S1} &= v_{12} - v_d \\ v_{S3} &= -v_d \\ v_{S5} &= v_{32} - v_d \end{aligned} \tag{6}$$

Depending on the sign of the corresponding line-to-line voltage, the voltages across S1, S3 and S5 can be lower, equal or higher than the momentary dc link voltage v_d.

2) Interruption in one of the conducting switches of the bottom half bridge (e.g. driver or IGBT failure)

Same as 1). Now the voltages across S2, S4 and S6 can be higher, equal or lower than v_d.

3) Simultaneous interruption in both half bridges (modulation fault, power supply failure, pulse off)

In this case, the dc link and the mains have no common potential any longer. The dc link current cannot flow through any of the bridge IGBTs and the dc link voltage rise is distributed across the top and bottom half bridge more or less symmetrically.

Fig. 6 shows a constructed time plot of the interruption case 1). It should clarify the voltage distribution across dc link, S1, S3, S5 and S4 for the example of a still conducting switch S4 and switch S1 being (unintentionally) turned off at a certain phase angle ($v_{12} = 566$ V). The overvoltage limiter should be assumed to be set to 1000 V limitation voltage.

It can be recognized that in the shown fault case only limiting the dc link voltage v_d below the IGBT breakdown voltage (here 1000 V limitation voltage) is not sufficient, as the voltage across S1, S3 or S5 could be higher than $-v_d$. In the considered example, the rating of even two IGBTs is exceeded (S1 and S5).

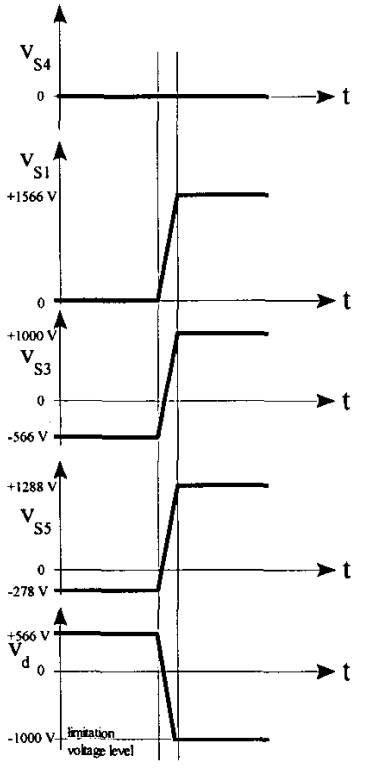

Fig. 6. Mains, switch and dc-link voltages of the line side power circuit

It is therefore inevitable to protect both half bridges individually from the dc link against overvoltages according to fig. 3.

The third limitation circuit across the dc link is not implicitly required. In fact in case 3) the dc link voltage may get twice as high as the limiting voltage of the half bridges, but this itself is not a problem. As the voltage across the

inductor could already be twice the rectified line-to-line voltage during normal operation, its isolation rating should be high enough to also withstand twice the limiting voltage. And the bridge IGBTs are protected by the limitation circuits of the half bridges.

The limitation of the dc link voltage v_d is only necessary to protect the freewheeling IGBT. This could be avoided by using a high voltage IGBT, but this seems to be out of all proportion compared to the use of a third MOSFET chain.

D. *Freewheeling path*

For freewheeling it is proposed to use devices (IGBT + series diode) with the same voltage rating as the main switches. The current rating can be much less, because the path is only conducting as long as the inductor current decays. The required time depends on the voltage drop across the freewheeling path, the initial dc link current and the inductance according to equation (7).

$$T_{fw,on} = \frac{L \cdot i_d}{v_{drop}} \tag{7}$$

In the example of the 22 kW CSI drive it takes about 100 ms until the inductor current becomes zero (a voltage drop of 12 V is assumed caused by two IGBTs and two series diodes in the freewheeling path).

Because the dc link voltage immediately drops after the freewheeling path is on, the trigger signal of the driver has to be latched at least until the inductor energy is dissipated.

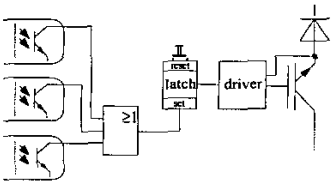

Fig. 7. Driving the freewheeling IGBT

Fig. 7 shows the signal path starting at the optocouplers of the limitation circuits. The trigger signals are connected in OR-logic to set a flipflop, which turns the driver on. The flipflop should be resettable only manually to improve fault immunity.

VI. EXPERIMENTAL VERIFICATION

To verify the protection circuit, it was built up in hardware and tested on a 22 kW laboratory CSI.

Fig. 8 shows a picture of the protection board for the line side converter.

The control logic (latch) and the optocouplers are powered by the same dc/dc converter, that also supplies the driver of the freewheeling IGBT. This voltage is buffered by a 2200µF/16V low voltage chemical capacitor (bottom left in the picture), which provides enough energy to power the circuit for more than 1 second. This ensures, that the freewheeling IGBT could be held on even if the power supply of the complete CSI fails (e.g. grid blackout).

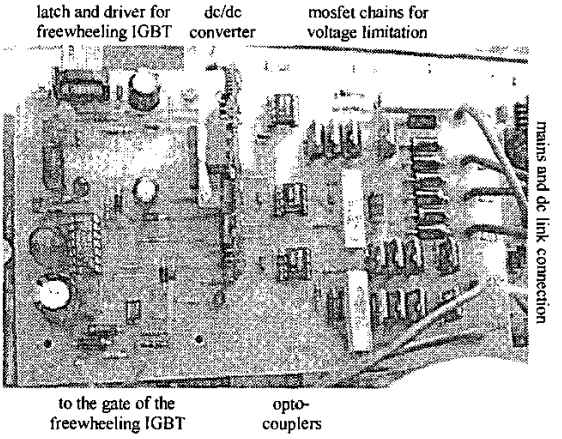

Fig. 8. Hardware of the dc link protection board

In fig. 9 the measurement results for a current interruption testcase are illustrated. For this the converter bridge was randomly pulsed off during operation at nominal current of 45 A. This represents case 3) in section V.C of this paper.

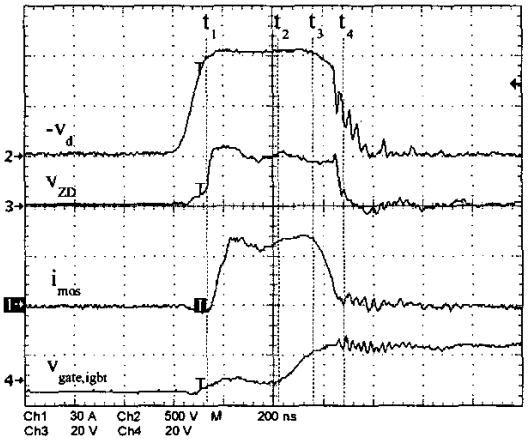

Fig. 9. Measurement result (total bridge pulse off)

The 8.3 kV/µs rise of the dc link voltage v_d is limited by the protection circuit at time t_1. The current commutates to the MOSFETs (i_{mos}) and the sender diode of the optocoupler gets power (zener-diode voltage drop v_{ZD}). After the propagation delay of optocoupler and driver (t_2-t_1), at t_2 the gate of the freewheeling IGBT is charged by the driver. At t_3 the IGBT starts conducting and as the forward voltage across the freewheeling IGBT is positive, the current immediately commutates from the MOSFETs to the IGBT. At t_4 this commutation has finished and the MOSFET limitation circuit becomes inactive.

It can be seen in fig. 9, that the MOSFET chain has to conduct the dc link current for less than 500 ns, what is well below the maximum clamping time, the used IRF640 MOSFETs can withstand. An estimation according to [5] using datasheets of some popular MOSFETs resulted in even smaller 200 V devices in TO-251AA or TO-252AA (SMT) packages being applicable in the 22 kW test CSI.

The measurement plots in fig. 10 show for the three possible failure cases (see section V.C) how the voltages are spread across the dc link and the half bridge limitation circuits. The failure cases are simulated by turning off the conducting IGBT in the top, the bottom or in both half bridges.

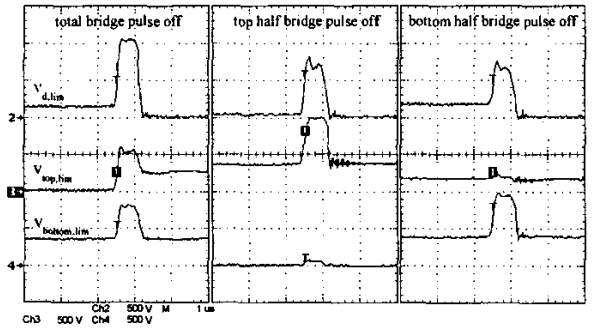

Fig. 10. Voltage distribution across the three limitation circuits

The figure on the left shows a total converter pulse off, where all switches are turned off simultaneously. The dc link voltage rise is here distributed to both, the top and the bottom half bridge, which causes none of their limitation circuits to become active. In this fault case, the limitation circuit across the dc link terminals limits the voltage.

In the mid figure only the conducting switch of the top half bridge is turned off (simulates an IGBT, diode or driver failure). As the IGBT in the bottom half bridge still conducts, the bottom dc link terminal is connected to one of the mains phases. The protection chain of the top half bridge therefore sees the rising dc link voltage superimposed to the rectified phase-to-phase voltage. This causes the voltage across the top protection circuit to be higher than the voltage across the dc link protection. The top limiting circuit is therefore activated.

Finally the figure on the right shows the turn off of the conducting switch in the bottom half bridge, which causes the bottom protection circuit to be issued.

VII. CONCLUSION

In this paper, the behaviour of a current source inverter equipped with IGBTs in the case of a current interruption in the dc link was analyzed. Based on this investigation, a novel strategy was presented for protecting the inverter against overvoltages caused by these interruptions.

In accordance to this strategy, a protection circuit was developed and built up in hardware. Its functionality was verified by measurements using testcases, that represent common failures, mainly the unintentional pulse off of one or more switches.

The devices required for this protection concept are quite small compared to the main inverter semiconductors and they are all commercially available at low prices. The protection circuit is completely independent from normal inverter operation, has no effect on the CSI behaviour and with appropriate power supply buffering (e.g. chemical capacitors) it provides protection even in the case of total grid blackout.

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