HYSTERETIC PULSE WIDTH MODULATION WITH INTERNALLY GENERATED CARRIER FOR A BOOST DC-DC CONVERTER

By

SONIYA NOORMUHAMED THEKKEVALAPPIL

A THESIS PRESENTED TO THE GRADUATE SCHOOL
OF THE UNIVERSITY OF FLORIDA IN PARTIAL FULFILLMENT
OF THE REQUIREMENTS FOR THE DEGREE OF
MASTER OF SCIENCE

UNIVERSITY OF FLORIDA

2005

Copyright 2005

by

Soniya Noormuhamed Thekkevalappil

This document is dedicated to my parents.

ACKNOWLEDGMENTS

I would like to express my gratitude towards my advisor, Dr. Khai D.T. Ngo, for his guidance and invaluable advice which were instrumental in this thesis work. I would like to thank Dr. William R. Eisenstadt and Dr. Haniph A. Latchman for their suggestions and for being on my thesis committee. I thank my parents and my friends for their support and encouragement towards the successful completion of this thesis.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

Abstract of Thesis Presented to the Graduate School
of the University of Florida in Partial Fulfillment of the
Requirements for the Degree of Master of Science

HYSTERETIC PULSE WIDTH MODULATION WITH INTERNALLY GENERATED CARRIER FOR A BOOST DC-DC CONVERTER

By

Soniya Noormuhamed Thekkevalappil

December 2005

Chair: Khai D. T. Ngo
Major Department: Electrical and Computer Engineering

The proposed control scheme falls under the self-oscillating analog modulator category. The control stage architecture for a boost converter consists of a band pass filter, a summer implicit in the filter architecture, and a hysteretic comparator. The voltage developed across the active switch (MOSFET) is integrated by the band pass filter to generate the carrier waveform. The carrier waveform is compared with two levels, generated using a summer and subtractor which receive the converter output voltage and hysteresis voltage as the inputs. The outputs of the comparators trigger a D flip-flop to yield the gating signal.

The main characteristics of the control approach which are advantageous in comparison to other schemes in use are as follows:

- Linearity: The control scheme achieves a linear relationship between the control variable and the converter output voltage.
- Direct control of output voltage: The output voltage of the converter varies in direct response to the control variable. The output voltage is in fact equal to the control variable in the absence of delays.

- Independent of converter input voltage: The control shows no dependency on the input voltage of the converter.

The boost dc-dc converter employing the control scheme was implemented on printed circuit board using Protel DXP. The test results obtained from the built circuit showed good consistency with theoretically predicted behavior. The limitation of the proposed control scheme is the restriction on the range of duty ratio of the converter, imposed by parasitics associated with non-ideal components. Consequently, the control variable has an acceptable range for which the control scheme functions. The delays imposed by comparators introduce control dependency on input voltage of the converter. Future work can focus on analysis of the control scheme in terms of transient analysis using a dynamically controlled load and frequency response in terms of gain and phase margins.

CHAPTER 1
INTRODUCTION

The aim of the chapter is to provide an introduction to the working of dc-dc converters and the need for the new control scheme outlined in this thesis. The chapter is organized as follows:

- General working of a power converter
- DC-DC converter: Description of power and control stage; motivation for new method.
- Thesis organization.

1.1. Power Converter

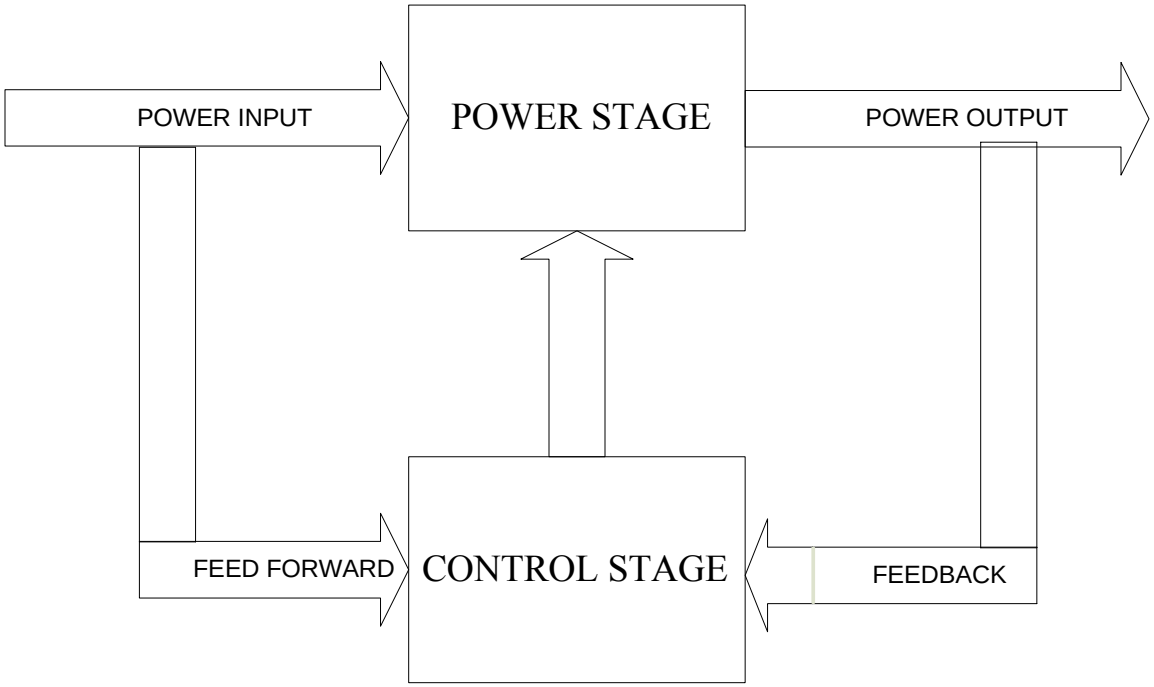

Figure 1-1 A power converter.

The field of power electronics deals with the processing of electric power using electronic devices. A power converter has a power stage and a control stage, as shown in

Figure 1-1. The power stage comprises the semiconductor switches and energy storage components. The power section converts the unregulated power at its input to regulated power at the load .The controller section is concerned with providing control signals to the power stage. This section can be implemented in analog or digital form.

A major concern in any power processing application is the efficiency. It is generally desired to construct high efficiency converters simply because realization of low efficiency converters is impractical. The power dissipated in a circuit is the difference between the input power and the power at the output. The power lost is dissipated in the form of heat, necessitating the presence of efficient cooling systems. A converter technology with very high efficiency will have low power loss. In realizing an efficient power processing system, semiconductor devices operating in switched mode, as well as capacitors and magnetic devices constitute the integral part. The power consumption by these components is zero ideally.

1.2. DC-DC Converter

A dc-dc converter converts a dc input voltage to a dc output voltage of different magnitude, possibly with opposite polarity. In general, any given voltage can be converted to any desired output voltage, using a converter containing switched devices embedded within a network of reactive elements. Depending on the way in which voltage is altered, there are different configurations of converters [1].

- Boost- Output voltage is of higher magnitude than the input.
- Buck- Output voltage is of lower magnitude than the input.
- Buck-Boost- Output voltage can be of either lower or higher magnitude than the input.
- Cuk- Functions similar to buck-boost and inverts the polarity.

1.2.1. Power Section

The power stage basically consists of switched-mode semiconductor devices that are turned on and off periodically by waveforms from the control stage. A low pass filter comprising of an inductor and a capacitor, with corner frequency considerably lower than the switching frequency is employed. This removes the undesirable harmonics in the output. The duty cycle D of the switching waveform defines the fraction of time that the switch remains on. In an ideal converter, the output voltage is a function of the duty cycle and the input voltage alone. In a practical scenario, the parasitic resistances such as the inductor resistance, equivalent series resistance of the capacitor and on resistance of the switching devices factor into the expression for output voltage.

1.2.2. Control Section

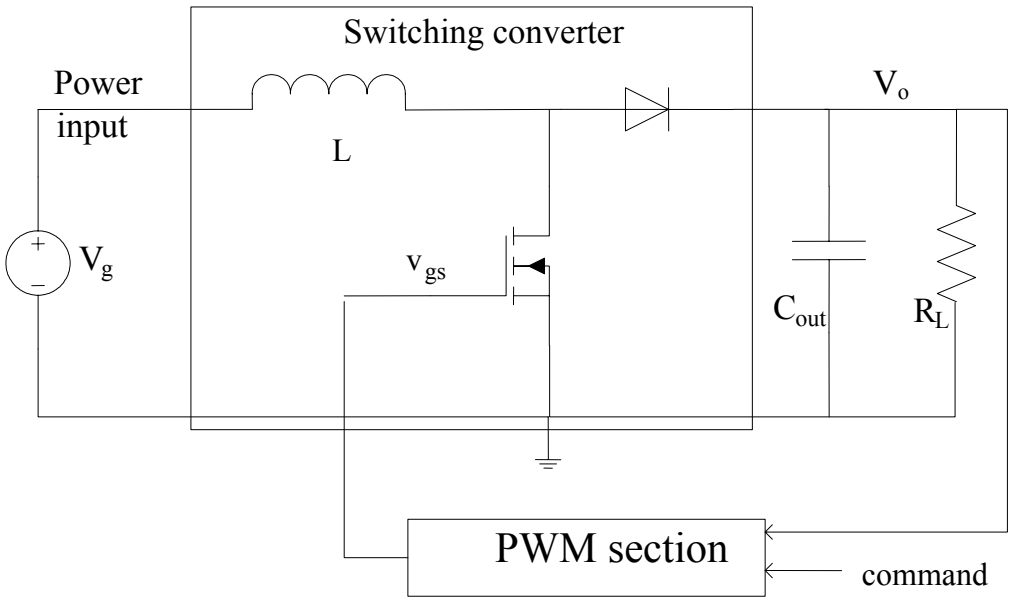

Figure 1-2 Boost DC-DC converter.

The control section of a converter deals with generation of switching signals for the semiconductor devices in the power section. The output voltage of the converter can be varied by modulating the pulse width of the switching signal. A control system which can

force the output voltage to follow a particular "command" by variation of the duty cycle is called Pulse Width Modulation (PWM). Various PWM techniques that are widely in use are explained in detail in Chapter 2.

A boost converter circuit is shown in Figure 1-2. When the MOSFET is switched on by the gating signal, the inductor is provided with a charging path through the MOSFET. The inductor transfers the stored energy to the load in the off cycle of the switching waveform.

The relationship between the output and input in this converter is

$$\frac{V_o}{V_g} = \frac{1}{1-D} \tag{1.1}$$

where D is the duty ratio of vgs and specifies the on time of the active switch.

1.2.3. Motivation for New Method

The methods employed for converter control falls under constant or variable frequency. In the conventional voltage mode constant frequency control, the output voltage and control variable shares a non-linear relationship. Linearity between control and output is a desirable trait especially in applications like switched audio power amplifiers. A linear system also lends itself better to stabilization. Current mode controls usually make use of the inductor current as the carrier waveform. Current sensing is difficult due to issues of power dissipation and inaccuracy [2]. Variable frequency controllers have also been known to use output voltage ripple as the carrier. This method is disadvantageous due to the poor quality of ripple attributed to the presence of equivalent series resistance of the output capacitor. The focus of the thesis is on the design and implementation of a control system that makes use of the information provided by the power section of the dc-dc converter for direct linear control of the

output voltage. The control system described would utilize the voltage across the active switch of the boost converter to generate the carrier signal for PWM. The control variable is added to the carrier waveform and compared with the output voltage of the converter in a hysteretic comparator. The carrier waveform is thus virtually bonded to the output voltage via the comparator.

1.3. Thesis organization

The thesis is structured as follows:

- Chapter 2 describes the different Pulse Width Modulation techniques and highlights the advantages and disadvantages associated with each.
- Chapter 3 focuses on the hysteretic PWM architecture. It explains the working of major blocks.
- Chapter 4 deals with design oriented modeling. The design of the hysteretic modulator is covered in this section.
- Chapter 5 presents experimental verification of the built circuit. It makes a comparative study of the experimental results with theory.

CHAPTER 2
PULSE WIDTH MODULATION

The structuring of the chapter is as follows:

- Introduction: A brief introduction to PWM control.
- Constant-frequency: Voltage-mode constant-frequency control is explained.
- Variable-frequency: Constant off-time, constant on-time and hysteretic control are described.

Switch mode controllers are favored in applications like audio power amplifiers, inverters and motors due to their high efficiency and low system design cost. The active components in a switching converter are controlled by PWM signals applied to their gates. The duration for which the switches remain on is determined by the duty cycle of the PWM signals, which in turn controls the energy delivered to the load. The major share of the energy received by the load will be a function of the modulation only if the switching frequency is ensured to be much higher than the modulating signal frequency. The major points of comparison between various modulation schemes are switching losses, power supply utilization, control linearity and harmonic content in the output. Highest performance is achieved with self-oscillating analog modulators, which makes use of no external carrier signal. Self-oscillating modulators [3] are a closed loop circuit with gain and phase characteristics that ensure a closed loop oscillation. First-order self-oscillating modulators are characterized by an open loop gain function as an integrator, which by itself results in a phase shift of -90°. The phase response is modified by introducing a time delay, which is equal to a linear phase shift. The oscillation starts automatically when the additional phase contribution approaches -90°. Standard PWM

modulators have achievable open loop bandwidth in the range of $f_s/10$ or f_s/π, where f_s is the switching frequency. In certain applications, this requires a very high switching frequency to provide enough control loop bandwidth for desired dynamic performance. Self oscillating modulators have open loop bandwidth of the order of f_s which makes it an ideal choice for applications requiring excellent dynamic capabilities.

2.1. Fixed-Frequency Method

Voltage-mode PWM. Constant-frequency modulators [4] are commonly implemented by the comparison of a control command with a carrier waveform, usually triangular or saw tooth in shape and of fixed frequency. The most common implementation of a constant-frequency modulator and corresponding waveforms are shown in Figure 2-1.The comparator output alters states when the carrier v_{car} (t) crosses the command value r (t), resulting in a square waveform.

The duty ratio D in a switching cycle is defined as the fraction of the switching time interval T_s when the square wave stays at logic high state. Let the carrier waveform vary from $V_{car\text{-}min}$ to $V_{car\text{-}max}$, then the duty cycle D can be estimated to be as follows:

$$D = \frac{\left(r(t) - V_{car-\min}\right)}{\left(V_{car-\max} - V_{car-\min}\right)} \tag{2.1}$$

The duty cycle is dependent on the input voltages to the comparator and the output voltage can be controlled using these voltages. In most applications, the command voltage alone serves as the control. The modulation of the carrier waveform allows the addition of more control dimensions to the modulator. The conventional PWM produces a linear relationship between the duty ratio and control signal. The voltage gain of an ideal boost converter is inversely dependent on the duty cycle and hence the output voltage is a nonlinear function of the control variable.

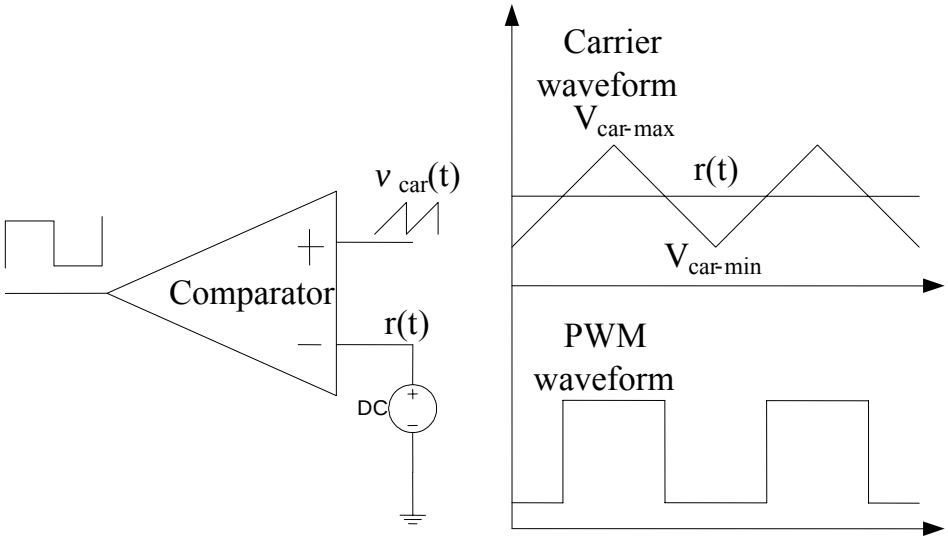

Figure 2-1 Constant-frequency PWM.

2.2. Variable-Frequency Methods

Variable frequency controls allow determination of the duty ratio, provided the switching period is known [5-7]. Constant on-time and constant off –time modulators can offer advantages in terms of low audio susceptibility, ease of implementation or lower power stage weight. Hysteretic control is favored due to its high linearity and simple design.

2.2.1. Constant Off-Time Control

The control here maintains a constant off-time whereas the on-time is determined at the beginning of each switching cycle [8]. Figure 2-2 displays the control scheme and associated waveforms. The modulator output is set high at the beginning of a switching cycle. During the on-time period, a carrier signal v_{car} (t) is compared with the command signal r (t) and the output is set low when the carrier signal reaches the command. The falling edge of the output waveform triggers a mono-stable multi-vibrator which ensures that the modulator output is kept low for a fixed time period. The falling edge of the mono-stable pulse initiates a new switching cycle.

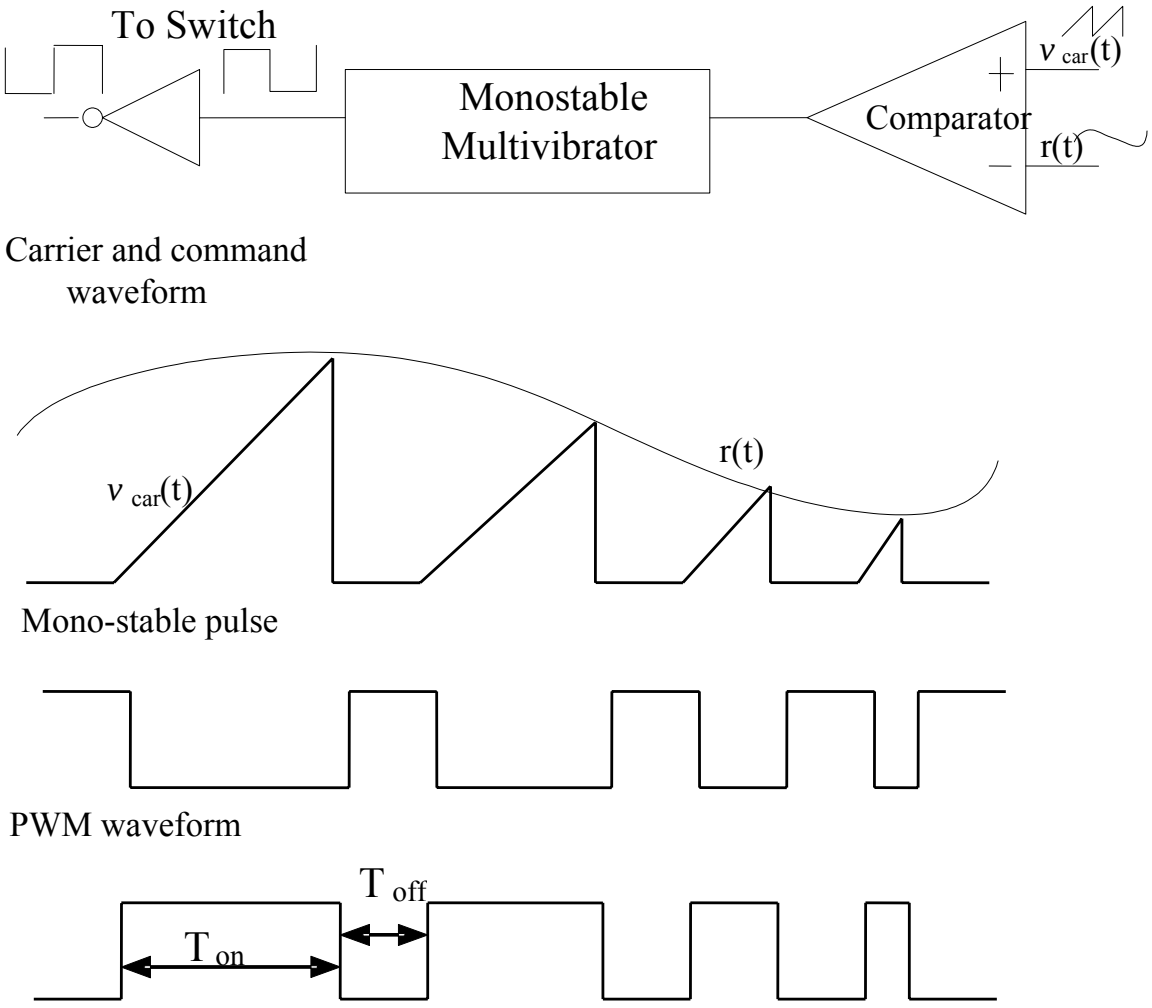

Figure 2-2 Constant off-time PWM.

2.2.2 Constant On-Time Control

In the case of constant on-time control [9], the duration for which the switching device remains on is fixed while the off-time is determined at the end of the switching cycle. The implementation of the method as well as the waveforms is shown in Figure 2-3. The switching is controlled by the mono-stable multi-vibrator output. The comparator compares the integrated difference between the switched variable and the control command. With the switch turned on by the one shot timer pulse, the integrated value increases from an initial zero value. The switch is turned off when the mono-stable multi-

vibrator changes state after a fixed duration. When the switch is off, the integrated value falls to zero, which causes the comparator to changes state, triggering the multi-vibrator, and a new cycle is initiated. The duty ratio for a constant on-time modulator would be determined at the end of the switching cycle. The waveforms for constant on-time case would be the dual of the constant off-time such that the command r (t) modulates the off time of the PWM signal. The on-time of the signal remains fixed as the duration of the multi-vibrator pulse.

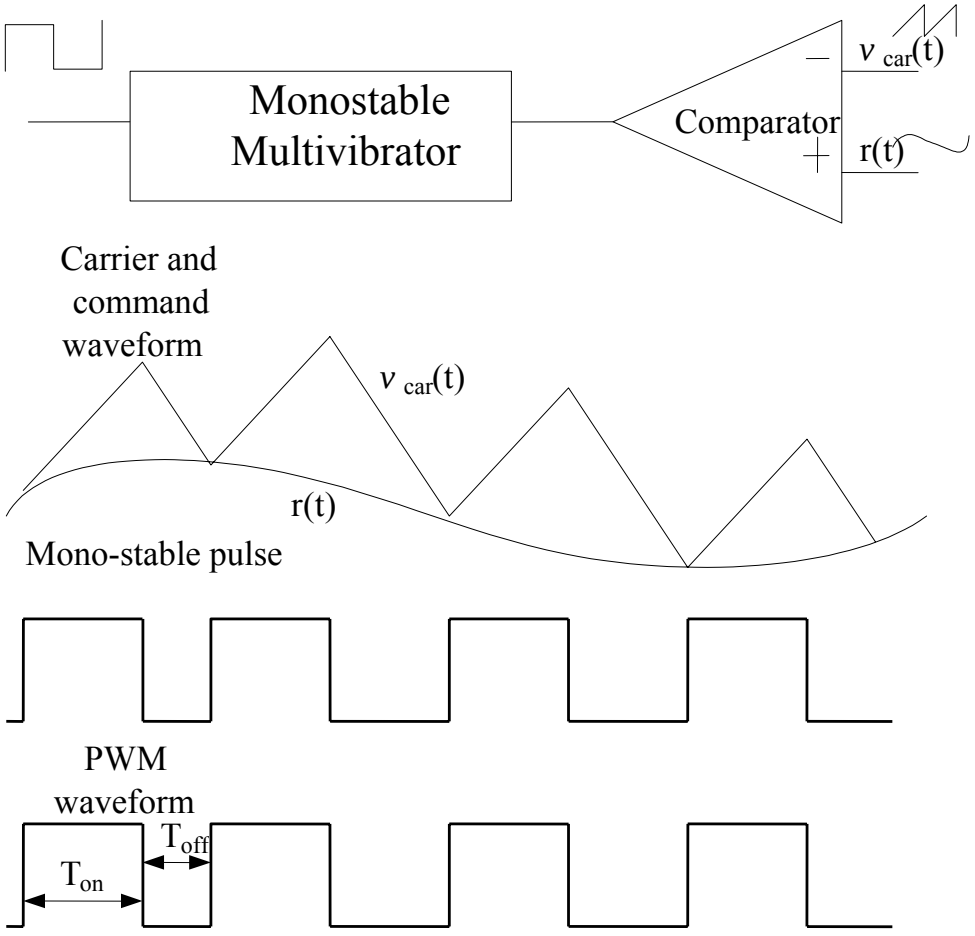

Figure 2-3 Constant on-time PWM.

2.2.2. Hysteretic Control

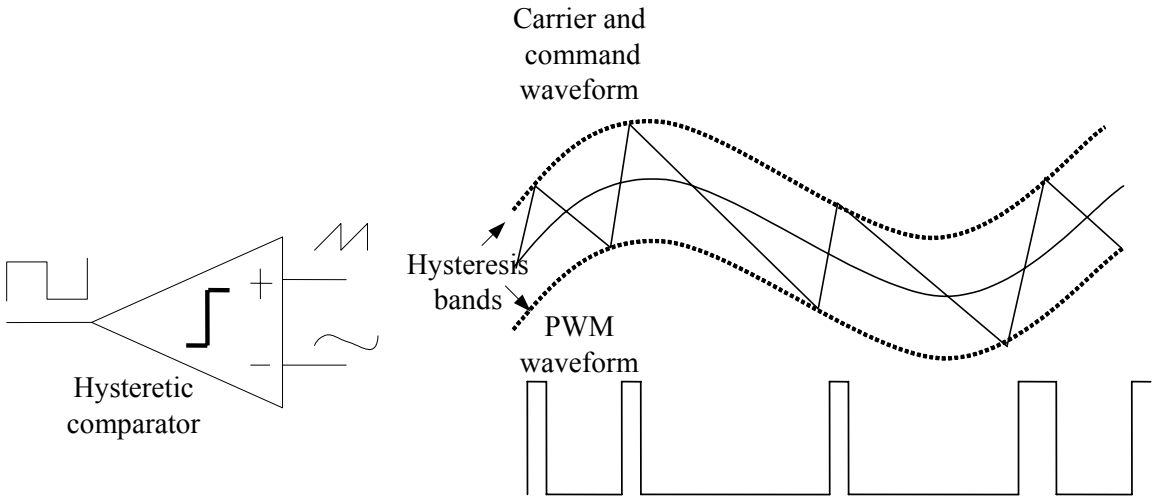

Figure 2-4 Hysteretic PWM.

Hysteretic PWM refers to a technique wherein the output is allowed to oscillate within a predefined error band called hysteresis bands [10-11]. Figure 2-4 shows the control scheme. The bands determine the instants at which the comparator output switches high or low. Whenever the triangular wave reaches either of the hysteresis bands, the comparator output switches states. Thus the duty cycle of the switching waveform is a function of the hysteresis.

The main advantage of this control scheme is its ability to respond rapidly to load and line transients. Another benefit is the linear modulation caused by the saw tooth shaped carrier waveform with ideally straight slopes, and by the infinite power supply rejection ratio, provided the supply variations are slow compared to the switching frequency. Power supply variations at high frequencies result in sum and difference products of the power supply variation and the command signal. But the operating frequency of a hysteretic regulator is a function of variables such as capacitor equivalent

series resistance, output filter inductance etc. Due to variable frequency, the switching losses can be higher compared to other techniques.

CHAPTER 3
HYSTERETIC PULSE WIDTH MODULATION WITH CONVERTER-DERIVED CARRIER

The chapter focuses on the architecture and working of the hysteretic control scheme employing internally generated carrier for a boost converter. The structuring of the chapter is as follows:

- General approach: This section describes the general architecture of the control scheme utilizing waveforms produced by the converter.
- Carrier generation from MOSFET voltage: The focus is on the control scheme implemented specifically for a boost dc-dc converter making use of the voltage generated across the active switch. The architecture of the control scheme as well as that of the constituent blocks is described.

3.1. General Approach

Pulse-width modulators employing converter current or voltage ripple as the carrier signal have been known to be advantageous in terms of simplicity, robustness, linearity, and speed. However, despite these advantages only a handful of converter-derived carrier signals have been used. The inductor current is the most popular choice for carrier signal [12-14] since it takes advantage of the significant amount of ripple in the inductor current, but is inconvenient to use since current sensing is required. The output voltage ripple has also been used [15], but is much less popular since the quality of the ripple on the output voltage is often marginal for the pulse-width modulation operation.

Triangular signals are generated from virtually any AC converter waveforms, and are bonded to virtually any variable that needs to be controlled to bring the benefits offered by the current mode controllers to those controlled variables carrying

insignificant ripple, such as the output voltage in low-voltage voltage-regulator modules (VRM).

A typical CDC-HPWM architecture comprises of a filter, an algebraic summer and a hysteretic comparator [16]. The input to the filter could be functions of the voltages or currents of converter components. The filter could contain low pass or allpass blocks, depending on whether the converter waveform is square or triangular, as well as algebraic operators. The filter output contains not only a triangular component, but also low frequency information useful for shaping the converter's frequency response. The summer that bonds the filter output to a controlled variable can often be realized implicitly in the filter or the comparator. The carrier signal thus generated is compared with two hysteretic thresholds to determine the commutation instants. Since the controlled variable is fed to the comparator without any delay, the converter switches are responsive to the transients in the controlled variable.

3.2. Carrier Generation from MOSFET Voltage

The control circuitry for a boost converter with internally generated carrier consists of a bandpass filter, a summer implicit in the filter architecture, and a hysteretic comparator. The complete architecture is displayed in Figure 3-1. The voltage v_{in} developed across the active switch (MOSFET) serves as the filter input and the converter output voltage V_o is the controlled variable. An external constant-valued voltage v_{cmd} added to the triangular carrier is used to control V_o. Since the triangular waveform generated across the parallel RC combination is out of phase with the output voltage, the carrier wave is fed to the positive input and the output voltage to the negative terminal of the comparator.

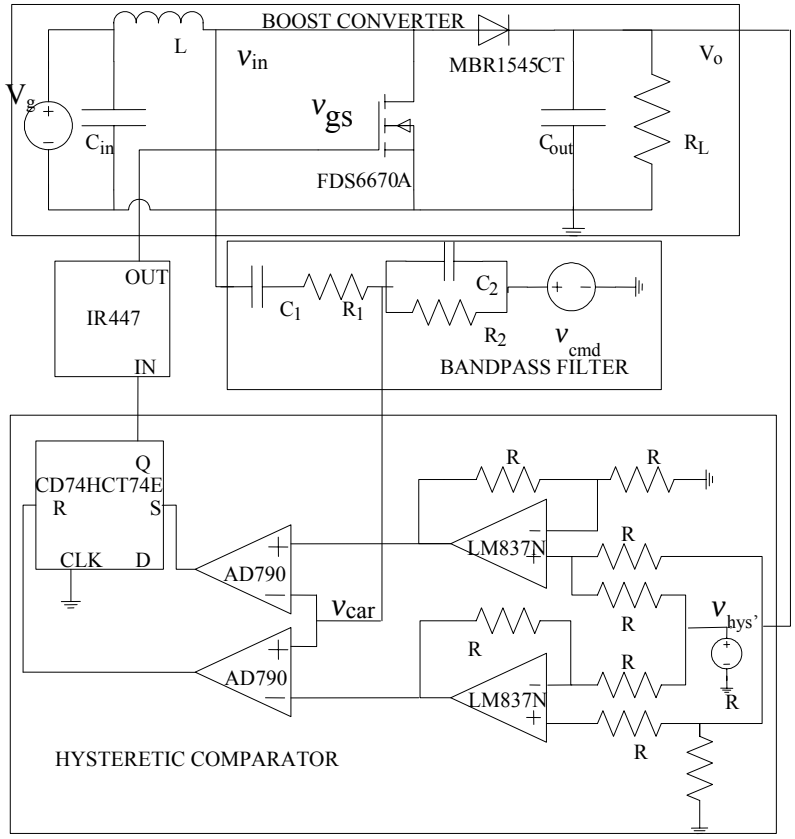

Figure 3-1 Boost converter with carrier generated from MOSFET voltage.

3.2.1. Bandpass Filter

The bandpass filter, as shown in Figure 3-2, is a combination of a low pass filter formed by parallel combination of the resistors R_1, R_2 and the parallel capacitor C_2, and a high pass filter formed by the series combination of the capacitor C_1 and the resistors. A constant-valued voltage v_{cmd} applied on to the parallel RC combination is the control variable. Here, the summer component is implicit in the filter architecture. The triangular carrier waveform is developed across the parallel RC combination and feeds into the positive input of the hysteretic comparator. In an ideal scenario, v_{cmd} is equal to V_o and the control system has no dependency on the converter input voltage V_g. The delays introduced by comparators and flip-flop causes the control to show dependency on V_g.

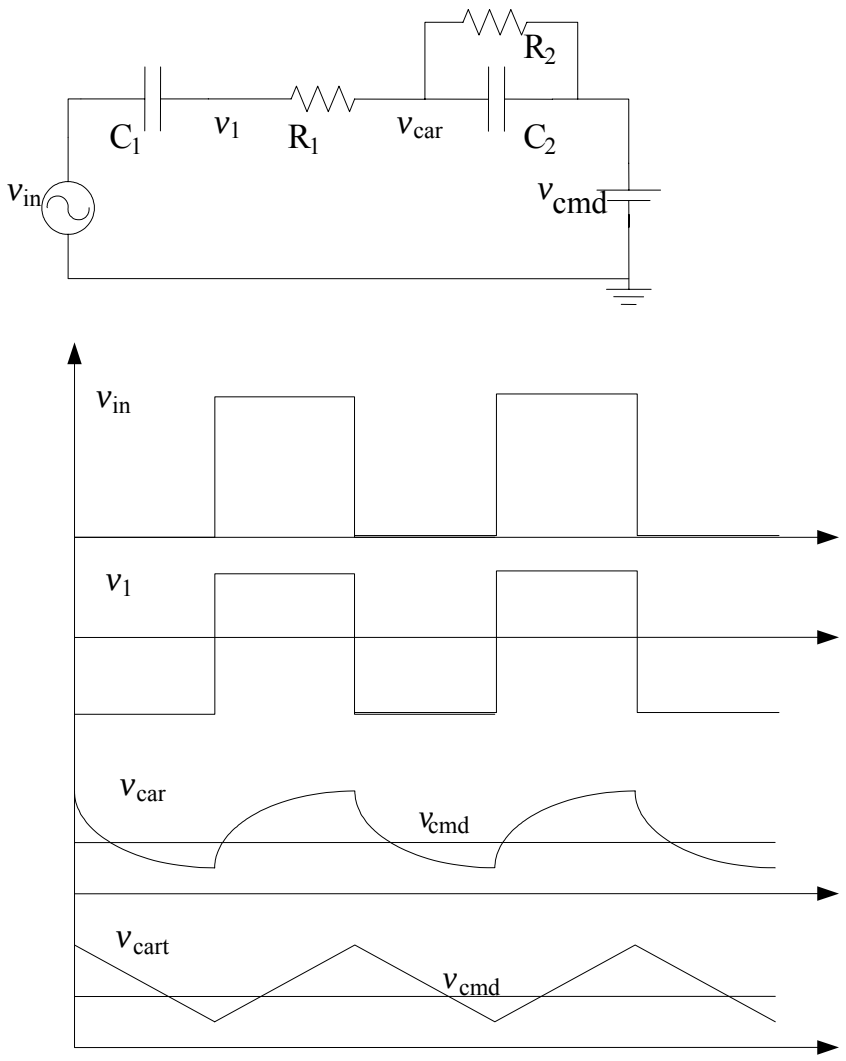

Figure 3-2 Bandpass filter and associated waveforms.

The accurate design of the dc-blocking capacitor C_1 ensures that the high pass filter cutoff frequency is high enough to eliminate the average component in the input signal v_{in}. The low pass filter acts on the waveform v_1 which is devoid of any average component. The time constant of the low pass filter in comparison to the time period of the input square wave determines the shape of the carrier waveform. A too low time constant causes the carrier to be exponential in nature as in v_{car}, while a higher value generates a triangular waveform like v_{cart}. For ideal integration, the time constant of the filter should be very high in comparison to the time period of the square wave input. The

summation of v_{cmd} to the low pass filter output causes the generated carrier to have an average value equal to the control voltage.

3.2.2. Hysteretic Comparator

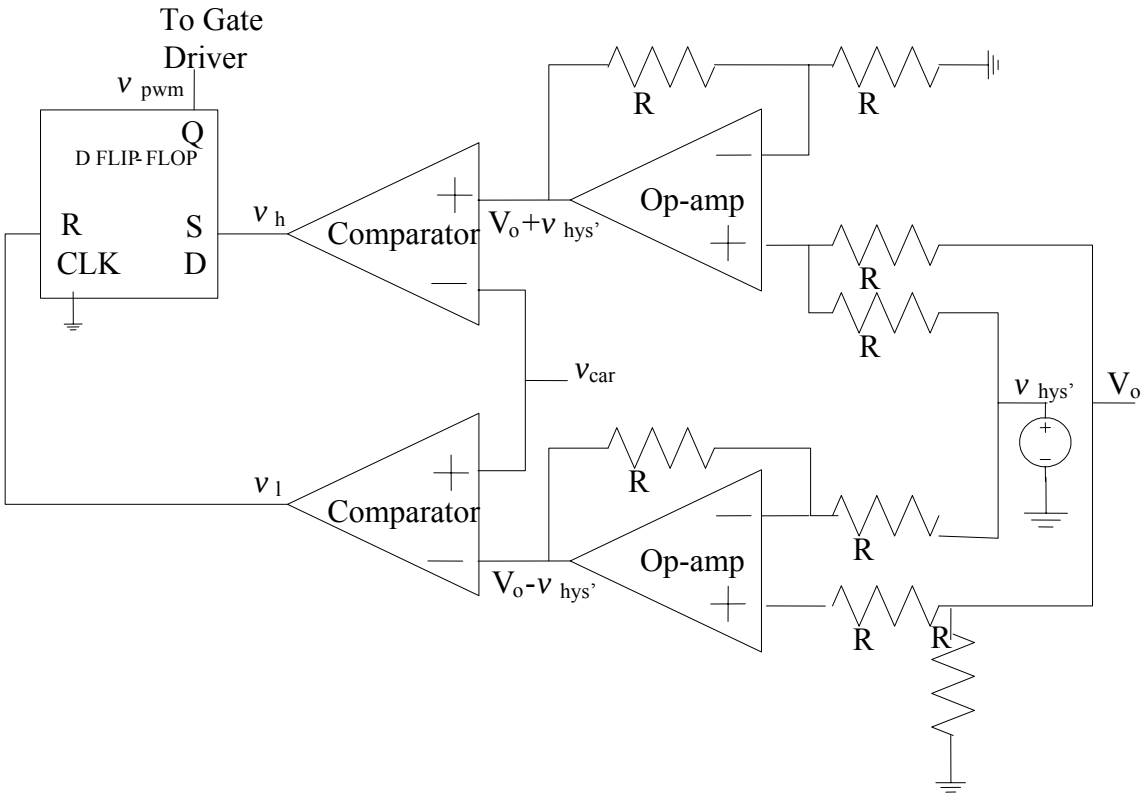

Figure 3-3 Hysteretic comparator.

The hysteretic comparator architecture, as seen in Figure 3-3, comprises of operational amplifier, comparator and D flip-flop with set and reset options. As opposed to the conventional hysteretic comparator which utilizes regenerative feedback, hysteresis is implemented by processing the output of two comparators operating in open loop mode via a flip-flop [15]. The threshold levels can be independently set and fine tuned, which allows convenient monitoring of switching frequency variation. Commutation instants occur in a hysteretic comparator whenever the input signal levels exceed the high and low hysteretic levels. Figure 3-4 shows the waveforms at various stages of the comparator.

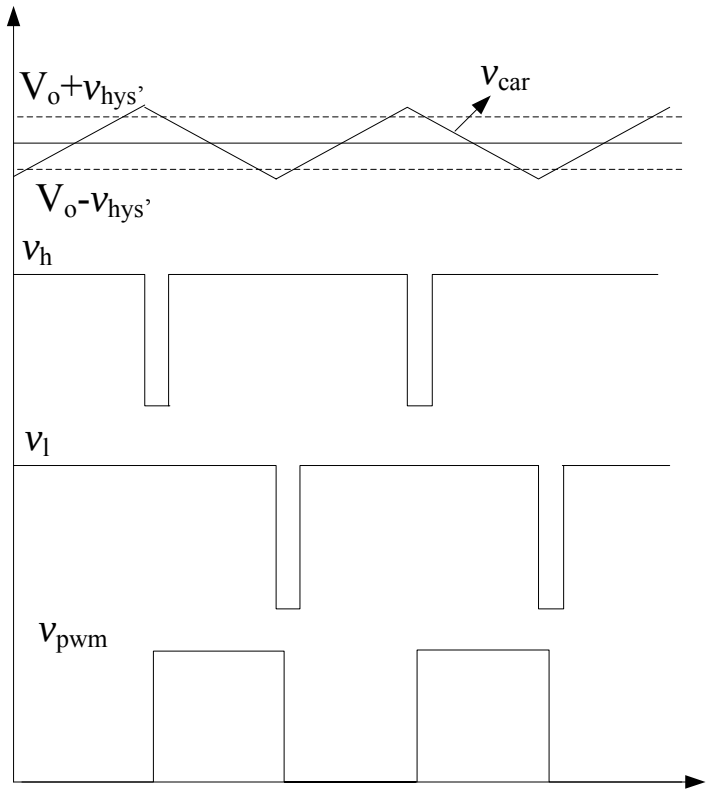

Figure 3-4 Outputs of blocks constituting hysteretic comparator.

The upper level ($V_o+v_{hys'}$) is generated by adding the converter output voltage and the hysteresis voltage $v_{hys'}$in an operational amplifier summer, and the lower level (V_o-$v_{hys'}$) by subtracting the same in an operational amplifier subtractor. The upper comparator switches when the carrier waveform value exceeds the high level, whereas the lower comparator alters state when the carrier goes below the low level. An edge triggered D flip-flop is set and reset in response to the comparator outputs, v_h and v_l, to yield the PWM waveform. In an ideal scenario, where in the comparators and flip-flop do not introduce any delays, the switching is instantaneous.

The switching frequency is a function of the hysteresis voltage; the bandpass filter components, the duty cycle as well as amplitude of the voltage across the MOSFET. In a non ideal case, delays and parasitic components also affect the switching frequency.

CHAPTER 4
DESIGN ORIENTED MODELLING

The design process for the pulse-width modulator with internally generated carrier is covered in this chapter. The main stages of the control scheme are the bandpass filter and the hysteretic comparator. The chapter is structured as follows:

- Transfer function of the bandpass filter: The design of the filter requires knowledge of the corner frequencies, centre frequency and mid-band gain expressed in terms of the component values. The transfer function derivation aids in achieving this objective.

- Switching frequency: The switching frequency of the converter is derived as a function of the filter parameters as well as the delays and the duty ratio of the gating signal. This section is instrumental in providing an idea on the acceptable values of the filter time-constants, applied hysteresis and converter parameters for a specified switching frequency.

- Design criteria: The actual design procedure is detailed here. The information gathered in the previous sections is effectively utilized in the methodology outlined in this section.

- Bandpass filter parameter variations: The aim of this section is to provide an insight on the effect of variation of filter component values on the frequency response as well as transient response of the filter.

The circuit specifications are detailed in Table 4-1.

Table 4-1 Design specifications

Parameters	Value
V_o	5V
V_{in}	3+-10%V
P_o	10W
f_s	500kHz
Efficiency, η	80%
Duty Ratio, D	0.34-0.46
I_o	2A
Ripple	1% of V_o

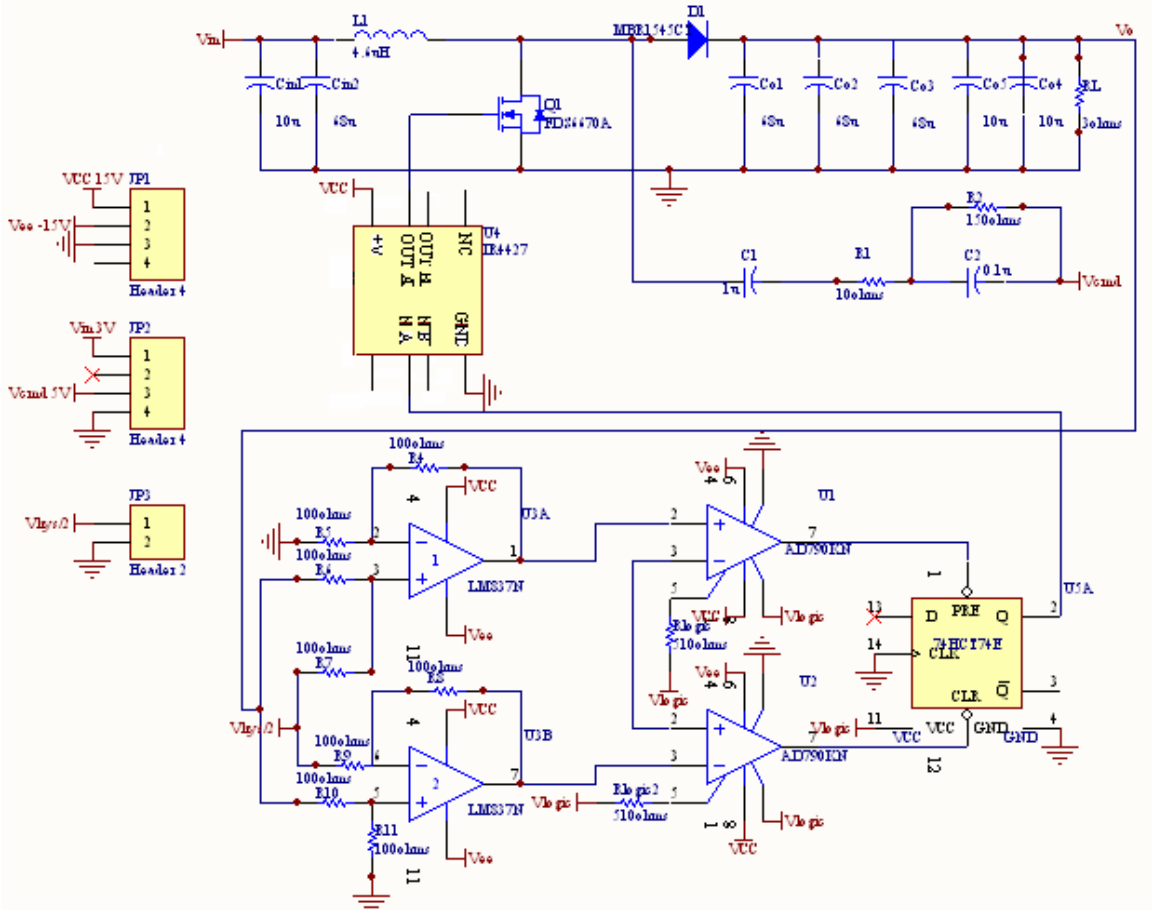

Figure 4-1 Protel schematic.

4.1. Transfer Function of Bandpass Filter

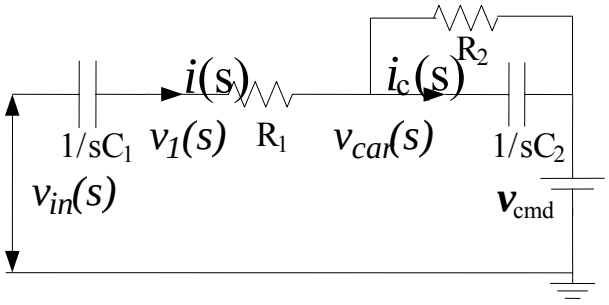

Figure 4-2 Bandpass filter in Laplace domain.

The bandpass filter schematic is shown in Figure 4-2. Let $v_{in}(s)$ and $v_{car}(s)$ be defined as the input and output voltages, respectively. The voltage after the dc

elimination capacitor C_1 is $v_1(s)$. Let *i(s)* be the total current flowing into the filter, and $i_c(s)$ be the current that flows through C_2.

The total input current can be expressed in terms of the voltage that appears across the series combination of capacitor C1 and resistor R1, and their impedance

$$i(s) = \frac{\left(v_{in}(s) - v_{car}(s)\right)}{R_1 + \frac{1}{sC_1}} \tag{4.1}$$

The current drawn by the capacitor C_2 can be expressed as a fraction of the total input current as indicated below:

$$i_c(s) = \frac{i(s)R_2}{R_2 + \frac{1}{sC_2}} \tag{4.2}$$

The output voltage vcar(s) is the product of the current through the capacitor C2 and the impedance. Inserting equations (4.1) and (4.2) results in the following:

$$\begin{aligned} v_{car}(s) &= i_c(s)\left(\frac{1}{sC_2}\right) \\ &= \left(v_{in}(s) - v_{car}(s)\right)\frac{\left(\frac{R_2}{sC_2}\right)}{\left(R_2 + \frac{1}{sC_2}\right)\left(R_1 + \frac{1}{sC_1}\right)} \end{aligned} \tag{4.3}$$

The above eqauation (4.3) can be rearranged to obtain a relation between the input $v_{in}(s)$ of the filter and its output $v_{car}(s)$ as shown below:

$$\frac{v_{car}(s)}{v_{in}(s)} = \frac{\left(\frac{R_2}{sC_2}\right)}{\left(R_2 + \frac{1}{sC_2}\right)\left(R_1 + \frac{1}{sC_1}\right) + \left(\frac{R_2}{sC_2}\right)} \tag{4.4}$$

The transfer function for the filter is the ratio of $v_{car}(s)$ over $v_{in}(s)$

$$\begin{aligned} H_c(s) &= \frac{v_{car}(s)}{v_{in}(s)} \\ &= \frac{R_2}{(R_1+R_2)} \frac{1}{\left[1+\frac{C_2}{C_1}\frac{R_2}{(R_1+R_2)}+\frac{1}{sC_1(R_1+R_2)}+sC_2\frac{R_1R_2}{(R_1+R_2)}\right]} \\ &= \frac{C_1R_2}{\left[C_1(R_1+R_2)+C_2R_2\right]} \frac{1}{\left\{1+\frac{1}{s\left[C_1(R_1+R_2)+C_2R_2\right]}+s\frac{C_1C_2R_1R_2}{\left[C_1(R_1+R_2)+C_2R_2\right]}\right\}} \\ &= A_m \frac{1}{1+\frac{\omega_L}{s}+\frac{s}{\omega_H}} \end{aligned} \tag{4.5}$$

The frequency response parameters can be extracted from the transfer function.

The low and high corners of the filter are obtained as

$$\omega_L = \frac{1}{C_1(R_1+R_2)+C_2R_2} \tag{4.6}$$

$$\omega_H = \frac{C_1(R_1+R_2)+C_2R_2}{C_1C_2R_1R_2} \tag{4.7}$$

The mid band gain is defined as

$$A_m = \frac{C_1R_2}{C_1(R_1+R_2)+C_2R_2} \tag{4.8}$$

The 3db corners of a bandpass filter are related to the centre frequency as

$$\omega_o = \sqrt{\omega_L\omega_H} \tag{4.9}$$

Equations (4.6) and (4.7) can be substituted in equation (4.9 to yield the centre frequency of the filter as

$$\omega_o = \frac{1}{\sqrt{C_1C_2R_1R_2}} \tag{4.10}$$

The term $\left[1+\frac{C_2}{C_1}\frac{R_2}{(R_1+R_2)}\right]$ is a deciding factor in the design equations. If the part involving the filter components becomes negligible, then the transfer function reduces to a much simpler format. The term becomes negligible if and only if the following conditions are satisfied:

$$C_2 \ll C_1$$
$$R_2 \gg R_1 \tag{4.11}$$

These conditions ensure that the interaction between the highpass and lowpass blocks is negligible. The bandpass filter transfer function can then be expressed as the product of individual lowpass and highpass sections, with the term specifying the interaction eliminated. The simplified expression is as follows:

$$\begin{aligned} H_{cs}(s) &= H_{HPF} * H_{LPF} \\ &= \left[\frac{1}{1+\frac{1}{sC_1(R_1+R_2)}}\right] * \left[\frac{1}{1+sC_2R_1 \mathrm{P} R_2}\right] \\ &= \frac{R_2}{(R_1+R_2)} \frac{1}{1+\frac{1}{sC_1(R_1+R_2)}+sC_2\frac{R_1R_2}{(R_1+R_2)}} \\ &= A_{ms}\frac{1}{1+\frac{\omega_{Ls}}{s}+\frac{s}{\omega_{Hs}}} \end{aligned} \tag{4.12}$$

The simplified frequency response parameters are detailed below.

The low corner of the filter is approximated as

$$\omega_{Ls} = \frac{1}{C_1(R_1+R_2)} \tag{4.13}$$

The high corner of the filter is simplified as

$$\omega_H = \frac{1}{C_2 (R_1 \| R_2)} \tag{4.14}$$

The simplified mid-band gain becomes a function of resistors only as seen below:

$$A_{ms} = \frac{R_2}{R_1 + R_2} \tag{4.15}$$

The centre frequency retains the same relationship to the low and high corners as before.

4.2. Switching Frequency

The switching frequency of the converter is derived as a function of the filter parameters, the converter parameters and the delay components. Figure 4-3 shows one cycle of the carrier waveform v_{car}, with peaks and valleys highlighted; in the presence as well as absence of delays. The ideal case waveform was confined between v_{car+} and v_{car-}, and the delays $t_1$and t_1' introduce new peak v_{car++} and valley v_{car--}.The effect of the delays is to increase the hysteresis from v_{hys} to an effective hysteresis value v_{hyse} and the average value of the carrier waveform from v_{cmd} to v_{cmde}.

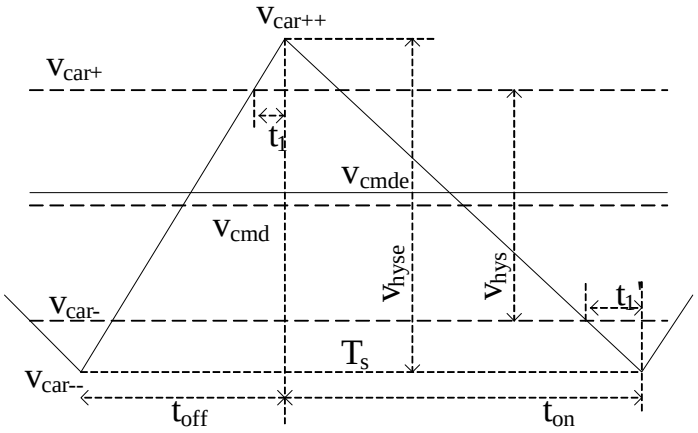

Figure 4-3 Carrier waveform with delays.

The new average and hysteresis values of the carrier waveform can be expressed in terms of the new edges of the carrier waveform, as follows:

The new average and hysteresis values of the carrier waveform can be expressed in terms of the new edges of the carrier waveform, as follows:

$$v_{cmde} = \frac{v_{car++} + v_{car--}}{2} \tag{4.16}$$

$$v_{hyse} = v_{car++} - v_{car--} \tag{4.17}$$

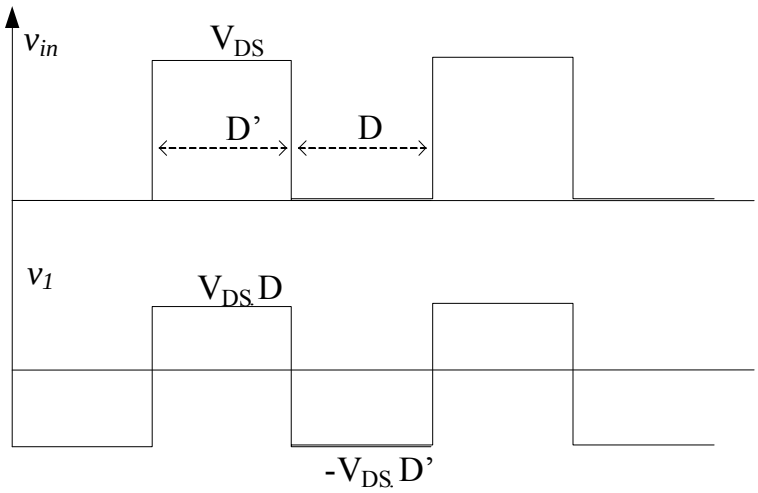

Figure 4-4 Input to bandpass filter, v_{in} and output after dc elimination, v_1.

The input to the filter is the voltage across the MOSFET. The voltage across the MOSFET v_{in}, as well as the intermediate voltage v_1 after the dc blocking capacitor C_1, is shown in Figure 4-4. When the transistor is off, the sum of output voltage V_o and the diode forward voltage drop V_f appears across it. The MOSFET is connected to ground potential when it is turned on. As seen in Figure 4-4, the voltage is V_{DS} during D' (off) and zero in D (on) stage.

$$V_{DS} = V_o + V_f \tag{4.18}$$

The average of the input waveform v_{in} can be determined as

$$\begin{aligned} \langle v_{in} \rangle &= \frac{1}{T_s}\int v_{in}.dt = \frac{1}{T_s}\left(V_{DS} * D'T_s\right) \\ &= V_{DS} * D' \end{aligned} \tag{4.19}$$

The blocking capacitor C_1 removes the average component in the square wave input to yield the voltage v_1. The voltage v_1 is expressed as

$$\begin{aligned} v_1 &= v_{in} - \langle v_{in} \rangle \\ &= v_{in} - \left(V_{DS} * D' \right) \\ &= V_{DS} * D \left\{ 0 \le t \le D'T_s \right\} \\ &= -V_{DS} * D' \left\{ D'T_s < t \le DT_s \right\} \end{aligned} \tag{4.20}$$

The carrier waveform v_{car} is formed by charging and discharging of the capacitor C_2 through resistance R_1, to the voltage levels defined by waveform v_1. The summer implicit in the filter architecture adds the control voltage v_{cmd} to the voltage developed across C_2. The expression for the exponential carrier is

$$v_{car} = v_1 \left(1 - \in^{\frac{-t}{R_1 C_2}} \right) + v_{cmd} \tag{4.21}$$

For perfect integrator operation, the carrier waveform is triangular as indicated below:

$$v_{cart} = v_1 \frac{t}{R_1 C_2} + v_{cmd} \tag{4.22}$$

The effective hysteresis voltage can be derived as a function of the slope of the carrier waveform and the ideal hysteresis value. The slope of the carrier waveform for exponential and triangular cases can be determined by differentiating (4.21) and (4.22), respectively, as shown below:

$$\begin{aligned} \frac{dv_{car}}{dt} &= \frac{v_1}{R_1 C_2} * e^{\frac{-t}{R_1 C_2}} \\ \frac{dv_{cart}}{dt} &= \frac{v_1}{R_1 C_2} \end{aligned} \tag{4.23}$$

The slope of an exponential carrier is a function of time as seen from (4.23). The

exponential function can be approximated to a triangular one if the time-constant R_1C_2 is much higher than the charging or discharging period of the capacitor C_2. Assuming this condition is satisfied, the effect of delays will be discussed in terms of slope of a triangular carrier.

The new edges of the triangular carrier expressed in terms of the ideal edges, the slope from (4.23) and delay are

$$\begin{aligned} v_{cart++} &= v_{car+} + \frac{V_{DS} * D}{R_1 C_2} * t_1 \\ v_{cart--} &= v_{car-} - \frac{V_{DS} * D'}{R_1 C_2} * t_1' \end{aligned} \tag{4.24}$$

Using equation (4.24), the control and hysteresis voltages for triangular carrier can be determined. The expressions thus obtained are

$$\begin{aligned} v_{cmde} &= v_{cmd} + \frac{V_{DS}}{2R_1 C_2}\left(Dt_1 - D't_1'\right) \\ v_{hyse} &= v_{hys} + \frac{V_{DS}}{R_1 C_2}\left(Dt_1 + Dt_1'\right) \end{aligned} \tag{4.25}$$

The switching frequency F_s is the inverse of the time period T_s. The time period T_s can be expressed as the sum of the on-time t_{on} and off-time t_{off}. The on-time and off-time can be determined using the slope of the carrier waveform v_{car} during the respective time interval, and the effective hysteresis voltage v_{hyse}. The expression for switching frequency is as in equation (4.27) for a triangular carrier. The switching frequency equation thus derived depicts the dependency of F_s on the following parameters.

- Duty ratio of the converter
- Voltage across the MOSFET
- Filter time constant
- Hysteresis

$$F_s = \frac{1}{t_{off} + t_{on}} = \frac{1}{\left\{ \frac{v_{hyse}}{\frac{dv_{car}}{dt}\Big|_{t_{off}}} + \frac{v_{hyse}}{\frac{dv_{car}}{dt}\Big|_{t_{on}}} \right\}} \tag{4.26}$$

In the exponential case, the slope of the carrier is a function of time and hence it is difficult to find a closed form expression for the switching frequency. When the filter components are properly designed such that the integrator condition is satisfied, the exponential dependency of the carrier waveform can be approximated to be a linear relationship with time. Inserting the slope for triangular carrier from equation (4.23), the switching frequency can be expressed as

$$F_s = \frac{V_{DS} DD'}{v_{hyse} R_1 C_2} \tag{4.27}$$

In an ideal case of no delays, v_{hyse} will be replaced by v_{hys} in the above equation.

4.3. Design Criteria

The design process assumes the approximation as specified in (4.11). The procedure then requires knowledge of relationship between the low and high corners, the mid band gain of the filter and the design specifications. Specifically, the switching frequency needs to be related to the filter frequency response parameters. The time constants for the high pass and low pass sections are the inverses of the low corners and high corners indicated in (4.13) and (4.14), respectively.

The simplified time constants for the high pass and low pass sections are defined as

$$\tau_{Ls} = C_1 \left(R_1 + R_2 \right) \tag{4.28}$$

$$\tau_{Hs} = C_2 \left(R_1 \| R_2 \right) \tag{4.29}$$

The low corner is chosen to sufficiently block the average component. A factor of 0.002 of the switching frequency ensures proper dc elimination. The design condition is

$$\begin{aligned} \omega_{Ls} &= 2\pi \frac{f_s}{500} \\ \tau_{Ls} &= \frac{500}{2\pi f_s} \end{aligned} \tag{4.30}$$

The criterion for choice of high corner is proper integrator operation. The low pass filter time constant should be very high in comparison to the switching frequency so that the filter output is linear, rather than exponential. The filter time constant also governs the value of the external hysteresis voltage that can be applied. There is a trade off between the hysteresis and the time constant for a specified switching frequency, as is evident from (4.27).A higher time constant necessitates lower value of hysteresis to maintain the same switching frequency. The time constant of the filter should be related to the fraction of the time period for which the low pass capacitor charges and discharges, which is indicated by the duty ratio. A low pass filter time constant of twice the switching frequency times the duty ratio serves as a good choice. The design criterion is

$$\begin{aligned} \tau_{Hs} &= 2 * D' * T_s \\ &= \frac{2 * D'}{f_s} \end{aligned} \tag{4.31}$$

Choose the mid-band gain to be as close to unity as possible. This criterion ensures that the square waveform at the input is not completely attenuated by the filter. The range for the mid-band gain is

$$0.8 \le A_{ms} \le 0.9$$

Assuming R_2 to be 'r' ohms, equation (4.15) can be re arranged to yield R_1 as seen below:

$$R_1 = \frac{(1 - A_{ms})}{A_{ms}} * R_2 \tag{4.32}$$

The design equations for the capacitors can be determined from equations (4.28) ,(4.29), (4.30) and (4.31) as

$$C_2 = \frac{\tau_H}{R_1 \| R_2} \quad C_1 = \frac{\tau_L}{R_1 + R_2} \tag{4.33}$$

The effect of delays is to increase the hysteresis voltage to v_{hyse} as discussed in section 4.2. Another factor that affects the hysteresis is the offset voltage of the comparators. An ideal comparator has zero offset voltage and consequently the switching occurs when the input differential voltage becomes zero. But in a practical scenario the switching occurs when the differential voltage becomes equal to the offset voltage. The comparators should be chosen such that the effect of the offset voltage is negligible.

4.4. Bandpass Filter Parameter Variations

The variation of the filter components affects the frequency response of the filter and thus the switching frequency of the modulator. As depicted in section 4.1, the 3-db corners, the centre frequency as well as the gain of the filter are a function of the capacitors and the resistors. The switching frequency expression in (4.27) shows the dependency on the low pass filter time-constant which is the product of C_2 and parallel combination of R_1 and R_2.

An ac analysis as well as a dc transient analysis was run in Saber, with the band pass filter parameters varied, and the accompanying graphs display the transient and frequency response parameters as a function of each of the filter components. The

observations help to validate the approximation of the bandpass filter transfer function carried out in section 4.1.

Define the ratios of the capacitors and resistors as follows:

$$\frac{C_1}{C_2} = x$$
$$\frac{R_2}{R_1} = y \tag{4.34}$$

For the specific case of 500 KHz switching frequency, the nominal values are indicated in Table 4-2. The ratios can then be determined from (4.34) as x=10 and y=15. The range of variation calculated for each component is indicated in Table 4-2.

Table 4-2 Nominal values and range of variation of bandpass filter components

Bandpass filter component	Nominal value	Range of variation
Capacitor C1	1μF	C1/x to xC1= 0.1 to10μF
Capacitor C2	0.1μF	C2/x to xC2= 0.01 to1μF
Resistor R1	10Ω	R1/y to yR1= 1 to150Ω
Resistor R2	150Ω	R2/y to yR2= 15 to 2250Ω

4.4.1. Effect of C_1

Observation. Capacitor C_1 is the dc-elimination capacitor. The effect of C_1 is more pronounced on the high pass cutoff than the low pass, as seen in Figure 4-5 .Specifically, the high pass cutoff decreases through the entire range, rapidly in the C_1/x to C_1 interval, and thereafter gradually declines to almost zero. As far as the low pass is concerned, in the initial C_1/x to C_1 range, there is an appreciable decline, after which it remains relatively constant. The centre frequency also drops swiftly in the start, and then slowly to near zero. The dc-transient analysis results are graphed in Figure 4-6, which shows that the peak-to-peak amplitude rising rapidly in the beginning stages of variation and then staying relatively fixed.

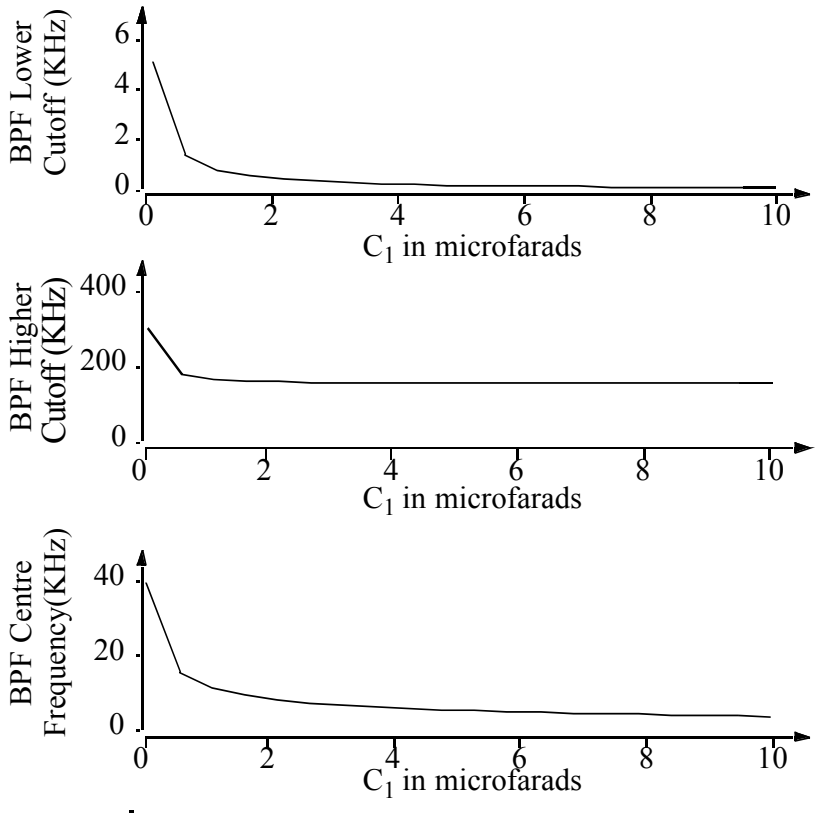

Figure 4-5 Bandpass frequency response parameters as a function of C_1; R_1=10Ω, C_2=0.1μF, R_2=150Ω.

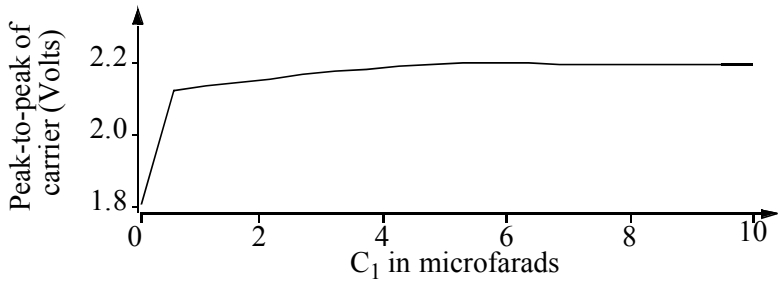

Figure 4-6 Peak-to-peak amplitude of carrier waveform as a function of C_1; R_1=10Ω, C_2=0.1μF, R_2=150Ω.

Interpretation. As shown in (4.13), if the conditions specified by (4.11) are met, then the high pass cutoff is primarily dependent on C_1 and the resistors only, while the low pass cutoff becomes a function of C_2 and the resistors. In the initial stages, C_1 is comparable to C_2 and hence the low pass cutoff shows an appreciable decline in this range. Beyond the nominal value of 1μF, the relationship between C_1 and C_2 satisfies the

stipulated condition, and hence its contribution towards low pass cutoff is minimal. The high pass cutoff is inversely dependent on C_1, which accounts for the deterioration observed. Since the centre frequency is the geometric mean of the low and high corners, the graph follows a decline similar to the behavior of the two cutoffs. Similarly, C_1 has an appreciable effect on the peak-to-peak amplitude of the carrier waveform as long as (4.11) is not fulfilled.

4.4.2. Effect of C_2

Observation. The frequency response of the filter as C_2 is varied is shown in Figure 4-8. The high pass filter cutoff declines gradually through out the entire range of C_2/x to xC_2, with the cutoff becoming more dependant on C_2 as C_1/C_2 falls below unity. The low pass cutoff displays a steep decrease in C_2/x to C_2 range, and then it reduces slowly to near zero. The centre frequency follows a curve bearing a strong resemblance to the low corner curve of the filter. A dc transient analysis run with C_2 varied results in the steady state carrier waveform shown in Figure 4-7. The alteration of the carrier amplitude is displayed in Figure 4-9.

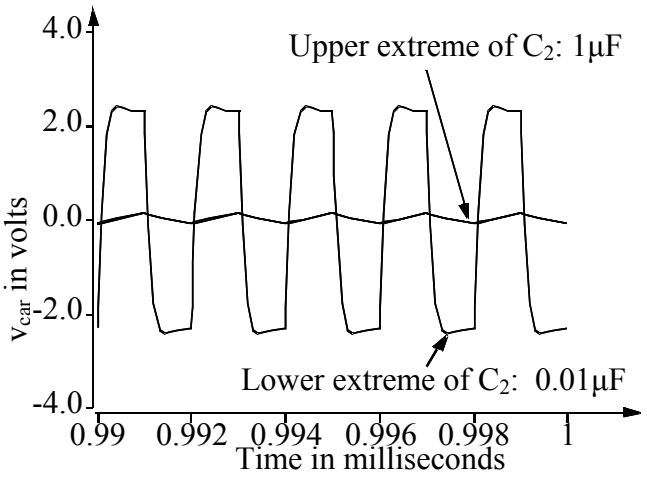

Figure 4-7 Carrier waveform as a function of C_2; R_1=10Ω, C_1=1μF, R_2=150Ω.

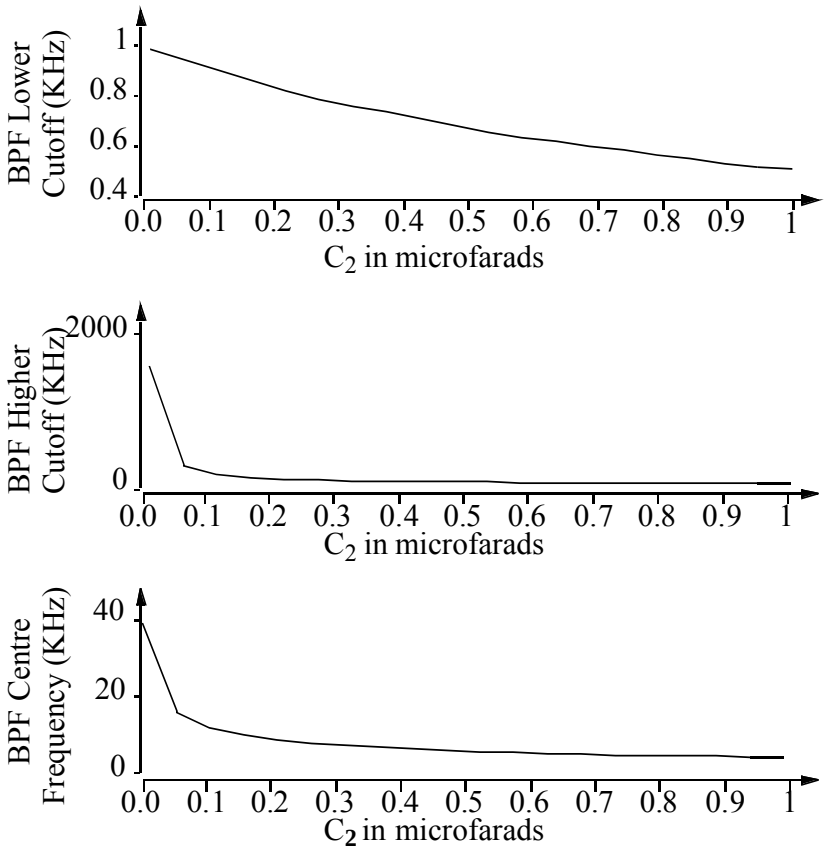

Figure 4-8 Bandpass frequency response parameters as a function of C_2; R_1=10Ω, C_1=1μF, R_2=150Ω.

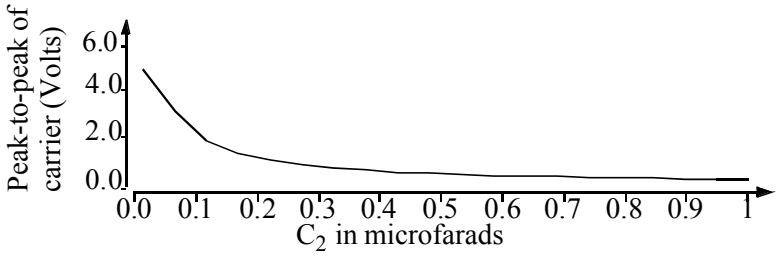

Figure 4-9 Peak-to-peak amplitude of carrier waveform as a function of C_2; R_1=10Ω, C_1=1μF, R_2=150Ω.

Interpretation. The dependence of the low pass cutoff on C_2 as seen in (4.6) is heightened in the initial stages because the condition defined by (4.11) is satisfied. The inverse proportionality between C_2 and the high pass cutoff justifies the decrease of the low corner in response to increase in C_2. The impact of C_2 on the shape and amplitude of carrier waveform can be explained using the gain and low pass cutoff equations. At the

lower end of C_2/x, the low pass cutoff is very high and the pass-band of the filter includes the frequency of the input square wave. The integrator ceases to function and the filter passes the square wave without change. This behavior is in compliance with the condition for integration, which states that the filter time constant should be much higher than the time period of the input waveform. At the higher end of xC_2, the carrier waveform is nearly triangular, but has a very low peak-to-peak value due to the deteriorating effect on the filter gain. The same reason applies to the observed decline of peak-to-peak value of carrier with rise in C_2.

4.4.3. Effect of R_1

Observation. As shown in Figure 4-10, the behavior of the band pass filter with variation of R_1 is similar to its reaction when C_2 is changed. The high pass cutoff displays a gradual decrease, and when R_1/R_2 exceeds unity, the cutoff becomes primarily dependant on R_1alone. The low pass cutoff exhibits a gradual decline to almost zero with an increase in R_1, but not as swiftly as in the case of C_2.The carrier wave amplitude falls to zero slowly over the entire range as seen in Figure 4-11.

Interpretation. The high pass cutoff behavior can be reasoned using the inverse proportionality between R_1 and the cutoff as seen in (4.6) and (4.13). When the approximation condition is violated, the decline of the low corner would be much more rapid due to the non negligible presence of R_1. As can be inferred from (4.14), when R_1 is much lesser than R_2, the impact on the low pass cutoff due to R_1 is more pronounced. The fall of the carrier amplitude is due to the decrease in gain with increase in R_1.

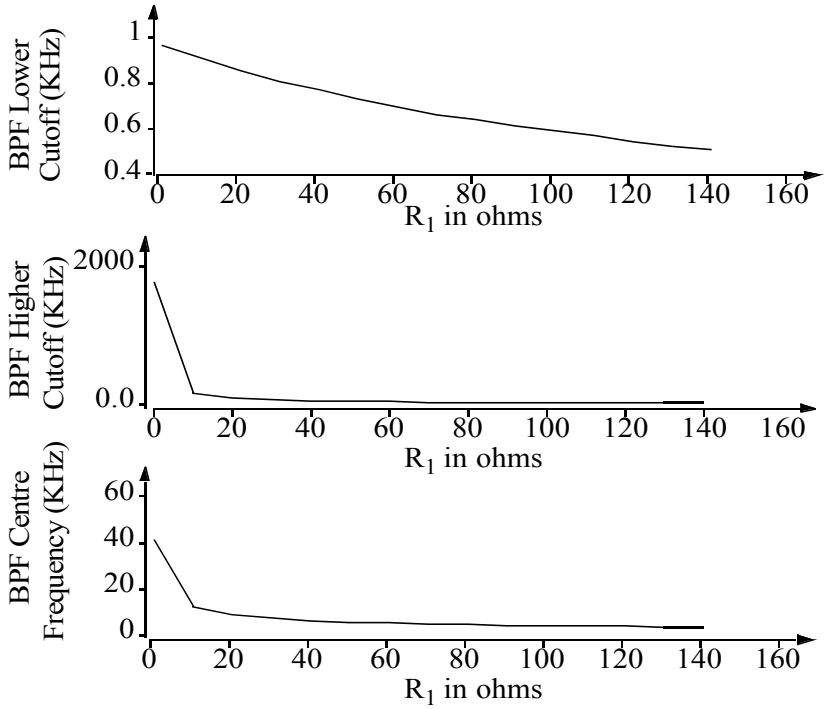

Figure 4-10 Bandpass frequency response parameters as a function of R_1; C_1=1μF, C_2=0.1μF, R_2=150Ω.

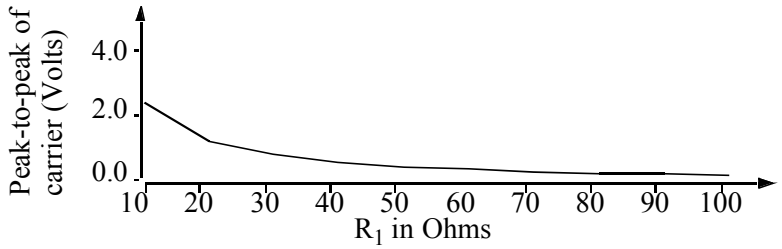

Figure 4-11 Peak-to-peak amplitude of carrier waveform as a function of R_1; C_1=1μF, C_2=0.1μF, R_2=150Ω.

4.4.4. Effect of R_2

Observation. In this case, the band pass filter's frequency and transient response follows a behavior similar to C_1 variation. The high pass cutoff falls rapidly in R_2/y to R_2 ohms range, and then slowly to almost zero. The low pass cutoff shows a steep decrease in the initial range, after which it remains constant. The amplitude of the carrier increases rapidly in the beginning stages, staying constant afterwards. Figure 4-12 and Figure 4-13 shows the results of ac analysis and transient analysis, respectively.

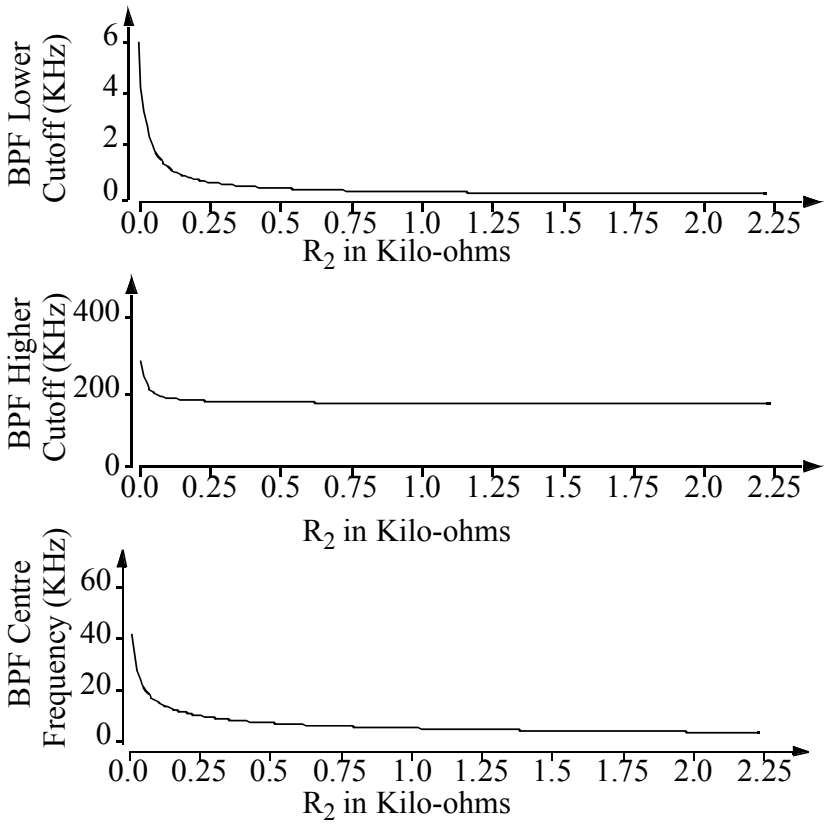

Figure 4-12 Bandpass frequency response parameters as a function of R_2; R_1=10Ω, C_1=1μF, C_2=0.1μF.

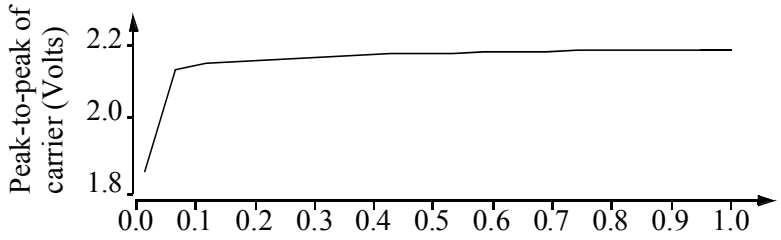

Figure 4-13 Peak-to-peak amplitude of carrier wave as a function of R_2; R_1=10Ω, C_1=1μF, C_2=0.1μF.

Interpretation. With other components at their nominal values shown in Table 4-2, apart from C_1, R_2 is the major contributor towards the high pass cutoff as seen in (4.13) . This explains the observed decline of the low corner of the filter. The effect of R_2 on low pass cutoff is visible in the initial stages because it becomes comparable to R_1 value and consequently, a deciding factor of (4.14).

As the observations show, when the condition specified by equation (4.11) is

approached in the range of variation, then the impact of C_1 and R_2 on the low corner is more pronounced, as is the effect of C_2 and R_1 on the high corner. The analysis of the bandpass filter parameter variations serves to justify the approximation made in derivation of transfer function of bandpass filter.

4.5. Hysteretic Comparator

The hysteretic comparator comprises of adder and subtractor, comparators and D flip flop with set and reset pins. The adder and subtractor receive V_o and the hysteresis voltage $v_{hys/2}$ as the inputs. The outputs $V_o + v_{hys/2}$ and $V_o - v_{hys/2}$ are fed to the comparators which compare them against the upper and lower edges of the carrier waveform v_{car}. The comparator outputs trigger the set and reset pins of the flip flop. The clock input of the flip-flop is disabled and no input is given to D pin.

The design of the comparators is dependent on the input voltage values. The comparators should be chosen so that the power supply rails are higher than the maximum input voltage swing. The summer and subtractor are realized using operational amplifiers with negative feedback. The inputs V_o and $v_{hys/2}$ are applied to the non-inverting terminals of the op-amp. Assuming ideal scenario, the design requires equal valued resistors, as well as op-amps whose power supplies are greater than the maximum input voltage swing. This condition necessitates the positive power supply to be greater than $V_o + v_{hys/2}$ and the negative power supply to be greater than $V_o - v_{hys/2}$.

- Choose equal valued resistors for realizing the adder and subtractor.
- Choose operational amplifiers whose power supply rails are sufficient to accommodate the maximum and minimum input voltage swings. Another criterion is that the gain-bandwidth should be greater than the maximum switching frequency. A converter output voltage of 5V and maximum hysteresis of 2V sets the maximum and minimum voltages to the operational amplifier as 6V and 4V, respectively. LM837N was chosen with minimum and maximum supply voltages

of 3V and 18V, respectively. The gain-bandwidth is 25MHz which is sufficient for a maximum operating frequency of 2MHz.

- Choose comparator with fast response time, low offset voltage and power supply rails higher than the input voltage. The comparator selected was AD790, with propagation delay of 45ns, maximum input offset voltage of 250μV and maximum input differential voltage of 15V.

- Choose D flip-flop with acceptable propagation delay. The flip-flop chosen was CD74HCT74E with maximum propagation delay of 40 ns. Maximum frequency of operation is 50MHz for a supply voltage of 5V, which is acceptable for the maximum switching frequency of 2MHz.

The designed values for the control stage are specified in Table 4-3.

Table 4-3 Designed values for the control stage

Component	Name
Bandpass filter	C_1=1μF,C_2=0.1μF R_1=10Ω,R_2=150Ω
Hysteretic Comparator	100Ω (adder, subtractor) Op-amp-LM837 Comparator-AD790N D flip-flop – CD74HCT74E
Gate Driver	IRF4427

CHAPTER 5
EXPERIMENTAL VERIFICATION

The hysteretic PWM with internally generated carrier as described in Chapter 3 was realized in printed circuit board using the components designed as per the methodology outlined in Chapter 4. The working of the circuit was verified, with each block tested individually and waveforms obtained.

The organization of the chapter is as follows:

- Modulator waveforms: The waveforms obtained from the control stage as well as the power stage are displayed in this section. The power section focuses on issues of converter efficiency and ripple in the output voltage. The control section deals with the bandpass filter, hysteretic comparator and gate driver. The images obtained are analyzed to establish a coherent relationship with the theoretical analysis performed in earlier chapters.

- Comparative study of theory and experiment: This section performs a systematic study of the measurements obtained from the actual circuit, with emphasis on consistency with theory and explanation of deviations.

5.1 Hysteretic PWM Waveforms

The hysteretic modulator for a boost dc-dc converter with internally generated carrier was implemented in printed circuit board. The Protel schematic and the built circuit are displayed in Figure 5-1 and Figure 5-2, respectively.

Equipments. The equipments that were used to test, analyze and verify the working of the built circuit are detailed.

- Tektronix TDS 460A Four Channel Digitizing Oscilloscope: Maximum analog bandwidth of 400 MHz, maximum digitizing rate of 100 mega samples/second.

- HP 6236B Triple Output Power Supply: 0-6V, 0-2.5A/0+ 20V, 0-0.5A.

- HP 6024A DC Power Supply: 0-60V/0-10A, 200W.

- Tektronix AM503 Current Probe Amplifier installed in TM502A Power Supply module, used with A6302 current probe: Maximum input current of 20 A (dc + peak ac), 50 MHz bandwidth, rise time of < 7 ns, deflection Factor of 1 - 5 A/div.

Design of bandpass filter. The main blocks of the control stage are the bandpass filter and hysteretic comparator. The design of the bandpass filter in the built circuit is as follows.

Given: Desired switching frequency, f_s = 500 KHz, Duty ratio, D'=0.5.

- The time constants are determined as follows:

$$\tau_{HPF} = \frac{500}{2*\pi*f_s} \qquad \tau_{LPF} = 2*\frac{D'}{f_s}$$
$$= 1.592*10^{-4}\,s \qquad = 2*10^{-6}\,s$$

- Select mid-band gain to be near unity, A_{ms}= 0.87
- Assume R_2=100 Ω, determine R_1 using the gain formula.

$$R_1 = \frac{(1-A_{ms})}{A_{ms}} * R_2$$
$$= 14.9\Omega$$

- Calculate the values of capacitors using the formula for highpass and lowpass time constants.

$$C_2 = \frac{\tau_{LPF}}{R_1 \| R_2}$$
$$C_1 = \frac{\tau_{HPF}}{R_1 + R_2} \qquad = \frac{2*10^{-6}}{14.9 \| 100}$$
$$= 1.386\mu F \qquad = 0.1542\mu F$$

As assumed in the design process, C_1>>C_2 and R_2>>R_1. The actual time constants as calculated from the designed values are $1.75*10^{-4}\,s$ and $1.823*10^{-6}\,s$ for the highpass and lowpass sections, respectively. The percentage of error is less than 10%.

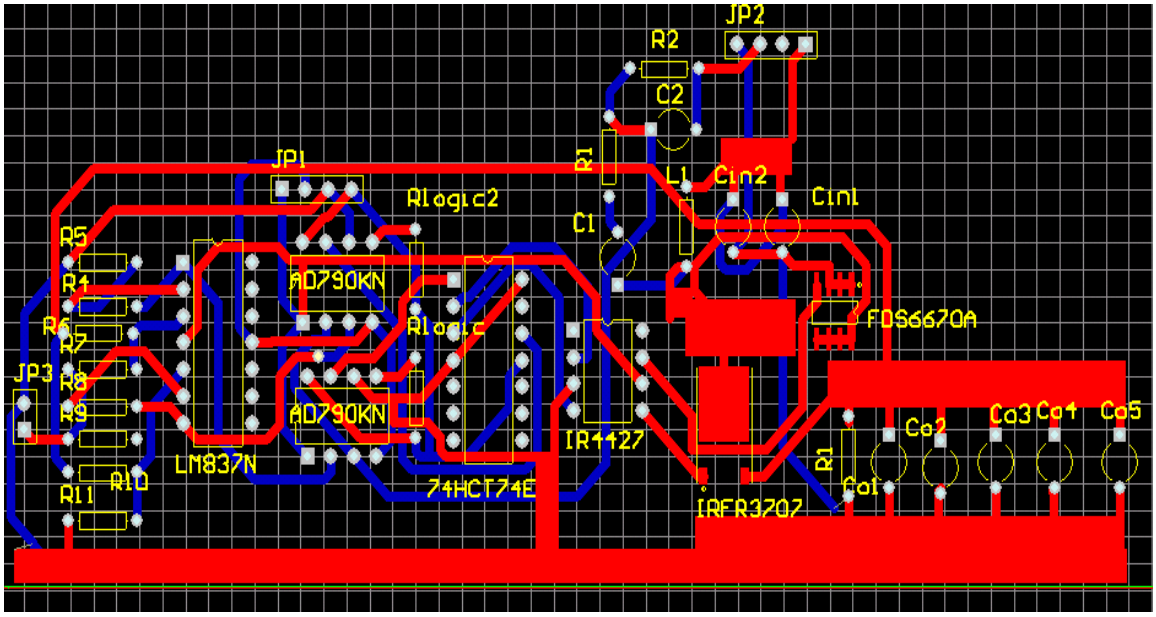

Figure 5-1 Protel layout of printed circuit board for the boost converter with hysteretic PWM control with internally generated carrier.

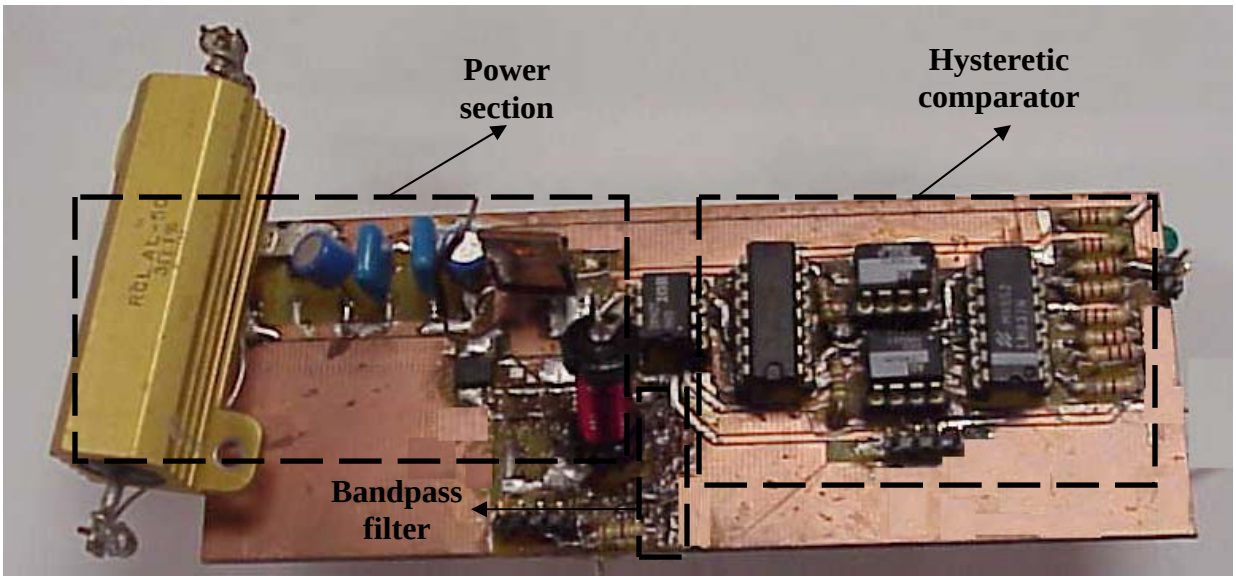

Figure 5-2 Boost converter implemented on printed circuit board.

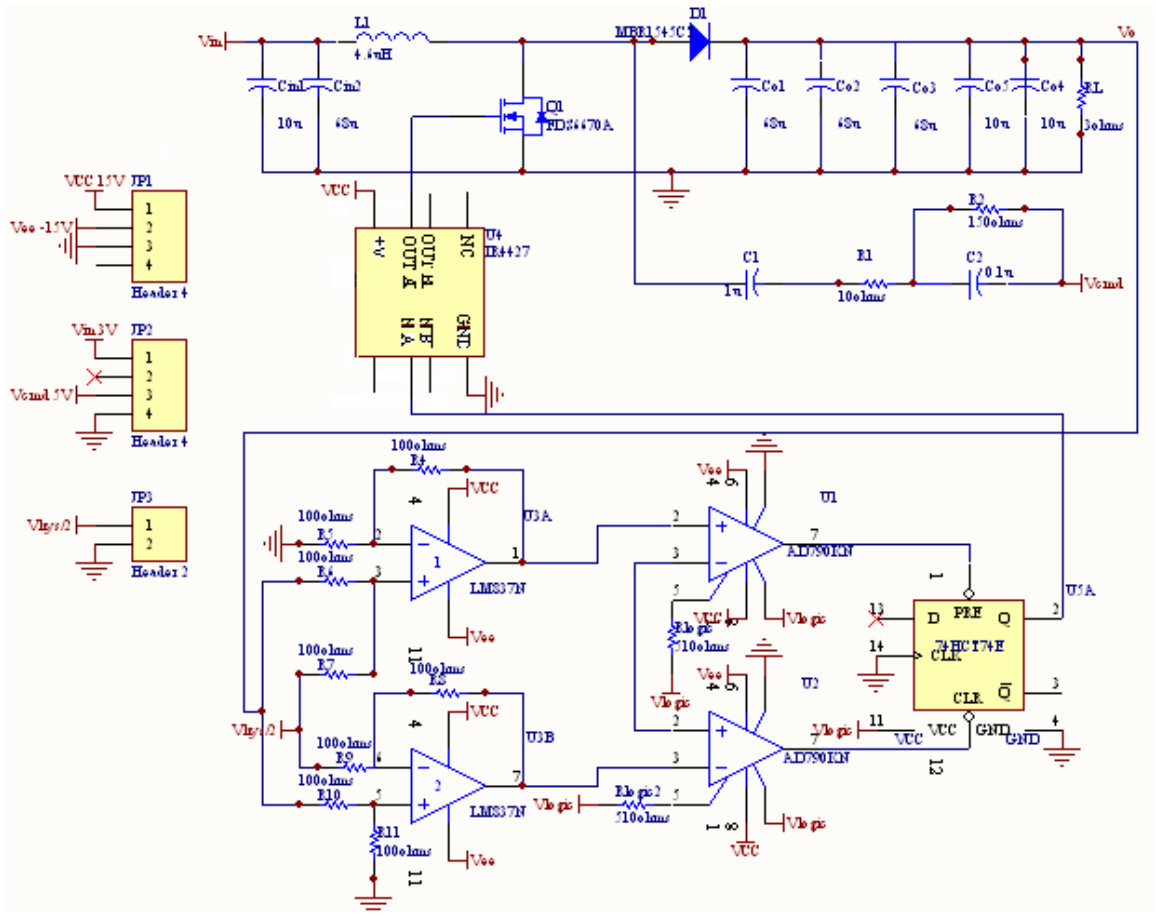

Figure 5-3 Protel schematic.

Table 5-1 Bill of materials

Component designator	Value	Qty	Manufacturer	Part number	Package
C_{in1}	10µF	1	Vishay	593D106X9025C2T	Axial-lead
C_{in2}	68µF	1	Vishay	94SP686X0020FBP	Axial-lead
L_1	4.6µH	1	Wilco	RLH47G	Radial-leaded
Q_1	MOSFET	1	Fairchild	FDS6670A	S0-8
D_1	Schottky diode	1	Fairchild	MBR1545CT	TO-220AB
C_{o1}	68µF	3	Vishay	94SP686X0020FBP	Axial-lead
C_{o4}	10µF	2	Vishay	593D106X9025C2T	Axial-lead
C_1	1µF	1	Vishay	C440C105M5U5HA	Axial-lead
R_1	10Ω	1	Multicomp	CR1/4W-5%-10R	Through-hole
R_2	150Ω	1	Multicomp	CR1/4W-5%-150R	Through-hole
C_2	0.1µF	1	Vishay	CW80C104KM	Axial-lead
R_4 to R_{11}	100Ω	8	Multicomp	CR1/4W-5%-100R	Through-hole
R_{logic}	510Ω	2	Multicomp	RC1/4G511JT	Through-hole
U3A, U3B	Op-amp	1	National Semiconductor	LM837	DIP
U1, U2	Comparator	2	Analog Devices	AD790N	8-pin plastic Mini-DIP
U5	D flip-flop	1	Texas Instruments	CD74HCT74E	PDIP
U4	Gate driver	1	International Rectifier	IR4427	8 Lead PDIP

5.1.1 Power Stage

The built circuit is a boost dc-dc converter which converts a dc input of 3 volts to dc output of 5 volts. Figure 5-4 shows the input and output voltages of the converter as

obtained from the actual circuit. The components were designed to ensure low power loss, high efficiency and low ripple. The final circuit works at an efficiency of 80% with an output voltage ripple of 120 mV.

5.1.1.1 Efficiency

The efficiency of the converter is a function of the parasitic elements associated with the components. The built circuit pulls an input current of 2.8 A at an input voltage of 3 V, while delivering 5 V at 1.3 A. The efficiency is the ratio of output power over input power, and it can be determined to be 80%. The efficiency is an indicator of the power dissipated in the unwanted resistances of the converter components. The power dissipated is in the form of heat, and a good way to keep the components from overheating is to use heat sinks as well as fans.

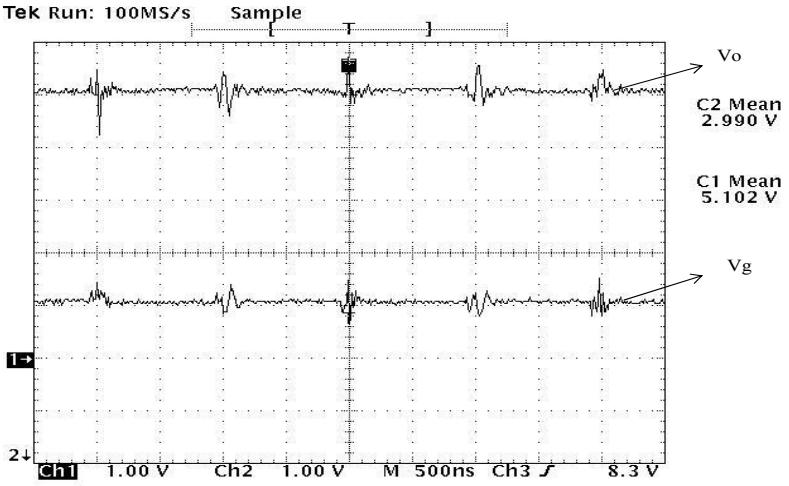

Figure 5-4 Converter output and input voltages.

5.1.1.2 Ripple

The ripple in the output voltage has to be within the acceptable limits. The circuit was designed to maintain a ripple of 1% of the output voltage, which comes to 50 mV. The actual circuit has a peak to peak ripple of 120 mV, as shown in Figure 5-5, which is

2.5% of the output. The output ripple is inversely proportional to the value of the capacitor in the output of the converter. Capacitors with low esr ensures that the jumps in the output dc voltage is as small as possible. Oscon capacitors with esr in the range of 30 mΩ were selected to achieve this.

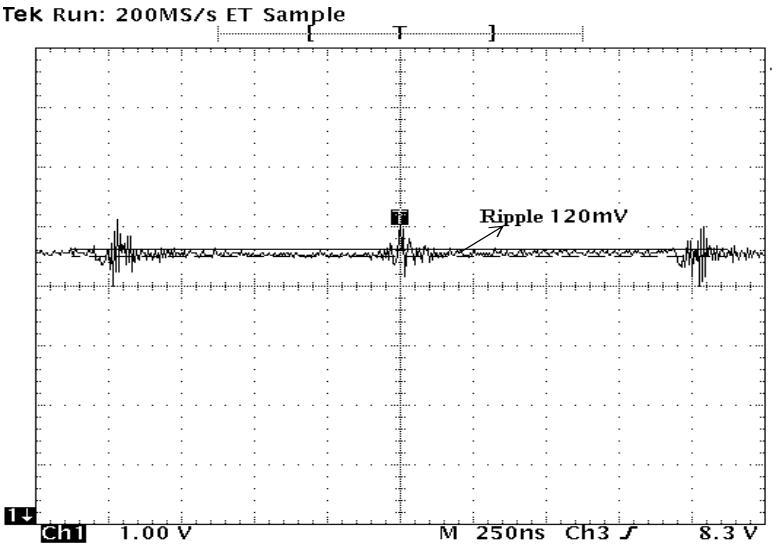

Figure 5-5 Converter output voltage focusing on ripple.

5.1.2 Control Stage

5.1.2.1 Bandpass filter

The bandpass filter comprising of capacitors and resistors, generates a triangular waveform, v_{car}, from the square waveform v_{in}, produced across the switching MOSFET. The intermediate waveform v_1 is the output of the series capacitor which removes the average content of v_{in}. Figure 5-6 displays the waveforms at input; intermediate and output stages of the filter. The spikes at the switching instants can be attributed to the current change involved in the MOSFET transition from saturation to cutoff. The slightly exponential nature of the carrier waveform is due to the fact that the low pass filter time constant is comparable to the on and off time periods of the MOSFET waveform. The

time constant R_1C_2 is 1.1 μ and the on time is 1.1 μs and off time is 0.9 μs. Larger values of time constant would require smaller values of external hysteresis voltage to be applied.

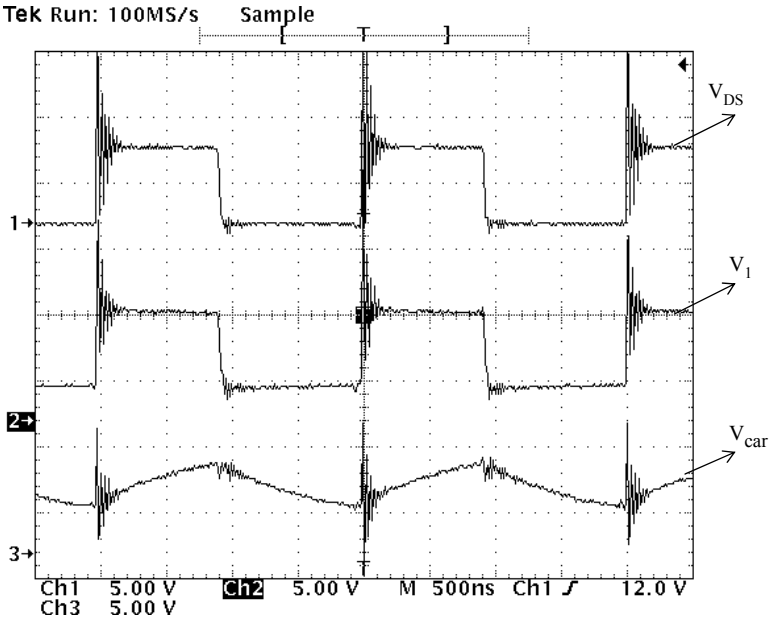

Figure 5-6 Bandpass filter input, output after dc elimination capacitor, and carrier waveform output.

5.1.2.2 Hysteretic comparator

Adder, subtractor, and comparator. The first stage of the hysteretic comparator consists of adder and subtractor built using operational amplifiers and resistors. These blocks produce the summed and subtracted outputs of converter output voltage V_o and externally applied hysteresis voltage $V_{HYS/2}$. There exists two comparators, both of which receive the carrier waveform as one of the inputs, and the adder and the subtractor provides the other input. The comparator which receives the added output and the carrier, switches low when the carrier waveform crosses the upper limit and turns high when the carrier goes below the limit. The comparator that accepts the subtracted output and the carrier, gives a low output when the carrier becomes lower than the low limit and switches to high level as the carrier becomes higher than the low limit. Figure 5-7 and

Figure 5-8 shows the inputs and output of the two comparators. The delay in switching of the upper comparator is shown in Figure 5-9, and can be determined to be 300 ns.

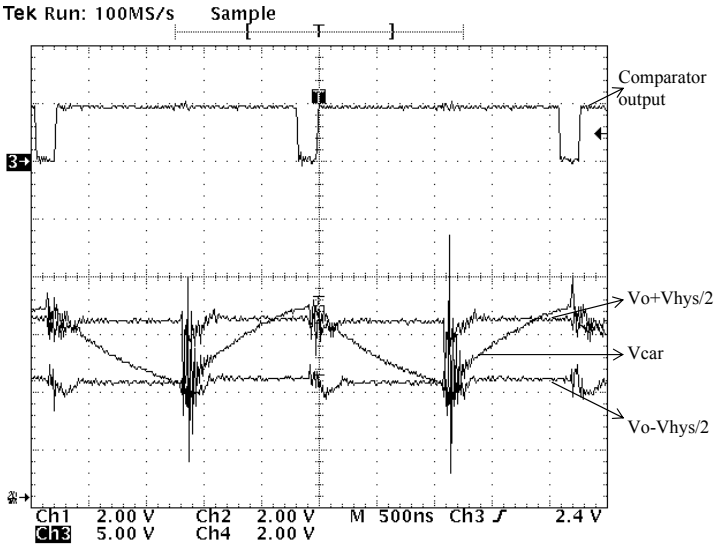

Figure 5-7 Upper comparator inputs and output.

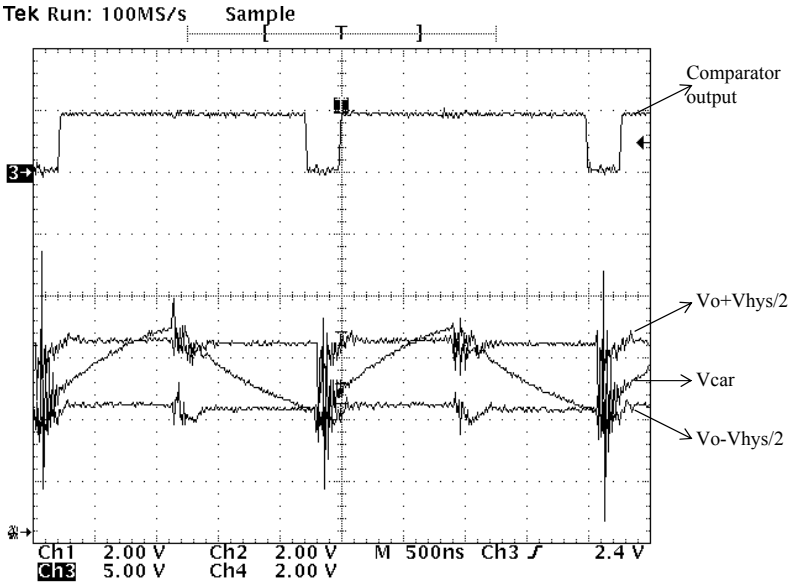

Figure 5-8 Lower comparator inputs and output.

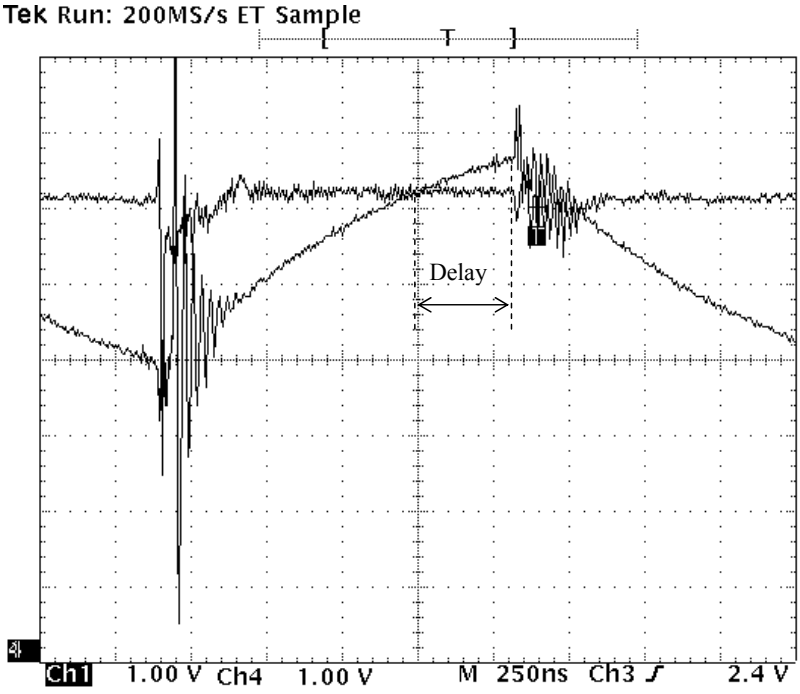

Figure 5-9 Carrier waveform showing the delay in switching.

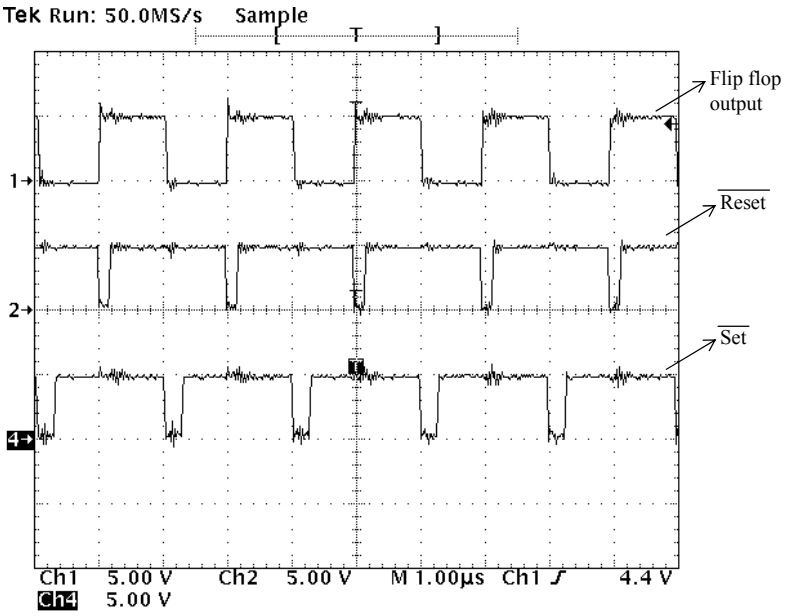

Figure 5-10 Inputs and output of D flip-flop.

D flip-flop. The final block in the hysteretic comparator is an edge triggered D flip-flop with set and reset pins. The outputs of the comparators are fed to the set and reset inputs of the flip-flop. The D input is not connected and the clock is tied to ground. As

shown in Figure 5-10, the flip-flop switches to high level when the Reset input makes a high to low transition. As the Set input makes a low to high transition, the flip-flop output switches low.

5.1.2.1 Gate driver

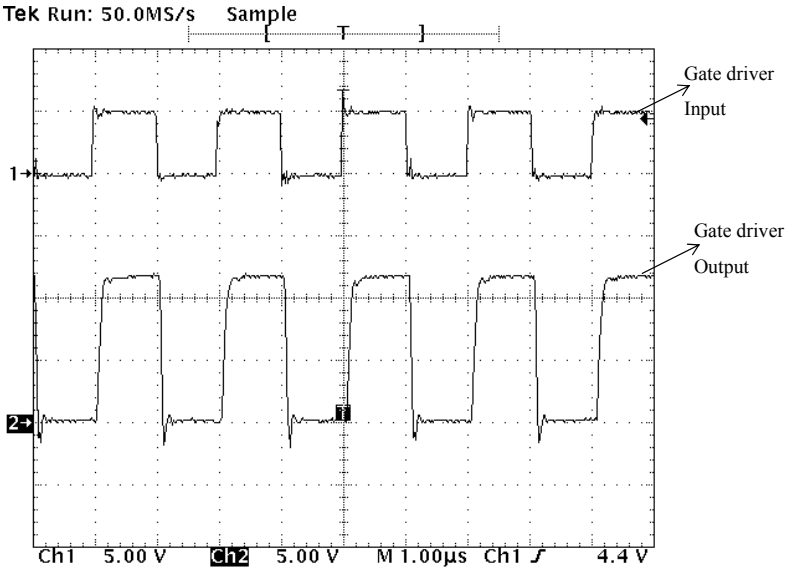

Figure 5-11 Input and output of gate driver.

The gate driver serves to boost the output of the flip-flop to a voltage high enough to be applied as the gating signal. As seen in Figure 5-11, the gate driver has boosted the input it received 5 V to 12 V which is sufficient for the MOSFET in use. The power supply rails of the driver determine the amount of output voltage it can provide. The gate driver chosen should have a peak current rating that is higher than the current required to charge the gate drain capacitance of the active switch.

5.2 Observations and Graphs

The relationship between the output voltage of the converter, V_o, and the control voltage v_{cmd} has been detailed, as well as the variation of the duty ratio as a function of v_{cmd}. The dependence of the switching frequency on the hysteresis voltage v_{hys} has been

studied. Line regulation curve is also plotted, which depicts a nearly constant V_o as converter input voltage V_g is varied. The range of values of the duty ratio which ensures proper working of the converter has been graphed.

5.2.1 Control Voltage

Duty ratio. The dependency of the duty ratio of the gating signal of the active switch on the control voltage v_{cmd} is depicted in Figure 5-12. Variation of v_{cmd} produces a set of values of the duty ratio which guarantees a working converter. The converter input fixed at 3 V, and v_{cmd} varied from 4.07 V to 5.76 V, the duty ratio spans over 0.227 to 0.773.

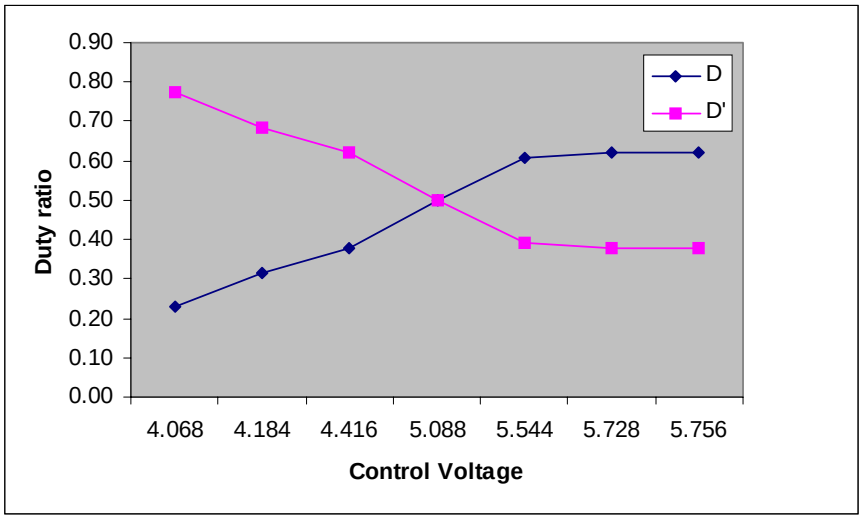

Figure 5-12 Relationship between duty ratio and control voltage.

In the absence of delays, the control voltage is identical to the output voltage and is hence inversely proportional to duty ratio D'. When delays are present, the extra term introduces an offset but maintains the inverse proportionality. The higher end of the duty ratio is limited by the efficiency of the converter, which causes the gain to drop and the converter to stop functioning. At the lower end, the on time of the MOSFET is too low and the gain once again drops to below unity. The converter gain is plotted as a function

of duty cycle in Figure 5-13. This plot clearly depicts the reason for the existence of a working range of the duty ratio. Beyond the shown range, the gain of the converter falls to less than unity.

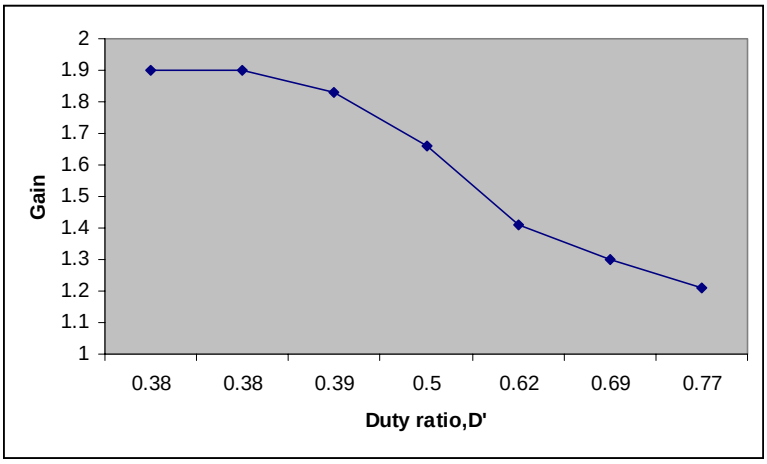

Figure 5-13 Converter gain as a function of duty cycle D'.

Converter output voltage. The output voltage follows the control voltage as it is varied from 4.07 to 5.76 V. It increases from 3.62 to 5.712 V during this range. The output voltage of the converter would be same as the control voltage if delays were not present. In the ideal case, V_o and v_{cmd} would be linearly dependent. The existence of delays alters the peak and valley of the carrier waveform, and consequently v_{cmd} changes to a new value v_{cmde}. The linear relationship is preserved in the presence of delays as well.

Table 5-2 Observations for control voltage variation

V_{DS} (V)	v_{cmde} (V)	D	D'	t_1 (ns)	t_1' (ns)
4	3.9	0.23	0.77	300	300
4.4	4.1	0.23	0.77	300	300
5.2	4.46	0.31	0.69	300	300
6	4.96	0.38	0.62	300	300
6.6	5.43	0.50	0.50	300	300
6.6	5.67	0.61	0.39	300	300
6.8	5.65	0.62	0.38	300	300

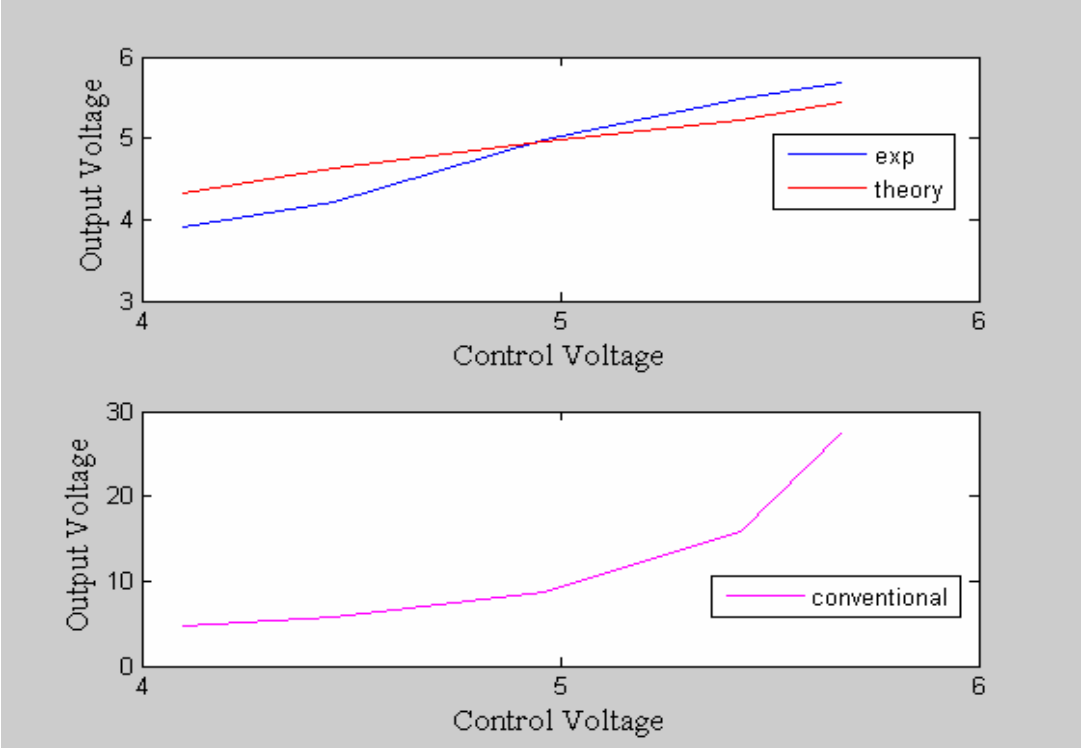

Figure 5-14 Relationship between control and output voltage; input voltage V_G=3 V.

Figure 5-14 depicts the relationship between V_o and v_{cmd}, for theory as well as experiment. . The output voltage for a particular value of control voltage can be calculated using equation 4.25. The equation expresses the effective control voltage v_{cmde} as a function of the ideal control voltage v_{cmd} and a term involving delays, duty ratio and voltage across the MOSFET. The ideal control voltage v_{cmd} is equal to the output voltage V_o of the converter and the equation can be re-arranged to determine V_o from v_{cmde} and the delay term. For each value of the control voltage, the voltage across the MOSFET, delays and duty ratio were observed on the oscilloscope and tabulated as seen in Table 5-2. The theory agrees well with the experiment, with percentage deviation less than 10%. The figure also shows the control-output relationship of a conventional voltage-mode constant-frequency PWM, for comparison purposes. Equations (1.1) and (2.1), with r(t) substituted by v_{cmd}, are used to determine the output voltage for the same set of control

voltage values as in the new control scheme. The maximum and minimum values of the carrier are taken as 6V and 4V here. It is clearly seen that the control-output relation is non-linear for the conventional case.

5.2.2 Switching Frequency

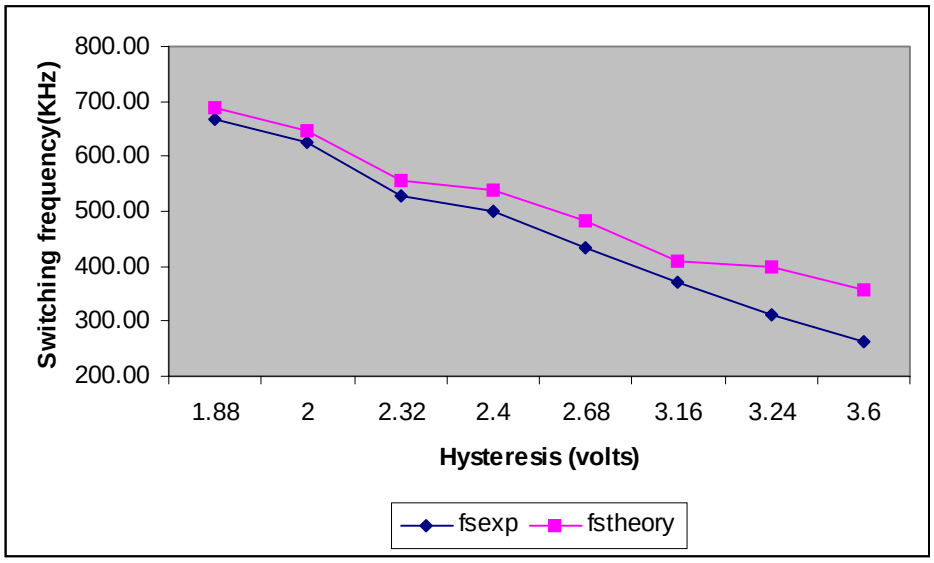

Figure 5-14 Switching frequency, experimental and theoretical.

Table 5-3 Observations for switching frequency with hysteresis variation

V_{DS} (V)	D	D'	v_{hyse} (V)
4	0.23	0.77	2.4
4.4	0.23	0.77	2.4
5.2	0.31	0.69	2.6
6	0.38	0.62	2.8
6.6	0.50	0.50	3.2
6.6	0.61	0.39	3
6.8	0.62	0.38	2.9

The switching frequency was derived as a function of the hysteresis, duty ratio, filter parameters and delay, in Chapter 4. A plot of the switching frequency as a function of hysteresis, for theory and experiment, is shown in Figure 5-14. The theoretical prediction was carried out using equation 4.27, which expresses the switching frequency as a function of hysteresis; duty ratio, voltage across MOSFET, and the low-pass filter

time-constant. The duty ratio and voltage across MOSFET were tabulated for each value of hysteresis, as shown in Table 5-3. The delays remained relatively constant at 300ns for the off-time and 250ns for the on-time, over the range of variation of hysteresis. The percentage of error between theoretical prediction and actual measured frequency is less than 10%. This error can be attributed to the fact that the carrier waveform is exponential in nature as opposed to the triangular approximation used in derivation of switching frequency in Chapter 4.

5.2.3 Line Regulation

The variation of the output voltage of the converter as a function of the line voltage is displayed in Figure 5-15. The curve remains relatively constant at 5 V as input V_G is altered over the range 2.2 to 4.2 V.

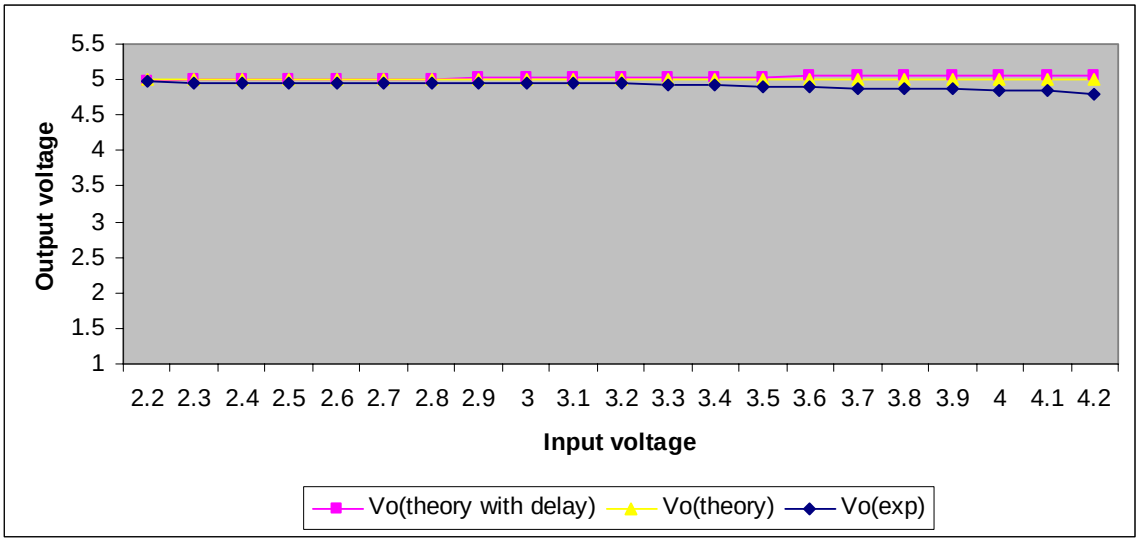

Figure 5-15 Line regulation.

The theoretical prediction was performed using equation 4.25, which expresses the control voltage in the presence of delays. The equation can be re-arranged to show the dependency of output voltage on the input voltage of the converter. As V_g is varied, the effective control voltage, the duty ratio and the delays are tabulated; which is then used to

calculate the output voltage. In the absence of delays, the input voltage variation will have no effect on the output voltage which will stay constant at the control voltage value of 5V.

CHAPTER 6
CONCLUSION

6.1 Summary

The hysteretic PWM with internally generated carrier was built, tested and analyzed for a boost dc-dc converter. The control system consists of generation of carrier waveform by integrating the voltage across the active switch and its subsequent comparison in a hysteretic comparator, with the converter output voltage. The control circuitry makes use of the information provided by the power stage of the converter to directly control the output voltage. Linearity is achieved between the control variable and the output voltage. There is a range of values of the control voltage which ensures proper working of the converter, and beyond which the input voltage is not boosted. This limit on the control voltage is imposed by the presence of parasitic elements which reduce the converter gain to less than unity. The switching frequency of the converter is dependent on hysteresis; lowpass filter time constant, output voltage of the converter and the duty ratio. The theoretical prediction of the modulator's behavior was in close agreement with the observations and measurements made on the built circuit.

6.2 Future Work

The thesis has concentrated only on steady state analysis of the control system. The transient response of the system can be studied using digitally controlled dynamic load. Also, future work could concentrate on the frequency analysis of the control system, with emphasis on phase margin, gain margin and stability issues.

APPENDIX
DESIGN OF POWER STAGE OF CONVERTER

The design of the power stage of the converter is covered here. The design specifications are indicated in Table 4-1.

Diode

The diode constitutes a fixed loss and necessitates it to be designed first. The parameters required are the blocking voltage and average current. Blocking voltage for the diode in a boost converter is the output voltage, V_o, and average current through the diode is the output current, I_o. The choice of MBR1545CT meets the specifications. The voltage drop across the diode, V_f, for the specified I_o is 0.5V. The loss in the diode is the product of the average current and the instantaneous voltage across it.

The diode loss is determined as

$$\begin{aligned} P_d &= V_f I_o \\ &= 0.5 * 2 \\ &= 1W \end{aligned} \tag{1}$$

The loss budget with the diode loss is now

$$\begin{aligned} P_R &= \frac{P_o}{\eta} - P_o - P_d \\ &= 1.5W \end{aligned} \tag{2}$$

MOSFET

The choice of the MOSFET requires knowledge of the blocking voltage and the Root Mean Square (RMS) current flowing through it.

The MOSFET blocks a voltage equal to, V_o ,in its off state. The RMS current is

$$I_{rms} = I_o \frac{\sqrt{D}}{D'} = 2.8A \tag{3}$$

Assuming MOSFET loss to be less than 70% of the loss budget, the drain-to-source resistance can be calculated as

$$R_{DSr} = 0.7 \frac{P_R}{I_{rms}^{\ 2}} = 0.13\Omega \tag{4}$$

FDS6670A was chosen to meet the specifications. The actual loss in the selected MOSFET with an R_{DS} of 8mΩ is

$$P_{MOS} = I_{rms}^{\ 2} R_{DS} = 1W \tag{5}$$

The revised loss budget is

$$P_{Rr} = P_R - P_{MOS} = 0.42W \tag{6}$$

Capacitor

The design of output capacitor is governed by the acceptable amount of ripple in the output voltage. Assuming the ripple to be 1% of the output voltage, the capacitor is designed as follows:

$$C_o = I_o \frac{D}{f_s \Delta V_{o-c}} = 40\mu F \tag{7}$$

OSCON capacitors which yield very low ESR values are chosen to ensure that the additional ripple contribution is negligible.

Inductor

The inductor was chosen to ensure Continuous Conduction Mode (CCM) in the converter. The inductor is designed as follows:

$$\begin{aligned} L &\geq \frac{\left(DD'^2\right)_{\max} V_o}{2I_{o\min} f_s} \\ &\geq \left(\frac{1}{3}\left(\frac{2}{3}\right)^2\right)\frac{5}{2*1.5*500kHz} \\ &\geq 0.5\mu H \end{aligned} \tag{8}$$

The RMS current through the inductor is a function of the load current as seen below:

$$\begin{aligned} I_{Lrms} &= \frac{I_o}{D'} \\ &= 4A \end{aligned} \tag{9}$$

Assuming the inductor loss to be 25% of the remaining loss, the inductor resistance is calculated to be

$$\begin{aligned} r_L &= 0.25\frac{P_{Rr}}{I_{Lrms}^{\ 2}} \\ &= 6.56m\Omega \end{aligned} \tag{10}$$

LIST OF REFERENCES

1. R.W. Erickson, *Fundamentals of Power Electronics.* New York: Chapman & Hall, 1997.

2. H.P. Forghani-zadeh, and G.A. Rincon-Mora, "Current-sensing techniques for DC-DC converters." Proceedings of the 45th IEEE Midwest Symposium on Circuits and Systems, MWSCAS '02, 4-7 Aug. 2002, Tulsa, Oklahoma, vol. 2, pp. II-577-II-580.

3. S. Poulsen, and M.A.E. Andersen, "Self oscillating PWM modulators, a topological comparision." Proceedings of the 26th International Power Modulator Symposium, 2004 and 2004 High-Voltage Workshop, 23-26 May 2004, San Francisco, California, pp. 403-407.

4. K.M. Smedley, and S. Cuk, "One-cycle control of switching converters." IEEE Transactions on Power Electronics, vol. 10, issue 6, pp. 625–633, Nov. 1995.

5. K.M. Smedley, "Integrators in pulse width modulation [switching circuits]." Proceedings of the 27th IEEE Power Electronics Specialists Conference, PESC '96, 24-27 June 1996, Baveno, Italy, vol. 1, pp. 773-781.

6. R. Redl, "Small-signal high-frequency analysis of the free-running current-mode-controlled converter." Proceedings of the 22nd IEEE Power Electronics Specialists Conference, PESC '91, 24-27 June 1991, Cambridge, Massachusetts, pp. 897-906.

7. D. Maksimovic, Jang Yungtaek, and R.W. Erickson, "Nonlinear-carrier control for high-power-factor boost rectifiers." IEEE Transactions on Power Electronics, vol. 11, issue 4, pp. 578-584, July 1996.

8. R. Liu, and C.Q. Lee, "Design of high frequency resonant factor correction circuits via input current programmed control schemes." Proceedings of the 35th IEEE Midwest Symposium on Circuits and Systems, MWSCAS '92, 9-12 Aug. 1992, Washington, DC, vol. 1, pp. 245-248.

9. D.-S. Chen, and J.-S. Lai, "A study of power correction boost converter operating at CCM-DCM mode." Proceedings of IEEE Southeastcon, 1993, 4-7 April 1993, Charlotte, North Carolina, p. 6.

10. S. Poulsen, and M.A.E. Andersen, "Hysteretic controller with constant switching frequency." IEEE Transactions on Consumer Electronics, vol. 51, issue 2, pp. 688-693, May 2005.

11. J.J. Spangler, and A.K. Behera, "A comparison between hysteretic and fixed frequency boost converters used for power factor correction." Proceedings of the 8th IEEE Applied Power Electronics Conference and Exposition, APEC '93, 7-11 March 1993, San Diego, California, pp. 281-286.

12. R. Redl, and N.O. Sokal, "Current –mode control, five different types, used with the three basic classes of power converters: small-signal ac and large-signal dc characterization, stability requirements, and implementation of practical circuits." Proceedings of the 16th IEEE Power Electronic Specialists Conference, PESC '85, 24-28 June 1985, Toulouse, France, pp. 771-785.

13. Q. Yao, and D.G. Holmes, "A simple, novel method for variable hysteretic-band current control of a three phase inverter with constant switching frequency." Proceedings of the 28th IEEE Industry Applications Society Annual Meeting, IAS '93, 2-8 October 1993, Toronto, Canada, vol. 2, pp. 1122-1129.

14. E.J.P. Mascarenhas, "Hysteretic control of a continuous boost regulator." Proceedings of IEE Colloquium on Static Power Conversion, 11 Nov. 1992, London, UK, pp. 7/1-7/4.

15. J.A. Abu Qahouq, Jia, Luo, and I. Batarseh "Voltage regulator module with interleaved synchronous buck converters and novel voltage-mode hysteretic control." Proceedings of the 44th IEEE Midwest Symposium on Circuits and Systems, MWSCAS '01, 13-17 August 2001, Dayton, Ohio, vol. 2, pp.972-975.

16. K.D.T. Ngo, S.K. Mishra, and S. Thekkevalappil, "Pulsewidth modulator with carriers derived from converter waveforms." Electronics Letters, vol. 41, issue 3, pp. 152-154, Feb. 2005.

17. S.R.R. Chavez, "Mixed-mode Schmitt trigger equivalent circuit." Electronics Letters, vol. 31, issue 3, pp.152-154, Feb. 1995.

BIOGRAPHICAL SKETCH

Soniya Noormuhamed Thekkevalappil was born on July 18, 1980, in Kerala, India. She completed her schooling from Chinmaya Vidyalaya Higher Secondary School. She obtained her bachelor's degree in electronics and communication engineering from Government Engineering College, Trichur, affiliated with University of Calicut, Kerala, India. She has been pursuing an MS in electrical and computer engineering at the University of Florida since January 2004. Her research interests include power management and circuit design.