intel®

8243
MCS-48® INPUT/OUTPUT EXPANDER

- ■ Low Cost
- ■ Simple Interface to MCS-48® Microcomputers
- ■ Four 4-Bit I/O Ports
- ■ AND and OR Directly to Ports

- ■ 24-Pin DIP
- ■ Single 5V Supply
- ■ High Output Drive
- ■ Direct Extension of Resident 8048 I/O Ports

The Intel® 8243 is an input/output expander designed specifically to provide a low cost means of I/O expansion for the MCS-48® family of single chip microcomputers. Fabricated in 5 volts NMOS, the 8243 combines low cost, single supply voltage and high drive current capability.

The 8243 consists of four 4-bit bidirectional static I/O ports and one 4-bit port which serves as an interface to the MCS-48 microcomputers. The 4-bit interface requires that only 4 I/O lines of the 8048 be used for I/O expansion, and also allows multiple 8243's to be added to the same bus.

The I/O ports of the 8243 serve as a direct extension of the resident I/O facilities of the MCS-48 microcomputers and are accessed by their own MOV, ANL, and ORL instructions.
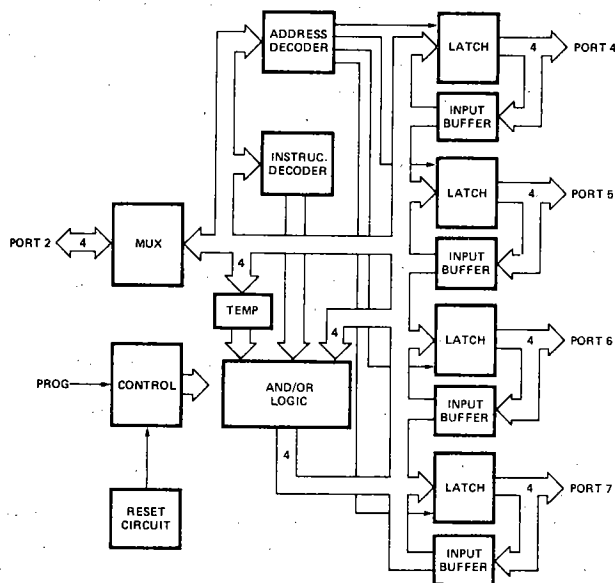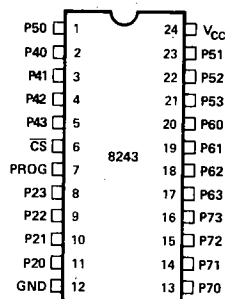

Figure 1. 8243
Block Diagram

Figure 2. 8243
Pin Configuration

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Table 1. Pin Description

Symbol	Pin No.	Function
PROG	7	Clock Input. A high to low transition on PROG signifies that address and control are available on P20-P23, and a low to high transition signifies that data is available on P20-P23.
$\overline{CS}$	6	Chip Select Input. A high on CS inhibits any change of output or internal status.
P20-P23	11-8	Four (4) bit bi-directional port contains the address and control bits on a high to low transition of PROG. During a low to high transition contains the data for a selected output port if a write operation, or the data from a selected port before the low to high transition if a read operation.
GND	12	0 volt supply.
P40-P43 P50-P53 P60-P63 P70-P73	2-5 1, 23-21 20-17 13-16	Four (4) bit bi-directional I/O ports. May be programmed to be input (during read), low impedance latched output (after write), or a tri-state (after read). Data on pins P20-P23 may be directly written, ANDed or ORed with previous data.
V_{CC}	24	+5 volt supply.

FUNCTIONAL DESCRIPTION

General Operation

The 8243 contains four 4-bit I/O ports which serve as an extension of the on-chip I/O and are addressed as ports 4-7. The following operations may be performed on these ports:

- Transfer Accumulator to Port.
- Transfer Port to Accumulator.
- AND Accumulator to Port.
- OR Accumulator to Port.

All communication between the 8048 and the 8243 occurs over Port 2 (P20-P23) with timing provided by an output pulse on the PROG pin of the processor. Each transfer consists of two 4-bit nibbles:

The first containing the "op code" and port address and the second containing the actual 4-bits of data. A high to low transition of the PROG line indicates that address is present while a low to high transition indicates the presence of data. Additional 8243's may be added to the 4-bit bus and chip selected using additional output lines from the 8048/8748/8035.

Power On Initialization

Initial application of power to the device forces input/output ports 4, 5, 6, and 7 to the tri-state and port 2 to the input mode. The PROG pin may be either high or low when power is applied. The first high to low transition of PROG causes device to exit power on mode. The power on sequence is initiated if VCC drops below 1V.

P21	P20	Address Code	P23	P22	Instruction Code
0	0	Port 4	0	0	Read
0	1	Port 5	0	1	Write
1	0	Port 6	1	0	ORLD
1	1	Port 7	1	1	ANLD

Write Modes

The device has three write modes. MOVD Pi, A directly writes new data into the selected port and old data is lost. ORLD Pi, A takes new data, OR's it with the old data and then writes it to the port. ANLD Pi, A takes new data, AND's it with the old data and then writes it to the port. Operation code and port address are latched from the input port 2 on the high to low transition of the PROG pin. On the low to high transition of PROG data on port 2 is transferred to the logic block of the specified output port.

After the logic manipulation is performed, the data is latched and outputed. The old data remains latched until new valid outputs are entered.

Read Mode

The device has one read mode. The operation code and port address are latched from the input port 2 on the high to low transition of the PROG pin. As soon as the read operation and port address are decoded, the appropriate outputs are tri-stated, and the input buffers switched on. The read operation is terminated by a low to high transition of the PROG pin. The port (4, 5, 6 or 7) that was selected is switched to the tri-stated mode while port 2 is returned to the input mode.

Normally, a port will be in an output (write mode) or input (read mode). If modes are changed during operation, the first read following a write should be ignored; all following reads are valid. This is to allow the external driver on the port to settle after the first read instruction removes the low impedance drive from the 8243 output. A read of any port will leave that port in a high impedance state.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias .... 0° C to 70° C
Storage Temperature .... -65° C to +150° C
Voltage on Any Pin
  With Respect to Ground .... -0.5 V to +7V
Power Dissipation .... 1 Watt

*NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
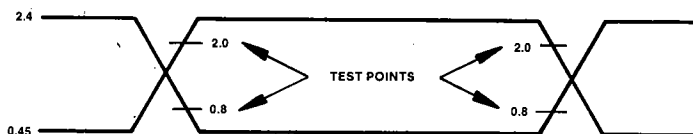
D.C. CHARACTERISTICS $T_A = 0°C$ to $70°C$, $V_{CC} = 5V$ 10%

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
VIL	Input Low Voltage	-0.5		0.8	V	
VIH	Input High Voltage	2.0		VCC+0.5	V	
VOL1	Output Low Voltage Ports 4-7			0.45	V	I_{OL} = 4.5 mA*
VOL2	Output Low Voltage Port 7			1	V	I_{OL} = 20 mA
VOH1	Output High Voltage Ports 4-7	2.4			V	I_{OH} = 240μA
IIL1	Input Leakage Ports 4-7	-10		20	μA	V_{in} = VCC to OV
IIL2	Input Leakage Port 2, CS, PROG	-10		10	μA	V_{in} = VCC to OV
VOL3	Output Low Voltage Port 2			.45	V	I_{OL} = 0.6 mA
ICC	VCC Supply Current		10	20	mA	
VOH2	Output Voltage Port 2	2.4				I_{OH} = 100μA
IOL	Sum of all I_{OL} from 16 Outputs			72	mA	4.5 mA Each Pin

*See following graph for additional sink current capability

A.C. CHARACTERISTICS $T_A = 0°C$ to $70°C$, $V_{CC} = 5V$ 10%

Symbol	Parameter	Min	Max	Units	Test Conditions
tA	Code Valid Before PROG	100		ns	80 pF Load
tB	Code Valid After PROG	60		ns	20 pF Load
tC	Data Valid Before PROG	200		ns	80 pF Load
tD	Data Valid After PROG	20		ns	20 pF Load
tH	Floating After PROG	0	150	ns	20 pF Load
tK	PROG Negative Pulse Width	700		ns	
tCS	CS Valid Before/After PROG	50		ns	
tPO	Ports 4-7 Valid After PROG		700	ns	100 pF Load
tLP1	Ports 4-7 Valid Before/After PROG	100		ns	
tACC	Port 2 Valid After PROG		650	ns	80 pF Load

2.4
2.0
2.0
TEST POINTS
0.8
0.8
0.45

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WAVEFORMS

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**GUARANTEED WORST CASE
CURRENT SINKING CAPABILITIES
OF ANY I/O PORT PIN vs. TOTAL
SINK CURRENT OF ALL PINS**

MAXIMUM SINK CURRENT ON ANY PIN @ .45V
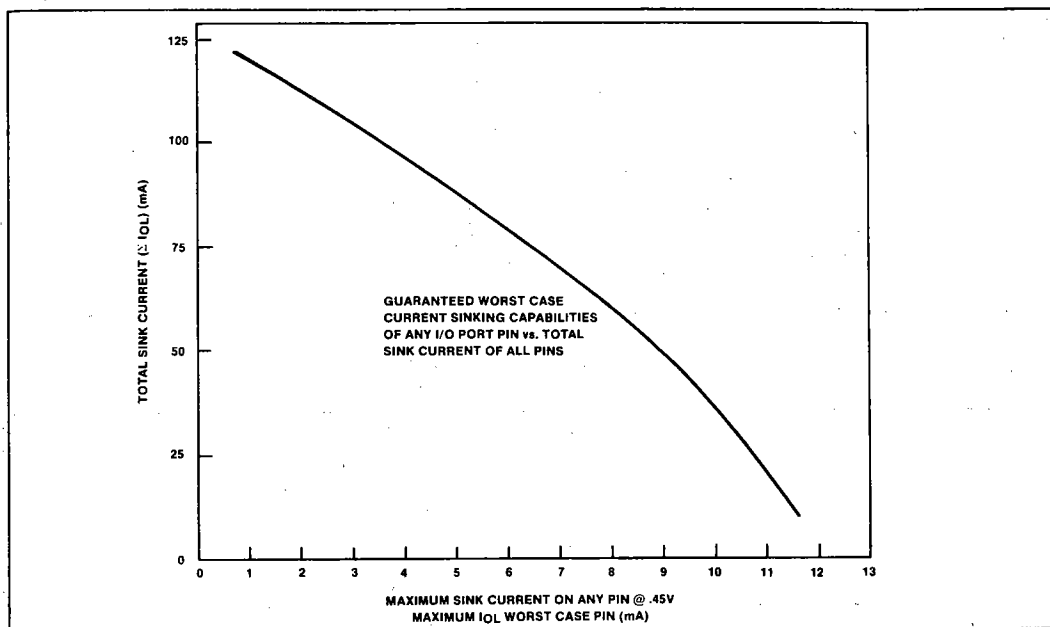MAXIMUM I_{OL} WORST CASE PIN (mA)
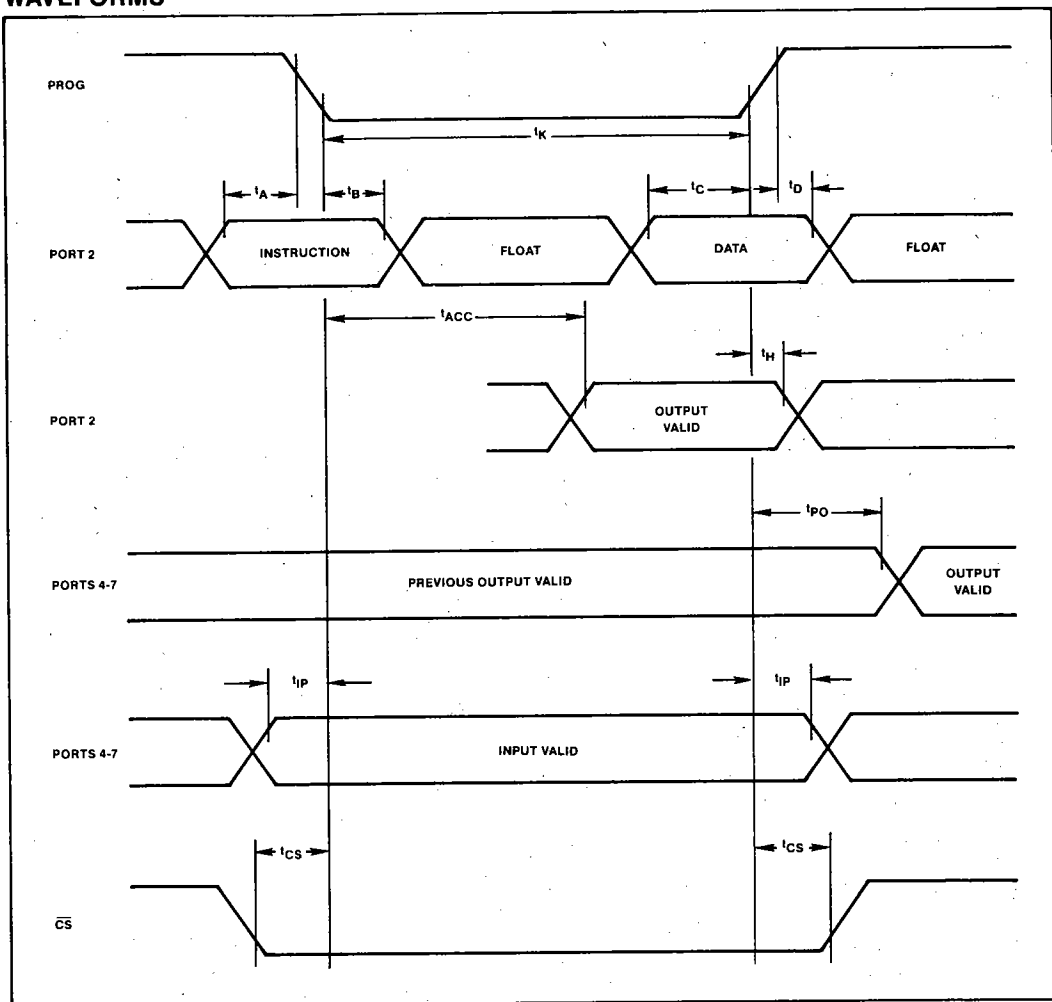
Figure 3

Sink Capability

The 8243 can sink 5 mA @ .45V on each of its 16 I/O lines simultaneously. If, however, all lines are not sinking simultaneously or all lines are not fully loaded, the drive capability of any individual line increases as is shown by the accompanying curve.

For example, if only 5 of the 16 lines are to sink current at one time, the curve shows that each of those 5 lines is capable of sinking 9 mA @ .45V (if any lines are to sink 9 mA the total I_{OL} must not exceed 45 mA or five 9 mA loads).

Example: How many pins can drive 5 TTL loads (1.6 mA) assuming remaining pins are unloaded?

I_{OL} = 5 x 1.6 mA = 8 mA
ϵI_{OL} = 60 mA from curve
pins = 60 mA ÷ 8 mA/pin = 7.5 = 7

In this case, 7 lines can sink 8 mA for a total of 56mA. This leaves 4 mA sink current capability which can be divided in any way among the remaining 8 I/O lines of the 8243.

Example: This example shows how the use of the 20 mA sink capability of Port 7 affects the sinking capability of the other I/O lines.

An 8243 will drive the following loads simultaneously.

2 loads — 20 mA @ 1V (port 7 only)
8 loads — 4 mA @ .45V
6 loads — 3.2 mA @ .45V
Is this within the specified limits?

ϵI_{OL} = (2 x 20) + (8 x 4) + (6 x 3.2) = 91.2 mA.
From the curve: for I_{OL} = 4 mA, ϵI_{OL} ≈ 93 mA. since 91.2 mA < 93 mA the loads are within specified limits.

Although the 20 mA @ 1V loads are used in calculating ϵI_{OL}, it is the largest current required @ .45V which determines the maximum allowable ϵI_{OL}.

NOTE: A10 to 50K Ω pullup resistor to +5V should be added to 8243 outputs when driving to 5V CMOS directly.
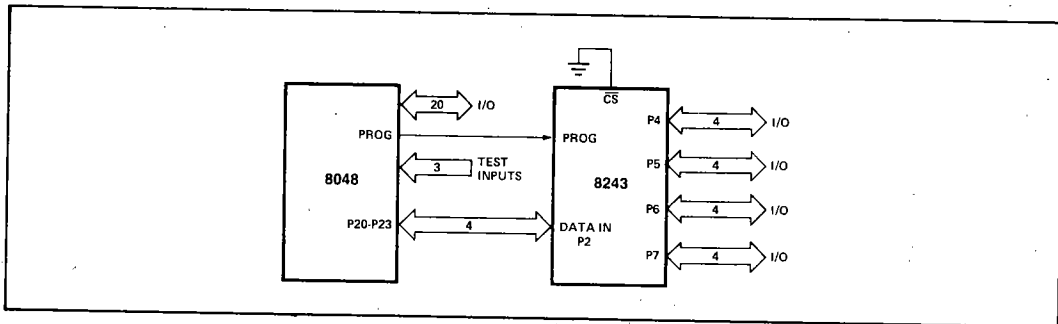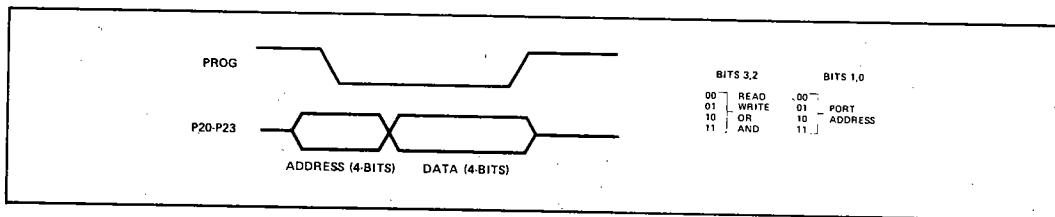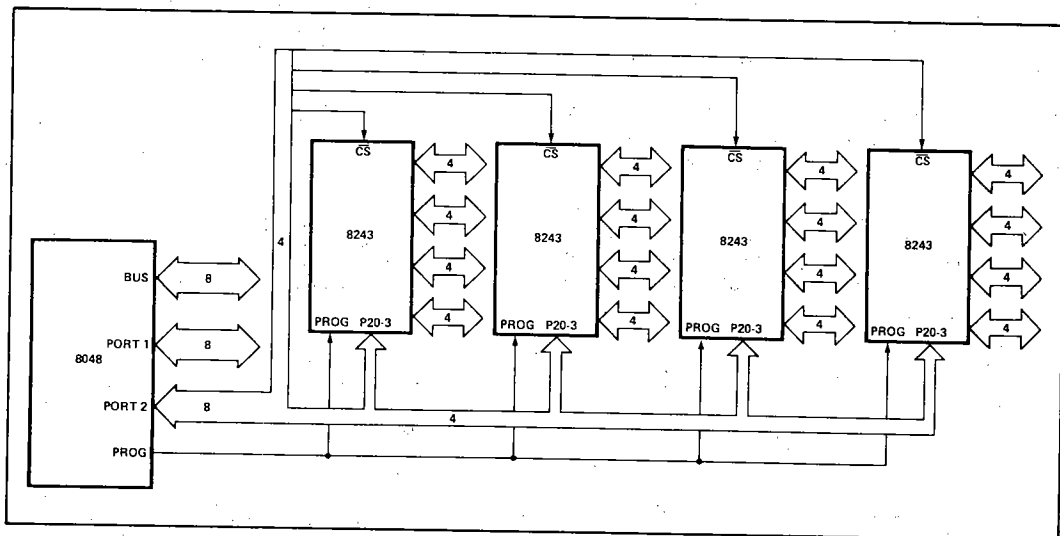
Figure 4. Expander Interface

Figure 5. Output Expander Timing

Figure 6. Using Multiple 8243's

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