# DOI: 10.1051/epjconf/201714108003

# Studies for an upgrade of ALICE Inner Tracking System: Pixel chip characterization

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**Abstract.** Inner Tracking System (ITS) of ALICE is used for vertex determination and tracking. Future heavy-ion program at the LHC aims to run with high luminosity. To address this challenge, upgrade program of ITS is underway, which aims at better position resolution (factor of 3), high detection efficiency (>99%), high-rate readout capabilities (100 kHz for Pb-Pb) and moderate radiation hardness (> 700 krad). The new ITS will be composed with 7 layers of silicon pixel chip based on Monolithic Active Pixel Sensor (MAPS) technology. The characterization test of various version of prototype chips at different phases of development has been performed. This contribution will provide the main characterization results obtained from the measurements performed at laboratories and using test beam for finalizing the pixel chip specification.

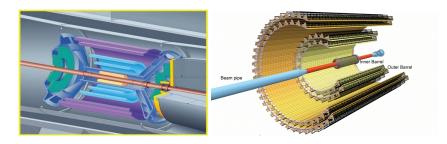
#### 1 Introduction

ALICE experiment is a dedicated heavy-ion experiment at the LHC. The main goal of ALICE experiment is to study properties of hot and dense matter (regarded as Quark-Gluon Plasma) expected to be produced heavy-ion collisions [1]. Up to now, ALICE has confirmed the creation of hot hadronic matter at high density and temperature by measurement of light and heavy flavours, flow, transverse momentum, jet, etc. However, the current experimental setup is not fully optimized to measure the rare probes over a broad range of  $p_T$ . Further progress on the characterization of QGP properties requires precision measurements of rare probes over a large kinematic range (from low  $p_T$  to high  $p_T$ ) and as a function of multi-differential observables. For significant improvement of vertexing and tracking capabilities at low  $p_T$ , ALICE ITS upgrade is underway, which aims at better position resolution, high detection efficiency and high-rate readout capabilities [2]. The ALICE collaboration confirmed the chip design after successfully performing chip characterization test for different prototypes in various phases. The results of the chip characterization test will be presented in the following sections.

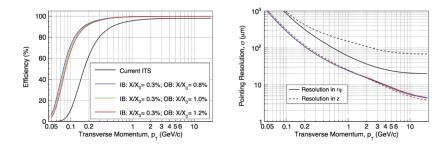
## 2 Upgrade plan of Inner Tracking System (ITS)

The ITS is located in a region closest to the beam pipe and used for vertex determination and tracking. The current ITS is constructed by 6 layers of three different technologies: 2 layers of silicon pixel

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**Figure 1.** Current inner tracking system(left) and new inner tracking system(right) schematics [4]. The current ITS is constructed by three different types of detectors (silicon pixel, silicon drift, silicon strip). The new ITS will be composed of only single type of detector, i.e. monolithic active pixel sensor having seven layers: three inner barrels and four outer barrels



**Figure 2.** Simulation results of tracking efficiency(left) and pointing resolution(right) for pion [5]. The results are compared between current ITS and new ITS with different material budget for new ITS outer barrel.

detector(Inner barrel), 2 layers of silicon drift detector and 2 layers of silicon strip detector (outer barrel) as shown in Figure 1. The silicon pixel detector of inner barrel is based on hybrid silicon pixel technology. During the second long shutdown (LS2) of the LHC in 2019-20, the current ITS will be replaced by a new ITS, which will be constructed by 7 layers (3 inner layers and 4 outer layers) of silicon pixel detector based on monolithic active pixel sensor technology. A schematics of the current and new ITS are shown in Figure 1.

The new ITS will achieve better position resolution by a factor of 3 and tracking efficiency higher than 99%. To improve position resolution, the innermost layer is moved close to the beam pipe from 39mm to 22mm, reducing material budget from 1.14% to 0.3% for inner barrel and reducing pixel size to  $28\mu\text{m}\times28\mu\text{m}$  (currently,  $50\mu\text{m}\times425\mu\text{m}$ ) [3, 4]. The tracking efficiency and the  $p_T$  resolution will be increased thanks to the increase of the radial extension and granularity of the detector. The simulation results for the tracking efficiency and pointing resolution of the new ITS compared to current ITS are shown in Figure 2. Furthermore, the new ITS will allow fast readout (Pb-Pb interaction rate of 100 kHz) and easy maintenance (fast insertion and removal of non-functioning detector modules) during yearly shutdown.

The new ITS silicon pixel chip is based on Monolithic Active Pixel Sensors (MAPS) technology with  $0.18\mu m$  CMOS imaging sensor by Tower Jazz. The CMOS circuitry is implemented on high-resistivity (>1k $\Omega$  cm) p-type epitaxial layer on p-type substrate shown in Figure 3. The electron-hole pairs are generated in expitaixal layer by charged particles and collected at NWELL collection diode.

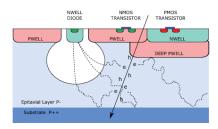
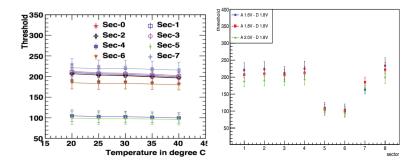


Figure 3. Cross-sectional diagram of the MAPS showing collection diode and transistors [4].



**Figure 4.** Temperature dependence (left) and analog supply voltage dependence (right) results. pALPIDE-3b chip is used with the back-bias voltage of -3V. The results show that the chip response is not changed in each conditions.

The DEEP PWELL shields NWELL containing PMOS transistor from collecting signal charge. It allows of full CMOS circuitry within active area [6].

## 3 Chip characterization test

The ALPIDE prototypes have 15 mm  $\times$  30 mm dimensions and contain  $1024 \times 512$  pixels. The ALPIDE prototype is UBS-based test system used both for laboratory measurements and test beam. It provides all readout and control functionality as well as ADCs for current measurements and has flexibility, which could be easily adapted for the tests of the other chips.

The laboratory test verified the dependence of the chip environment on the chip responses. For temperature dependence study, the chip temperature is changed between 20 and 40 degree by 5 degree steps and the threshold values are compared with different temperature shown in Figure 4. Threshold values remain same with increasing temperature for the back-bias voltage of -3V. For supply voltage dependence study, the analog supply voltage is changed from 1.6V to 2.2V by 0.2V steps. When the analog supply voltage is changed, the chip responses such as the threshold and the noise are also changed because real voltage and current on in-pixel circuitry are changed. However, change in analog supply voltage is compensated by tuning DAC values as shown in Figure 4. At the condition of the tuned DAC values, the threshold and noise values remain almost constant for all back-bias voltage condition. For the both studies, the cluster multiplicities were measured. The cluster multiplicities are found to be independent of chip temperature and of the analogue supply voltage.

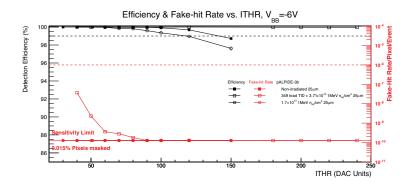


Figure 5. Detection efficiency and fake-hit rates for pALPIDE-3 with the back-bias voltage of -6V before and after irradiation.

The characterization of chip by test beam has been progressing at following sites: CREN, Pohang (Korea), SLRI (Thailand), Frascati (Italy). The ALPIDE prototypes are tested before and after irradiation up to the expected maximum levels of the radiation. The ALPIDE maintains the detection efficiency of  $\geq 99\%$  over a wide threshold value range and achieved very low fake-hit rates before and after irradiation as shown in Figure 5.

### 4 Summary

The ALICE ITS upgrade program is underway for significant improvement of vertexing and tracking capabilities at low  $p_{\rm T}$  and high readout rate. The chip which will be used in new ITS is developed after characterization of various prototype chips at various level to optimize its engineering design. The design goal of the chip is achieved from lab test and test beam. The ALPIDE prototype has been confirmed high detection efficiency( $\geq 99\%$ ), low fake hit rates( $<10^{-6}$ ), temperature and radiation hardness, etc. In future heavy-ion experiment, the new ITS will allow to measure rare probes and will improve the accuracy of the measurements.

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