module halfadder(

input a,b,

output sum,cout);

xor a1(sum,a,b);

and a2(cout,a,b);

endmodule

module fulladder(

input a,b,cin,

output s,cout);

wire s1,c1,c2;

halfadder ha1(cin,b,s1,c1);

halfadder ha2(s1,a,s,c2);

or or1(cout,c1,c2);

endmodule



