A Major Project Report

On

**Design and Analysis of Low Leakage 6T SRAM Cell and its Array Architecture in 45nm Technology**

Submitted in partial fulfilment for the award of

Bachelor of Technology in

Electronics and Communication Engineering



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Dec, 2015

Certificate

This is to certify that the work carried out by Jimmy Rajpal(9912102188), Nitij Agarwal(9912102333), Puneet Dua(9912102202) titled on ”Design and analysis of low leakage 6T SRAM cell” is carried out by them under my supervision.

Signature of Supervisor

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**Declaration by students**

In this report we have presented our views, thoughts and understanding of various concepts by us on “**Design and analysis of low leakage 6T SRAM cell in 45 nm technology**” and this report has been prepared by us and submitted for evaluation purpose.

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**Abstract**

High leakage current in deep-submicrometer regimes is becoming a significant contributor to power dissipation of CMOS circuits as threshold voltage, channel length, and gate oxide thickness are reduced. Consequently, the identification and modeling of different leakage components is very important for estimation and reduction of leakage power, especially for low-power applications. Since Leakage power becomes big percentage of total active power especially for small geometry CMOS technology. It is estimated that 20-50% of total average power during normal operation lost to leakage power. In this project, we studied about six transistor single SRAM cell, different parameters affecting leakage current in a SRAM cell and have applied few leakage reduction techniques individually.

**Acknowledgement**

This project consumed huge amount of work, research and dedication. Still, implementation would not have been possible if we did not have a support of many individuals. Therefore we would like to extend our sincere gratitude to all of them.

First of all we are thankful to Jaypee institute of information technology Noida, sector 128 for their financial and logistical support and for providing necessary guidance concerning projects implementation.

We are also grateful to our Mentor Mr. Siddhartha Sankar Rout and our teacher Mr. Satyendar Kumar for provision of expertise and technical support in the implementation. Without their superior knowledge and experience, the Project would have lack in quality of outcomes; thus their support has been essential.

Nevertheless, we express our gratitude toward our families and colleagues for their kind co-operation and encouragement which help us in completion of this project.

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1. **Introduction**

Semiconductor memories are one of the most important subsystem of modern digital systems. A memory is a storage unit. In previous years many hardware devices like magnetic tapes, drives and optical disks were used. Random access memory (RAM) is widely used in all the devices for storage.

Among RAMs; SRAM has become a major component in many VLSI Chips due to their large storage density and small access time. Since scaling of technology has going on, so large amount of memory can be fabricated on a single chip and due to that memories can able to do the operation speedy. Because of high density of chip, power dissipation increases. So the need for low power memory arises. Because of this, SRAM has become the topic of substantial research due to the rapid development for low power, low voltage memory design during recent years due to increase demand for notebooks, laptops, IC memory cards and hand held communication devices. SRAMs are widely used for mobile applications as both on chip and off-chip memories, because of their ease of use and low standby leakage.

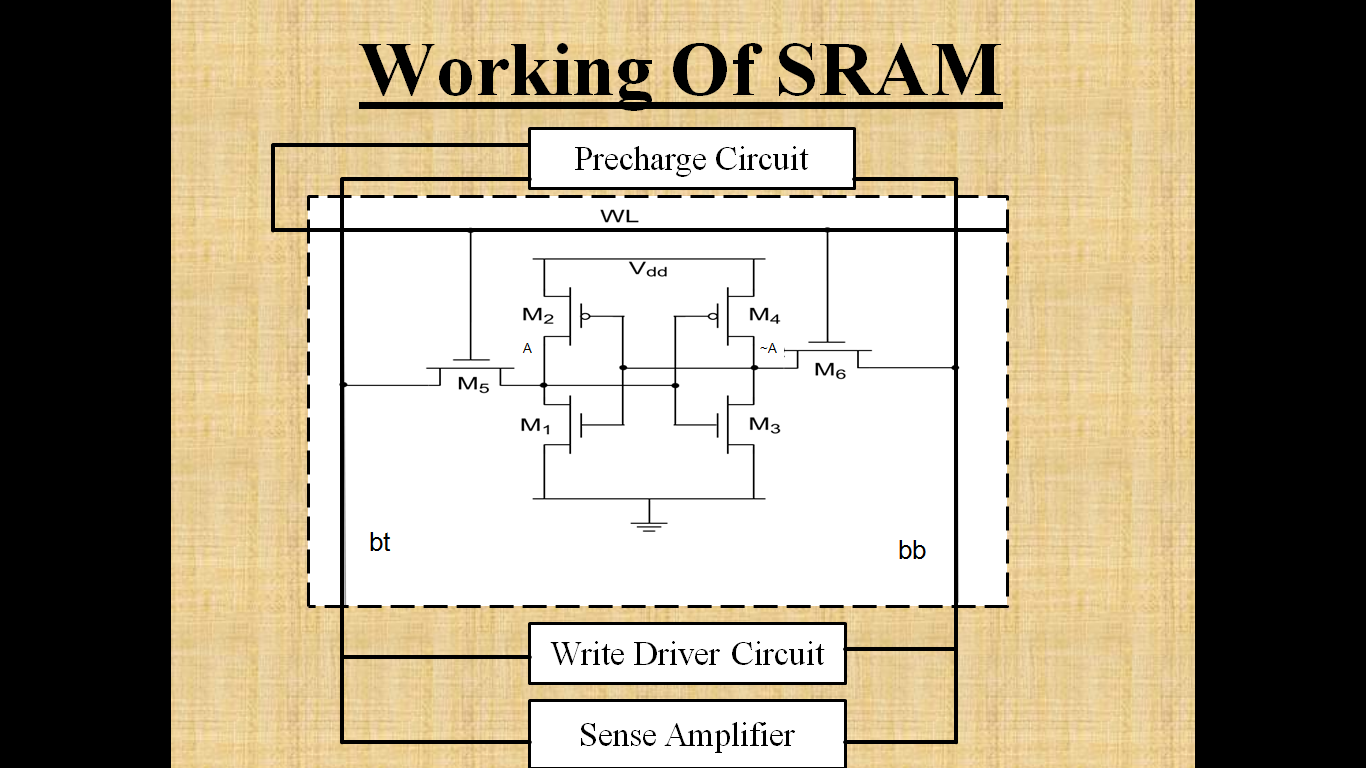
With movement from one technology generation to the next technology generation, the leakage power component is increasing and as it is known that in 70 nanometer technology, the leakage power dissipation has overtaken the dynamic power. Since the leakage power is becoming a large component of total power dissipation and it is also observable from the studies that more than 50 percent. And also another important issue is runtime leakage power, earlier the leakage power was minimized only when the circuit was not in the standby mode, because in the active condition, the percentage of leakage power was insignificant compared to dynamic power. So, at runtime people were primarily considering the reduction of dynamic power, but now that is not so, that is why the reduction of stand by leakage power i.e. the leakage current has become important.

1. **Design Circuitries**
   1. **SRAM**
      1. **Introduction**

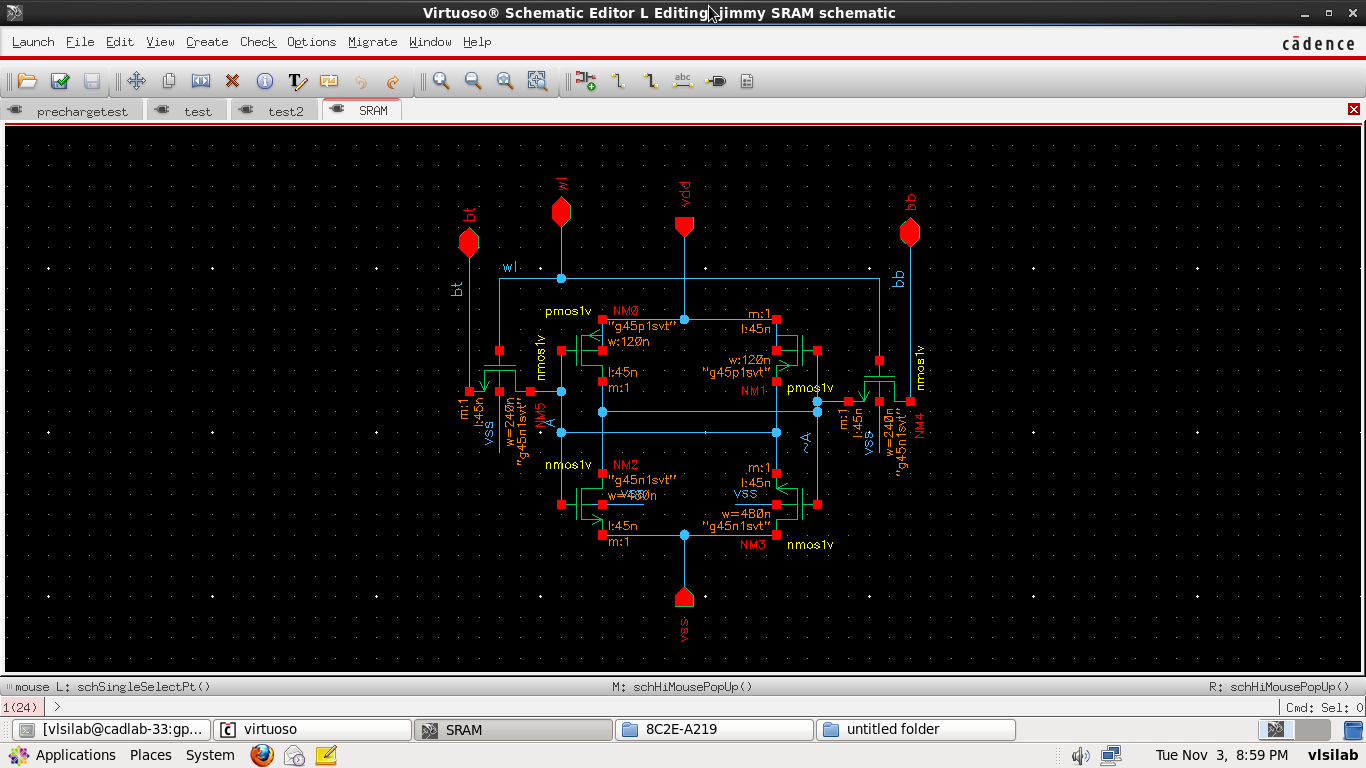
Static random-access memory (SRAM or static RAM) is a type of semiconductor memory that uses bistable latching circuitry to store each bit. The term static differentiates it from dynamic RAM (DRAM) which must be periodically refreshed. SRAM exhibits data remanence, but it is still volatile in the conventional sense that data is eventually lost when the memory is not powered. The term ``random access'' means that in an array of SRAM cells each cell can be read or written in any order, no matter which cell was last accessed.

* + 1. **Structure**

The structure of a 6 transistor SRAM cell, storing one bit of information, can be seen in Figure2.1 The core of the cell is formed by two CMOS inverters, where the output potential of each inverter ‘q’ is fed as input into the other ‘~A’. This feedback loop stabilizes the inverters to their respective state.



**Figure:2.1**



**Figure:2.2**

The access transistors and the word and bit lines, WL and Bit, are used to read and write from or to the cell. In standby mode the word line is low, turning the access transistors off. In this state the inverters are in complementary state. When the p-channel MOSFET of the left inverter is turned on, the potential ‘A’ is high and the p-channel MOSFET of inverter two is turned off, ‘~A’ is low.

* + 1. **Operation**
       1. **READ Mode**

Consider a data read operation, shown in Figure 2.2 assuming that logic '0' is stored in the cell. The transistors M2 and M5 are turned off, while the transistors M1 and M6 operate in linear mode. Thus internal node voltages are V1 = 0 and V2 = VDD before the cell access transistors are turned on. After the pass transistors M3 and M4 are turned on by the row selection circuitry, the voltage at node A will not change any significant variation since no current flows through M4. On the other hand M1 and M3 will conduct a nonzero current and the voltage level of ~A will begin to drop slightly. The node voltage V1 will increase from its initial value of '0'V. The node voltage V1 may exceed the threshold voltage of M2 during this process, forcing an unintended change of the stored state. Therefore voltage must not exceed the threshold voltage of M2, so the transistor M2 remains turned off during read phase, i.e.,

V1max≤Vt2

The transistor M3 is in saturation whereas M1 is linear, equating the current equations

→βn3 (VDD-V1-VTN)2 = βn1 (2(VDD-VTN) V1-V12)

→βn3/βn1= (W/L)3 /(W/L)1≤(2VTN)(VDD-1.5VTN)/(VDD-2VTN)2

**Figure:2.3**

* + - 1. **WRITE mode**

Consider the write '0' operation assuming that logic '1' is stored in the SRAM cell initially. The transistors M1 and M6 are turned off, while M2 and M5 are operating in the linear mode. Thus the internal node voltage V1 = VDD and V2 = 0 before the access transistors are turned on. The column voltage Vb is forced to '0' by the write circuitry. Once M3 and M4 are turned on, we expect the nodal voltage V2 to remain below the threshold voltage of M1, since M2 and M4 are designed. The voltage at node 2 would not be sufficient to turn on M1. To change the stored information, i.e., to force V1 = 0 and V2 = VDD, the node voltage V1 must be reduced below the threshold voltage of M2, so that M2 turns off. When V1-VTN >0 then the transistor M3 operates in linear region while M5 operates in saturation region. Equating their current equations we get

→βp5(0-VDD-VTP)2=βn3(2(VDD-VTN)V1-V12)

**Figure:2.4(a)**

Rearranging the condition of in the result we get

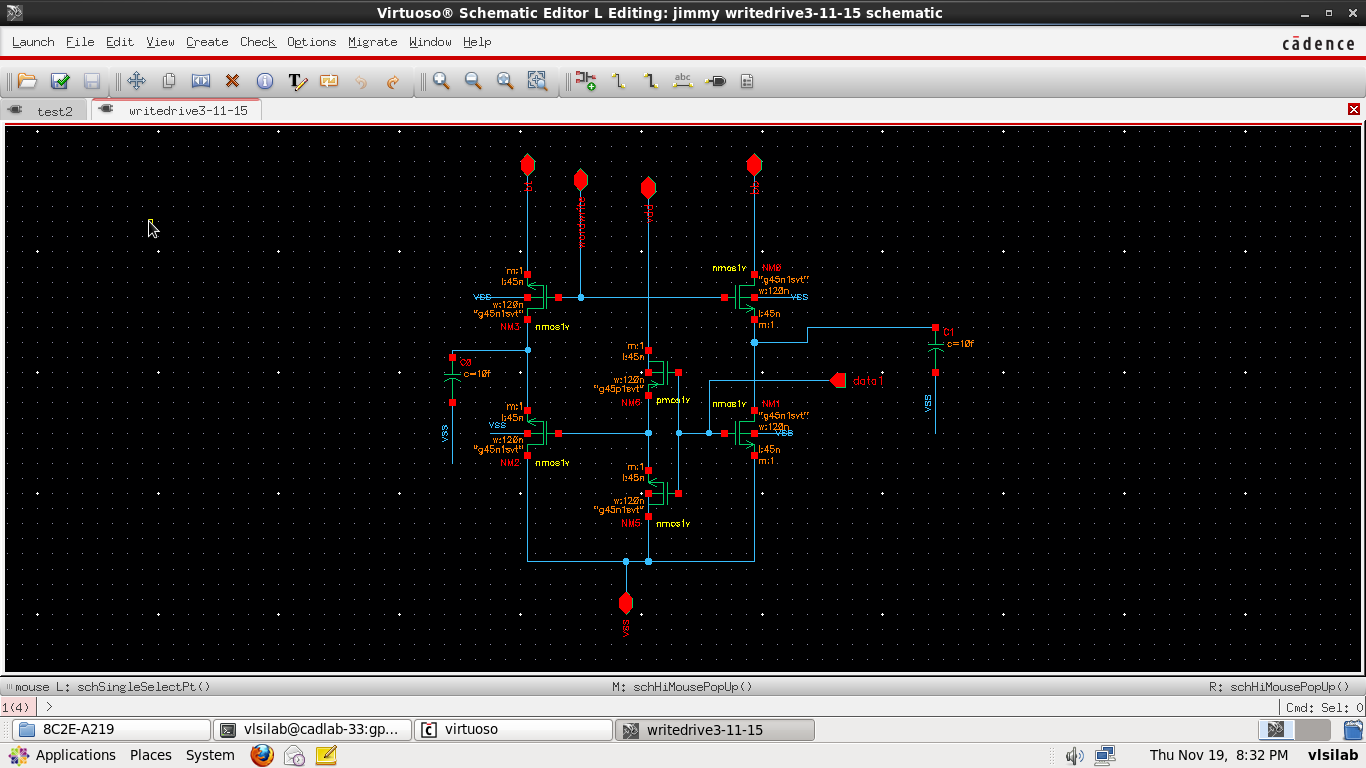
βp5 μp (W/L)5 ≤2(VDD-1.5VTN) VTN

βn3 μn (W/L)3 2(VDD-VTP)

**Figure:2.4(b)**

* 1. **WRITE Circuit**

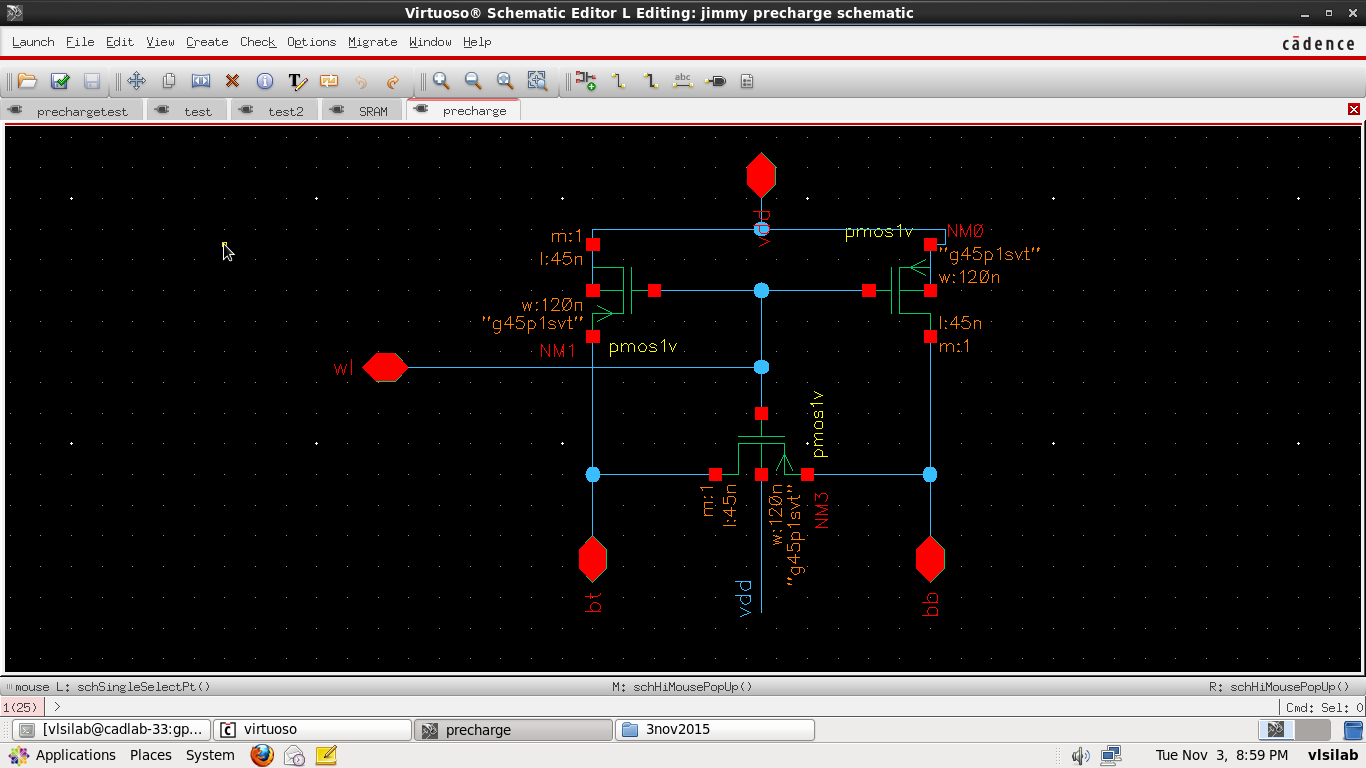
The principle of write circuit is to assert voltage of one of the columns to a low level. This can be achieved by connecting either or to ground through transistor M3 and either of M2 or M1. The transistor M3 is driven by the column decoder selecting the specified column. The transistor M1 is on only in the presence of the write enable signal and when the data bit to be written is '0'. The transistor M2 is on only in the presence of the write signal and when the data bit to be written is '1'. The circuit for write operation is shown in figure 2.5



**Figure:2.5**

* 1. **Precharge Circuit:**

bt and bb lines have capacitances of the order of femto farads; due to which they would lose their potential with time in standby mode and hence cell might become inefficient. So to sustain voltage in standby mode, an additional circuitry is applied to charge the lines. The design of such circuitry is as shown in figure2.6, during run time mode, the circuit is kept off by the PMOS transistors.



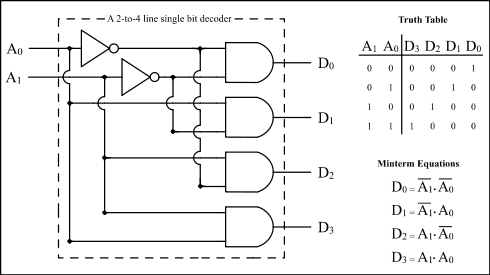
**Figure:2.6**

* 1. **Other circuits:**
     1. **Sense amplifiers:**

Sense amplifier is part of the read circuitry that is used when data is read from the memory; its role is to sense the low power signals from a bit line that represents a data bit (1 or 0) stored in a memory cell, and amplify the small voltage swing to recognizable logic levels so the data can be interpreted properly by logic outside the memory. There is one sense amplifier for each column of memory cells, so there are usually hundreds or thousands of identical sense amplifiers on a modern memory chip. As such, sense amplifiers are one of the only analog circuits in a computer's memory sub-system. To read a bit from a particular memory cell, the word line along the cell's row is turned on, activating all the cells in the row. The stored value (Logic 0 or 1) from the cell then comes to the Bit-lines associated with it. The sense amplifier at the end of the two complimentary bit-lines amplifies the small voltages to a normal logic level. The bit from the desired cell is then latched from the cell's sense amplifier into a buffer, and put on the output bus.

* + 1. **Decoders:**

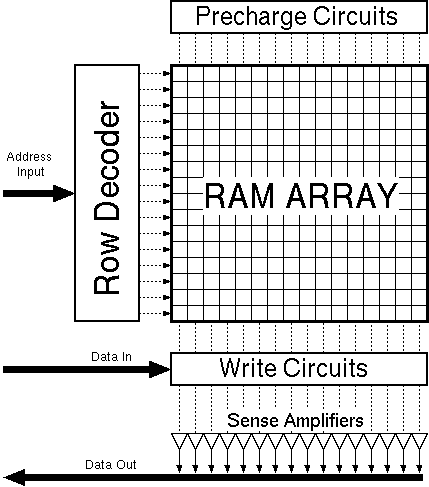
To select a particular bit cell from the array of cells, there is need of two decoders referred as row decoder (to select a particular word line) and column decoder (to select a particular bit line and bb line).



**Figure:2.7**

1. **Array Architecture of SRAM**

As shown in figure3.1, data can be read and write from any cell in the array architecture randomly.



**Figure:3.1**

1. **Leakage Currents and its Reduction**

In electronics, leakage may refer to a gradual loss of energy from a charged capacitor. It is primarily caused by electronic devices attached to the capacitors, such as transistors or diodes, which conduct a small amount of current even when they are turned off. Even though this off current is an order of magnitude less than the current through the device when it is on, the current still slowly discharges the capacitor. Another contributor to leakage from a capacitor is from the undesired imperfection of some dielectric materials used in capacitors, also known as dielectric leakage. It is a result of the dielectric material not being a perfect insulator and having some non-zero conductivity, allowing a leakage current to flow, slowly discharging the capacitor [1][3][5].

We describe six short-channel leakage mechanisms where

1. I1 is the reverse-bias PN junction leakage
2. I2 is the Subthreshold leakage
3. I3 is the oxide tunneling current
4. I4 is the gate current due to hot-carrier injection
5. I5 is the GIDL
6. I6 is the channel punch through current

* Currents I2, I5, and I6 are off-state leakage mechanisms,
* I1 and I3 occur in both ON and OFF states.
* I4 can occur in the off state, but more typically occurs during the transistor bias states in transition.
  1. **Types of Leakage Currents**
     1. **PN Junction Reverse-Bias Current**

Drain and source to well junctions are typically reverse biased, causing PN junction leakage current. A reverse-bias PN junction leakage I1 has two main components: one is minority carrier diffusion/drift near the edge of the depletion region; the other is due to electron-hole pair generation in the depletion region of the reverse-biased junction. For an MOS transistor, additional leakage can occur between the drain and well junction from gated diode device action (overlap of the gate to the drain-well PN junctions) or carrier generation in drain to well depletion regions with influence of the gate on these current components. PN junction reverse- bias leakage current is a function of junction area and doping concentration. If both n and p regions are heavily doped (this is the case for advanced MOSFETs using heavily doped shallow junctions and halo doping for better SCE), band-to-band tunneling (BTBT) dominates the PN junction leakage.

* + 1. **Subthreshold Leakage**

Subthreshold or weak inversion conduction current between source and drain in an MOS transistor occurs when gate voltage is below Vth. In the weak inversion, the minority carrier concentration is small, but not zero. Let us consider that the source of the n-channel MOSFET is grounded, Vg<Vth, and the drain to source voltage is Vds ≥0.1 V. For such weak inversion condition, Vds drops almost entirely across the reverse-biased substrate-drain PN junction.

As a result, the variation of the electrostatic potential ФS at the semiconductor surface along the channel (the Y axis) is small. The component of the electric field vector E(EY), being equal to ∂Ф/∂y, is also small. With both the number of mobile carriers and the longitudinal electric field small, the drift component of the subthreshold drain-to-source current is negligible. Therefore, unlike the strong inversion region in which the drift current dominates, the subthreshold conduction is dominated by the diffusion current. The carriers move by diffusion along the surface similar to charge transport across the base of bipolar transistors. The exponential relation between driving voltage on the gate and the drain current is a straight line in a semi log plot of ID versus Vg. Weak inversion typically dominates modern device off-state leakage due to the low Vth.

Where

**Figure:4.1**

Where Vth is the threshold voltage, and VT =KT/q is the thermal voltage. Cox is the gate oxide capacitance; u0 is the zero bias mobility; and m is the subthreshold swing coefficient (also called body effect coefficient). Wdm is the maximum depletion layer width, and tox is the gate oxide thickness. Cdm is the capacitance of the depletion layer. In long-channel devices, the subthreshold current is independent of the drain voltage for Vds larger than a few VT. On the other hand, the dependence on the gate voltage is exponential. The inverse of the slope of the log10(Ids) versus Vgs characteristic is called the subthreshold slope (St) and is given by

**Figure:4.2**

Subthreshold slope indicates how effectively the transistor can be turned off (rate of decrease of) when is decreased below. As device dimensions and the supply voltage are scaled down to enhance performance, power efficiency, and reliability, subthreshold characteristics may limit the scalability of the supply voltage. The parameter St is measured in mill volts per decade of the drain current. For the limiting case of tox→0 and at room temperature, St ═60 mV/decade. Typical values for a bulk CMOS process can range from 70 to 120 mV/decade. A low value for subthreshold slope is desirable. It can be noted from the preceding expression that can be made smaller by using a thinner oxide (insulator) layer to reduce or a lower substrate doping concentration (resulting in larger). Changes in operating conditions namely, lower temperature or a substrate bias also modifies St.

* + 1. **Tunneling into and Through Gate Oxide**

Reduction of gate oxide thickness results in an increase in the field across the oxide. The high electric field coupled with low oxide thickness results in tunneling of electrons from substrate to gate and also from gate to substrate through the gate oxide, resulting in the gate oxide tunneling current. To understand the phenomenon of tunneling, let us consider an MOS capacitor with a heavily doped n+-type polysilicon gate and a p-type substrate. Also, for simplicity, let us now focus only on the electron tunneling. When a positive bias is applied to the gate, the energy-band diagram changes. Due to the small oxide thickness, which results in a small width of the potential barrier, the electrons at the strongly inverted surface can tunnel into or through the SiO2 layer and hence give rise to the gate current. On the other hand, if a negative gate bias is applied, electrons from the n+ polysilicon can tunnel into or through the oxide layer and give rise to the gate current.

* + 1. **Injection of Hot Carriers from Substrate to Gate Oxide**

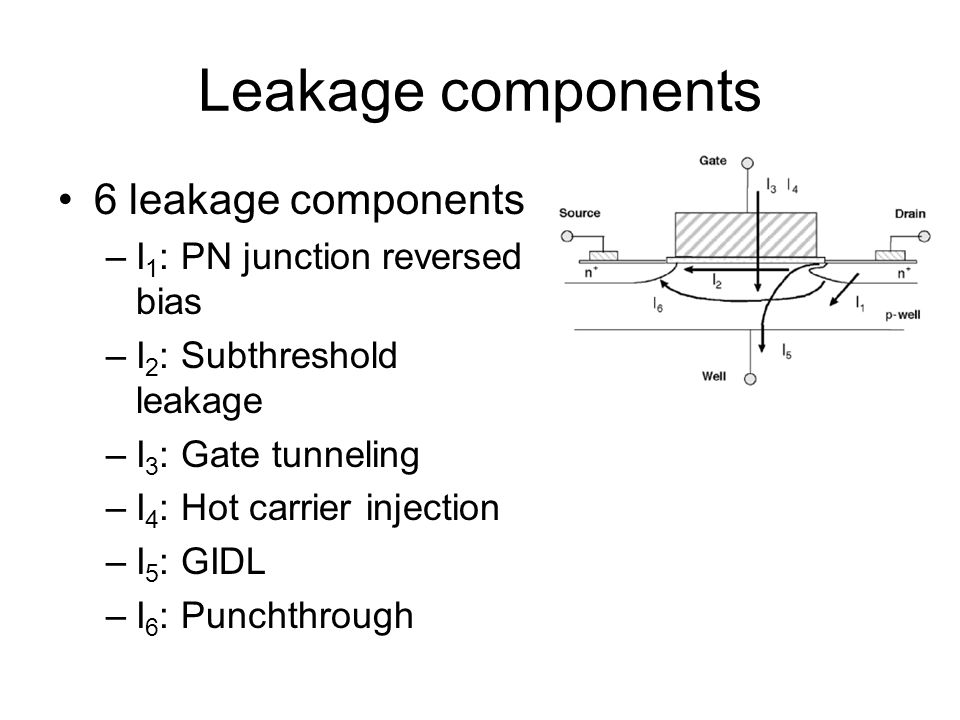
In a short-channel transistor, due to high electric field near the Si–SiO2 interface, electrons or holes can gain sufficient energy from the electric field to cross the interface potential barrier and enter into the oxide layer. This effect is known as hot-carrier injection. The injection from Si to SiO2 is more likely for electrons than holes, as electrons have a lower effective mass than that of holes, and the barrier height for holes (4.5 eV) is more than that for electrons (3.1 eV).

* + 1. **Gate-Induced Drain Leakage(GIDL)**

GIDL is due to high field effect in the drain junction of an MOS transistor. When the gate is biased to form an accumulation layer at the silicon surface, the silicon surface under the gate has almost same potential as the p-type substrate. Due to presence of accumulated holes at the surface, the surface behaves like a p region more heavily doped than the substrate. This causes the depletion layer at the surface to be much narrower than elsewhere. The narrowing of the depletion layer at or near the surface causes field crowding or an increase in the local electric field, thereby enhancing the high field effects near that region. When the negative gate bias is large (i.e., gate at zero or negative and drain at VDD), the n+ drain region under the gate can be depleted and even inverted. This causes more field crowding and peak field increase, resulting in a dramatic increase of high field effects such as avalanche multiplication and BTBT. The possibility of tunneling via near-surface traps also increases. As a result of all these effects, minority carriers are emitted in the drain region underneath the gate. Since the substrate is at a lower potential for minority carriers, the minority carriers that have been accumulated or formed at the drain depletion region underneath the gate are swept laterally to the substrate, completing a path for the GIDL. Thinner oxide thickness and higher VDD (higher potential between gate and drain) enhance the electric field and therefore increase GIDL. The impact of drain and well doping on GIDL is rather complicated. At low drain doping, the electric field is not high enough to cause tunneling. At very high drain doping, the depletion width—and, therefore, the tunneling volume—are limited, causing less GIDL. Hence, GIDL is worse for moderate drain doping (in between the extremes previously mentioned), where both the electric field and depletion width (tunneling volume) are considerable. Very high and abrupt drain doping is preferred for minimizing GIDL, as it provides lower series resistance required for high transistor drive current.

* + 1. **Punch through**

In short-channel devices, due to the proximity of the drain and the source, the depletion regions at the drain-substrate and source-substrate junctions extend into the channel. As the channel length is reduced, if the doping is kept constant, the separation between the depletion region boundaries decreases. An increase in the reverse bias across the junctions (with increase in Vds) also pushes the junctions nearer to each other. When the combination of channel length and reverse bias leads to the merging of the depletion regions, punch through is said to have occurred. In submicrometer MOSFETs, a Vth adjust implant is used to have a higher doping at the surface than that in the bulk. This causes a greater expansion of the depletion region below the surface (due to smaller doping there) as compared to the surface. Thus, the punch through occurs below the surface. An increase in the drain voltage beyond the value required to establish the punch through lowers the potential barrier for the majority carriers in the source. Thus, more of these carriers across the energy barrier and enter into the substrate, and the drain collects some of them. The net effect is an increase in the subthreshold current. Furthermore, punch through degrades the subthreshold slope. The device parameter commonly used to characterize the punch through is the punch through voltage VPT , which estimates the value of Vds for which the punch through occurs (i.e., the subthreshold current reaches a particular value) at Vgs=0. It is roughly estimated as the value of the Vds for which the sum of the widths of the drain and source depletion regions is equal to effective channel length where NB is the doping concentration at the bulk; L is the channel length; and Wj is the junction width. The most suitable method for controlling the punch through is to use additional implants. A layer of higher doping at a depth equal to that of the bottom of the junction depletion regions is one possible solution. Another approach could be to form a halo implant at the leading edges of the drain and source junctions.



**Figure:4.3**

* 1. **Leakage Reduction Approaches**

Leakage reduction can be done either at run time i.e. When data is either reading or writing in a particular cell or at stand by time i.e. When the SRAM cell is in ideal mode(no operation is done). According to which, there are many ways of reducing leakages in a SRAM cell.

* + 1. **Run time leakage reduction**

The primary contributor to power dissipation in CMOS circuits has been the charging and discharging of load capacitances, often referred to as the dynamic power dissipation. This component of power dissipation is quadratically proportional to the supply voltage level.

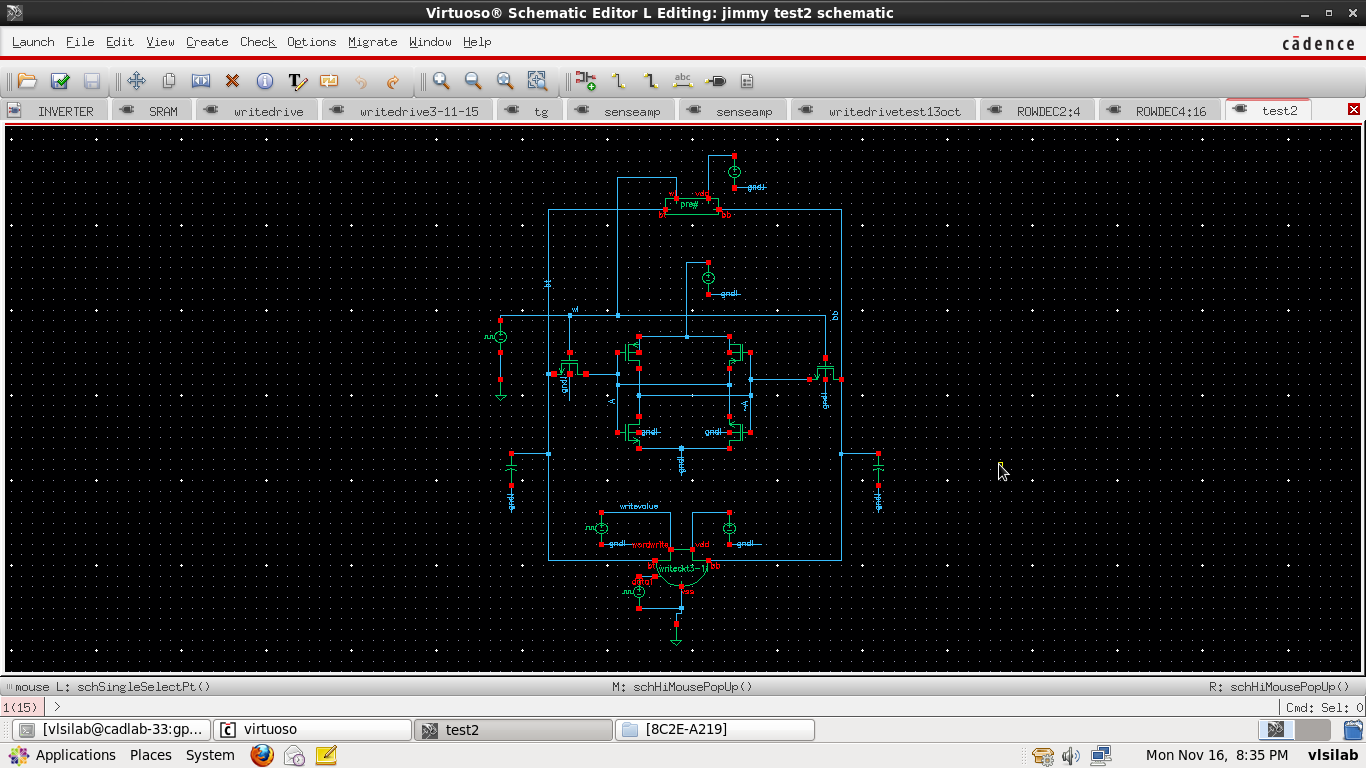
Therefore, in the past, chip designers have relied on scaling down the supply voltage to reduce the dynamic power dissipation. Maintaining the transistor switching speeds requires a proportionate Downscaling of the transistor’s threshold voltages in lock step with the supply voltage reduction. However, threshold voltage scaling results in a significant amount of leakage power dissipation due to an exponential increase in the sub-threshold leakage current conduction.

* + 1. **Standby time leakage reduction**

The leakage power component further is comprised of stand-by and active leakage currents. Most microelectronic circuits remain for considerable amount of time in static state. Therefore, low power design approach should also include stand-by leakage power reduction in static CMOS circuits. Stand-by leakage power dissipation dominates the dynamic power dissipation in deep sub-micron circuits and also in circuits that remain in idle mode for long time such as mobile phones, laptops etc.

1. **Implementations**

We started our project with designing of single SRAM cell and its peripheral devices including precharge circuit and write drive circuit; so the designed circuit is as shown in figure5.1

****

**Figure:5.1**

Output includes bt, bb, wl, writevalue, data, A, ~A. In the circuit (figure5.1), at the top there is a precharge circuit which charges the bt and bb line whenever the wl line is low. And in the middle there is an SRAM circuit designed with following specifications:

W/L of PMOS inverter transistors=120nm

W/L of NMOS access transistors=180nm

W/L of NMOS inverter transistors=270nm

And at the bottom, there is a write drive circuit which writes in the evaluation phase in the SRAM cell or remains off. On and Off is controlled by the writevalue pulse whereas the value which is to be written is supported by the data line.

The pulses provided to various lines is described as

wl line pulse => T= 50 nanoseconds => duty cycle = 25%

writvalue line pulse => T= 100 nanoseconds => duty cycle = 50%

data line pulse => T= 200 nanoseconds => duty cycle =100%

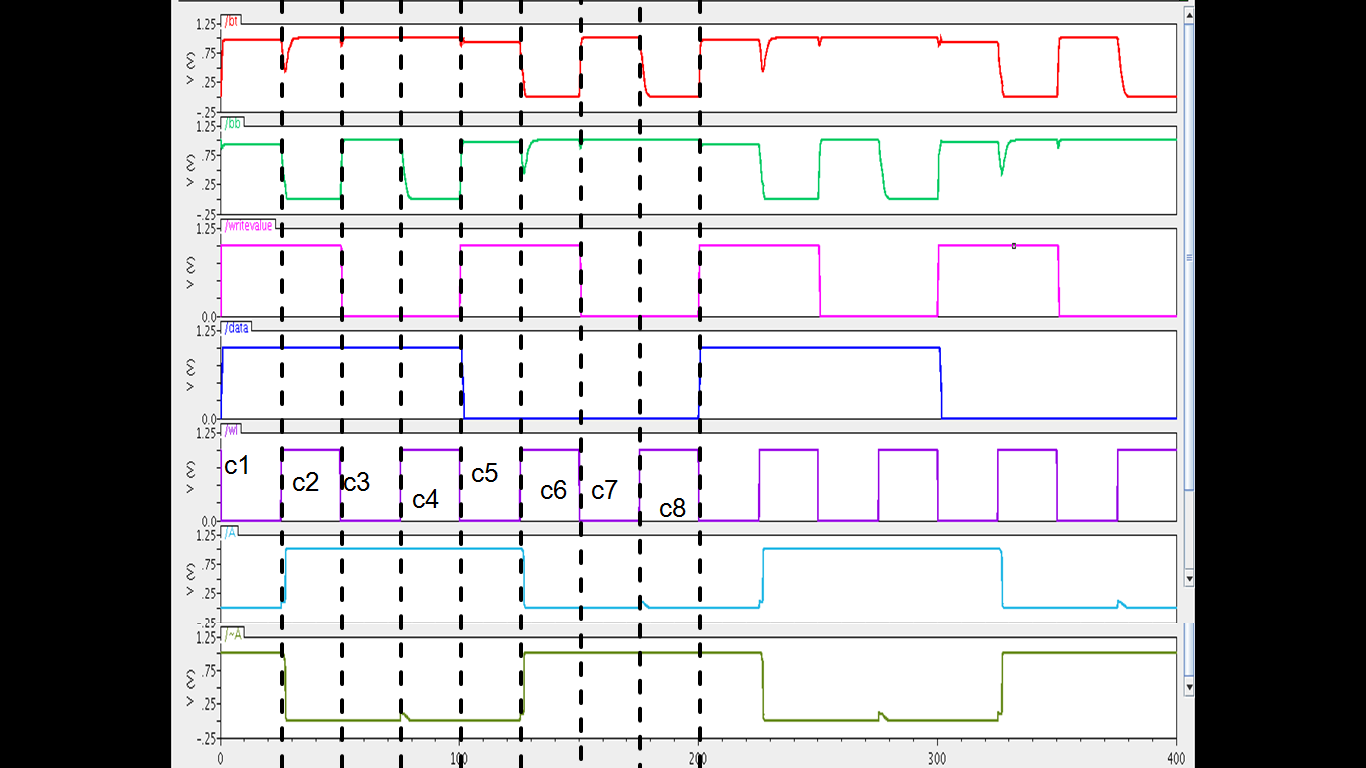
**Explanation of output**

The total output is of 400 nanoseconds in which we are writing ‘1’ and ‘0’ both two times each and then read the value simultaneously.

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Cycle number** | **Type** | **wl** | **writevalue** | **data** | **bt** | **bb** | **A** | **~A** |
| c1 | precharge cycle | 0 | 1 | 1 | 1 | 0 | 1 | 0 |
| c2 | write ‘1’ cycle | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| c3 | precharge cycle | 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| c4 | read ‘1’ cycle | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| c5 | precharge cycle | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| c6 | write ‘0’ cycle | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| c7 | precharge cycle | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| c8 | read ‘0’ cycle | 1 | 0 | 0 | 1 | 1 | 1 | 1 |

**Table:5.2**

After 200 nanoseconds; cycles c1 to c8 are repeated again in same order till 400 nanoseconds.

****

**Figure:5.3**

1. **Conclusions**

As shown in figure:5.1, table:5.2 and figure:5.3; the circuit for working of single 6 transistor SRAM cell is designed and the outputs thus found have also verified the objective but there are gliches in plot of bt and bb at certain positions due to transitions of various clock pulses. The reason for the gliches is the presence of parasitic capacitances (100fF cap at bt and bb) which was applied to model the practical scenario. Since the actual capacitance value can’t be realized thus gliches are of such high values but with full custom design, the gliches will surely be reduced.

1. **Future Work to be done**
2. Study of various figure of merits and how to apply on tool
3. Full custom design of single SRAM cell
4. Array architectural design of SRAM cells
5. Leakage schemes for single cell as well as for array of cells.
6. Design of those schemes on tool

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**APPENDIX**

1. **Cadence Virtuoso Analog Design Environment**

Cadence Design Systems, Inc (NASDAQ: CDNS) is an American electronic design automation (EDA) software and engineering services company, founded in 1988 by the merger of SDA Systems and ECAD, Inc. The company produces software and hardware for designing integrated circuits, Systems on Chip (SOC) and printed circuit boards.

Virtuoso Platform - Tools for designing full-custom integrated circuits includes schematic entry, behavioral modeling (Verilog-AMS), circuit simulation, custom layout, physical verification, extraction and back-annotation used mainly for analog, mixed-signal, RF, and standard-cell designs, but also memory and FPGA designs. Cadence design tools are used in a variety of undergraduate and graduate classes to provide practical experience in the design of integrated circuits and systems. Additionally, they are used by several research groups in the design of chips integrating analog, digital, RF and MEMS circuitry, with foundry fabrication through europractice, lfoundry, MOSIS, Samsung, ST Microelectronics, towerjazz, and UMC.

1. **Terminlogies Used**

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| **Serial No.** | **Terms** | **Description** |
|  | ~A node | Complementary value node of SRAM cell |
|  | A node | Actual value node of SRAM cell |
|  | bb line | Bit line present at left side of SRAM cell connected through access transistor to actual value node(~A) |
|  | bt line | Bit line present at left side of SRAM cell connected through access transistor to actual value node(A) |
|  | data line | Value written in cell by write driver circuit |
|  | Ids | Drain current; current associated to single MOSFET |
|  | k | Boltzmann constant |
|  | T | Temperature |
|  | Vds | Drain to substrate bias voltage |
|  | Vgs | Gate to substrate voltage |
|  | Vth | Threshold voltage |
|  | wl line | Pulse voltage as clock to SRAM cell |
|  | writevalue line | Pulse voltage for controlling write driver circuit’s switching |