

GPU Implementation of Data-Aided Equalizers

Jeffrey T. Ravert

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Master of Science

Michael D. Rice, Chair
Brian D. Jeffs
Brian A. Mazzeo

Department of Electrical and Computer Engineering

Brigham Young University

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ABSTRACT

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Multipath is one of the dominant causes for link loss in aeronautical telemetry. Equalizers have been studied to combat multipath interference in aeronautical telemetry. Blind Constant Modulus Algorithm (CMA) equalizers are currently being used on SOQPSK-TG. The Preamble Assisted Equalization (PAQ) has been funded by the Air Force to study data-aided equalizers on SOQPSK-TG. PAQ compares side by side no equalization, data-aided zero forcing equalization, data-aided MMSE equalization, data-aided initialized CMA equalization, data-aided frequency domain equalization, and blind CMA equalization. A real time experimental test setup has been assembled including an RF receiver for data acquisition, FPGA for hardware interfacing and buffering, GPUs for signal processing, spectrum analyzer for viewing multipath events, and an 8 channel bit error rate tester to compare equalization performance. Lab tests were done with channel and noise emulators. Flight tests were conducted in March 2016 and June 2016 at Edwards Air Force Base to test the equalizers on live signals. The test setup achieved a 10Mbps throughput with a 6 second delay. Counter intuitive to the simulation results, the flight tests at Edwards AFB in March and June showed blind equalization is superior to data-aided equalization. Lab tests revealed some types of multipath caused timing loops in the RF receiver to produce garbage samples. Data-aided equalizers based on data-aided channel estimation leads to high bit error rates. A new experimental setup is been proposed, replacing the RF receiver with a RF data acquisition card. The data acquisition card will always provide good samples because the card has no timing loops, regardless of severe multipath.

Keywords: MISSING

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Students may use the acknowledgments page to express appreciation for the committee members, friends, or family who provided assistance in research, writing, or technical aspects of the dissertation, thesis, or selected project. Acknowledgments should be simple and in good taste.

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Chapter 1

Introduction

1.1 Multipath in Aeronautical Telemetry

Multipath interference is one of the dominant causes for link loss in aeronautical telemetry. Strong multipath interference occurs in aeronautical telemetry when the transmitted signal is received from multiple paths because a test article is in a low elevation angle scenario as shown in Figure 1.1. Receivers use equalizers to combat multipath but often the transmitted information can not be recovered. Equalizers have been studied to combat multipath interference in aeronautical telemetry [1, 2].

There are two types of equalizers, blind and data-aided. Blind equalizers combat multipath using known properties of the transmitted signal but no knowledge of the data or multipath channel. Data-aided equalizers require knowing something about the received signal. One method of providing data that can be used in data-aided equalization is for the transmitter to periodically insert a known bit sequence called a “pilot” into the data stream. The receiver compares the received signal with a locally stored copy to estimate parameters such as multipath channels, frequency offsets, phase offsets and noise variance. Data-aided equalizers are finite impulse response filters (FIR). The impulse response of the FIR filters are computed based on the estimated parameters to better mitigate multipath.

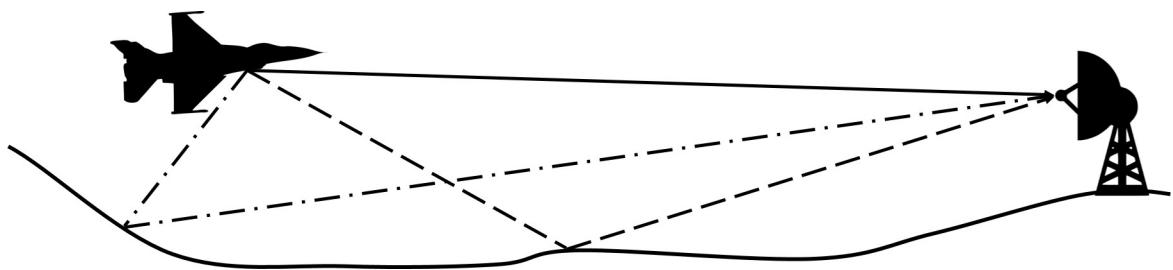


Figure 1.1: Multipath can occur when a signal is received multiple paths like line-of-sight or ground bounce or reflections.

1.2 Preamble Assisted Equalization Project

Data-aided equalization in aeronautical telemetry has been studied and tested by the Preamble Assisted Equalization (PAQ) project [3]. The PAQ project built a TRL 6 system that compares five data-aided equalizers to blind equalization and no equalization [4]. Bit error statistics were used as the figure of merit for the equalization algorithms. Live flight tests were conducted at Edwards AFB in March and June 2016. The five data-aided equalizers the PAQ project studied are

- zero-forcing (ZF) equalizer
- minimum mean square Error (MMSE) equalizer
- MMSE initialized constant modulus algorithm (CMA) equalizer
- frequency domain equalizer one (FDE1)
- frequency domain equalizer Two (FDE2).

Hardware

A block diagram of the PAQ project physical system is shown in Figure 1.2. A picture of the physical components is shown in Figure 1.3. The major components, and their functions are summarized in the following.

- The **T/M mixer** down-converts from L or C band RF to IF (70 MHz) then applies an anti-aliasing filter.
- The **rack mounted server** is a high powered computer that houses an ADC, a FPGA and three GPUs slotted into a 32 pin PCIe bus.
- The **ADC** produces 14-bit samples of the real-valued bandpass signal centered at IF sampled at $931/3$ Msamples/s. The samples are transferred to the host CPU via the PCIe bus.
- The **host CPU** initiates memory transfers between itself and the ADC, GPUs and FPGA via the PCIe bus. The host CPU also launches the digital signal processing algorithms on the GPUs.

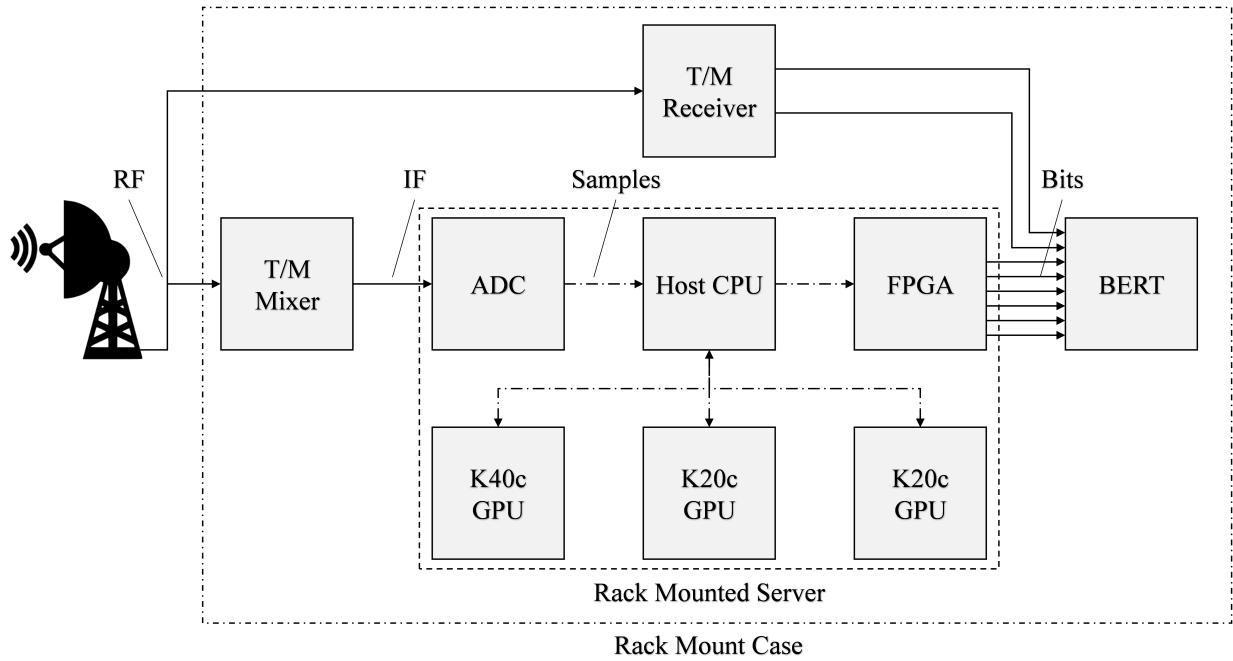


Figure 1.2: A block diagram of the physical PAQ project hardware. The components inside the rack mounted server are in the dashed box. All the components in the dashed and dotted box are housed in a rack mounted case.

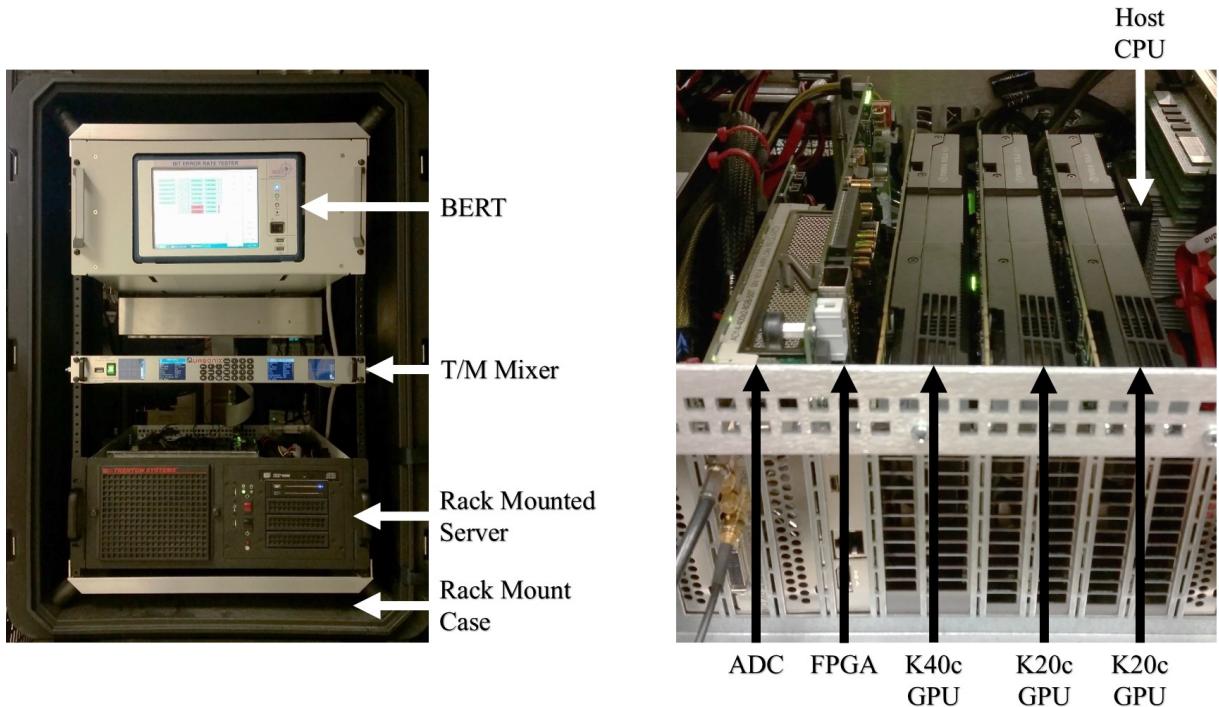


Figure 1.3: A picture of the physical PAQ project hardware. Right: Components in the dashed and dotted box from Figure 1.2. Left: Components in dashed box in Figure 1.2. Note that the T/M Receiver is not pictured.

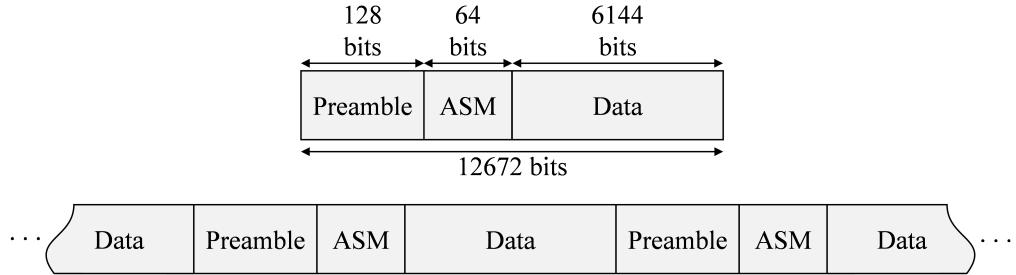


Figure 1.4: A diagram showing the PAQ packetized sample structure.

- The three **GPUs** are where all the detection, estimation, equalization and demodulation resides. While the CPU has one to eight powerful processors, GPUs have thousands of small less powerful processors that work in parallel. The signal processing is done in GPUs rather than FPGAs or a CPU because programming GPUs is faster and easier than programming FPGAs and CPUs do not possess the required processing power.
- The **FPGA** receives all the bit streams from the host CPU via the PCIe bus then clocks each stream out in parallel to the BERT for BER testing.
- The bit error rate tester (**BERT**) counts the errors in each input bit stream by comparing the streams to a PN sequence.
- The **T/M Receiver** outputs bit streams for blind equalization and no equalization for BER comparison.

To enable data-aided equalization, the PAQ project bit stream has a packetized structure shown in Figure 1.4. The bit stream has a pilot bit sequence, in the form of the iNET preamble and ASM, periodically inserted into the data bits. The iNET preamble comprises eight repetitions of the 16-bit sequence $CD98_{\text{hex}}$ and the ASM field is

$$034776C7272895B0_{\text{hex}}. \quad (1.1)$$

The data payload is a known length- $(2^{11} - 1)$ PN sequence. Each packet contains 128 preamble bits, 64 ASM bits and 6,144 data bits making each iNET packet 6,336 bits. The data bits modulate

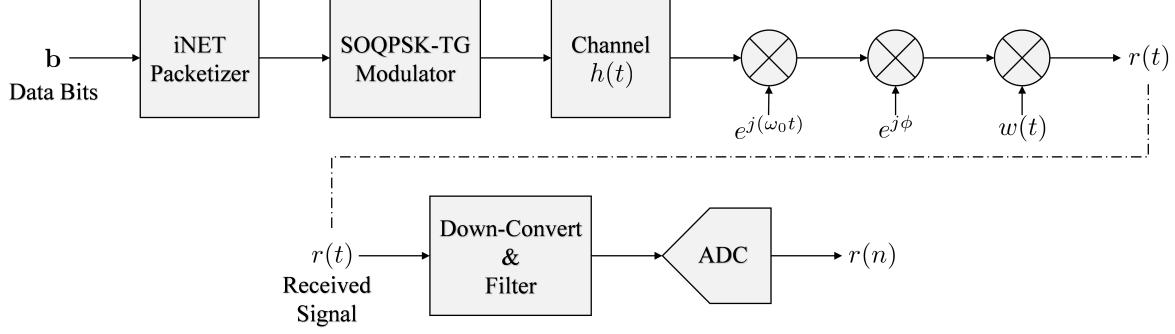


Figure 1.5: Received signal has multipath interference, frequency offset, phase offset and additive white Gaussian noise. The received signal is down-converted filtered and sampled to produce the sample sequence $r(n)$.

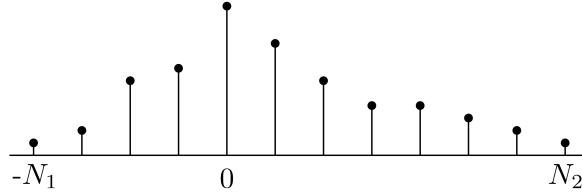


Figure 1.6: An illustration of the discrete-time channel of length $N_1 + N_2 + 1$ with a non-causal component comprising N_1 samples and a causal component comprising N_2 samples.

a SOQPSK-TG carrier at 10 Mbits/second. With the preamble and ASM periodically inserted, the over the air bit rate is 10.3125 Mbits/second.

After modulation, the transmitted signal experiences multipath interference modeled as the channel $h(t)$. The transmitted signal also experiences a frequency offset ω_0 , a phase offset ϕ and additive white Gaussian noise $w(t)$. The received signal is down-converted, filtered in the T/M mixer, sampled at $93^{1/3}$ Msamples/second by the ADC then down-converted again to baseband and resampled by $99/448$ in the GPUs resulting in the sampled sequence $r(n)$ at rate 20.625 Msamples/second or 2 samples/bit.

The model of the received signal is shown in Figure 1.5. At baseband and 2 samples/bit, the FIR channel impulse response is assumed to have a non-causal component comprising N_1 samples and a causal component comprising N_2 samples. Figure 1.6 shows the full discrete-time $L_h = N_1 + N_2 + 1$ sample channel. The received signal is sampled at 20.625M samples. The iNET packet is $L_{\text{pkt}} = 12672$ samples long with the preamble $L_p = 256$ samples and the ASM $L_{\text{ASM}} = 128$ samples.

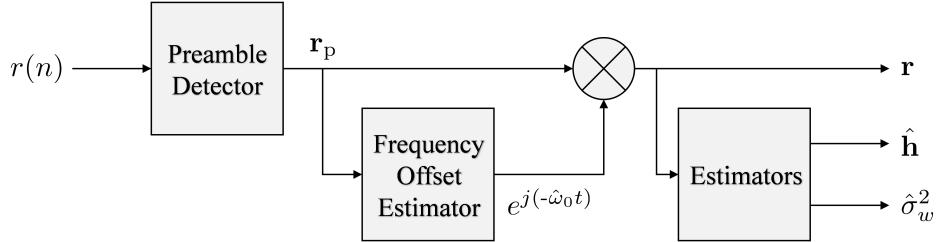


Figure 1.7: A block diagram of the estimators in the PAQ project.

Digital Signal Processing

A high-level digital signal processing flow is shown in Figure 1.7 and 1.8. Because the frequency offset, channel, and noise variance are estimated using the preamble and ASM, the first step is to find the samples correlating to the preamble in the received sample sequence $r(n)$. The preamble detector block correlates received samples with L_P samples of a locally stored copy of the pilot in (1.2). The preamble detector block outputs the vector of samples \mathbf{r}_p with the iNET packetized structure. The first $L_P + L_{ASM}$ samples in \mathbf{r}_p correlate with the received pilot samples.

$$\mathbf{p} = [p(0) \quad p(1) \quad \cdots \quad p(L_P + L_{ASM} - 1)] \quad (1.2)$$

The located preamble samples are used first to estimate the frequency offset. The estimated frequency offset $\hat{\omega}_0$ rads/sample is then used to “de-rotate” the vector of samples \mathbf{r}_p to produce \mathbf{r} . The de-rotated samples in the vector \mathbf{r} that correlate to the preamble and ASM are used to estimate the channel $\hat{\mathbf{h}}$ and noise variance $\hat{\sigma}_w^2$. The channel and noise variance estimates are done in the estimators block.

Equipped with knowledge of the estimated channel and noise variance, data-aided finite impulse response (FIR) equalizer filters can be computed. All the data-aided equalizer filters are computed using the same channel and noise variance estimates. The blocks shown in Figure 1.8 are duplicated in five independent branches producing five estimated vectors of bits $\hat{\mathbf{b}}$, one for each equalizer.

The PAQ project designed the data-aided FIR equalizer filters to be 5 times longer than the channel estimate. The equalizer filter has a non-causal component comprising $L_1 = 5N_1 = 60$

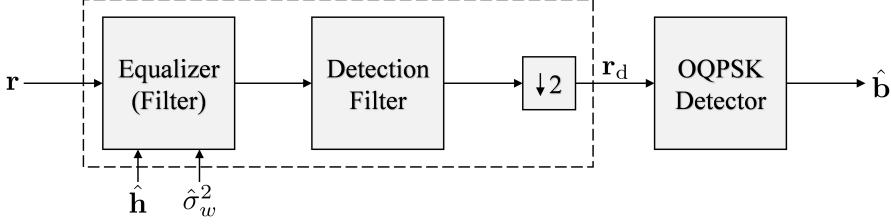


Figure 1.8: A block diagram of application of the FIR equalizer and detection filters in the Preamble Assisted Equalization (PAQ) project.

samples and a causal component comprising $L_2 = 5N_2 = 125$ samples. The $L_{\text{EQ}} = L_1 + L_2 + 1$ sample full discrete-time equalizer filters are computed and applied in the equalizer filter block.

The output of the equalizer filters are then filtered by a SOQPSK-TG detection filter and down-sampled by 2 in preparation for an OQPSK detector. The r_d in each equalizer branch has a sample rate of 1 sample/bit or 2 samples/symbol. The OQPSK detector block outputs the vector of estimated bits \hat{b} . Finally the BER for each equalizer is obtained by comparing the vectors of estimated bits \hat{b} to the PN sequence.

The GPUs in Figure 1.2 and 1.3 perform all the digital signal processing in parallel. To introduce as much parallelism as possible, the received samples are processed in 39,321,600 sample sets. At 20.625 Msamples/second, each set of 39,321,600 samples is 1907 milliseconds worth of data. Each set has at most 3104 independent 12672 sample iNET packets. The GPU processes 3104 packets in parallel by leveraging batched processing. Each packet is a batch and each batch performs the algorithms shown in Figures 1.7 and 1.8.

This thesis, will illustrate how the five PAQ data-aided equalizers were computed and applied to the received samples in GPUs. The dashed box in Figure 1.8 emphasizes which processing blocks are focused on.

Chapter 2 shows the equations for these block diagrams. Chapter 3 will shed some light on signal processing in GPUs. Chapter 4 will illustrate how the five equalizers are implemented in GPUs. Chapter 5 will summarize.

Chapter 2

PAQ Equations

This thesis studies GPU implementation of the PAQ project data-aided FIR equalizer filters. The impulse response of the FIR equalizer filters are computed using channel and noise variance estimates based on the iNET preamble and ASM in the received signal. All the estimates are data-aided and thus require finding the preamble and the ASM in the received signal. A preamble detector is employed to estimate the start of each iNET packet in the set. Figure 1.7 shows a block diagram of the estimators in the PAQ project. The data-aided FIR equalizer filters are then computed and the received samples are equalized. With the received samples equalized, a detection filter is applied and the symbols are estimated using a OQPSK detector. Figure 1.8 shows a block diagram of the FIR filters and symbol detector in the PAQ project.

The estimators, detection filter and OQPSK detector will be briefly explained in Section 2.1. Section 2.2 will explain the equations for the FIR equalizer filters and the application of the equalizers and detection filter.

2.1 Estimators

2.1.1 Preamble Detection

To compute data-aided equalizers, preambles in the received signal are found then used to estimate parameters. The goal of the preamble detection step is to structure the received samples $r(n)$ into L_{pkt} sample packets \mathbf{r}_p . Each vector of samples \mathbf{r}_p has the structure shown in Figure 1.4.

Before the structuring the received samples into packets, the preambles are found using the preamble detector explained in [5]. The preamble detector computes the function $L(n)$ for each sample in the set. Peaks in $L(n)$ identify the locations of a preamble or the start of a packet. The

function $L(n)$ is given by

$$L(n) = \sum_{m=0}^7 [I^2(n, m) + Q^2(n, m)] \quad (2.1)$$

where

$$\begin{aligned} I(n, m) \approx & \sum_{\ell \in \mathcal{L}_1} r_R(\ell + 32m + n) - \sum_{\ell \in \mathcal{L}_2} r_R(\ell + 32m + n) + \sum_{\ell \in \mathcal{L}_3} r_I(\ell + 32m + n) - \sum_{\ell \in \mathcal{L}_4} r_I(\ell + 32m + n) \\ & + 0.7071 \left[\sum_{\ell \in \mathcal{L}_5} r_R(\ell + 32m + n) - \sum_{\ell \in \mathcal{L}_6} r_R(\ell + 32m + n) \right. \\ & \quad \left. + \sum_{\ell \in \mathcal{L}_7} r_I(\ell + 32m + n) - \sum_{\ell \in \mathcal{L}_8} r_I(\ell + 32m + n) \right], \end{aligned} \quad (2.2)$$

and

$$\begin{aligned} Q(n, m) \approx & \sum_{\ell \in \mathcal{L}_1} r_I(\ell + 32m + n) - \sum_{\ell \in \mathcal{L}_2} r_I(\ell + 32m + n) \\ & - \sum_{\ell \in \mathcal{L}_3} r_R(\ell + 32m + n) + \sum_{\ell \in \mathcal{L}_4} r_R(\ell + 32m + n) \\ & + 0.7071 \left[\sum_{\ell \in \mathcal{L}_5} r_I(\ell + 32m + n) - \sum_{\ell \in \mathcal{L}_6} r_I(\ell + 32m + n) \right. \\ & \quad \left. - \sum_{\ell \in \mathcal{L}_7} r_R(\ell + 32m + n) + \sum_{\ell \in \mathcal{L}_8} r_R(\ell + 32m + n) \right] \end{aligned} \quad (2.3)$$

with

$$\begin{aligned}
\mathcal{L}_1 &= \{0, 8, 16, 24\} \\
\mathcal{L}_2 &= \{4, 20\} \\
\mathcal{L}_3 &= \{2, 10, 14, 22\} \\
\mathcal{L}_4 &= \{6, 18, 26, 30\} \\
\mathcal{L}_5 &= \{1, 7, 9, 15, 17, 23, 25, 31\} \\
\mathcal{L}_6 &= \{3, 5, 11, 12, 13, 19, 21, 27, 28, 29\} \\
\mathcal{L}_7 &= \{1, 3, 9, 11, 12, 13, 15, 21, 23\} \\
\mathcal{L}_8 &= \{5, 7, 17, 19, 25, 27, 28, 29, 31\}.
\end{aligned} \tag{2.4}$$

A correlation peak in $L(n)$ indicates the index n is the start of a preamble. The vector of packet samples starting at index n are

$$\mathbf{r}_p = \begin{bmatrix} r(n) \\ \vdots \\ r(n + L_{\text{pkt}} - 1) \end{bmatrix} = \begin{bmatrix} r_p(0) \\ \vdots \\ r_p(L_{\text{pkt}} - 1) \end{bmatrix} \tag{2.5}$$

2.1.2 Frequency Offset Compensation

The frequency offset estimator shown in Figure 1.7 is the estimator taken from [6, eq. (24)]. With the notation adjusted slightly, the frequency offset estimate is

$$\hat{\omega}_0 = \frac{1}{L_q} \arg \left\{ \sum_{n=i+2L_q}^{i+7L_q-1} r_p(n)r_p^*(n-L_q) \right\} \quad \text{for } i = 1, 2, 3, 4, 5. \tag{2.6}$$

The frequency offset is estimated for every packet or each vector of samples \mathbf{r}_p in the set. Frequency offset compensation is performed by de-rotating the received samples by $-\hat{\omega}_0$:

$$r(n) = r_p(n)e^{-j\hat{\omega}_0 n}. \tag{2.7}$$

Equations (2.6) and (2.7) are easily implemented into GPUs.

2.1.3 Channel Estimation

The channel estimator is the ML estimator taken from [2, eq. 8].

$$\hat{\mathbf{h}} = \underbrace{(\mathbf{X}^\dagger \mathbf{X})^{-1} \mathbf{X}^\dagger}_{\mathbf{X}_{\text{lpi}}} \mathbf{r} \quad (2.8)$$

where

$$\mathbf{X} = \begin{bmatrix} p(N_2) & & & \\ \vdots & p(N_2) & & \\ p(L_p + L_{\text{ASM}} - N_1) & \vdots & \ddots & \\ & p(L_p + L_{\text{ASM}} - N_1) & & p(N_2) \\ & & \vdots & \\ & & & p(L_p + L_{\text{ASM}} - N_1) \end{bmatrix} \quad (2.9)$$

is a $(L_p + L_{\text{ASM}} - N_1 - N_2) \times (N_1 + N_2 + 1)$ convolution matrix formed from the ideal preamble and ASM samples. The $(N_1 + N_2 + 1) \times (L_p + L_{\text{ASM}} - N_1 - N_2)$ matrix \mathbf{X}_{lpi} is the left pseudo-inverse of \mathbf{X} . The ML channel estimator is the result of the matrix operation

$$\hat{\mathbf{h}} = \mathbf{X}_{\text{lpi}} \mathbf{r}. \quad (2.10)$$

The matrix operation $\mathbf{X}_{\text{lpi}} \mathbf{r}$ is implemented simply and efficiently in GPUs.

2.1.4 Noise Variance Estimation

The noise variance estimator is also taken from [2, eq. 9]

$$\hat{\sigma}_w^2 = \frac{1}{2\rho} \left| \mathbf{r} - \mathbf{X} \hat{\mathbf{h}} \right|^2 \quad (2.11)$$

where

$$\rho = \text{Trace} \left\{ \mathbf{I} - \mathbf{X} (\mathbf{X}^\dagger \mathbf{X})^{-1} \mathbf{X}^\dagger \right\}. \quad (2.12)$$

Equation (2.11) is easily implemented into GPUs.

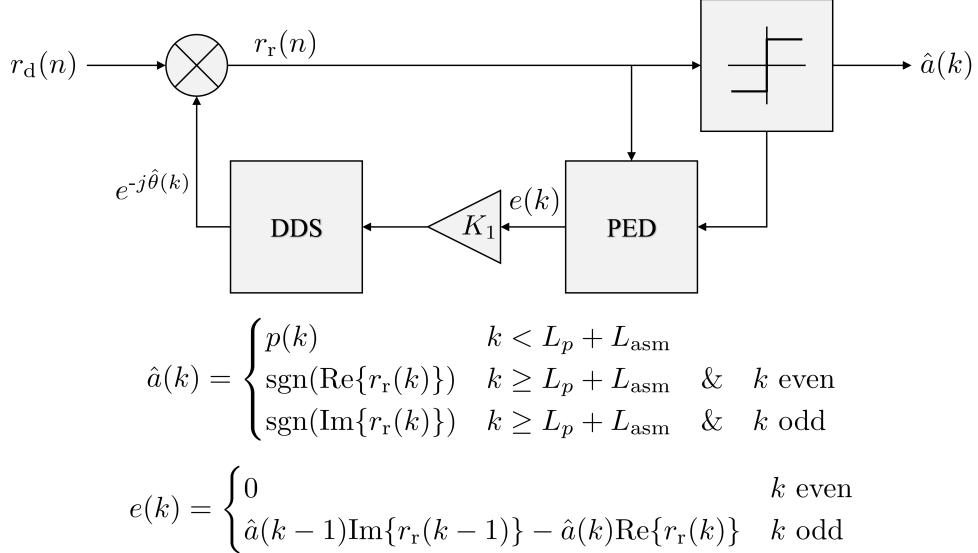


Figure 2.1: Offset Quadrature Phase Shift Keying symbol by symbol detector.

2.1.5 Symbol-by-Symbol Detector

Symbol-by-symbol detection comprises a detection filter and a phase lock loop (PLL) to track out the residual frequency offset. Before the symbols are detected, the equalized samples are passed through the detection filter then down-sampled by 2. The detection filter is a “numerically optimized” SOQPSK detection filter H_{NO} [7, Fig. 3]. The symbol-by-symbol detector block in Figure 1.8 is a Offset Quaternary Phase Shift Keying (OQPSK) detector. Using the simple OQPSK detector in place of a complex MLSE SOQPSK-TG detector leads to less than 1 dB loss in detection efficiency [7].

A Phase Lock Loop (PLL) is needed in the OQPSK detector to track out residual frequency offset. The residual frequency offset results from a frequency offset estimation error. While phase offset, timing offset and multipath are combated with equalizers, batched based equalizers cannot remove residual frequency offset. The PLL tracks out the residual frequency offset using a feedback control loop.

Implementing a PLL may not seem feasible in GPUs because the feedback loop cannot be parallelized. But the PAQ system processes 3104 batches of data at a time by parallelizing on a packet by packet basis. Running the PLL and detector serially through a full packet of samples

is relatively fast because each iteration requires only 10 floating point operations and a few logic decisions.

2.2 Equalizers

This thesis examines that performance and GPU implementation of five FIR equalizer filters. While the performance and GPU implementation is interesting, this thesis makes no claim of theoretically expanding understanding of equalizers. The data-aided equalizers studied in this thesis are:

- zero-forcing (ZF) equalizer
- minimum mean square Error (MMSE) equalizer
- MMSE initialized constant modulus algorithm (CMA) equalizer
- frequency domain equalizer one (FDE1)
- frequency domain equalizer Two (FDE2).

The final equations for ZF and MMSE FIR equalizer filters are very similar but differ in formulation. The equations for FDE1 and FDE2 are also very similar but differ by one subtle difference. The CMA FIR equalizer filter is computed using a steepest decent algorithm initialized by MMSE. More CMA iterations lead to lower BER but ZF, MMSE, FDE1 and FDE2 only require one iteration. The equations explained in this section will be referenced heavily in Chapter 4.

2.2.1 Zero-Forcing and Minimum Mean Square Error Equalizers

The ZF and MMSE equalizers are treated together here because they have many common features. Both equalizers are found by solving linear equations

$$\mathbf{Ac} = \mathbf{b} \tag{2.13}$$

where \mathbf{c} is a vector of desired equalizer coefficients and the matrix \mathbf{A} and vector \mathbf{b} are known. It will be shown that the only difference between ZF and MMSE lies in the matrix \mathbf{A} .

Zero-Forcing

The ZF equalizer is an FIR filter defined by the coefficients

$$c_{\text{ZF}}(-L_1) \quad \cdots \quad c_{\text{ZF}}(0) \quad \cdots \quad c_{\text{ZF}}(L_2). \quad (2.14)$$

The filter coefficients are the solution to the matrix vector equation [8, eq. (311)]

$$\mathbf{c}_{\text{ZF}} = (\mathbf{H}^\dagger \mathbf{H})^{-1} \mathbf{H}^\dagger \mathbf{u}_{n_0} \quad (2.15)$$

where

$$\mathbf{c}_{\text{ZF}} = \begin{bmatrix} c_{\text{ZF}}(-L_1) \\ \vdots \\ c_{\text{ZF}}(0) \\ \vdots \\ c_{\text{ZF}}(L_2) \end{bmatrix}, \quad (2.16)$$

$$\mathbf{u}_{n_0} = \begin{bmatrix} 0 \\ \vdots \\ 0 \\ 1 \\ 0 \\ \vdots \\ 0 \end{bmatrix} \left. \right\} \begin{array}{l} n_0 - 1 \text{ zeros} \\ \\ \\ \\ \\ N_1 + N_2 + L_1 + L_2 - n_0 + 1 \text{ zeros} \end{array}, \quad (2.17)$$

where $n_0 = N_1 + L_1 + 1$ and

$$\mathbf{H} = \begin{bmatrix} \hat{h}(-N_1) & & & \\ \hat{h}(-N_1 + 1) & \hat{h}(-N_1) & & \\ \vdots & \vdots & \ddots & \\ \hat{h}(N_2) & \hat{h}(N_2 - 1) & \hat{h}(-N_1) & \\ & \hat{h}(N_2) & \hat{h}(-N_1 + 1) & \\ & & \vdots & \\ & & \hat{h}(N_2) & \end{bmatrix}. \quad (2.18)$$

Equation (2.15) can be implemented directly but there are many optimization that greatly reduce computation. The heaviest computation is the $\mathcal{O}(n^3)$ inverse operation followed by the $\mathcal{O}(n^2)$ matrix matrix multiplies. Rather than performing a heavy inverse, multiplying $\mathbf{H}^\dagger \mathbf{H}$ on both sides of equation (2.15) results in

$$\begin{aligned} \mathbf{H}^\dagger \mathbf{H} \mathbf{c}_{\text{ZF}} &= \mathbf{H}^\dagger \mathbf{u}_{n_0} \\ \mathbf{R}_{\hat{h}} \mathbf{c}_{\text{ZF}} &= \hat{\mathbf{h}}_{n_0} \end{aligned} \quad (2.19)$$

where

$$\mathbf{R}_{\hat{h}} = \mathbf{H}^\dagger \mathbf{H} = \begin{bmatrix} r_{\hat{h}}(0) & r_{\hat{h}}^*(1) & \cdots & r_{\hat{h}}^*(L_{eq} - 1) \\ r_{\hat{h}}(1) & r_{\hat{h}}(0) & \cdots & r_{\hat{h}}^*(L_{eq} - 2) \\ \vdots & \vdots & \ddots & \\ r_{\hat{h}}(L_{eq} - 1) & r_{\hat{h}}(L_{eq} - 2) & \cdots & r_{\hat{h}}(0) \end{bmatrix} \quad (2.20)$$

is the auto-correlation matrix of the channel estimate $\hat{\mathbf{h}}$ and

$$\hat{\mathbf{h}}_{n_0} = \mathbf{H}^\dagger \mathbf{u}_{n_0} = \begin{bmatrix} \hat{h}^*(L_1) \\ \vdots \\ \hat{h}^*(0) \\ \vdots \\ \hat{h}^*(-L_2) \end{bmatrix} \quad (2.21)$$

is a vector with the time reversed and conjugated channel estimate $\hat{\mathbf{h}}$ centered at n_0 . The channel estimate auto-correlation sequence is

$$r_{\hat{h}}(k) = \sum_{n=-N_1}^{N_2} \hat{h}(n)\hat{h}^*(n-k). \quad (2.22)$$

Note that the auto-correlation matrix $\mathbf{R}_{\hat{h}}$ is comprised of

$$\mathbf{r}_{\hat{h}} = \begin{bmatrix} r_{\hat{h}}(0) \\ \vdots \\ r_{\hat{h}}(L_{ch}) \\ r_{\hat{h}}(L_{ch} + 1) \\ \vdots \\ r_{\hat{h}}(L_{eq} - 1) \end{bmatrix} = \begin{bmatrix} r_{\hat{h}}(0) \\ \vdots \\ r_{\hat{h}}(L_{ch}) \\ 0 \\ \vdots \\ 0 \end{bmatrix}. \quad (2.23)$$

Using $\mathbf{r}_{\hat{h}}$ eliminates the need for matrix matrix multiply of $\mathbf{H}^\dagger \mathbf{H}$. Also, $r_{\hat{h}}(k)$ only has support on $-(L_{ch} - 1) \leq k \leq L_{ch} - 1$ making $\mathbf{R}_{\hat{h}}$ sparse or %63 zeros. NEEDS CHECKING!!!! The sparseness of $\mathbf{R}_{\hat{h}}$ can be leveraged to reduce computation drastically.

MMSE Equalizer

The MMSE equalizer is an FIR filter defined by the coefficients

$$c_{\text{MMSE}}(-L_1) \quad \cdots \quad c_{\text{MMSE}}(0) \quad \cdots \quad c_{\text{MMSE}}(L_2). \quad (2.24)$$

The filter coefficients are the solution to the matrix vector equation [8, eq. (330) and (333)]

$$\mathbf{c}_{\text{MMSE}} = [\mathbf{G}\mathbf{G}^\dagger + 2\hat{\sigma}_w^2 \mathbf{I}_{L_1+L_2+1}]^{-1} \mathbf{g}^\dagger \quad (2.25)$$

where $\mathbf{I}_{L_1+L_2+1}$ is the $(L_1 + L_2 + 1) \times (L_1 + L_2 + 1)$ identity matrix, $\hat{\sigma}_w^2$ is the estimated noise variance, \mathbf{G} is the $(L_1 + L_2 + 1) \times (N_1 + N_2 + L_1 + L_2 + 1)$ matrix given by

$$\mathbf{G} = \begin{bmatrix} \hat{h}(N_2) & \cdots & \hat{h}(-N_1) \\ & \ddots & \\ \hat{h}(N_2) & \cdots & \hat{h}(-N_1) \\ & \ddots & \\ & & \hat{h}(N_2) \end{bmatrix} \quad (2.26)$$

and \mathbf{g}^\dagger is the $(L_1 + L_2 + 1) \times 1$ vector given by

$$\mathbf{g}^\dagger = \hat{\mathbf{h}}_{n_0} = \begin{bmatrix} \hat{h}^*(L_1) \\ \vdots \\ \hat{h}^*(0) \\ \vdots \\ \hat{h}^*(-L_2) \end{bmatrix}. \quad (2.27)$$

Computing \mathbf{c}_{MMSE} can be simplified by noticing that $\mathbf{g}^\dagger = \hat{\mathbf{h}}_{n_0}$, $\mathbf{G}\mathbf{G}^\dagger = \mathbf{R}_{\hat{h}}$ in Equation (2.20). To further simplify MMSE, twice the estimated noise variance is added down the diagonal of the channel estimate auto-correlation matrix

$$\mathbf{R} = \mathbf{R}_{\hat{h}} + 2\hat{\sigma}_w^2 \mathbf{I}_{L_1+L_2+1} = \begin{bmatrix} r_h(0) + 2\hat{\sigma}_w^2 & r_h^*(1) & \cdots & r_h^*(L_{eq}-1) \\ r_h(1) & r_h(0) + 2\hat{\sigma}_w^2 & \cdots & r_h^*(L_{eq}-2) \\ \vdots & \vdots & \ddots & \\ r_h(L_{eq}-1) & r_h(L_{eq}-2) & \cdots & r_h(0) + 2\hat{\sigma}_w^2 \end{bmatrix}. \quad (2.28)$$

By placing Equation (2.28) and (2.27) into (2.25) results in

$$\mathbf{c}_{\text{MMSE}} = \mathbf{R}^{-1} \hat{\mathbf{h}}_{n_0}. \quad (2.29)$$

Solving for the MMSE equalizer coefficients \mathbf{c}_{MMSE} takes the form like the ZF equalizer coefficients in (2.19)

$$\mathbf{R}\mathbf{c}_{\text{MMSE}} = \hat{\mathbf{h}}_{n_0}. \quad (2.30)$$

The only difference between solving for the ZF and MMSE equalizer coefficients is \mathbf{R} and $\mathbf{R}_{\hat{h}}$. The MMSE equalizer coefficients \mathbf{c}_{MMSE} uses the noise variance estimate when building \mathbf{R} . The sparseness of \mathbf{R} can also be leveraged to reduce computation drastically because \mathbf{R} has the same sparse properties as $\mathbf{R}_{\hat{h}}$.

2.2.2 The Constant Modulus Algorithm

The b th CMA equalizer is an FIR filter defined by the coefficients

$$c_{\text{CMA}(b)}(-L_1) \quad \dots \quad c_{\text{CMA}(b)}(0) \quad \dots \quad c_{\text{CMA}(b)}(L_2). \quad (2.31)$$

The filter coefficients are calculated by a steepest decent algorithm

$$\mathbf{c}_{\text{CMA}(b+1)} = \mathbf{c}_{\text{CMA}(b)} - \mu \nabla J \quad (2.32)$$

initialized by the MMSE equalizer coefficients

$$\mathbf{c}_{\text{CMA}(0)} = \mathbf{c}_{\text{MMSE}}. \quad (2.33)$$

The vector \mathbf{J} is the cost function and ∇J is the cost function gradient [8, eq. (352)]

$$\nabla J = \frac{2}{L_{pkt}} \sum_{n=0}^{L_{pkt}-1} \left[y(n)y^*(n) - 1 \right] y(n)\mathbf{r}^*(n). \quad (2.34)$$

where

$$\mathbf{r}(n) = \begin{bmatrix} r(n + L_1) \\ \vdots \\ r(n) \\ \vdots \\ r(n - L_2) \end{bmatrix}. \quad (2.35)$$

This means ∇J is defined by

$$\nabla J = \begin{bmatrix} \nabla J(-L_1) \\ \vdots \\ \nabla J(0) \\ \vdots \\ \nabla J(L_2) \end{bmatrix}. \quad (2.36)$$

A DSP engineer could implement the steepest decent algorithm by computing the cost function gradient directly. The L_{pkt} sample summation for ∇J in (2.34) does not map well to GPUs. Chapter 3 will show how well convolution performs in GPUs. The computation for ∇J can be massaged and re-expressed as convolution.

To begin messaging ∇J , the term

$$z(n) = 2 \left[y(n)y^*(n) - 1 \right] y(n) \quad (2.37)$$

is defined to simplify the expression of ∇J to

$$\nabla J = \frac{1}{L_{pkt}} \sum_{n=0}^{L_{pkt}-1} z(n) \mathbf{r}^*(n). \quad (2.38)$$

Expanding the expression of ∇J into vector form

$$\nabla J = \frac{z(0)}{L_{pkt}} \begin{bmatrix} r^*(L_1) \\ \vdots \\ r^*(0) \\ \vdots \\ r^*(L_2) \end{bmatrix} + \frac{z(1)}{L_{pkt}} \begin{bmatrix} r^*(1+L_1) \\ \vdots \\ r^*(1) \\ \vdots \\ r^*(1-L_2) \end{bmatrix} + \dots + \frac{z(L_{pkt}-1)}{L_{pkt}} \begin{bmatrix} r^*(L_{pkt}-1+L_1) \\ \vdots \\ r^*(L_{pkt}-1) \\ \vdots \\ r^*(L_{pkt}-1-L_2) \end{bmatrix} \quad (2.39)$$

shows a pattern in $z(n)$ and $\mathbf{r}(n)$. The k th value of ∇J is

$$\nabla J(k) = \frac{1}{L_{pkt}} \sum_{m=0}^{L_{pkt}-1} z(m) r^*(m-k), \quad -L_1 \leq k \leq L_2. \quad (2.40)$$

The summation almost looks like a convolution accept the conjugate on the element $r(n)$. To put the summation into the familiar convolution form, define

$$\rho(n) = r^*(n). \quad (2.41)$$

Now

$$\nabla J(k) = \frac{1}{L_{\text{pkt}}} \sum_{m=0}^{L_{\text{pkt}}-1} z(m)\rho(k-m). \quad (2.42)$$

Note that $z(n)$ has support on $0 \leq n \leq L_{\text{pkt}} - 1$ and $\rho(n)$ has support on $-L_{\text{pkt}} + 1 \leq n \leq 0$, the long result of the convolution sum $b(n)$ has support on $-L_{\text{pkt}} + 1 \leq n \leq L_{\text{pkt}} - 1$. Putting all the pieces together, we have

$$\begin{aligned} b(n) &= \sum_{m=0}^{L_{\text{pkt}}-1} z(m)\rho(n-m) \\ &= \sum_{m=0}^{L_{\text{pkt}}-1} z(m)r^*(m-n) \end{aligned} \quad (2.43)$$

Comparing Equation (2.42) and (2.43) shows that

$$\nabla J(k) = \frac{1}{L_{\text{pkt}}} b(k), \quad -L_1 \leq k \leq L_2. \quad (2.44)$$

The values of interest are shown in Figure 2.2.2.

This suggest the following matlab code for computing computing the gradient vector ∇J and implementing CMA.

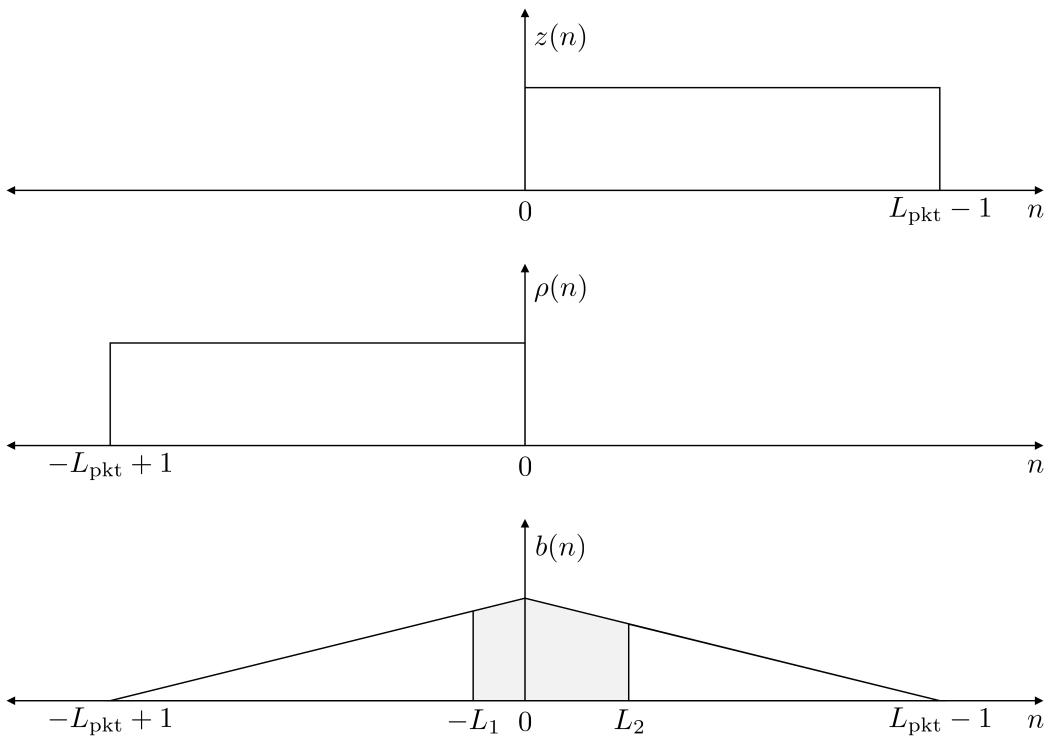


Figure 2.2: Diagram showing the relationships between $z(n)$, $\rho(n)$ and $b(n)$.

Table 2.1: CMA

```

1 c_CMA = c_MMSE;
2 for i = 1:its
3 yy = conv(r,c_CMAb);
4 y = yy(L1+1:end-L2); % trim yy
5 z = 2*(y.*conj(y)-1).*y;
6 Z = fft(z,Nfft);
7 R = fft(conj(r(end:-1:1)),Nfft)
8 b = ifft(Z.*R);
9 delJ = b(Lpkt-L1:Lpkt+L2);
10 c_CMAb1 = c_CMAb -mu*delJ;
11 c_CMAb = c_CMAb1;
12 end
13 yy = conv(r,c_CMA);
14 y = yy(L1+1:end-L2); % trim yy

```

2.2.3 The Frequency Domain Equalizers

Frequency Domain Equalizer One (FDE1) and Frequency Domain Equalizer Two (FDE2) are very similar and have the same structure. FDE1 and FDE2 are adapted from Williams and Saquib [9, eq. (11) and (12)].

Frequency Domain Equalizer One

FDE1 is the MMSE applied in the frequency domain from Williams' and Saquib's paper [9, eq. (11)].

$$C_{\text{FDE1}}(e^{j\omega_k}) = \frac{\hat{H}^*(e^{j\omega_k})}{|\hat{H}(e^{j\omega_k})|^2 + \frac{1}{\hat{\sigma}_w^2}} \quad \text{where } \omega_k = \frac{2\pi}{L} \text{ for } k = 0, 1, \dots, L-1. \quad (2.45)$$

The term $C_{\text{FDE1}}(e^{j\omega_k})$ is FDE1's frequency response at ω_k . The term $\hat{H}(e^{j\omega_k})$ is the channel estimate frequency response at ω_k . The term $\hat{\sigma}^2$ is the noise variance estimate, this term is completely independent of frequency because the noise is assumed to be spectrally flat or white.

Equation (2.45) is straight forward to implement in GPUs. FDE1 is extremely fast and computationally efficient.

Frequency Domain Equalizer Two

FDE2 is also the MMSE or Wiener filter applied in the frequency domain but knowledge of the SOQPSK-TG spectrum is leveraged [9, eq. (12)]. The frequency response of FDE2 is

$$C_{\text{FDE2}}(e^{j\omega_k}) = \frac{\hat{H}^*(e^{j\omega_k})}{|\hat{H}(e^{j\omega_k})|^2 + \frac{\Psi(e^{j\omega_k})}{\hat{\sigma}_w^2}} \quad \text{where } \omega_k = \frac{2\pi}{L} \text{ for } k = 0, 1, \dots, L-1 \quad (2.46)$$

where $\Psi(e^{j\omega_k})$ is the power spectral density of SOQPSK-TG shown in Figure 2.2.3. The term $\Psi(e^{j\omega_k})$ eliminates out of band multipath that may be challenging to estimate and overcome.

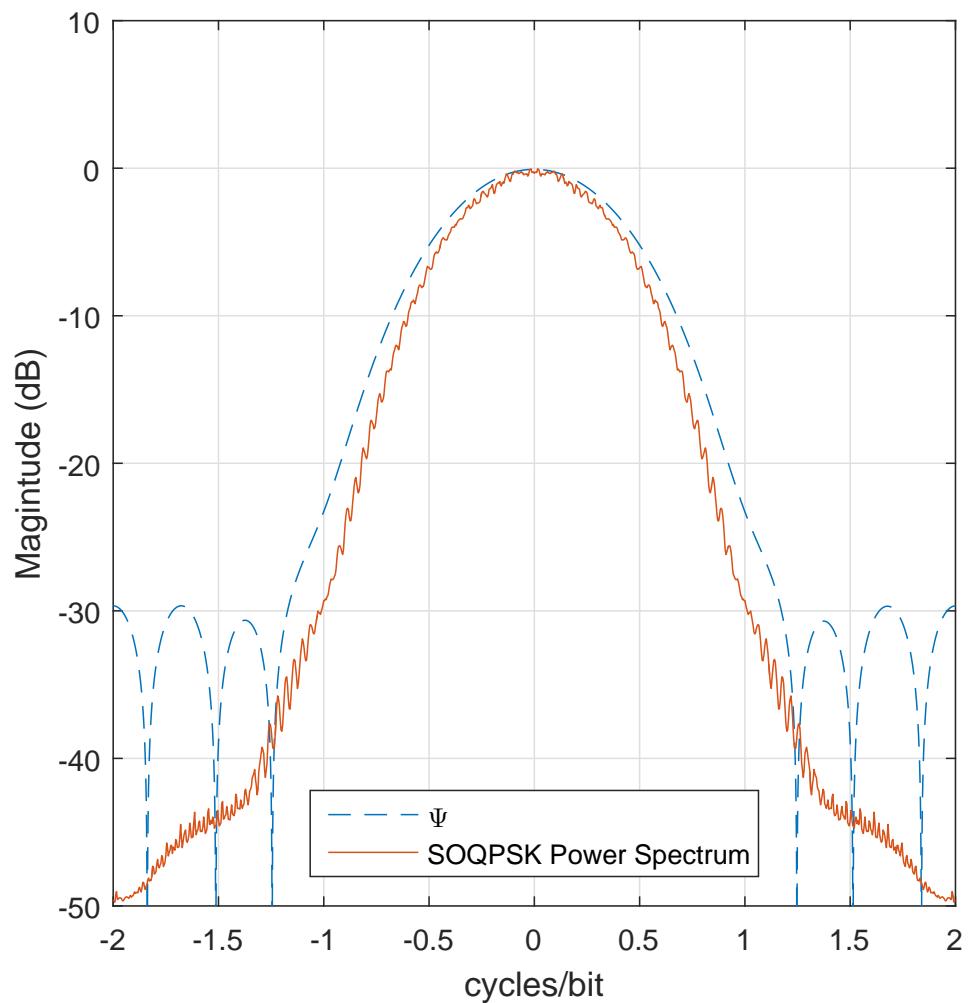


Figure 2.3: I need help on this one!!!!

Chapter 3

Signal Processing in GPUs

A Graphics Processing Unit (GPU) is a computational unit with a highly-parallel architecture well-suited for executing the same function on many data elements. In the past, GPUs were used to process graphics data but in 2008 NVIDIA released the Tesla GPU. Tesla GPUs are built for general purpose high performance computing. Figure 3.1 shows the form factor of a Tesla K40c and K20c. In 2007 NVIDIA released an extension to C, C++ and Fortran called CUDA (Compute Unified Device Architecture). CUDA enables GPUs to be used for high performance computing in computer vision, deep learning, artificial intelligence and signal processing [11]. CUDA allows a programmer to write C++ like functions that are massively parallel called *kernels*. To invoke parallelism, a GPU kernel executed N times with the work distributed to N_{\min} total *threads* that run concurrently. To achieve the full potential of high performance GPUs, kernels must be written with some basic concepts about GPU architecture and memory in mind.

This chapter will show optimizing memory access leads to faster execution time rather than optimizing number of floating point operations. Processing larger data sets leads to faster execution time per operation. The number of threads per block can majorly affect execution time. CPU and GPU work can be pipelined.

3.1 CPU verse CUDA example

If a programmer has some C++ experience, learning how to program GPUs using CUDA comes fairly easily. GPU code still runs top to bottom and memory still has to be allocated. The only real difference is the physical location of the memory and how functions run on GPUs. To run functions or kernels on GPUs, the memory must be copied from the host (CPU) to the device



Figure 3.1: NVIDIA Tesla K40c and K20c.

(GPU). Once the memory has been copied, parallel GPU kernels are called. After GPU kernel execution, results are usually copied back from the device (GPU) to the host (CPU).

Listing 3.1 shows a simple program that implements:

$$\begin{aligned} \mathbf{C}_1 &= \mathbf{A}_1 + \mathbf{B}_1 \\ \mathbf{C}_2 &= \mathbf{A}_2 + \mathbf{B}_2 \end{aligned} \tag{3.1}$$

where \mathbf{C}_1 is computed in the CPU and \mathbf{C}_2 is computed in the GPU. Line 42 the CPU computes \mathbf{C}_1 by summing elements of \mathbf{A}_1 and \mathbf{B}_1 together *sequentially*. Figure 3.2 shows how the CPU computes \mathbf{C}_1 sequentially.

The vector addition in the GPU takes a little more work. On lines 60 and 61 the vectors in host memory \mathbf{A}_1 and \mathbf{B}_1 are copied to device memory vectors \mathbf{A}_2 and \mathbf{B}_2 . The vector \mathbf{C}_2 is

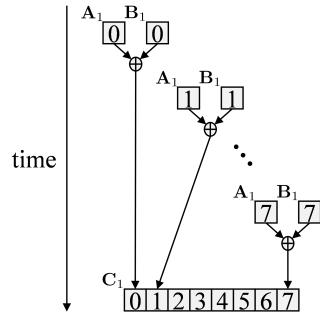


Figure 3.2: A block diagram of how a CPU sequentially performs vector addition.

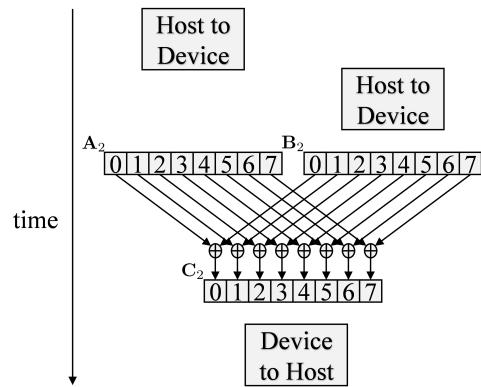


Figure 3.3: A block diagram of how a GPU performs vector addition in parallel.

computed by calling the GPU kernel `VecAddGPU` on line 75. The vector is then copied from device memory to host memory on line 78. Figure 3.3 shows how the GPU computes \mathbf{C}_2 *in parallel*.

Listing 3.1: Comparison of CPU verse GPU code.

```

1 #include <iostream>
2 #include <stdlib.h>
3 #include <math.h>
4 using namespace std;
5
6 void VecAddCPU(float* destination, float* source0, float* source1, int myLength) {
7     for(int i = 0; i < myLength; i++)
8         destination[i] = source0[i] + source1[i];
9 }
10
11 __global__ void VecAddGPU(float* destination, float* source0, float* source1, int lastThread) {
12     int i = blockIdx.x*blockDim.x + threadIdx.x;
13
14     // don't access elements out of bounds
15     if(i >= lastThread)
16         return;
17
18     destination[i] = source0[i] + source1[i];
19 }
20
21 int main(){
22     int N = pow(2,22);
23     cout << N << endl;
24     /**
25      * Vector Addition on CPU
26      */
27     // allocate memory on host
28     float *A1;
29     float *B1;
30     float *C1;
31     A1 = (float*) malloc (N*sizeof(float));
32     B1 = (float*) malloc (N*sizeof(float));
33     C1 = (float*) malloc (N*sizeof(float));
34
35     // Initialize vectors 0-99
36     for(int i = 0; i < N; i++){
37         A1[i] = rand()%100;
38         B1[i] = rand()%100;
39     }
40
41     // vector sum C1 = A1 + B1
42     VecAddCPU(C1, A1, B1, N);
43
44     /**
45      * Vector Addition on GPU
46      */
47     // allocate memory on host for result
48     float *C2;
49     C2 = (float*) malloc (N*sizeof(float));
50
51     // allocate memory on device for computation
52     float *A2_gpu;
53     float *B2_gpu;
54     float *C2_gpu;
55     cudaMalloc(&A2_gpu, sizeof(float)*N);
56     cudaMalloc(&B2_gpu, sizeof(float)*N);
57     cudaMalloc(&C2_gpu, sizeof(float)*N);
58
59     // Copy vectors A and B from host to device
60     cudaMemcpy(A2_gpu, A1, sizeof(float)*N, cudaMemcpyHostToDevice);
61     cudaMemcpy(B2_gpu, B1, sizeof(float)*N, cudaMemcpyHostToDevice);
62
63     // Set optimal number of threads per block
64     int T_B = 32;
65
66     // Compute number of blocks for set number of threads

```

```

67     int B = N/T_B;
68
69     // If there are left over points, run an extra block
70     if(N % T_B > 0)
71         B++;
72
73     // Run computation on device
74     //for(int i = 0; i < 100; i++)
75     VecAddGPU<<<B, T_B>>>(C2_gpu, A2_gpu, B2_gpu, N);
76
77     // Copy vector C2 from device to host
78     cudaMemcpy(C2, C2_gpu, sizeof(float)*N, cudaMemcpyDeviceToHost);
79
80     // Compare C2 to C1
81     bool equal = true;
82     for(int i = 0; i < N; i++)
83         if(C1[i] != C2[i])
84             equal = false;
85     if(equal)
86         cout << "C2 is equal to C1." << endl;
87     else
88         cout << "C2 is NOT equal to C1." << endl;
89
90     // Free vectors on CPU
91     free(A1);
92     free(B1);
93     free(C1);
94     free(C2);
95
96     // Free vectors on GPU
97     cudaFree(A2_gpu);
98     cudaFree(B2_gpu);
99     cudaFree(C2_gpu);
100 }
```

3.2 GPU kernel using threads and thread blocks

A GPU kernel is executed by launching blocks with a set number of threads per block. In the Listing 3.1, VecAddGPU is launched on line 75 with 32 threads per block. The total number of threads launched on the GPU is the number of blocks times the number of threads per block. VecAddGPU needs to be launched with at least $N = 2^{22}$ (line 22) threads or $2^{22}/32$ blocks of 32 threads.

CUDA gives each thread launched in a GPU kernel a unique index called threadIdx and blockIdx. threadIdx is the thread index inside the assigned thread block. blockIdx is the index of the block that the thread is assigned to. Both threadIdx and blockIdx are three dimensional and have x, y and z components. In this thesis only the x dimension is used because GPU kernels operate only on one dimensional vectors. blockDim is the number of threads assigned per block, in fact blockDim is equal to the number of threads per block because the vectors are one dimensional.

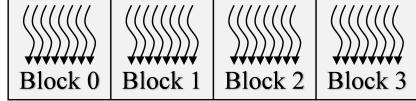


Figure 3.4: 32 threads launched in 4 thread blocks with 8 threads per block.

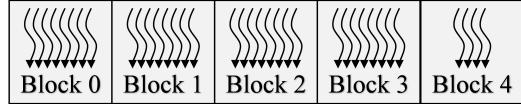


Figure 3.5: 36 threads launched in 5 thread blocks with 8 threads per block with 4 idle threads.

To turn CPU the N long “for loop” on line 7 into a GPU kernel, at least N threads are launched with T threads per thread block. The number of blocks needed is $B = \frac{N}{T_B}$ or $B = \frac{N}{T} + 1$ if N is not an integer multiple of T . Figure 3.4 shows $N = 32$ threads launched in $B = 4$ thread blocks with $T = 8$ threads per block. Figure 3.5 shows $N = 36$ threads launched in $B = 5$ thread blocks with $T = 8$ threads per block. An full extra thread block is launched with $T = 8$ threads but 4 threads are idle. Note that thread blocks are executed independent of other thread blocks. The GPU does not guarantee Block 0 will execute before Block 2.

3.3 GPU Memory

GPUs have plenty of computational resources but the most GPU kernels are limited by accessing memory to feed the computational units. GPU kernels will execute faster if the kernel is designed to access memory efficiently rather than reducing the computational burden. NVIDIA GPUs have many different types of memory to maximize speed and efficiency.

The fastest memory is private local memory in the form of registers, L1 cache and shared memory but only kilobytes are available. The slowest memory is public memory in the form of L2 cache and global memory and gigabytes are available. Figure 3.6 shows the trade off of memory speed and the size of different types of memory.

Figure 3.7 shows a picture of the GPU hardware. The solid boxes show that L2 cache or global memory are physically located *off* the GPU chip. The dashed box shows that registers, L1

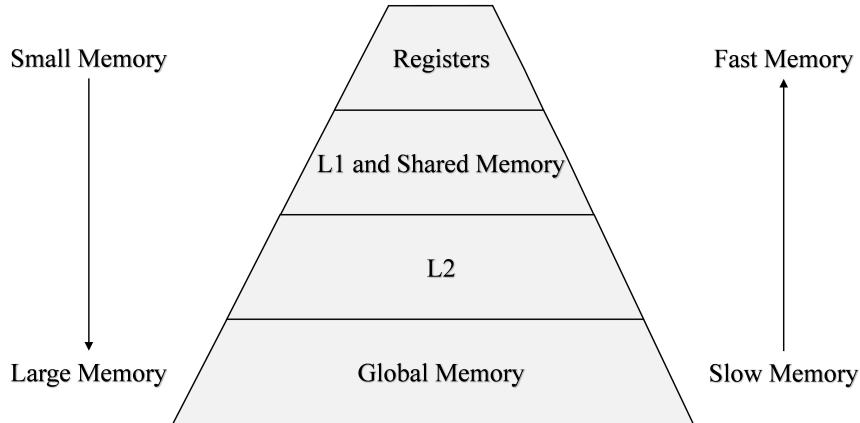


Figure 3.6: Diagram comparing memory size and speed. Global memory is massive but extremely slow. Registers are extremely fast but there are very few.

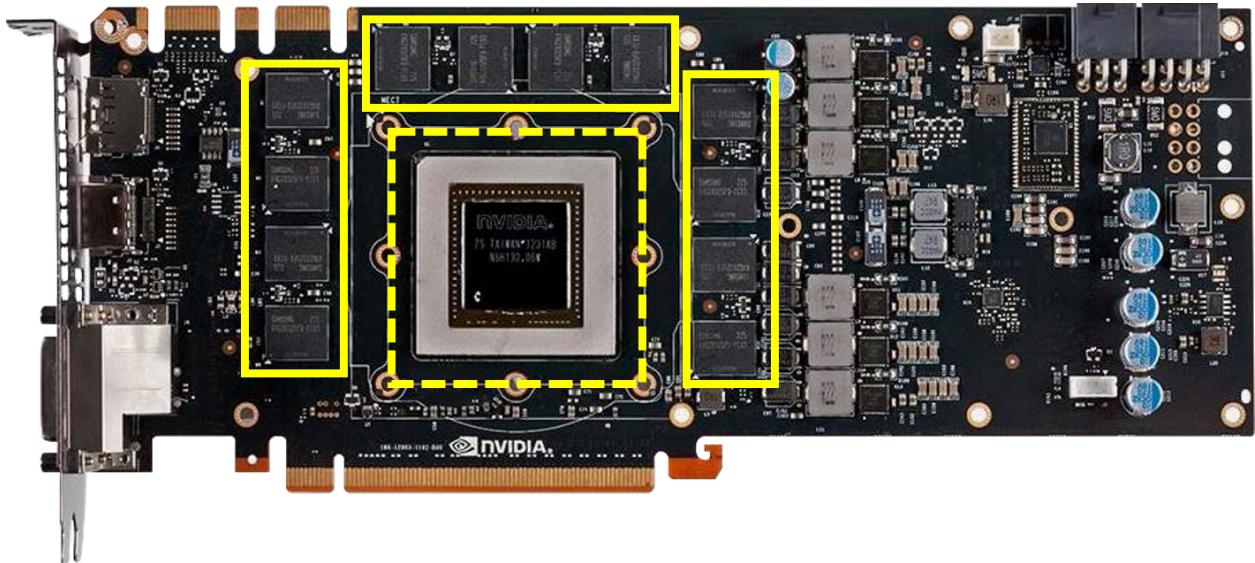


Figure 3.7: Example of an NVIDIA GPU card. The GPU chip with registers, L1 cache and shared memory is shown in the dashed box. The L2 cache and global memory is shown off chip in the solid boxes.

cache or shared memory are physically located *on* the GPU chip. A L2 cache or global memory access takes over 60 clock cycles because the memory is off chip. A registers, L1 cache or shared memory access is only a few clock cycles because the memory is on chip.

Figure 3.8 illustrates where each type of memory is located. Threads have access to their own registers and L1 cache. Threads in a block can coordinate using shared memory because

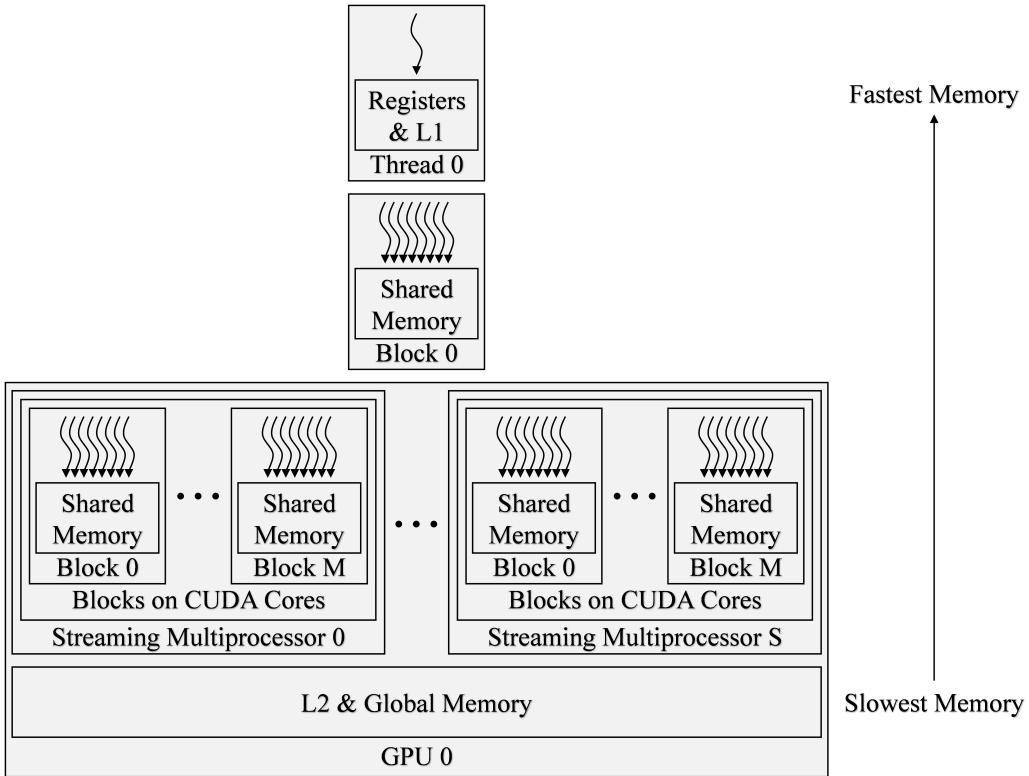


Figure 3.8: A block diagram where local, shared, and global memory is located. Each thread has private local memory. Each thread block has private shared memory. The GPU has global memory that all threads can access.

shared memory private to the thread block. All threads have access to L2 cache and global memory. The figure also shows that thread blocks are assigned to streaming multiprocessors (SMs). CUDA handles all the thread block assignments to SMs. Table 3.1 lists Tesla K40c and K20c resources.

3.4 Thread Optimization

Most resources listed in Table 3.1 show how much memory per thread block is available. The number of threads per block and the amount of resources available have an inverse relationship. Threads will have very little memory resources available if a GPU kernel launches 1024 threads per block. Threads will have a lot of memory resources available if a GPU kernel launches 32 threads per block. This section will show that finding the optimum number of threads per block can drastically speed up GPU kernels.

Table 3.1: The resources available with three NVIDIA GPUs used in this thesis (1x Tesla K40c 2x Tesla K20c). Note that CUDA configures the size of the L1 cache needed.

Feature	Per	Tesla K40c	Tesla K20c
Global Memory	GPU	12 GB	5 GB
L2 Cache Size	GPU	1.6 GB	1.3 GB
Memory Bandwidth		288 GB/s	208 GB/s
Shared Memory	Thread Block	49 kB	49 kB
L1 Cache Size	Thread Block	variable	variable
Registers	Thread Block	65536	65536
Maximum Threads	Thread Block	1024	1024
CUDA Cores	GPU	2880	2496
Base Core Clock		745 MHz	732 MHz

Improving memory accesses should always be the first optimization when a GPU kernel needs to be faster. The next step is to find the optimal number of threads per block to launch. Knowing the perfect number of threads per block to launch is challenging to calculate. Luckily, there is a finite number of possible threads per block in the Tesla K40c and K20c GPUs, 1 to 1024. Listing 3.2 shows a simple test program that times GPU kernel execution time while sweeping the number of possible threads per block. The number of threads per block with the fastest computation time is the optimal number of threads per block for that specific GPU kernel.

Listing 3.2: Code snippet for thread optimization.

```
1 float milliseconds_opt = pow(2,10); // initiaize to "big" number
2 int T_B_opt;
3 int minNumTotalThreads = pow(2,20); // set to minimum number of required threads
4 for(int T_B = 1; T_B<=1024; T_B++) {
5     int B = minNumTotalThreads/T_B;
6     if(minNumTotalThreads % T_B > 0)
7         B++;
8     cudaEvent_t start, stop;
9     cudaEventCreate(&start);
10    cudaEventCreate(&stop);
11    cudaEventRecord(start);
12
13    GPUkernel<<<B, T_B>>>(dev_vec0, dev_vec1);
14
15    cudaEventRecord(stop);
16    cudaEventSynchronize(stop);
17    float milliseconds = 0;
18    cudaEventElapsedTime(&milliseconds, start, stop);
19    cudaEventDestroy(start);
20    cudaEventDestroy(stop);
21    if(milliseconds<milliseconds_opt){
22        milliseconds_opt = milliseconds;
23        T_B_opt = T_B;
24    }
25 }
26 cout << "Optimal Threads Per Block " << T_B_opt << endl;
27 cout << "Optimal Execution Time " << milliseconds_opt << endl;
```

Most of the time the optimal number of threads per block is a multiple of 32. At the lowest level of architecture, GPUs do computations in *warps*. Warps are groups of 32 threads that do every computation together in lock step. If the number of threads per block is a non multiple of 32, some threads in a warp will be idle and the GPU will have unused computational resources.

Figure 3.9 shows the execution time of an example GPU kernel. The optimal execution time is 0.1078 ms at the optimal 96 threads per block. By simply adjusting the number of threads per block, the execution time of this example kernel can be reduced by 2.

Adjusting the number of threads per block does not always drastically reduce execution time. Figure 3.10 shows the execution time for another GPU kernel with varying threads per block. The execution time of this example kernel can be reduced by 1.12 by launching 560 threads per block.

While writing a custom GPU kernel then figuring out how to optimize it is extremely satisfying, CUDA has super optimized GPU libraries that are extremely useful and efficient. The CUDA libraries are written by NVIDIA engineers that know how to squeeze out every drop of

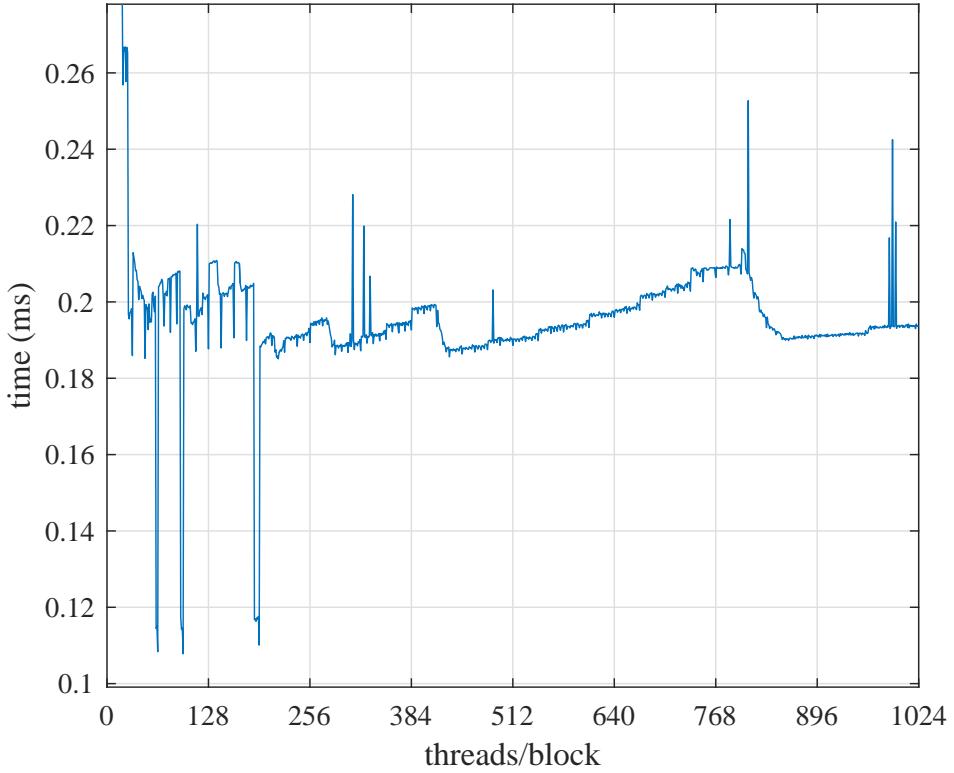


Figure 3.9: Plot showing how execution time is affected by changing the number of threads per block. The optimal execution time for an example GPU kernel is 0.1078 ms at the optimal 96 threads per block.

performance out of NVIDIA GPUs. Some libraries used in this thesis are cuFFT, cuBLAS and cuSolverSp.

3.5 CPU GPU Pipelining

A basic program flow is shown in Listing 3.3. The CPU acquires data from myADC on Line 5. After taking time to acquire data, the data is copied to the CPU, the data is processed in the GPU then result is copied back to the CPU on Lines 8 to 10. `cudaDeviceSynchronize` on line 13 causes the CPU to wait until all instructions on the GPU are complete. Acquiring and copying data takes precious processing time. What if the GPU could be processing data while the CPU acquires and copied data? How much computation time could be gained by pipelining acquiring data and processing data? How much would the throughput increase?

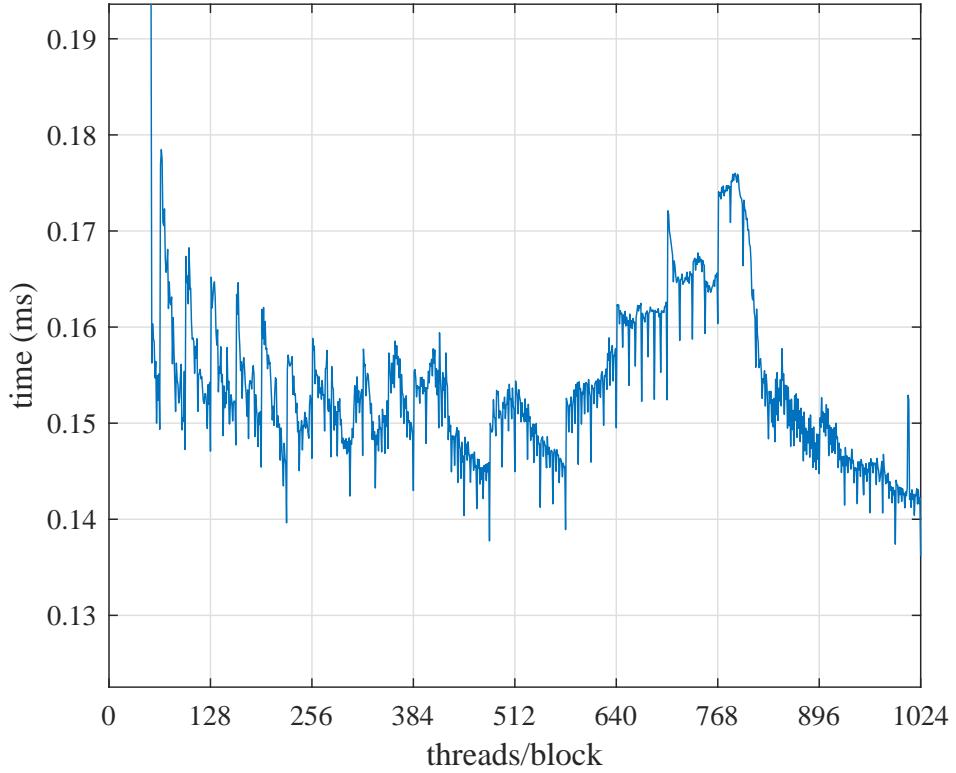


Figure 3.10: Plot showing the number of threads per block doesn't always drastically affect execution time.

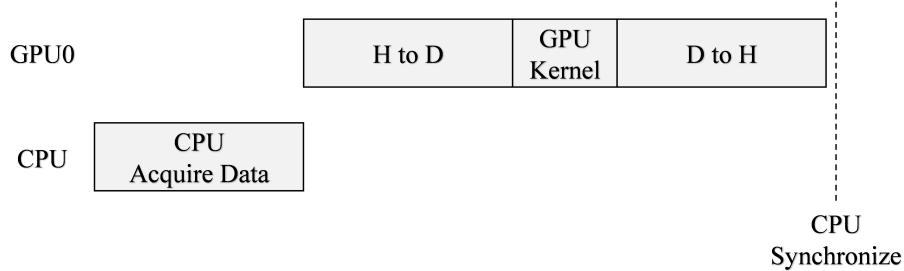


Figure 3.11: The typical approach of CPU and GPU operations. This block diagram shows the profile of Listing 3.3.

Figure 3.11 shows a block diagram of what is happening on the CPU and GPU in Listing 3.3. The GPU is idle while the CPU is acquiring data. The CPU is idle while the GPU is processing and data is being transferred to and from the GPU.

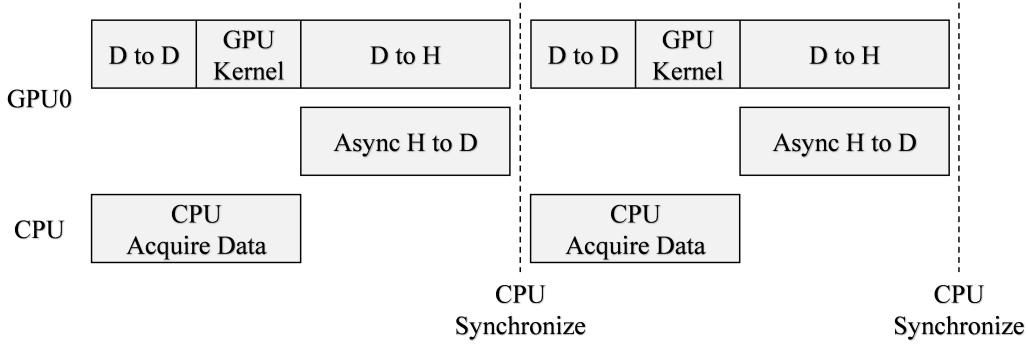


Figure 3.12: GPU and CPU operations can be pipelined. This block diagram shows a Profile of Listing 3.4.

Listing 3.3: Example code Simple example of the CPU acquiring data from myADC, copying from host to device, processing data on the device then copying from device to host. No processing occurs on device while CPU is acquiring data.

```

1 int main()
2 {
3     ...
4     // CPU Acquire Data
5     myADC.acquire(vec);
6
7     // Launch instructions on GPU
8     cudaMemcpy(dev_vec0, vec, numBytes, cudaMemcpyHostToDevice);
9     GPUkernel<<<1, N>>>(dev_vec0);
10    cudaMemcpy(vec, dev_vec0, numBytes, cudaMemcpyDeviceToHost);
11
12    // Synchronize CPU with GPU
13    cudaDeviceSynchronize();
14    ...
15 }
```

Can the throughput increase by using idle time on the GPU and CPU? Yes, CPU and GPU operations can sacrifice latency for throughput by pipelineing. After the CPU gives instructions to the GPU, the CPU can do other operations like acquire data or perform algorithms better suited for CPUs than the GPUs. Once the CPU has finished its operations, the CPU can wait for the GPU to finish.

Listing 3.4 shows how to pipeline CPU and GPU operations. Assuming data is already on the GPU from a prior iteration, the CPU gives instructions to the GPU then starts acquiring data. The CPU then does an asynchronous data transfer to a temporary vector on the GPU. The GPU first performs a device to device transfer from the temporary vector. The GPU then runs the GPUkernel and transfers the result to the host. This system suffers a full cycle latency.

Listing 3.4: Example code Simple of the CPU acquiring data from myADC, copying from host to device, processing data on the device then copying from device to host. No processing occurs on device while CPU is acquiring data.

```

1 int main()
2 {
3     ...
4     // Launch instructions on GPU
5     cudaMemcpy(dev_vec, dev_temp, numBytes, cudaMemcpyDeviceToDevice);
6     GPUkernel<<<N, M>>>(dev_vec);
7     cudaMemcpy(vec,      dev_vec,  numBytes, cudaMemcpyDeviceToHost);
8
9     // CPU Acuire Data
10    myADC.acquire(vec);
11    cudaMemcpyAsync(dev_temp, vec, numBytes, cudaMemcpyHostToDevice);
12
13    // Synchronize CPU with GPU
14    cudaDeviceSynchronize();
15    ...
16
17    ...
18    // Launch instructions on GPU
19    cudaMemcpy(dev_vec, dev_temp, numBytes, cudaMemcpyDeviceToDevice);
20    GPUkernel<<<N, M>>>(dev_vec);
21    cudaMemcpy(vec,      dev_vec,  numBytes, cudaMemcpyDeviceToHost);
22
23    // CPU Acuire Data
24    myADC.acquire(vec);
25    cudaMemcpyAsync(dev_temp, vec, numBytes, cudaMemcpyHostToDevice);
26
27    // Synchronize CPU with GPU
28    cudaDeviceSynchronize();
29    ...
30 }
```

Pipelineing can be extended to multiple GPUs for even more throughput but only suffer latency of copying memory to one GPU. Figure 3.13 shows a block diagram of how three GPUs can be pipelined. A strong understanding of the full system is required to pipeline at this level.

3.6 GPU Convolution

Convolution is one of the most important tools in digital signal processing. The PAQ system explained in the Introduction uses convolution at least 10 times, depending on the number of CMA iterations. If convolution execution time improves by 10 ms, the full system execution time improves by 100 ms. This chapter explores the how to optimize GPU convolution.

Discrete time convolution can be implemented in the time or frequency domain. Discrete time convolution computed in the time domain is

$$y(n) = \sum_{m=0}^{L-1} x(m)h(n-m) \quad (3.2)$$

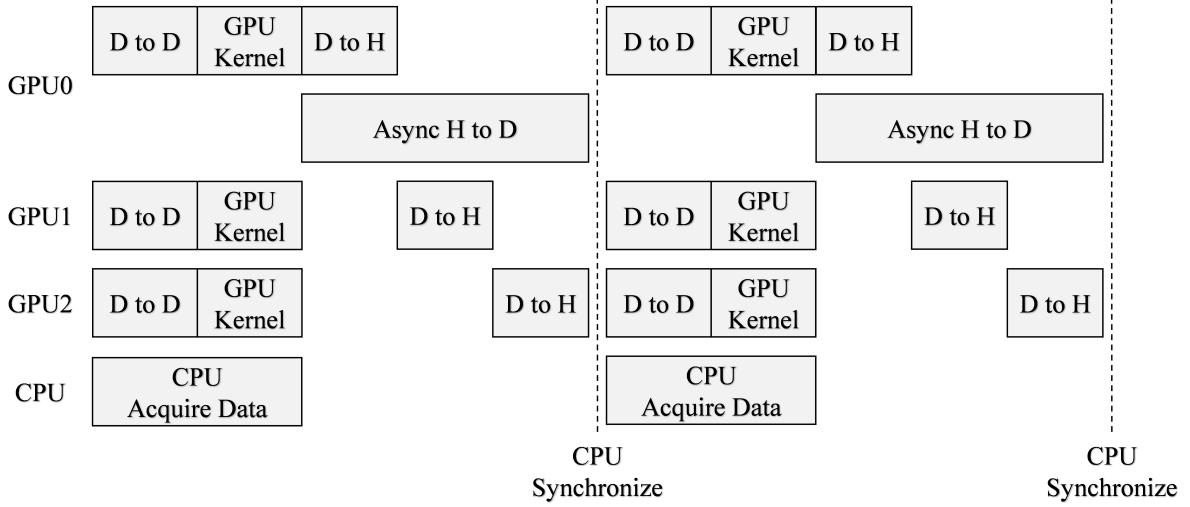


Figure 3.13: A block diagram of pipelining a CPU with three GPUs.

and discrete time convolution computed in the frequency domain is

$$\mathbf{y} = \mathcal{F}^{-1}(\mathcal{F}(\mathbf{x}) \times \mathcal{F}(\mathbf{h})) \quad (3.3)$$

where the N sample complex signal \mathbf{x} is convolved with the L tap filter complex \mathbf{h} .

Traditionally the number of flops is used to estimate how computationally intense an algorithm is. Each complex multiply

$$(A + jB) \times (C + jD) = (AC - BD) + j(AD + BC) \quad (3.4)$$

is 6 flops, 4 multiplies and 2 additions/subtractions. Each output element of \mathbf{y} in Equation (3.2) requires $8L$ flops. Each term in the L long summation takes 8 flops, 6 flops per multiply plus 2 flops (real and imaginary) for the sum. The output vector \mathbf{y} is $N + L - 1$ samples long. The number of flops required for convolution is

$$8L(N + L - 1) \text{ flops.} \quad (3.5)$$

The length of the convolution, $M = N + L - 1$ is the minimum point Fourier Transform possible. To leverage the Cooley-Tukey radix 2 Fast Fourier Transform (FFT), it is common practice append zeros to the next power of to above M . The current most popular CPU based FFT is the Fastest Fourier Transform in the West (FFTW) library, FFTW uses the Cooley-Tukey radix 2 transform. Each radix 2 forward or backward Fourier transform requires $5M \log_2(M)$ flops [12, 13]. As shown by Equation (3.3), frequency-domain convolution requires

$$3 \times 5M \log_2(M) + 6M \text{ flops} \quad (3.6)$$

from 3 FFTs and a length M point to point multiply.

Comparing Equations (3.5) and 3.6, if a signal or filter length is relatively long the frequency domain is the best choice. What constitutes a “long” signal or filter? When should convolution be done in the frequency domain rather than time-domain?

Figure 3.14 compares the number of flop required to convolve a 12672 sample complex signal with a varied length tap complex filter. According to the number of flops in the figure, frequency-domain convolution requires less flops if the filter is longer 40 taps.

Figure 3.15 compares the number of flops required for time-domain verse frequency-domain convolution of a 12672 sample complex signal with a 186 tap complex filter. Figure 3.16 compares the number of flops required for time-domain verse frequency-domain convolution of a 12672 sample complex signal with a 21 tap complex filter. Appending zeros to the next power of 2 causes the stair stepping pattern. Judging by the figures with varied signal lengths, a 186 tap filter is “long” and a 21 tap filter is “short.”

3.7 CPU and GPU Single Batch Convolution

With an understanding of the number of flops in time verses frequency domain required to implement convolution, do the number of flops have a direct relationship to execution time in CPUs and GPUS? To explore the flop to execution time relationship Listing 3.5 shows five different ways of implementing convolution:

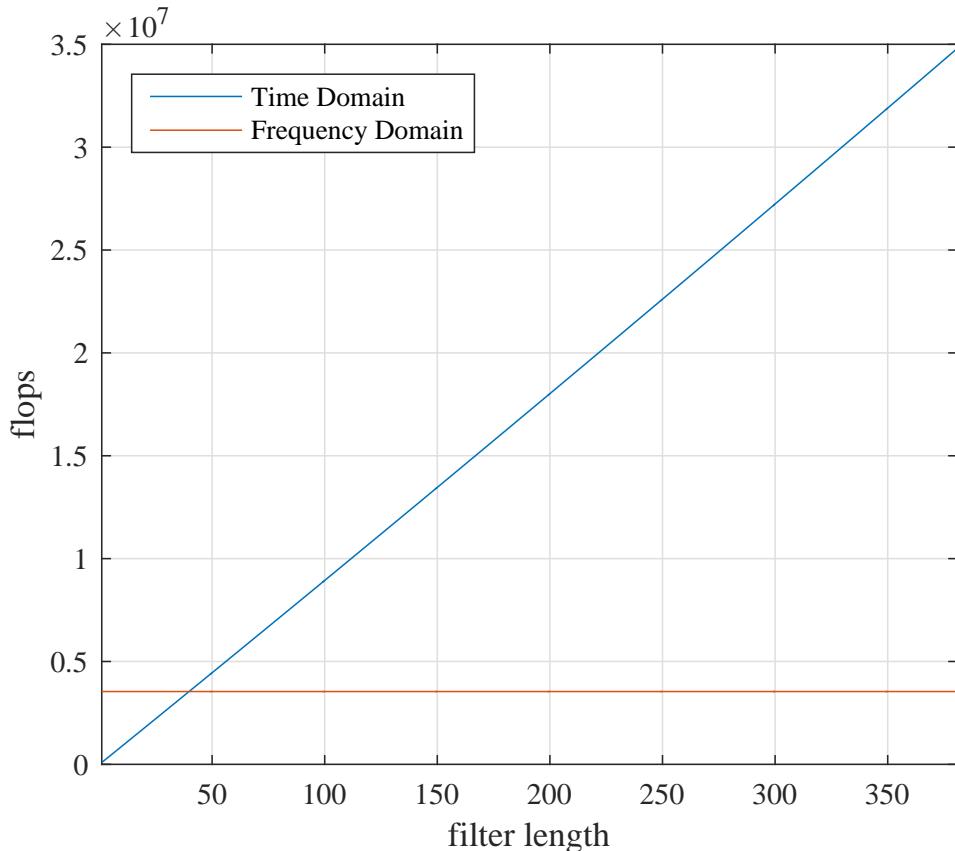


Figure 3.14: Comparison of number of floating point operations (flops) required to convolve a 12672 sample complex signal with a varied length tap complex filter.

- time-domain convolution in a CPU
- frequency-domain convolution in a CPU
- time-domain convolution in a GPU using global memory
- time-domain convolution in a GPU using shared memory
- frequency-domain convolution in a GPU using CUDA libraries

The CPU implements Equation (3.2) in ConvCPU directly on line 209 using a function from lines 11 to 34. The CPU implements Equation (3.3) using the FFTW library on lines 214 to 258.

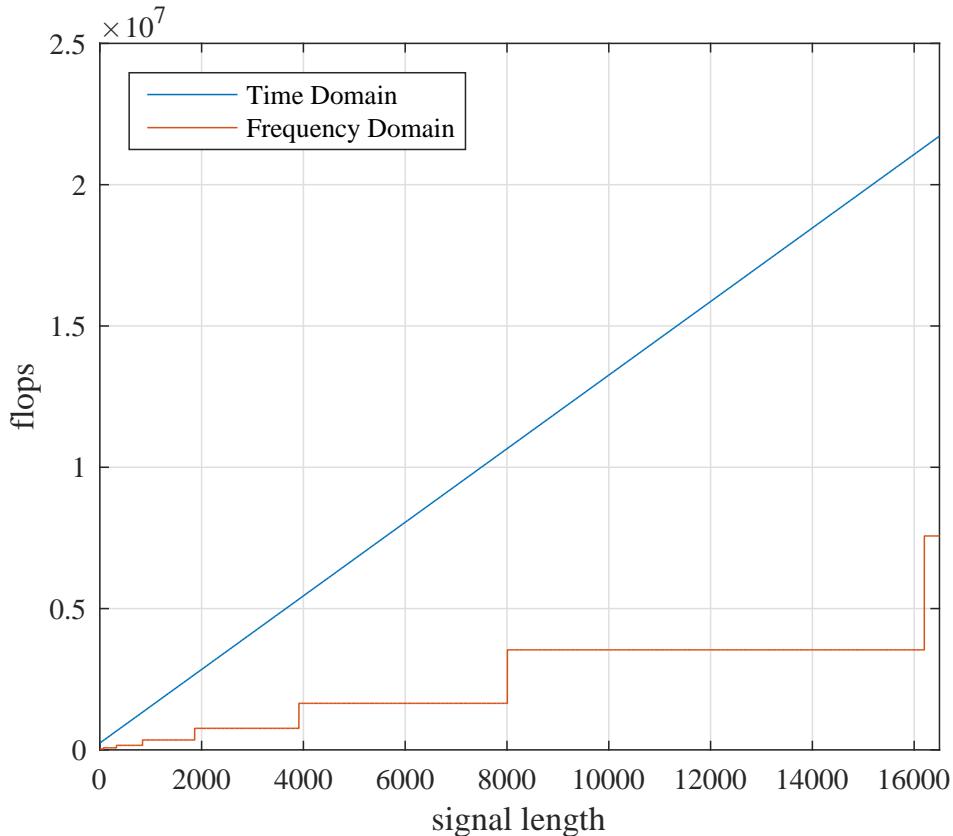


Figure 3.15: Comparison of number of floating point operations (flops) required to convolve a varied length complex signal with a 186 tap complex filter.

The GPU implements time-domain convolution using global memory in lines 268 to 277.

The GPU kernel ConvGPU on lines 36 to 64 is a parallel version of ConvCPU. ConvGPU performs time-domain convolution by fetching every element of the signal and filter from global memory.

The GPU implements time-domain convolution using shared memory in lines 283 to 292.

The GPU kernel ConvGPUshared on lines 67 to 101 is nearly identical to ConvGPU. Threads accessing the same elements of the filter in global memory can be a waste of valuable clock cycles. ConvGPUshared pays an initial price on lines 72 to 76 to move L_h filter coefficients from off chip global memory to the on chip shared memory. Finally, the GPU implements frequency-domain convolution using the cuFFT library on lines 298 to 326.

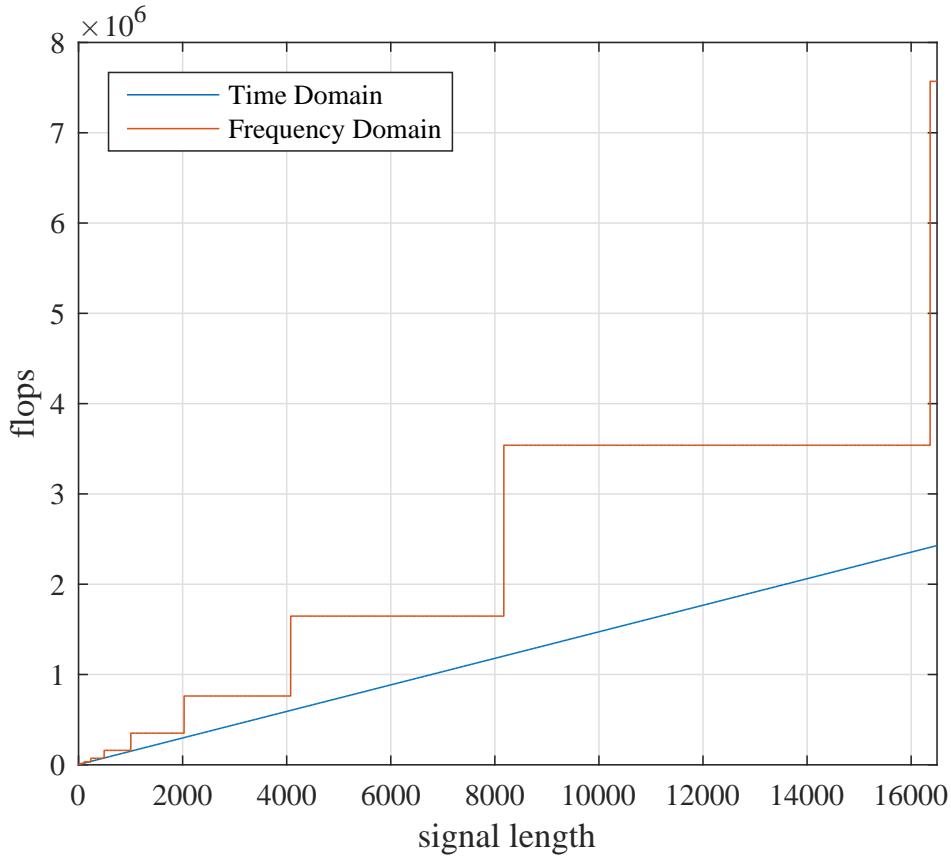


Figure 3.16: Comparison of number of floating point operations (flops) required to convolve a varied length complex signal with a 21 tap complex filter.

The questions are: Do flops have a direct relationship to execution time on CPUs? Do flops have a direct relationship to execution time on GPUs? When is the initial cost to use shared memory worth it? When should convolution be done in the frequency domain?

The short answer to all of the questions is: GPU execution time depend on the signal length, filter length, CPU, GPU and memory. A good CUDA programmer can make an educated guess on which algorithm may be faster in the GPU, but until all the algorithms have been implemented and timed, there is no definite answer.

To demonstrate that there is no definite answer in GPUs, the execution time of the code in Listing 3.1 was timed. All the memory transfers to and from the host were timed for a fair comparison of GPU to CPU. Table 3.2 shows where timing was started and stopped for each convolution implementation.

Table 3.2: Defining start and stop lines for timing comparison in Listing 3.5.

Algorithm	Function	Start Line	Stop Line
CPU time domain	ConvCPU	208	210
CPU frequency domain	FFTW	213	259
GPU time domain global	ConvGPU	267	278
GPU time domain shared	ConvGPUshared	282	293
GPU frequency domain	cuffFT	301	327

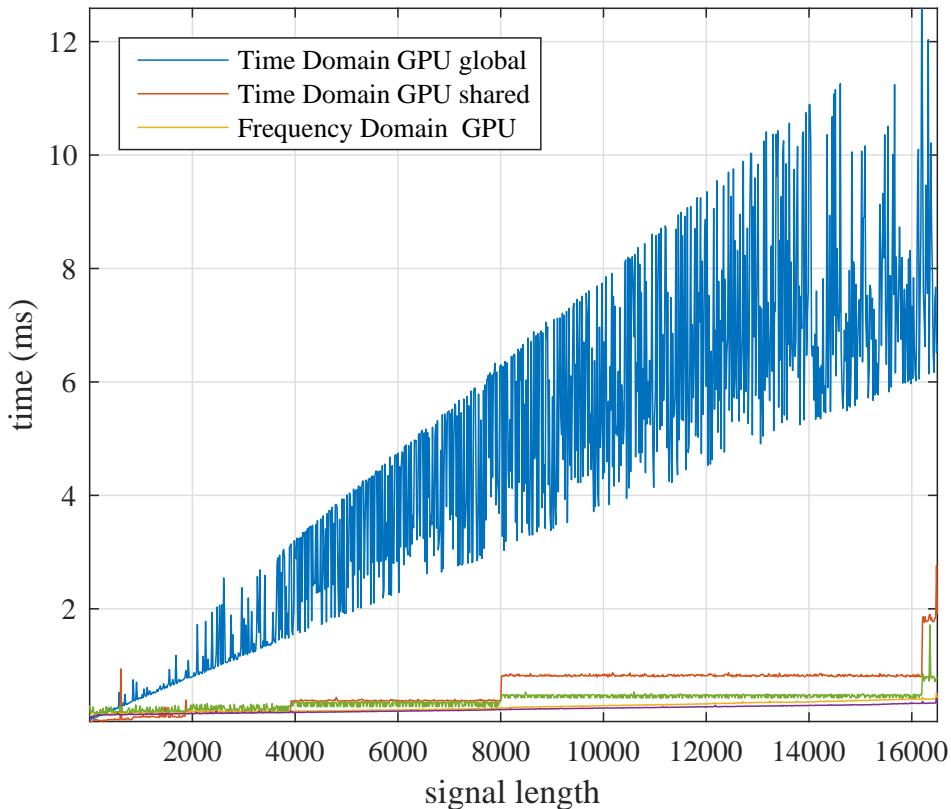


Figure 3.17: Comparison of a complex convolution on CPU verse GPU. The signal length is varied and the filter is fixed at 186 taps. The comparison is messy with out lower bounding.

The execution times shown in Figure 3.17 compares the computation time of a fixed length 186 tap filter convolved with a varied length signal. The CPU execution time varies enough that the plot is messy. Figure 3.18 shows the lower bounds of execution times by finding the local minimums in 15 sample windows.

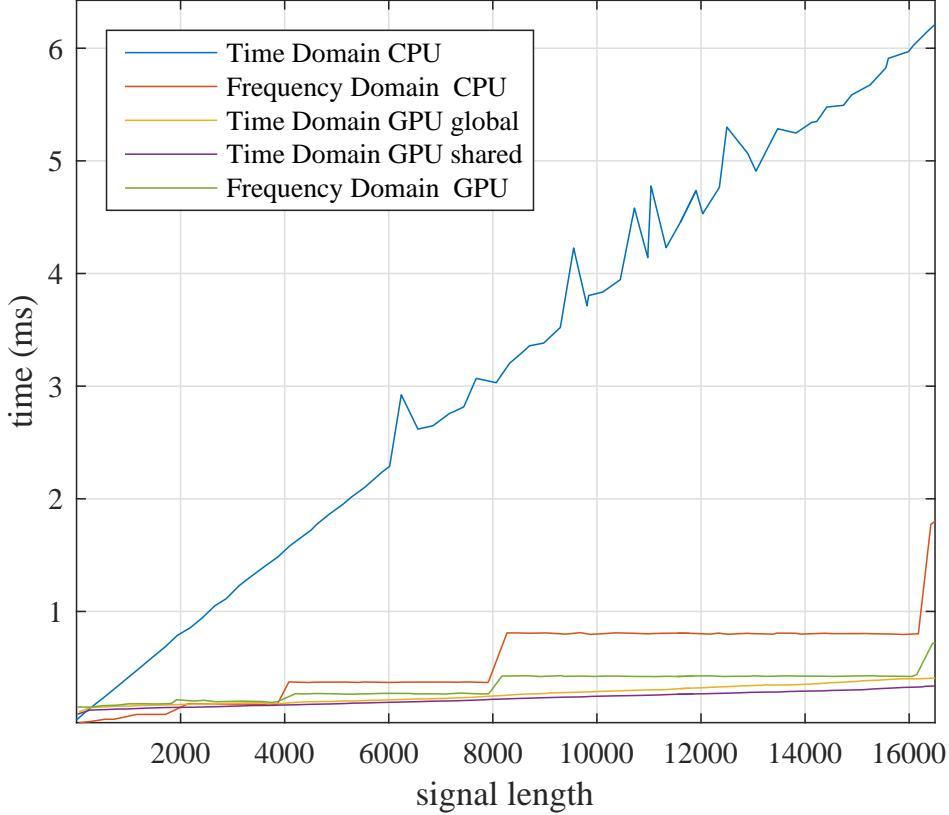


Figure 3.18: Comparison of a complex convolution on CPU verse GPU. The signal length is varied and the filter is fixed at 186 taps. A lower bound was applied by searching for a local minimum in 15 sample width windows.

With the plot lower bounded, compare Figure 3.18 to Figure 3.15. Does the CPU and GPU follow the same trend as the number of flops? The CPU has the exact structure that the number of flops predicted. The GPU does have the stair stepping from appending zeros for the frequency domain, but the time domain GPU kernels perform better than the number of flops predicted.

The GPU execution time does not follow the same trend as the number of flops. Why? As mentioned in Section 3.3, GPUs have a ridiculous amount of computational resources and limited memory bandwidth. Over 90% of GPU kernels are memory bandwidth limited. Fast GPU kernels access memory efficiently.

To provide more proof, compare Figures 3.19 and 3.16. Once again, the CPU follows the same trend as the number of flops. The GPU also follows the number of flops trends but to a lesser

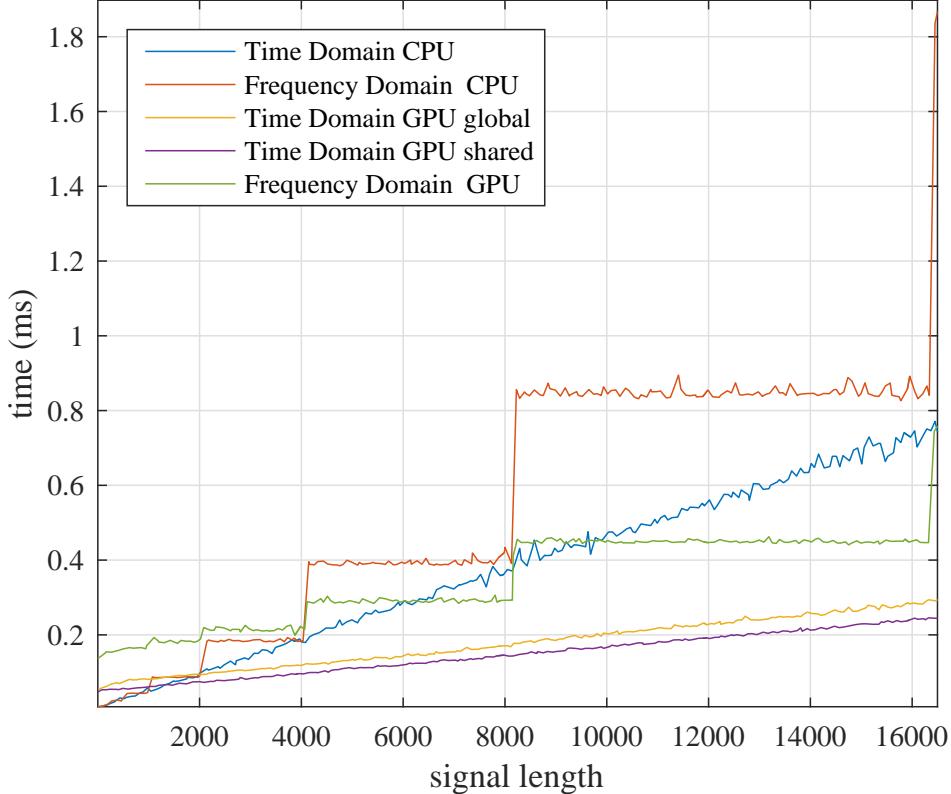


Figure 3.19: Comparison of a complex convolution on CPU verse GPU. The signal length is varied and the filter is fixed at 21 taps. A lower bound was applied by searching for a local minimum in 5 sample width windows.

extent than the CPU. Using shared memory will perform better than using only global memory for “short” filters.

What if the signal length was set and the filter length was varied? Comparing Figure 3.20 to Figure 3.14 shows the CPU follows the trend of flops also. The time domain CPU execution time is obviously affected as the number of flops increases. Neither CPU or GPU frequency domain execution time is affected by varying filter length.

The execution time of both time-domain GPU convolutions are slightly affected by increasing filter length. The number of memory accesses per output sample increase as the filter length increases. Bottom line, the length of the signal is the largest factor as Equations 3.5 and 3.6 suggest.

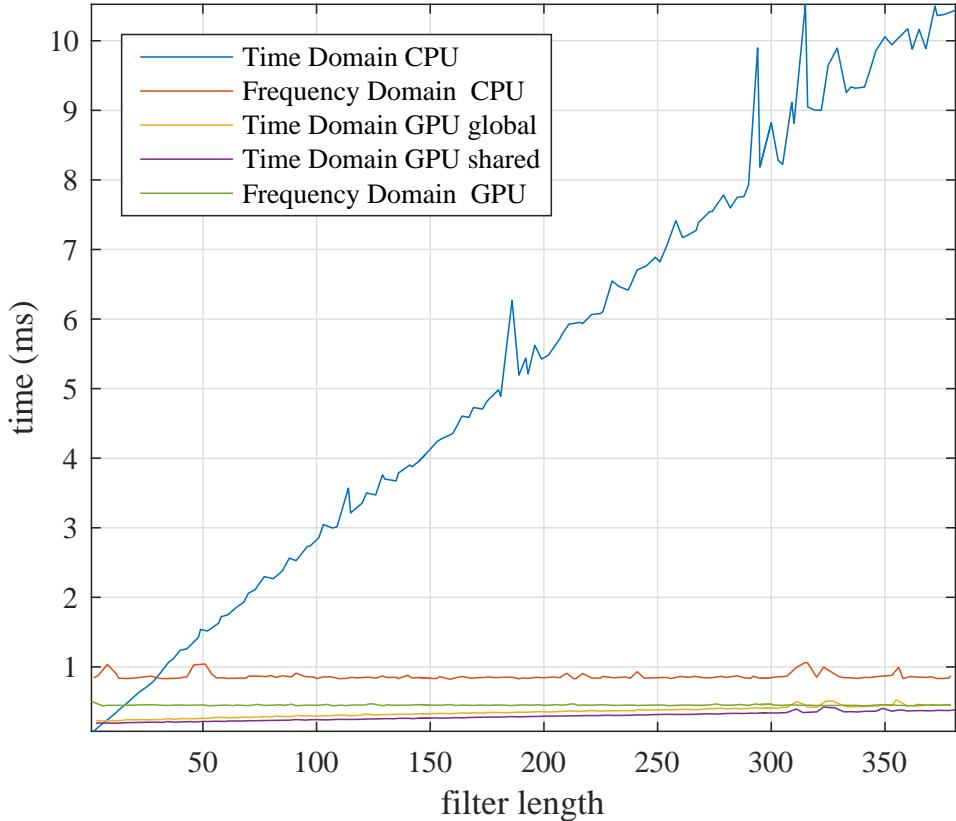


Figure 3.20: Comparison of a complex convolution on CPU verse GPU. The filter length is varied and the signal is fixed at 12672 samples. A lower bound was applied by searching for a local minimum in 3 sample width windows.

For most convolution implementations, the signal and filter lengths are set “magic” numbers. To find the best option, implement convolution every way possible for the given lengths, time each implementation execution time, choose which algorithm is fastest. As Figures 3.17 through 3.20 have shown, unless every implementation is explored, there is no way of saying which implementation will absolutely be fastest.

Table 3.3 shows the GPU frequency-domain algorithm is fastest when convolving a 12672 sample signal with a 186 tap filter. Table 3.4 shows the GPU time-domain algorithm using shared memory is fastest when convolving a 12672 sample signal with a 21 tap filter.

Table 3.3: Convolution computation times with signal length 12672 and filter length 186 on a Tesla K40c GPU.

Algorithm	Function or Library	Execution Time (ms)
CPU time domain	ConvCPU	5.3000
CPU frequency domain	FFTW	0.7972
GPU time domain global	ConvGPU	0.3321
GPU time domain shared	ConvGPUshared	0.2748
GPU frequency domain	cuFFT	0.4224

Table 3.4: Convolution computation times with signal length 12672 and filter length 21 on a Tesla K40c GPU.

Algorithm	Function or Library	Execution Time (ms)
CPU time domain	ConvCPU	0.5878
CPU frequency domain	FFTW	0.8417
GPU time domain global	ConvGPU	0.4476
GPU time domain shared	ConvGPUshared	0.1971
GPU frequency domain	cuFFT	0.3360

3.8 Batched Convolution

As shown in section 3.7, single convolution doesn’t leverage the full power of parallel processing in GPUs. The introduction showed the PAQ project received signal has a packetized structure. The received signal has 3104 packets or batches. Batched processing introduces an extra level of parallelism in GPUs because each batch can be processed independently. CUDA has many libraries that are “batched,” meaning a GPU kernel is launched for each independent packet or batch of received samples. Some CUDA batched libraries used in PAQ system are cuFFT, cuBLAS and cuSolver.

Batched libraries perform much better than calling a single GPU kernel multiple times with each independent batch of data. Haidar et al. showed batched libraries in GPUs achieve more Gflops than calling GPU kernels multiple times [14]. Batched processing performs very well in GPUs

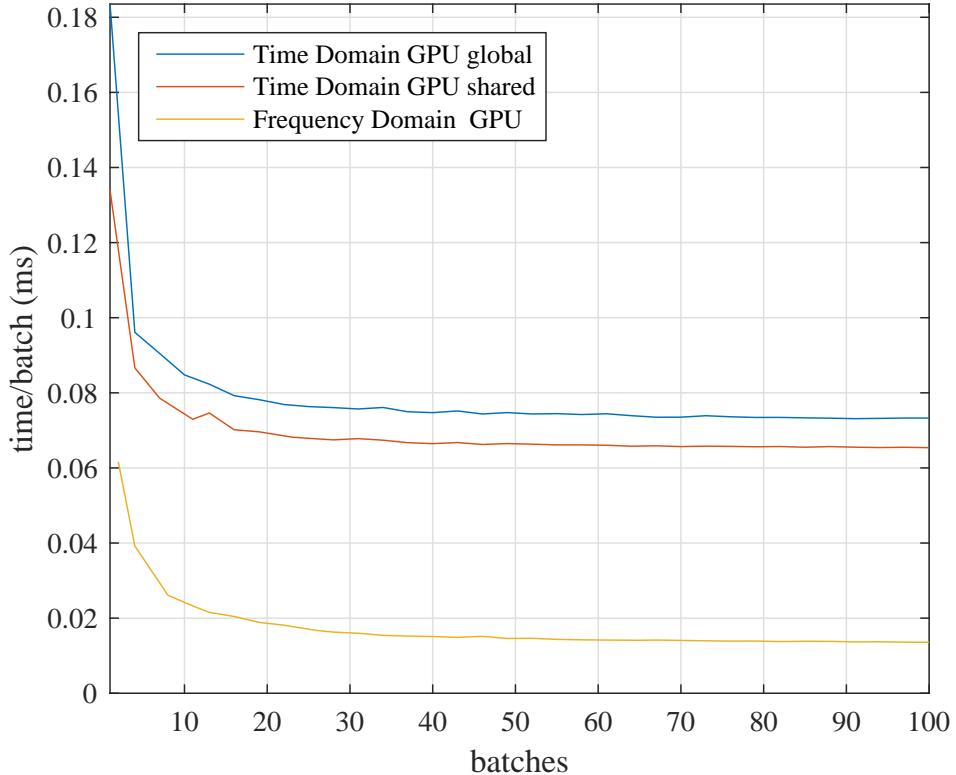


Figure 3.21: Comparison on execution time per batch for complex convolution. The number of batches is varied while the signal and filter length is set to 12672 and 186.

because it increases parallelism, reduces overhead on the CPU and provides more opportunities for NVIDIA engineers to optimize.

As the number of batches increases, does CPU and GPU execution time increase linearly?

To illustrate how batch processing performs on GPUs, Figure 3.21 shows the execution time per batch for batched convolution in GPUs. The execution time per batch decreases as the number of batches increases but converges after 70 batches.

Figure 3.22 shows how the execution time increases with the number of batches varied. Note that no lower bounding is needed to produce clean batched processing results. This figure shows that frequency-domain convolution leverages batch processing better than time-domain convolution. No surprise CPU time and frequency domain execution time skyrockets as the number of batches increases.

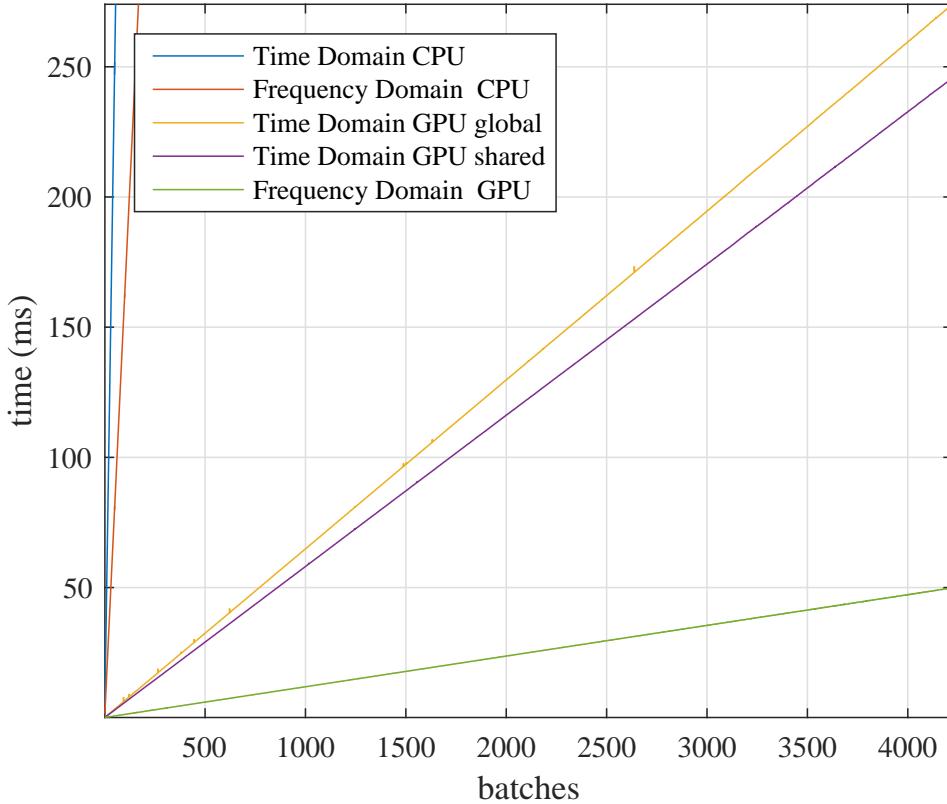


Figure 3.22: Comparison of a batched complex convolution on a CPU and GPU. The number of batches is varied while the signal and filter length is set to 12672 and 186.

Judging by Figure 3.22, CPU is not a contender in batched processing compared to the GPU. CPU batched processing will not be explored any further. Listing 3.6 shows three implementations of batched convolution in CUDA

- time-domain convolution in a GPU using global memory
- time-domain convolution in a GPU using shared memory
- frequency-domain convolution in a GPU using the cuFFT library.

Now that the GPU execution time isn't being compared to the CPU, transfers between host and device will not be a factor for algorithm comparison. Table 3.5 shows how Listing 3.6 is timed. Figure 3.23 shows execution time for 3104 batches of 186 tap filters convolved with varying signal lengths. Performing frequency-domain convolution is always faster than time-domain convolution

Table 3.5: Defining start and stop lines for timing comparison in Listing 3.6.

Algorithm	Function	Start Line	Stop Line
GPU time domain global	ConvGPU	197	204
GPU time domain shared	ConvGPUshared	212	219
GPU frequency domain	cufft	227	245

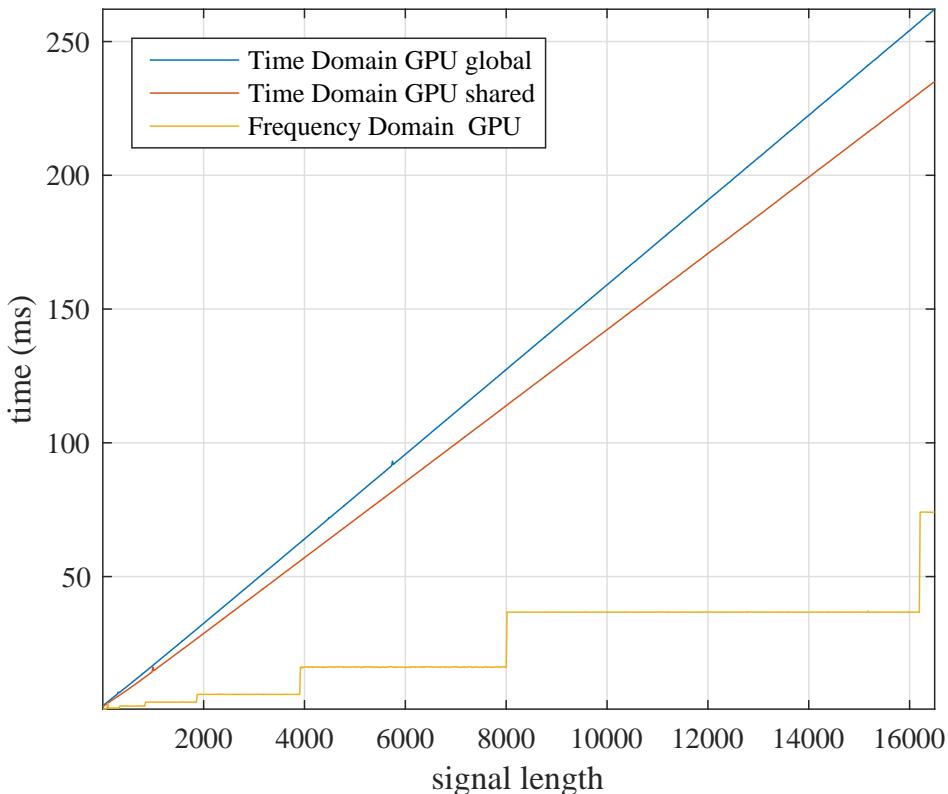


Figure 3.23: Comparison of a batched complex convolution on a GPU. The signal length is varied and the filter is fixed at 186 taps.

because the cuFFT library is better optimized for batched processing. The batched GPU implementation of convolution in the frequency-domain convolution takes just 36.8 ms for 3104 batches, 12672 sample signals and 186 tap filters. The average execution time per batch for 3104 batches is 0.0119 ms per batch! Compare 0.0119 ms per batch to single batched execution time in Table 3.3, one batch took 0.4224. Batched processing introduced a 35× speed up!

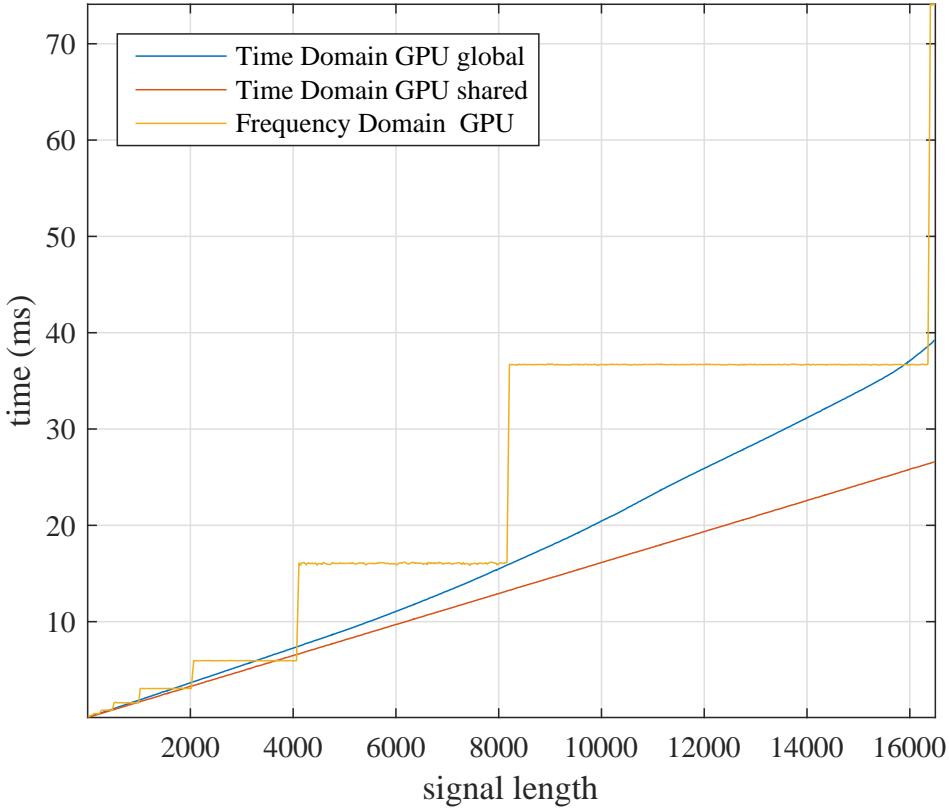


Figure 3.24: Comparison of a batched complex convolution on a GPU. The signal length is varied and the filter is fixed at 21 taps.

Figure 3.24 shows execution time for 3104 batches of 21 tap filters convolved with varying signal lengths. This figure exhibits the same characteristics of single batch convolution execution time shown in Figure 3.19. For most signal lengths, performing time-domain convolution using shared memory is fastest.

Figure 3.25 shows execution time for 3104 batches of 12672 sample signal convolved with varying filter lengths. This figure exhibits nearly the same characteristics of single batch convolution execution time shown in Figure 3.20 accept the varied filter length has no affect on execution time. For very short filter lengths, time-domain convolution using shared memory is fastest. For longer filters , frequency-domain convolution is fastest.

Though this section has show the power of batched processing, the algorithm leading to the fastest execution time still depends on signal and filter length, One important concept has been over looked. Figure 1.8 shows there are two filters that need to be applied to the received samples.

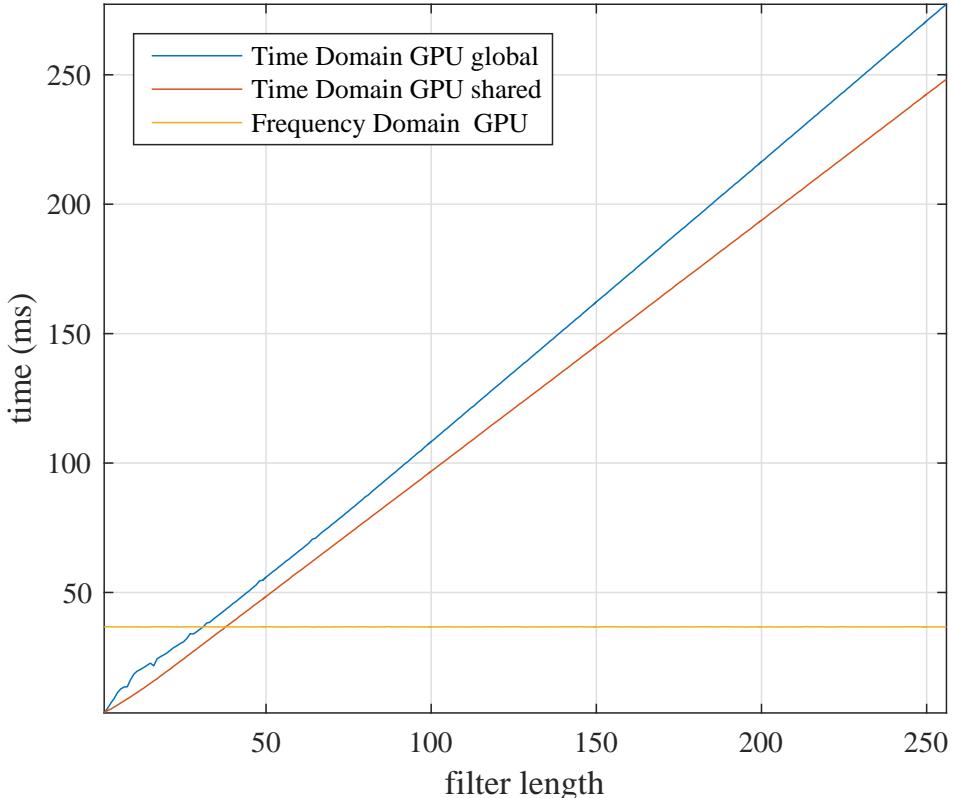


Figure 3.25: Comparison of a batched complex convolution on a GPU. The filter length is varied and the signal length is set at 12672 samples.

If convolution is implemented in the time domain, ConvGPU or ConvGPUshared must run twice. The first call of time-domain convolution performs an extremely fast “short” convolution of the 186 tap equalizer and 21 detection filter. The second call performs a slower “long” convolution of the 12672 sample signal with the convolved $186 + 21 - 1$ tap filter.

If convolution is implemented in the frequency domain, only the GPU kernel PointToPoint-Multiply has to be updated. PointToPointMultiply is changed from two to three input vectors. For every point the number of memory accesses increases by 1 element and the number of flops doubles from 6 to 12. An extra cuFFT call would be expected accept the detection filter is predefined in Figure 1.8. The FFT of the detection filter is calculated and stored at initialization.

Table 3.6 shows the batched convolution execution time for a 12672 sample signal and 186 tap filter. Table 3.7 shows the batched convolution execution time for a 12672 sample signal and 21

Table 3.6: Batched convolution execution times with for a 12672 sample signal and 186 tap filter on a Tesla K40c GPU.

Algorithm	Function or Library	Execution Time (ms)
GPU time domain global	ConvGPU	201.29
GPU time domain shared	ConvGPUsShared	180.272
GPU frequency domain	cuFFT	36.798

Table 3.7: Batched convolution execution times with for a 12672 sample signal and 21 tap filter on a Tesla K40c GPU.

Algorithm	Function or Library	Execution Time (ms)
GPU time domain global	ConvGPU	27.642
GPU time domain shared	ConvGPUsShared	20.4287
GPU frequency domain	cuFFT	36.7604

tap filter. Table 3.8 shows batched cascaded 21 and 186 tap filters convolved with a 12672 sample signal execution time.

Tables 3.6 and 3.7 agree with Figures 3.24 and 3.23. time-domain convolution is faster with a short 21 tap filter but frequency-domain convolution is faster with a long 186 tap filter.

Figure 3.26 shows two ways to cascade the signal r through two filters. The upper blocks apply both filters to the signal taking 180.272 ms then 20.4287 ms. The lower blocks first convolve the filters to build a $186 + 21 - 1$ tap composite filter then apply the 206 tap composite to the signal.

Table 3.8: Batched convolution execution times with for a 12672 sample signal and cascaded 21 and 186 tap filter on a Tesla K40c GPU.

Algorithm	Function or Library	Execution Time (ms)
GPU time domain global	ConvGPU	223.307
GPU time domain shared	ConvGPUsShared	200.018
GPU frequency domain	cuFFT	39.0769

Table 3.9: Batched convolution execution times with for a 12672 sample signal and 206 tap filter on a Tesla K40c GPU.

Algorithm	Function or Library	Execution Time (ms)
GPU time domain global	ConvGPU	223.064
GPU time domain shared	ConvGPUsshared	199.844
GPU frequency domain	cuFFT	36.7704

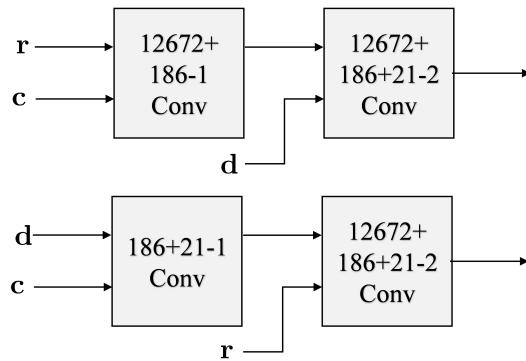


Figure 3.26: Two ways to convolve the signal r with the 186 tap filter c and 21 tap filter d .

Table 3.8 shows the execution time of implementing cascaded filters, convolving the 21 and 186 tap filters is extremely fast in the GPU. While building the composite filter is extremely fast, time-domain convolution suffers a 22.0170 ms or 19.7460 ms slow down because the composite filter is now 206 taps. Applying an extra filter in the frequency domain only costs 2.3165 ms. Table 3.9 confirms it costs an extra 20 ms or so to apply a 206 vs 186 tap filter.

Listing 3.5: CUDA code to performing complex convolution five different ways: time domain CPU, frequency domain CPU time domain GPU, time domain GPU using shared memory and frequency domain GPU.

```

1 #include <iostream>
2 #include <stdlib.h>
3 #include <math.h>
4 #include <cufft.h>
5 #include <fstream>
6 #include <string>
7 #include <fftw3.h>
8 using namespace std;
9
10
11 void ConvCPU(cufftComplex* y,cufftComplex* x,cufftComplex* h,int Lx,int Lh){
12     for(int yIdx = 0; yIdx < Lx+Lh-1; yIdx++){
13         cufftComplex temp;
14         temp.x = 0;
15         temp.y = 0;
16         for(int hIdx = 0; hIdx < Lh; hIdx++){
17             int xAccessIdx = yIdx-hIdx;
18             if(xAccessIdx>=0 && xAccessIdx<Lx) {
19                 // temp += x[xAccessIdx]*h[hIdx];
20                 float A = x[xAccessIdx].x;
21                 float B = x[xAccessIdx].y;
22                 float C = h[hIdx].x;
23                 float D = h[hIdx].y;
24                 cufftComplex result;
25                 result.x = A*C-B*D;
26                 result.y = A*D+B*C;
27                 temp.x += result.x;
28                 temp.y += result.y;
29             }
30         }
31         y[yIdx] = temp;
32     }
33 }
34 }
35
36 __global__ void ConvGPU(cufftComplex* y,cufftComplex* x,cufftComplex* h,int Lx,int Lh){
37     int yIdx = blockIdx.x*blockDim.x + threadIdx.x;
38
39     int lastThread = Lx+Lh-1;
40
41     // don't access elements out of bounds
42     if(yIdx >= lastThread)
43         return;
44
45     cufftComplex temp;
46     temp.x = 0;
47     temp.y = 0;
48     for(int hIdx = 0; hIdx < Lh; hIdx++){
49         int xAccessIdx = yIdx-hIdx;
50         if(xAccessIdx>=0 && xAccessIdx<Lx) {
51             // temp += x[xAccessIdx]*h[hIdx];
52             float A = x[xAccessIdx].x;
53             float B = x[xAccessIdx].y;
54             float C = h[hIdx].x;
55             float D = h[hIdx].y;
56             cufftComplex result;
57             result.x = A*C-B*D;
58             result.y = A*D+B*C;
59             temp.x += result.x;
60             temp.y += result.y;
61         }
62     }
63     y[yIdx] = temp;
64 }
```

```

65
66
67 __global__ void ConvGPUshared(cufftComplex* y,cufftComplex* x,cufftComplex* h,int Lx,int Lh) {
68     int yIdx = blockIdx.x*blockDim.x + threadIdx.x;
69
70     int lastThread = Lx+Lh-1;
71
72     extern __shared__ cufftComplex h_shared[];
73     if(threadIdx.x < Lh) {
74         h_shared[threadIdx.x] = h[threadIdx.x];
75     }
76     __syncthreads();
77
78     // don't access elements out of bounds
79     if(yIdx >= lastThread)
80         return;
81
82     cufftComplex temp;
83     temp.x = 0;
84     temp.y = 0;
85     for(int hIdx = 0; hIdx < Lh; hIdx++){
86         int xAccessIdx = yIdx-hIdx;
87         if(xAccessIdx>=0 && xAccessIdx<Lx) {
88             // temp += x[xAccessIdx]*h[hIdx];
89             float A = x[xAccessIdx].x;
90             float B = x[xAccessIdx].y;
91             float C = h_shared[hIdx].x;
92             float D = h_shared[hIdx].y;
93             cufftComplex result;
94             result.x = A*C-B*D;
95             result.y = A*D+B*C;
96             temp.x += result.x;
97             temp.y += result.y;
98         }
99     }
100    y[yIdx] = temp;
101 }
102
103 __global__ void PointToPointMultiply(cufftComplex* v0, cufftComplex* v1, int lastThread) {
104     int i = blockIdx.x*blockDim.x + threadIdx.x;
105
106     // don't access elements out of bounds
107     if(i >= lastThread)
108         return;
109     float A = v0[i].x;
110     float B = v0[i].y;
111     float C = v1[i].x;
112     float D = v1[i].y;
113
114     // (A+jB) (C+jD) = (AC-BD) + j(AD+BC)
115     cufftComplex result;
116     result.x = A*C-B*D;
117     result.y = A*D+B*C;
118
119     v0[i] = result;
120 }
121
122 __global__ void ScalarMultiply(cufftComplex* vec0, float scalar, int lastThread) {
123     int i = blockIdx.x*blockDim.x + threadIdx.x;
124
125     // Don't access elements out of bounds
126     if(i >= lastThread)
127         return;
128     cufftComplex scalarMult;
129     scalarMult.x = vec0[i].x*scalar;
130     scalarMult.y = vec0[i].y*scalar;
131     vec0[i] = scalarMult;
132 }

```

```

133
134 int main(){
135     int mySignalLength = 1000;
136     int myFilterLength = 186;
137     int myConvLength    = mySignalLength + myFilterLength - 1;
138     int Nfft           = pow(2, ceil(log(myConvLength)/log(2)));
139
140     cufftComplex *mySignal1;
141     cufftComplex *mySignal2;
142     cufftComplex *mySignal2_fft;
143
144     cufftComplex *myFilter1;
145     cufftComplex *myFilter2;
146     cufftComplex *myFilter2_fft;
147
148     cufftComplex *myConv1;
149     cufftComplex *myConv2;
150     cufftComplex *myConv2_timeReversed;
151     cufftComplex *myConv3;
152     cufftComplex *myConv4;
153     cufftComplex *myConv5;
154
155     mySignal1           = (cufftComplex*)malloc(mySignalLength*sizeof(cufftComplex));
156     mySignal2           = (cufftComplex*)malloc(Nfft           *sizeof(cufftComplex));
157     mySignal2_fft       = (cufftComplex*)malloc(Nfft           *sizeof(cufftComplex));
158
159     myFilter1           = (cufftComplex*)malloc(myFilterLength*sizeof(cufftComplex));
160     myFilter2           = (cufftComplex*)malloc(Nfft           *sizeof(cufftComplex));
161     myFilter2_fft       = (cufftComplex*)malloc(Nfft           *sizeof(cufftComplex));
162
163     myConv1             = (cufftComplex*)malloc(myConvLength  *sizeof(cufftComplex));
164     myConv2             = (cufftComplex*)malloc(Nfft           *sizeof(cufftComplex));
165     myConv2_timeReversed= (cufftComplex*)malloc(Nfft           *sizeof(cufftComplex));
166     myConv3             = (cufftComplex*)malloc(myConvLength  *sizeof(cufftComplex));
167     myConv4             = (cufftComplex*)malloc(myConvLength  *sizeof(cufftComplex));
168     myConv5             = (cufftComplex*)malloc(Nfft           *sizeof(cufftComplex));
169
170     srand(time(0));
171     for(int i = 0; i < mySignalLength; i++){
172         mySignal1[i].x = rand()%100-50;
173         mySignal1[i].y = rand()%100-50;
174     }
175
176     for(int i = 0; i < myFilterLength; i++){
177         myFilter1[i].x = rand()%100-50;
178         myFilter1[i].y = rand()%100-50;
179     }
180
181     cufftComplex *dev_mySignal3;
182     cufftComplex *dev_mySignal4;
183     cufftComplex *dev_mySignal5;
184
185     cufftComplex *dev_myFilter3;
186     cufftComplex *dev_myFilter4;
187     cufftComplex *dev_myFilter5;
188
189     cufftComplex *dev_myConv3;
190     cufftComplex *dev_myConv4;
191     cufftComplex *dev_myConv5;
192
193     cudaMalloc(&dev_mySignal3, mySignalLength*sizeof(cufftComplex));
194     cudaMalloc(&dev_mySignal4, mySignalLength*sizeof(cufftComplex));
195     cudaMalloc(&dev_mySignal5, Nfft           *sizeof(cufftComplex));
196
197     cudaMalloc(&dev_myFilter3, myFilterLength*sizeof(cufftComplex));
198     cudaMalloc(&dev_myFilter4, myFilterLength*sizeof(cufftComplex));
199     cudaMalloc(&dev_myFilter5, Nfft           *sizeof(cufftComplex));
200

```

```

201     cudaMalloc(&dev_myConv3,    myConvLength *sizeof(cufftComplex));
202     cudaMalloc(&dev_myConv4,    myConvLength *sizeof(cufftComplex));
203     cudaMalloc(&dev_myConv5,    Nfft           *sizeof(cufftComplex));
204
205
206     /**
207      * Time-domain Convolution CPU
208      */
209     ConvCPU(myConv1,mySignal1,myFilter1,mySignalLength,myFilterLength);
210
211     /**
212      * Frequency Domain Convolution CPU
213      */
214     fftwf_plan forwardPlanSignal = fftwf_plan_dft_1d(Nfft, (fftwf_complex*)mySignal2, (fftwf_complex*)mySignal2_fft, FFTW_FORWARD, FFTW_MEASURE);
215     fftwf_plan forwardPlanFilter = fftwf_plan_dft_1d(Nfft, (fftwf_complex*)myFilter2, (fftwf_complex*)myFilter2_fft, FFTW_FORWARD, FFTW_MEASURE);
216     fftwf_plan backwardPlanConv = fftwf_plan_dft_1d(Nfft, (fftwf_complex*)mySignal2_fft, (fftwf_complex*)myConv2_timeReversed, FFTW_FORWARD, FFTW_MEASURE);
217
218     cufftComplex zero; zero.x = 0; zero.y = 0;
219     for(int i = 0; i < Nfft; i++){
220         if(i<mySignalLength)
221             mySignal2[i] = mySignal1[i];
222         else
223             mySignal2[i] = zero;
224
225         if(i<myFilterLength)
226             myFilter2[i] = myFilter1[i];
227         else
228             myFilter2[i] = zero;
229     }
230
231     fftwf_execute(forwardPlanSignal);
232     fftwf_execute(forwardPlanFilter);
233
234     for (int i = 0; i < Nfft; i++){
235         // mySignal2_fft = mySignal2_fft*myFilter2_fft;
236         float A = mySignal2_fft[i].x;
237         float B = mySignal2_fft[i].y;
238         float C = myFilter2_fft[i].x;
239         float D = myFilter2_fft[i].y;
240         cufftComplex result;
241         result.x = A*C-B*D;
242         result.y = A*D+B*C;
243         mySignal2_fft[i] = result;
244     }
245
246     fftwf_execute(backwardPlanConv);
247
248     // myConv2 from fftwf must be time reversed and scaled
249     // to match Matlab, myConv1, myConv3, myConv4 and myConv5
250     cufftComplex result;
251     for (int i = 0; i < Nfft; i++){
252         result.x = myConv2_timeReversed[Nfft-i].x/Nfft;
253         result.y = myConv2_timeReversed[Nfft-i].y/Nfft;
254         myConv2[i] = result;
255     }
256     result.x = myConv2_timeReversed[0].x/Nfft;
257     result.y = myConv2_timeReversed[0].y/Nfft;
258     myConv2[0] = result;
259
260     fftwf_destroy_plan(forwardPlanSignal);
261     fftwf_destroy_plan(forwardPlanFilter);
262     fftwf_destroy_plan(backwardPlanConv);
263
264     /**

```

```

266     * Time-domain Convolution GPU Using Global Memory
267     */
268     cudaMemcpy(dev_mySignal3, mySignal1, sizeof(cufftComplex)*mySignalLength,
269             cudaMemcpyHostToDevice);
270     cudaMemcpy(dev_myFilter3, myFilter1, sizeof(cufftComplex)*myFilterLength,
271             cudaMemcpyHostToDevice);
272
273     int T_B = 512;
274     int B = myConvLength/T_B;
275     if(myConvLength % T_B > 0)
276         B++;
277     ConvGPU<<<B, T_B>>>(dev_myConv3, dev_mySignal3, dev_myFilter3, mySignalLength,
278                             myFilterLength);
279
280     cudaMemcpy(myConv3, dev_myConv3, myConvLength*sizeof(cufftComplex),
281             cudaMemcpyDeviceToHost);
282
283 /**
284     * Time-domain Convolution GPU Using Shared Memory
285     */
286     cudaMemcpy(dev_mySignal4, mySignal1, sizeof(cufftComplex)*mySignalLength,
287             cudaMemcpyHostToDevice);
288     cudaMemcpy(dev_myFilter4, myFilter1, sizeof(cufftComplex)*myFilterLength,
289             cudaMemcpyHostToDevice);
290
291     T_B = 512;
292     B = myConvLength/T_B;
293     if(myConvLength % T_B > 0)
294         B++;
295     ConvGPUshared<<<B, T_B,myFilterLength*sizeof(cufftComplex)>>>(dev_myConv4, dev_mySignal4,
296                         dev_myFilter4, mySignalLength, myFilterLength);
297
298     cudaMemcpy(myConv4, dev_myConv4, myConvLength*sizeof(cufftComplex),
299             cudaMemcpyDeviceToHost);
299
300 /**
301     * Frequency-domain Convolution GPU
302     */
303     cufftHandle plan;
304     int n[1] = {Nfft};
305     cufftPlanMany(&plan, 1, n, NULL, 1, 1, NULL, 1, 1, CUFFT_C2C, 1);
306
307     cudaMemset(dev_mySignal5, 0, Nfft*sizeof(cufftComplex));
308     cudaMemset(dev_myFilter5, 0, Nfft*sizeof(cufftComplex));
309
310     cudaMemcpy(dev_mySignal5, mySignal2, Nfft*sizeof(cufftComplex), cudaMemcpyHostToDevice);
311     cudaMemcpy(dev_myFilter5, myFilter2, Nfft*sizeof(cufftComplex), cudaMemcpyHostToDevice);
312
313     cufftExecC2C(plan, dev_mySignal5, dev_mySignal5, CUFFT_FORWARD);
314     cufftExecC2C(plan, dev_myFilter5, dev_myFilter5, CUFFT_FORWARD);
315
316     T_B = 512;
317     B = Nfft/T_B;
318     if(Nfft % T_B > 0)
319         B++;
320     PointToPointMultiply<<<B, T_B>>>(dev_mySignal5, dev_myFilter5, Nfft);
321
322     cufftExecC2C(plan, dev_mySignal5, dev_mySignal5, CUFFT_INVERSE);
323
324     T_B = 128;
325     B = Nfft/T_B;
326     if(Nfft % T_B > 0)
327         B++;
328     float scalar = 1.0/((float)Nfft);
329     ScalarMultiply<<<B, T_B>>>(dev_mySignal5, scalar, Nfft);

```

```

326     cudaMemcpy(myConv5, dev_mySignals5, Nfft*sizeof(cufftComplex), cudaMemcpyDeviceToHost);
327
328     cufftDestroy(plan);
329
330     free(mySignal1);
331     free(mySignal2);
332
333     free(myFilter1);
334     free(myFilter2);
335
336     free(myConv1);
337     free(myConv2);
338     free(myConv2_timeReversed);
339     free(myConv3);
340     free(myConv4);
341     free(myConv5);
342     fftwf_cleanup();
343
344     cudaFree(dev_mySignal3);
345     cudaFree(dev_mySignal4);
346     cudaFree(dev_mySignal5);
347
348     cudaFree(dev_myFilter3);
349     cudaFree(dev_myFilter4);
350     cudaFree(dev_myFilter5);
351
352     cudaFree(dev_myConv3);
353     cudaFree(dev_myConv4);
354     cudaFree(dev_myConv5);
355
356     return 0;
357 }
```

Listing 3.6: CUDA code to perform batched complex convolution three different ways in a GPU: time domain using global memory, time domain using shared memory and frequency domain GPU.

```

1 #include <cufft.h>
2 #include <iostream>
3 using namespace std;
4
5 __global__ void ConvGPU(cufftComplex* y_out, cufftComplex* x_in, cufftComplex* h_in, int Lx, int Lh,
6     int maxThreads) {
7     int threadNum = blockIdx.x*blockDim.x + threadIdx.x;
8     int convLength = Lx+Lh-1;
9
10    // Don't access elements out of bounds
11    if(threadNum >= maxThreads)
12        return;
13
14    int batch = threadNum/convLength;
15    int yIdx = threadNum%convLength;
16    cufftComplex* x = &x_in[Lx*batch];
17    cufftComplex* h = &h_in[Lh*batch];
18    cufftComplex* y = &y_out[convLength*batch];
19
20    cufftComplex temp;
21    temp.x = 0;
22    temp.y = 0;
23    for(int hIdx = 0; hIdx < Lh; hIdx++) {
24        int xAccessIdx = yIdx-hIdx;
25        if(xAccessIdx>=0 && xAccessIdx<Lx) {
26            // temp += x[xAccessIdx]*h[hIdx];
27            // (A+jB)(C+jD) = (AC-BD) + j(AD+BC)
28            float A = x[xAccessIdx].x;
29            float B = x[xAccessIdx].y;
30            float C = h[hIdx].x;
31            float D = h[hIdx].y;
32            cufftComplex complexMult;
33            complexMult.x = A*C-B*D;
34            complexMult.y = A*D+B*C;
35
36            temp.x += complexMult.x;
37            temp.y += complexMult.y;
38        }
39        y[yIdx] = temp;
40    }
41
42 __global__ void ConvGPUshared(cufftComplex* y_out, cufftComplex* x_in, cufftComplex* h_in, int Lx,
43     int Lh, int maxThreads) {
44
45    int threadNum = blockIdx.x*blockDim.x + threadIdx.x;
46    int convLength = Lx+Lh-1;
47    // Don't access elements out of bounds
48    if(threadNum >= maxThreads)
49        return;
50
51    int batch = threadNum/convLength;
52    int yIdx = threadNum%convLength;
53    cufftComplex* x = &x_in[Lx*batch];
54    cufftComplex* h = &h_in[Lh*batch];
55    cufftComplex* y = &y_out[convLength*batch];
56
57    extern __shared__ cufftComplex h_shared[];
58    if(threadIdx.x < Lh)
59        h_shared[threadIdx.x] = h[threadIdx.x];
60
61    __syncthreads();
62
63    cufftComplex temp;
64    temp.x = 0;

```

```

64     temp.y = 0;
65     for(int hIdx = 0; hIdx < Lh; hIdx++){
66         int xAccessIdx = yIdx-hIdx;
67         if(xAccessIdx>=0 && xAccessIdx<Lx) {
68             // temp += x[xAccessIdx]*h[hIdx];
69             // (A+jB) (C+jD) = (AC-BD) + j(AD+BC)
70             float A = x[xAccessIdx].x;
71             float B = x[xAccessIdx].y;
72             float C = h_shared[hIdx].x;
73             float D = h_shared[hIdx].y;
74             cufftComplex complexMult;
75             complexMult.x = A*C-B*D;
76             complexMult.y = A*D+B*C;
77
78             temp.x += complexMult.x;
79             temp.y += complexMult.y;
80         }
81     }
82     y[yIdx] = temp;
83 }
84
85 __global__ void PointToPointMultiply(cufftComplex* vec0, cufftComplex* vec1, int maxThreads) {
86     int i = blockIdx.x*blockDim.x + threadIdx.x;
87     // Don't access elements out of bounds
88     if(i >= maxThreads)
89         return;
90     // vec0[i] = vec0[i]*vec1[i];
91     // (A+jB) (C+jD) = (AC-BD) + j(AD+BC)
92     float A = vec0[i].x;
93     float B = vec0[i].y;
94     float C = vec1[i].x;
95     float D = vec1[i].y;
96     cufftComplex complexMult;
97     complexMult.x = A*C-B*D;
98     complexMult.y = A*D+B*C;
99     vec0[i] = complexMult;
100 }
101
102 __global__ void ScalarMultiply(cufftComplex* vec0, float scalar, int lastThread) {
103     int i = blockIdx.x*blockDim.x + threadIdx.x;
104     // Don't access elements out of bounds
105     if(i >= lastThread)
106         return;
107     cufftComplex scalarMult;
108     scalarMult.x = vec0[i].x*scalar;
109     scalarMult.y = vec0[i].y*scalar;
110     vec0[i] = scalarMult;
111 }
112
113 int main(){
114     int numBatches      = 3104;
115     int mySignalLength = 12672;
116     int myFilterLength = 186;
117     int myConvLength   = mySignalLength + myFilterLength - 1;
118     int Nfft           = pow(2, ceil(log(myConvLength)/log(2)));
119     int maxThreads;
120     int T_B;
121     int B;
122
123     cufftHandle plan;
124     int n[1] = {Nfft};
125     cufftPlanMany(&plan, 1, n, NULL, 1, 1, NULL, 1, 1, CUFFT_C2C, numBatches);
126
127     // Allocate memory on host
128     cufftComplex *mySignal1;
129     cufftComplex *mySignal1_pad;
130     cufftComplex *myFilter1;
131     cufftComplex *myFilter1_pad;

```

```

132     cufftComplex *myConv1;
133     cufftComplex *myConv2;
134     cufftComplex *myConv3;
135     mySignal1      = (cufftComplex*) malloc(mySignalLength*numBatches*sizeof(cufftComplex));
136     mySignal1_pad   = (cufftComplex*) malloc(Nfft           *numBatches*sizeof(cufftComplex
137             ));
137     myFilter1       = (cufftComplex*) malloc(myFilterLength*numBatches*sizeof(cufftComplex));
138     myFilter1_pad   = (cufftComplex*) malloc(Nfft           *numBatches*sizeof(cufftComplex));
139     myConv1         = (cufftComplex*) malloc(myConvLength  *numBatches*sizeof(cufftComplex));
140     myConv2         = (cufftComplex*) malloc(myConvLength  *numBatches*sizeof(cufftComplex));
141     myConv3         = (cufftComplex*) malloc(Nfft           *numBatches*sizeof(cufftComplex
142             ));
142
143     srand(time(0));
144     for(int i = 0; i < mySignalLength; i++){
145         mySignal1[i].x = rand()%100-50;
146         mySignal1[i].y = rand()%100-50;
147     }
148
149     for(int i = 0; i < myFilterLength; i++){
150         myFilter1[i].x = rand()%100-50;
151         myFilter1[i].y = rand()%100-50;
152     }
153
154     cufftComplex zero;
155     zero.x = 0;
156     zero.y = 0;
157     for(int i = 0; i<Nfft*numBatches; i++){
158         mySignal1_pad[i] = zero;
159         myFilter1_pad[i] = zero;
160     }
161     for(int batch=0; batch < numBatches; batch++){
162         for(int i = 0; i < mySignalLength; i++){
163             mySignal1[batch*mySignalLength+i] = mySignal1[i];
164             mySignal1_pad[batch*Nfft+i] = mySignal1[i];
165         }
166         for(int i = 0; i < myFilterLength; i++){
167             myFilter1[batch*myFilterLength+i] = myFilter1[i];
168             myFilter1_pad[batch*Nfft+i] = myFilter1[i];
169         }
170     }
171
172     // Allocate memory on device
173     cufftComplex *dev_mySignal1;
174     cufftComplex *dev_mySignal2;
175     cufftComplex *dev_mySignal3;
176     cufftComplex *dev_myFilter1;
177     cufftComplex *dev_myFilter2;
178     cufftComplex *dev_myFilter3;
179     cufftComplex *dev_myConv1;
180     cufftComplex *dev_myConv2;
181     cufftComplex *dev_myConv3;
182     cudaMalloc(&dev_mySignal1, mySignalLength*numBatches*sizeof(cufftComplex));
183     cudaMalloc(&dev_mySignal2, mySignalLength*numBatches*sizeof(cufftComplex));
184     cudaMalloc(&dev_mySignal3, Nfft           *numBatches*sizeof(cufftComplex));
185     cudaMalloc(&dev_myFilter1, myFilterLength*numBatches*sizeof(cufftComplex));
186     cudaMalloc(&dev_myFilter2, myFilterLength*numBatches*sizeof(cufftComplex));
187     cudaMalloc(&dev_myFilter3, Nfft           *numBatches*sizeof(cufftComplex));
188     cudaMalloc(&dev_myConv1, myConvLength  *numBatches*sizeof(cufftComplex));
189     cudaMalloc(&dev_myConv2, myConvLength  *numBatches*sizeof(cufftComplex));
190     cudaMalloc(&dev_myConv3, Nfft           *numBatches*sizeof(cufftComplex));
191
192     /**
193      * Time-domain Convolution GPU Using Global Memory
194      */
195     cudaMemcpy(dev_mySignal1, mySignal1, numBatches*sizeof(cufftComplex)*mySignalLength,
196               cudaMemcpyHostToDevice);

```

```

196     cudaMemcpy(dev_myFilter1, myFilter1, numBatches*sizeof(cufftComplex)*myFilterLength,
197                 cudaMemcpyHostToDevice);
198
199     maxThreads = myConvLength*numBatches;
200     T_B = 128;
201     B = maxThreads/T_B;
202     if(maxThreads % T_B > 0)
203         B++;
204     ConvGPU<<<B, T_B>>>(dev_myConv1, dev_mySignal1, dev_myFilter1, mySignalLength,
205                               myFilterLength, maxThreads);
206
207     cudaMemcpy(myConv1, dev_myConv1, myConvLength*numBatches*sizeof(cufftComplex),
208                 cudaMemcpyDeviceToHost);
209
210     /**
211      * Time-domain Convolution GPU Using Shared Memory
212      */
213     cudaMemcpy(dev_mySignal2, mySignal1, numBatches*sizeof(cufftComplex)*mySignalLength,
214                 cudaMemcpyHostToDevice);
215     cudaMemcpy(dev_myFilter2, myFilter1, numBatches*sizeof(cufftComplex)*myFilterLength,
216                 cudaMemcpyHostToDevice);
217
218     maxThreads = myConvLength*numBatches;
219     T_B = 256;
220     B = maxThreads/T_B;
221     if(maxThreads % T_B > 0)
222         B++;
223     ConvGPUsShared<<<B, T_B, myFilterLength*sizeof(cufftComplex)>>>(dev_myConv2, dev_mySignal2
224                               , dev_myFilter2, mySignalLength, myFilterLength,maxThreads);
225
226     cudaMemcpy(myConv2, dev_myConv2, myConvLength*numBatches*sizeof(cufftComplex),
227                 cudaMemcpyDeviceToHost);
228
229     /**
230      * Frequency-domain Convolution GPU
231      */
232     cudaMemcpy(dev_mySignal3, mySignal1_pad, Nfft*numBatches*sizeof(cufftComplex),
233                 cudaMemcpyHostToDevice);
234     cudaMemcpy(dev_myFilter3, myFilter1_pad, Nfft*numBatches*sizeof(cufftComplex),
235                 cudaMemcpyHostToDevice);
236
237     cufftExecC2C(plan, dev_mySignal3, dev_mySignal3, CUFFT_FORWARD);
238     cufftExecC2C(plan, dev_myFilter3, dev_myFilter3, CUFFT_FORWARD);
239
240     maxThreads = Nfft*numBatches;
241     T_B = 96;
242     B = maxThreads/T_B;
243     if(maxThreads % T_B > 0)
244         B++;
245     PointToPointMultiply<<<B, T_B>>>(dev_mySignal3, dev_myFilter3, maxThreads);
246     cufftExecC2C(plan, dev_mySignal3, dev_mySignal3, CUFFT_INVERSE);
247
248     T_B = 640;
249     B = maxThreads/T_B;
250     if(maxThreads % T_B > 0)
251         B++;
252     float scalar = 1.0/((float)Nfft);
253     ScalarMultiply<<<B, T_B>>>(dev_mySignal3, scalar, maxThreads);
254
255     cudaMemcpy(myConv3, dev_mySignal3, Nfft*numBatches*sizeof(cufftComplex),
256                 cudaMemcpyDeviceToHost);
257
258     cufftDestroy(plan);
259
260     // Free vectors on CPU
261     free(mySignal1);
262     free(myFilter1);
263     free(myConv1);

```

```
254     free (myConv2);
255     free (myConv3);
256
257     // Free vectors on GPU
258     cudaFree (dev_mySignal1);
259     cudaFree (dev_mySignal2);
260     cudaFree (dev_mySignal3);
261     cudaFree (dev_myFilter1);
262     cudaFree (dev_myFilter2);
263     cudaFree (dev_myFilter3);
264     cudaFree (dev_myConv1);
265     cudaFree (dev_myConv2);
266     cudaFree (dev_myConv3);
267
268     return 0;
269 }
```

Chapter 4

Equalizer GPU Implementation

Each equalizer presents an interesting challenge from a GPU implementation perspective. This is why in Chapter blah the equalizer equations were massaged and conditioned. This chapter will explain how the equalizers were computed and applied in batch processing.

Chapter 3.6 showed the true power of batched processing in GPUs. Each batch of data is totally independent of other batches. For this reason and to simplify figures, assume every block diagram in this chapter is duplicated 3104 times on the GPU. If a block diagram shows how to compute one equalizer coefficients vector, assume that the block diagram is repeated 3104 times to compute 3104 equalizer coefficient vectors.

Convolution is used many times in this chapter. Frequency domain convolution has many little steps that make a block diagram look busy. Figures 4 and 4 show how frequency domain convolution will be represented as one block in this chapter.

4.1 Zero-Forcing and MMSE GPU Implementation

The ZF and MMSE equalizer coefficient computations have exactly the same form as shown in Equations (2.19) and (2.30)

$$\mathbf{R}_{\hat{h}} \mathbf{c}_{\text{ZF}} = \hat{\mathbf{h}}_{n_0} \quad (4.1)$$

$$\mathbf{R} \mathbf{c}_{\text{MMSE}} = \hat{\mathbf{h}}_{n_0}. \quad (4.2)$$

The only difference is $\mathbf{R}_{\hat{h}}$ in ZF and \mathbf{R} in MMSE. Computing the ZF and MMSE equalizer coefficients is extremely computationally heavy.

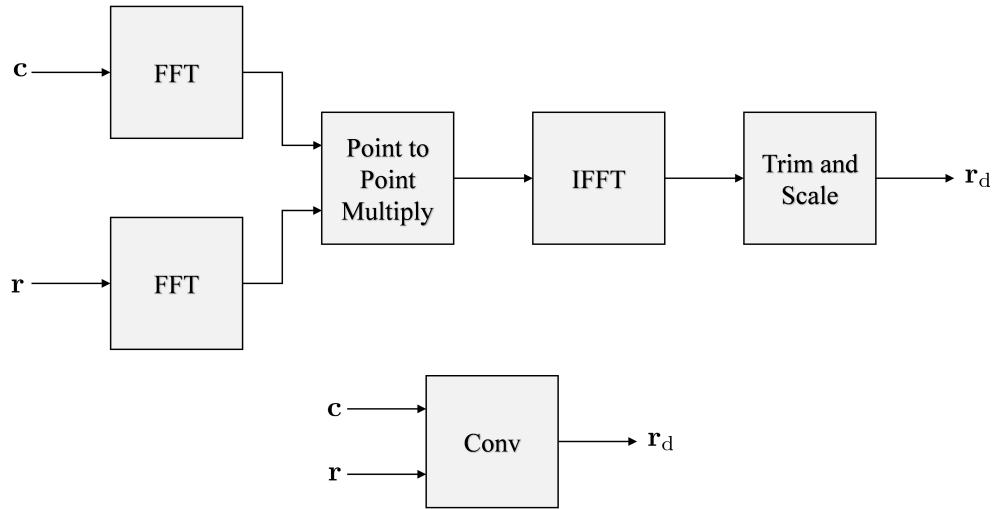


Figure 4.1: Convolution of vectors c and r block diagram simplified to one block marked Conv.

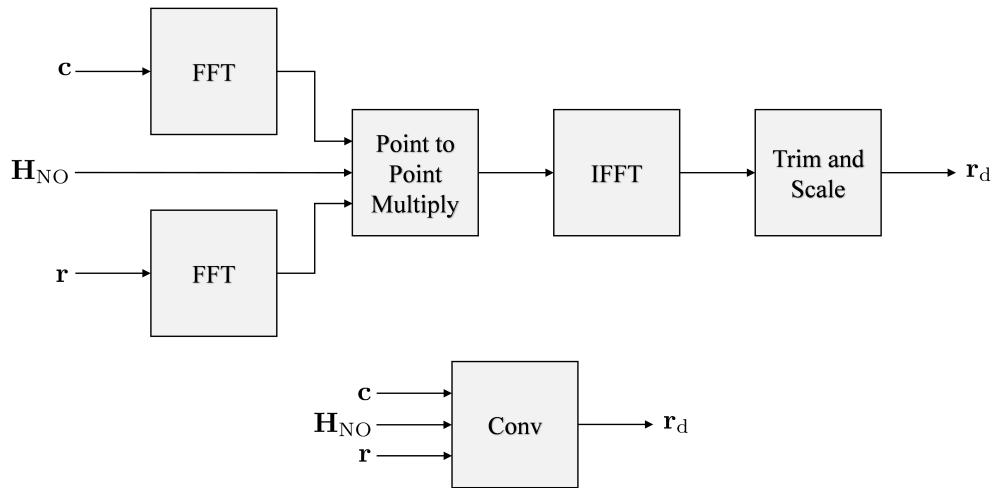


Figure 4.2: Convolution of vectors c , r and H_{NO} block diagram simplified to one block marked Conv.

It is possible to obtain the ZF and MMSE equalizer coefficients by computing the inverse of

$$\mathbf{c}_{ZF} = \mathbf{R}_{\hat{h}}^{-1} \hat{\mathbf{h}}_{n_0} \quad (4.3)$$

$$\mathbf{c}_{MMSE} = \mathbf{R}^{-1} \hat{\mathbf{h}}_{n_0}. \quad (4.4)$$

Before solving Equation (4.3), $\mathbf{R}_{\hat{h}}$ and $\hat{\mathbf{h}}_{n_0}$ need to be built and calculated given $\hat{\mathbf{h}}$. The matrix $\mathbf{R}_{\hat{h}}$ requires the sample auto-correlation of the estimated channel $\mathbf{r}_{\hat{h}}$ and the time reversed channel and shifted channel $\hat{\mathbf{h}}_{n_0}$.

The vector $\hat{\mathbf{h}}_{n_0}$ is just the time reversed and conjugated estimated channel $\hat{\mathbf{h}}$. Building $\hat{\mathbf{h}}_{n_0}$ is trivial in the GPU and very little optimizing needs to be performed. Computing the sample auto-correlation $\mathbf{r}_{\hat{h}}$ is done by implementing Equation (2.22) directly in one GPU kernel. The computation of $\mathbf{r}_{\hat{h}}$ is very fast because the length of the channel estimate L_{ch} is very short.

Section 2.2.1 showed that $\mathbf{R}_{\hat{h}}$ is sparse because $r_{\hat{h}}(k)$ only has support on $-L_{ch} \leq k \leq L_{ch}$. To reduce computation time, the sparseness of $\mathbf{R}_{\hat{h}}$ will be leveraged. With out leveraging the sparse properties of $\mathbf{R}_{\hat{h}}$, even the mighty Tesla K40c cannot produce \mathbf{c}_{ZF} in less than 500ms.

The sparseness of $\mathbf{R}_{\hat{h}}$ is leveraged using a sparse solver function called “cusolverSpCcsqrsvBatched”. cusolverSpCcsqrsvBatched is a batched complex solver that leverages the sparse properties of $\mathbf{R}_{\hat{h}}$ by utilizing Compressed Row Storage (CRS) [15]. The Compressed Row Storage reduces a large 186×186 matrix $\mathbf{R}_{\hat{h}}$ to a 12544 element CSR matrix $\mathbf{R}_{\hat{h}_{CRS}}$. Before cusolverSpCcsqrsvBatched can be called, the CSR matrix $\mathbf{R}_{\hat{h}_{CRS}}$ has to be built using $\mathbf{r}_{\hat{h}}$. An example of how to use the CUDA cusolverSp library can be found [10].

Figure 4.1 shows how the Zero-Forcing equalizer coefficients are implemented in the GPU. The MMSE equalizer coefficients are computed nearly identically to ZF accept when calculating $\mathbf{R}_{\hat{h}_{CRS}}$, $\hat{\sigma}_w^2$ is added to the main diagonal elements.

Using cusolverSpCcsqrsvBatched wasn’t the only implementation researched. Table 4.1 lists the algorithms researched and their respective execution times. A custom GPU Levinson Recursion algorithm was built to leverage the Toeplitz structure of $\mathbf{R}_{\hat{h}}$ and \mathbf{R} [16, Chap. 5]. The Levinson Recursion algorithm initially showed promise when operating on real floats but when converted to complex data Levinson wasn’t feasable.

Rather than solving for \mathbf{c}_{ZF} or \mathbf{c}_{MMSE} , computing the full inverse of $\mathbf{R}_{\hat{h}}$ was researched using the cuBLAS LU Decomposition. While using staying real time using cuBLAS was feasable, cusolverSp out performed cuBLAS by almost $2\times$.

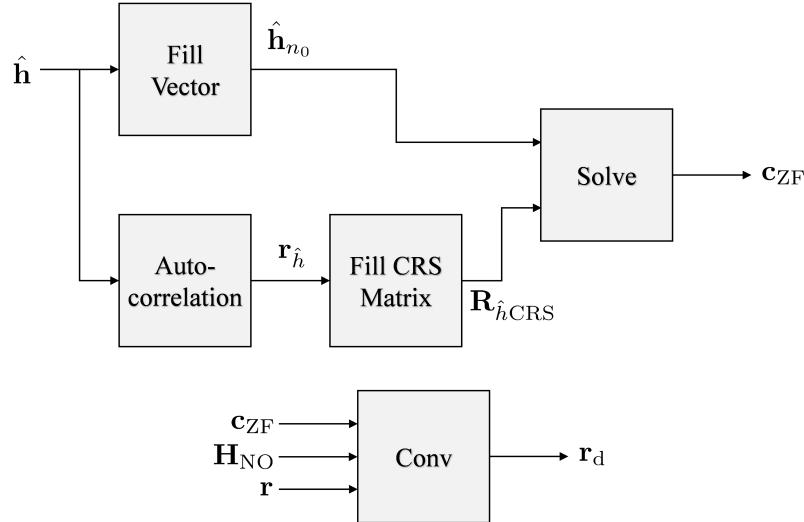


Figure 4.3: Block Diagram showing how the Zero-Forcing equalizer coefficients are implemented in the GPU.

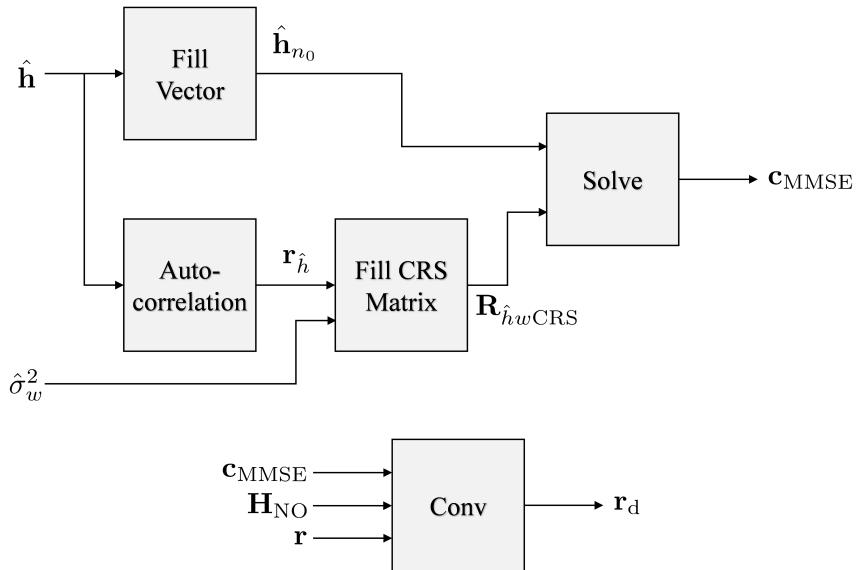


Figure 4.4: Block Diagram showing how the Minimum Mean Squared Error equalizer coefficients are implemented in the GPU.

Table 4.1: Defining start and stop lines for timing comparison in Listing 3.5.

Algorithm	Data type	Execution Time (ms)
Levinson Recursion	floats	500
Levinson Recursion	Complex	2500
LU Decomposition	Complex	600
cuSolver	Complex	355.96

4.2 Constant Modulus Algorithm GPU Implementation

The Constant Modulus Algorithm (CMA) is quite a bit more complicated than all other equalizers. CMA presented real challenges when implementing into a GPU. The direct approach didn't allow for multiple iterations. The more iterations CMA performed, the better CMA becomes because CMA is a steepest decent.

Each iteration of CMA uses the signal equalized by the most recent $\mathbf{c}_{\text{CMA}b}$

$$\mathbf{y} = \mathbf{r} * \mathbf{c}_{\text{CMA}b}. \quad (4.5)$$

The element of the gradient $\nabla J(k)$ is calculate by convolving the 12672 sample \mathbf{z} and with the 12672 sample ρ . Note that all other frequency domain convolutions in this Thesis are $\text{Nfft} = 2^{14}$, but the convolution length $12672 + 12672 - 1 > 2^{14}$. The FFTs in the computation of $\nabla J(k)$ are $\text{Nfft} = 2^{15}$ point FFTs. The element of the gradient vector $\nabla J(k)$ is calculated by

$$\nabla J(k) = \frac{1}{L_{pkt}} b(k), \quad -L_1 \leq k \leq L_2 \quad (4.6)$$

where

$$\begin{aligned} b(n) &= \sum_{m=0}^{L_{pkt}-1} z(m)\rho(n-m) \\ &= \sum_{m=0}^{L_{pkt}-1} z(m)r^*(m-n) \end{aligned} \quad (4.7)$$

using convolution. Once ∇J is calculated, the steepest decent algorithm is applied

$$\mathbf{c}_{\text{CMA}(b+1)} = \mathbf{c}_{\text{CMA}(b)} - \mu \nabla J. \quad (4.8)$$

The goal of CMA is to perform as many iterations as possible. Once done iterating, apply the last $\mathbf{c}_{\text{CMA}(b+1)}$ to the received signal \mathbf{r} .

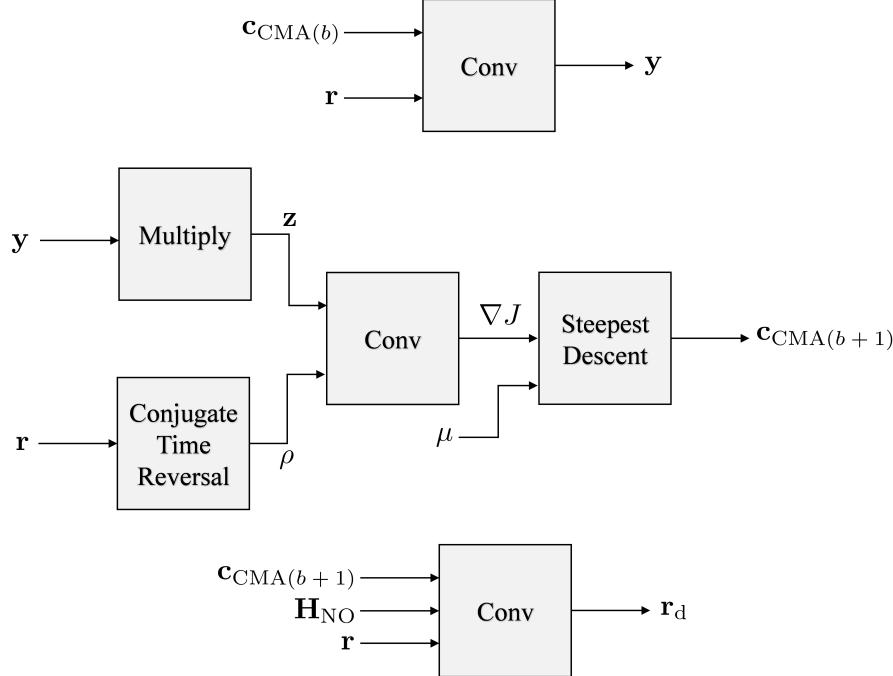


Figure 4.5: Diagram showing the relationships between $z(n)$, $\rho(n)$ and $b(n)$.

In Section 2.2.2, the direct application of CMA was massaged into convolution. Figure 4.2 shows a block diagram of how the CMA algorithm runs on the GPU.

The most computationally heavy part of CMA is computing $\nabla J(k)$. Computing $\nabla J(k)$ directly is almost $5\times$ slower than using convolution. The direct computation is done by performing a long 12672 sample summation from Equation (2.40)

$$\nabla J(k) = \frac{1}{L_{pkt}} \sum_{m=0}^{L_{pkt}-1} z(m)r^*(m-k), \quad -L_1 \leq k \leq L_2. \quad (4.9)$$

Long summations are slow in GPUs. Table 4.2 lists the comparison on computing $\nabla J(k)$ verse using convolution.

Table 4.2: The gradient vector $\nabla J(k)$ can be computed using convolution or computed directly.

CMA Iteration Algorithm	Execution Time (ms)
∇J directly	421.317
∇J using convolution	88.7743

Table 4.3: Defining start and stop lines for timing comparison in Listing 3.5.

Algorithm	Execution Time (ms)
Frequency Domain Equalizer One	57.156
Frequency Domain Equalizer Two	58.841

4.3 Frequency Domain Equalizer One and Two GPU Implementation

The Frequency Domain Equalizers are by far the fastest and easiest to implement into GPUs. The block diagram looks just like convolution accept that point to point multiply isn't a simple two or three point complex multiply.

Equation (2.45) and is implemented directly in the GPU. To save execution time, the FFT of the detection filter \mathbf{H}_{NO} multiplied at the same time FDE1 is calculated

$$R_{d1}(e^{j\omega_k}) = \frac{R(e^{j\omega_k})\hat{H}^*(e^{j\omega_k})H_{\text{NO}}(e^{j\omega_k})}{|\hat{H}(e^{j\omega_k})|^2 + \frac{1}{\hat{\sigma}_w^2}} \quad \text{where } \omega_k = \frac{2\pi}{L} \text{ for } k = 0, 1, \dots, L-1 \quad (4.10)$$

$$R_{d2}(e^{j\omega_k}) = \frac{R(e^{j\omega_k})\hat{H}^*(e^{j\omega_k})H_{\text{NO}}(e^{j\omega_k})}{|\hat{H}(e^{j\omega_k})|^2 + \frac{\Psi(e^{j\omega_k})}{\hat{\sigma}_w^2}} \quad \text{where } \omega_k = \frac{2\pi}{L} \text{ for } k = 0, 1, \dots, L-1 \quad (4.11)$$

where $R(e^{j\omega_k})$ and $R_d(e^{j\omega_k})$ is the FFT \mathbf{r} and \mathbf{r}_d at ω_k . Figures 4.3 and 4.3 show block diagrams of how FDE1 and FDE2 are implemented in the GPUs.

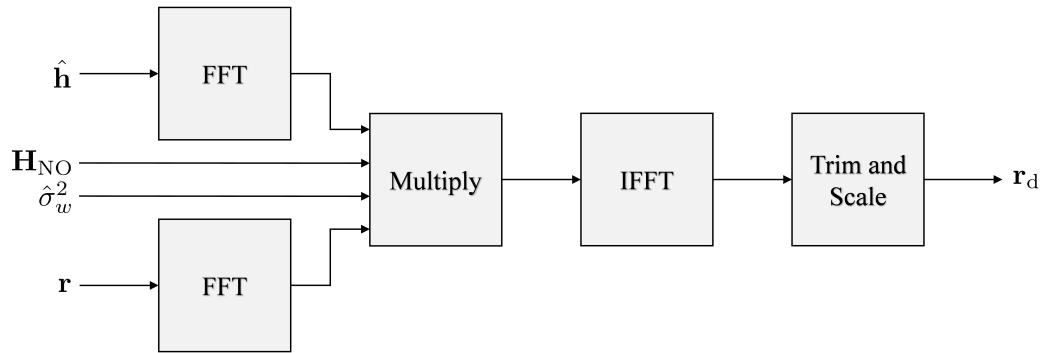


Figure 4.6: Diagram showing Frequency Domain Equalizer One is implemented in the frequency domain in GPUs.

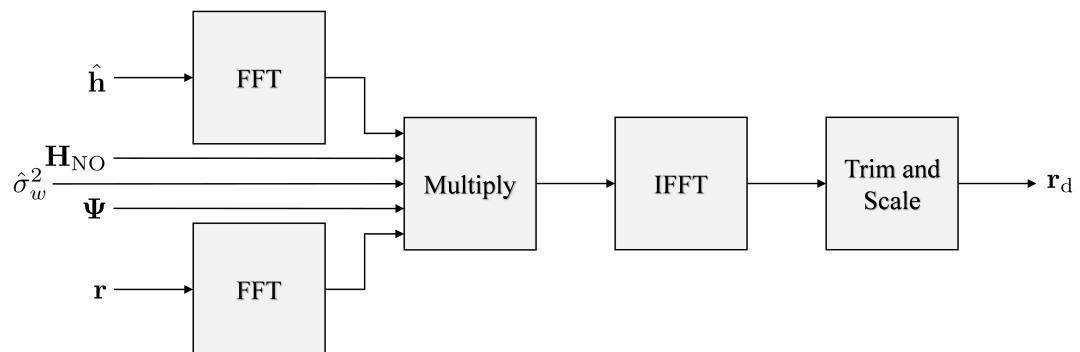


Figure 4.7: Diagram showing Frequency Domain Equalizer Two is implemented in the frequency domain in GPUs.

Chapter 5

Final Summary

this is the final summary

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