24.2.3 Mode Comparison

The comparison table of programming and erasing related items about boot mode, user program mode, user boot mode, and programmer mode is shown in table 24.2.

Table 24.2 Comparison of Programming Modes

	Boot Mode	User Program Mode	User Boot Mode	Programmer Mode
Programming/ erasing environment	On-board programming	On-board programming	On-board programming	Off-board programming
Programming/ erasing enable MAT	User MAT User boot MAT	User MAT	User MAT	User MAT User boot MAT
Programming/ erasing control	Command method	Programming/ erasing interface	Programming/ erasing interface	Command method
All erasure	O (Automatic)	O	O	O (Automatic)
Block division erasure	O*[1]	O	O	X
Program data transfer	From host via SCI	From optional device via RAM	From optional device via RAM	Via programmer
User branch function	X	O	O	X
RAM emulation	X	O	X	X
Reset initiation MAT	Embedded program storage MAT	User MAT	User boot MAT*[2]	Embedded program storage MAT
Transition to user mode	Mode setting change and reset	FWE setting change	Mode setting change and reset	—

Notes: 1. All-erasure is performed. After that, the specified block can be erased.
2. Initiation starts from the embedded program storage MAT. After checking the flash-memory related registers, initiation starts from the reset vector of the user MAT.

- The user boot MAT can be programmed or erased only in boot mode and programmer mode.
- The user MAT and user boot MAT are all erased in boot mode. Then, the user MAT and user boot MAT can be programmed by means of the command method. However, the contents of the MAT cannot be read until this state. Only user boot MAT is programmed and the user MAT is programmed in user boot mode or only user MAT is programmed because user boot mode is not used.
- In user boot mode, the boot operation of the optional interface can be performed by a mode pin setting different from user program mode.

24.2.4 Flash Memory Configuration

This LSI's flash memory is configured by the 1-Mbyte user MAT and 12-Kbyte user boot MAT.

The start address is allocated to the same address in the user MAT and user boot MAT. Therefore, when the program execution or data access is performed between the two MATs, the MAT must be switched by using FMATS. The user MAT is divided into two 512-Kbyte banks (bank 0 and bank 1).

The user MAT or user boot MAT can be read in all modes if it is in ROM valid mode. However, the user boot MAT can be programmed only in boot mode and programmer mode.

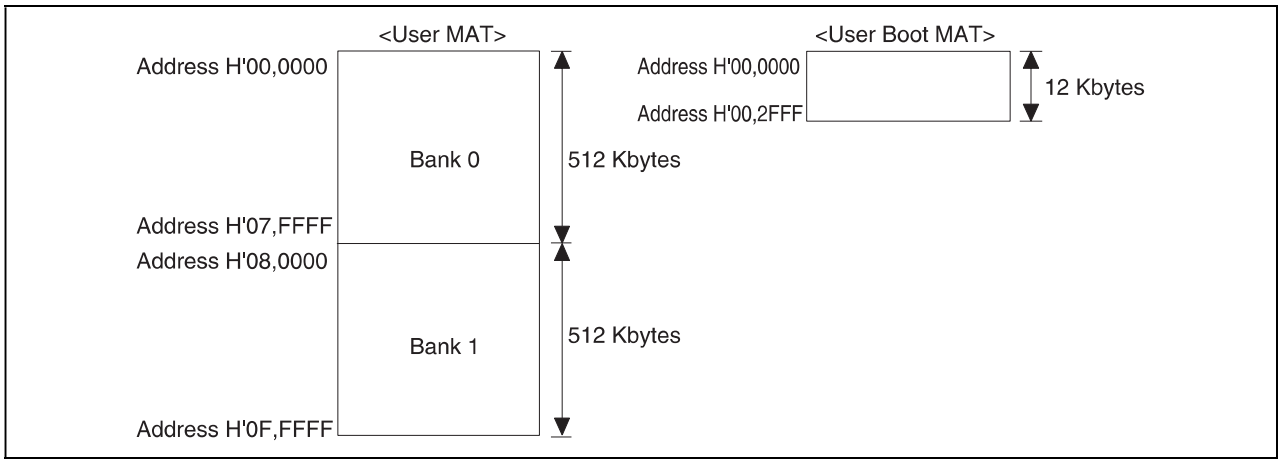

Figure 24.3 Flash Memory Configuration

The user MAT and user boot MAT have different memory sizes. Do not access a user boot MAT that is 12 Kbytes or more. When a user boot MAT exceeding 12 Kbytes is read from, an undefined value is read.

24.2.5 Block Division

The user MAT is divided into 128 Kbytes (seven blocks), 96 Kbytes (one block), and 4 Kbytes (eight blocks) as shown in figure 24.4. The user MAT can be erased in this divided-block units and the erase-block number of EB0 to EB15 is specified when erasing.

The RAM emulation can be performed in the eight blocks of 4 Kbytes.

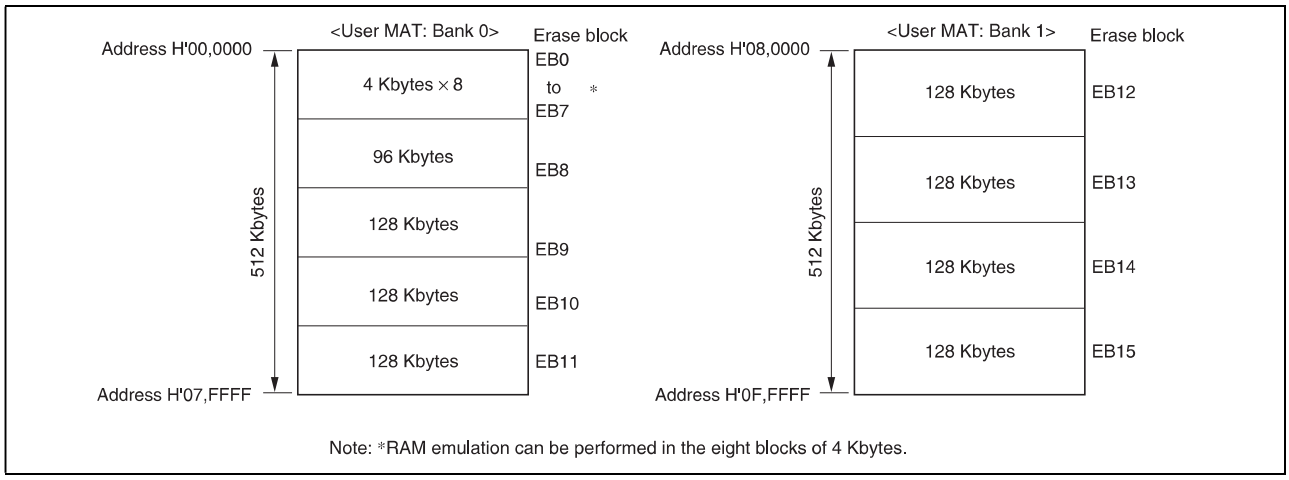

Figure 24.4 Block Division of User MAT

24.2.6 Programming/Erasing Interface

Programming/erasing is executed by downloading the on-chip program to the on-chip RAM and specifying the program address/data and erase block by using the interface registers/parameters.

The procedure program is made by the user in user program mode and user boot mode. The overview of the procedure is as follows. For details, see section 24.5.2, User Program Mode.

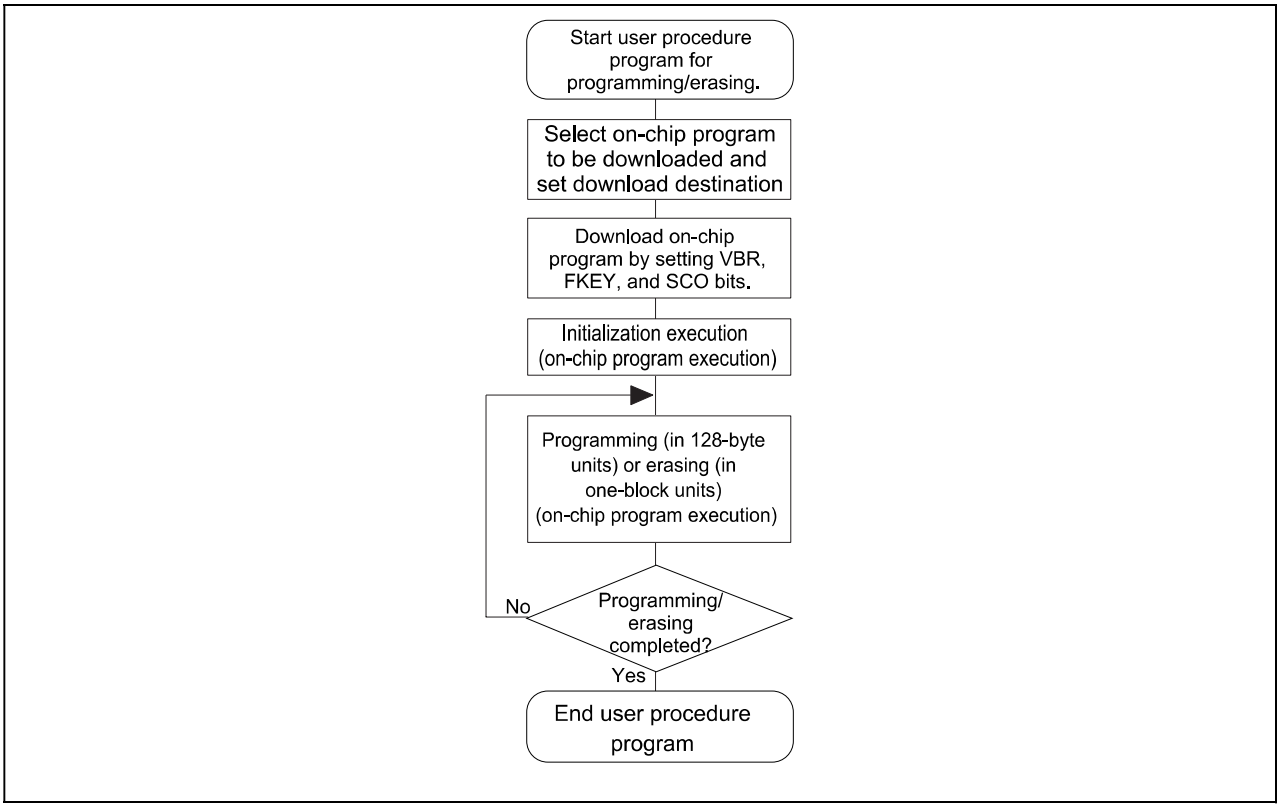

Figure 24.5 Overview of User Procedure Program

(1) Selection of On-Chip Program to be Downloaded and Setting of Download Destination

This LSI has programming/erasing programs and they can be downloaded to the on-chip RAM. The on-chip program to be downloaded is selected by setting the corresponding bits in the programming/erasing interface registers. The download destination can be specified by FTDAR.

(2) Download of On-Chip Program

The on-chip program is automatically downloaded by clearing VBR of the CPU to H'00000000 and then setting the SCO bit in the flash key code register (FKEY) and the flash code control and status register (FCCS), which are programming/erasing interface registers.

The user MAT is replaced to the embedded program storage area when downloading. Since the flash memory cannot be read when programming/erasing, the procedure program, which is working from download to completion of programming/erasing, must be executed in a space other than the flash memory to be programmed/erased (for example, on-chip RAM).

Since the result of download is returned to the programming/erasing interface parameters, whether the normal download is executed or not can be confirmed.

Note that VBR can be changed after download is completed.

(3) Initialization of Programming/Erasing

The operating frequency and user branch are set before execution of programming/erasing. The user branch destination must be in an area other than the user MAT area which is in the middle of programming and the area where the on-chip program is downloaded. These settings are performed by using the programming/erasing interface parameters.

(4) Programming/Erasing Execution

To program or erase, the FWE pin must be brought high and user program mode must be entered.

The program data/programming destination address is specified in 128-byte units when programming.

The block to be erased is specified in erase-block units when erasing.

These specifications are set by using the programming/erasing interface parameters and the on-chip program is initiated. The on-chip program is executed by using the JSR or BSR instruction to perform the subroutine call of the specified address in the on-chip RAM. The execution result is returned to the programming/erasing interface parameters.

The area to be programmed must be erased in advance when programming flash memory.

There are limitations and notes on the interrupt processing during programming/erasing. For details, see section 24.8.2, Interrupts during Programming/Erasing.

(5) When Programming/Erasing is Executed Consecutively

When the processing is not ended by the 128-byte programming or one-block erasure, the program address/data and erase-block number must be updated and consecutive programming/erasing is required.

Since the downloaded on-chip program is left in the on-chip RAM after the processing, download and initialization are not required when the same processing is executed consecutively.

24.3 Pin Configuration

Flash memory is controlled by the pins as shown in table 24.3.

Table 24.3 Pin Configuration

Pin Name	Abbreviation	Input/Output	Function
Power-on reset	$\overline{\text{RES}}$	Input	Reset
Flash programming enable	FWE	Input	Hardware protection when programming flash memory
Mode 2	MD2	Input	Sets operating mode of this LSI
Mode 1	MD1	Input	Sets operating mode of this LSI
Mode 0	MD0	Input	Sets operating mode of this LSI
Transmit data	TxD1	Output	Serial transmit data output (used in boot mode)
Receive data	RxD1	Input	Serial receive data input (used in boot mode)

Note: For the pin configuration in PROM mode, see section 24.9, Programmer Mode.

24.4 Register Configuration

24.4.1 Registers

The registers/parameters which control flash memory when the on-chip flash memory is valid are shown in table 24.4.

There are several operating modes for accessing flash memory, for example, read mode/program mode.

There are two memory MATs: user MAT and user boot MAT. The dedicated registers/parameters are allocated for each operating mode and MAT selection. The correspondence of operating modes and registers/parameters for use is shown in table 24.5.

Table 24.4 (1) Register Configuration

Name	Abbreviation*4	R/W	Initial Value	Address	Access Size
Flash code control status register	FCCS	R, W*1	H'00*2 H'80*2	H'FFFFE800	8
Flash program code select register	FPCS	R/W	H'00	H'FFFFE801	8
Flash erase code select register	FECS	R/W	H'00	H'FFFFE802	8
Flash key code register	FKEY	R/W	H'00	H'FFFFE804	8
Flash MAT select register	FMATS	R/W	H'00*3 H'AA*3	H'FFFFE805	8
Flash transfer destination address register	FTDAR	R/W	H'00	H'FFFFE806	8
RAM emulation register	RAMER	R/W	H'0000	H'FFFFEC26	8, 16, 32

Notes: All registers except for RAMER can be accessed only in bytes, and the access requires three cycles. RAMER can be accessed in bytes or words, and the access requires three cycles.

1. The bits except the SCO bit are read-only bits. The SCO bit is a programming-only bit. (The value which can be read is always 0.)
2. The initial value is H'00 when the FWE pin goes low.
   The initial value is H'80 when the FWE pin goes high.
3. The initial value at initiation in user mode or user program mode is H'00.
   The initial value at initiation in user boot mode is H'AA.
4. The registers except RAMER can be accessed only in bytes, and the access requires four cycles. Since the RAMER register is in BSC, when it is accessed in bytes, the access requires four cycles, and when it is accessed in longwords, the access requires eight cycles.

Table 24.4 (2) Parameter Configuration

Name	Abbreviation	R/W	Initial Value	Address	Access Size
Download pass/fail result	DPFR	R/W	Undefined	On-chip RAM*	8, 16, 32
Flash pass/fail result	FPFR	R/W	Undefined	R0 of CPU	8, 16, 32
Flash multipurpose address area	FMPAR	R/W	Undefined	R5 of CPU	8, 16, 32
Flash multipurpose data destination area	FMPDR	R/W	Undefined	R4 of CPU	8, 16, 32
Flash erase block select	FEBS	R/W	Undefined	R4 of CPU	8, 16, 32
Flash program and erase frequency control	FPEFEQ	R/W	Undefined	R4 of CPU	8, 16, 32
Flash user branch address set parameter	FUBRA	R/W	Undefined	R5 of CPU	8, 16, 32

Note: * One byte of the start address in the on-chip RAM area specified by FTDAR is valid.

Table 24.5 Register/Parameter and Target Mode

		Download	Initialization	Programming	Erasure	Read	RAM Emulation
Programming/ erasing interface registers	FCCS	O	—	—	—	—	—
	FPCS	O	—	—	—	—	—
	PECS	O	—	—	—	—	—
	FKEY	O	—	O	O	—	—
	FMATS	—	—	O*[1]	O*[1]	O*[2]	—
	FTDAR	O	—	—	—	—	—
Programming/ erasing interface parameters	DPFR	O	—	—	—	—	—
	FPFR	O	O	O	O	—	—
	FPEFEQ	—	O	—	—	—	—
	FUBRA	—	O	—	—	—	—
	FMPAR	—	—	O	—	—	—
	FMPDR	—	—	O	—	—	—
	FEBS	—	—	—	O	—	—
RAM emulation	RAMER	—	—	—	—	—	O

Notes: 1. The setting is required when programming or erasing user MAT in user boot mode.
2. The setting may be required according to the combination of initiation mode and read target MAT.

24.4.2 Programming/Erasing Interface Registers

The programming/erasing interface registers are as described below. They are all 8-bit registers that can be accessed in bytes. These registers are initialized at a power-on reset, in hardware standby mode, or in software standby mode.

(1) Flash Code Control and Status Register (FCCS)

FCCS is configured by bits which request the monitor of the FWE pin state and error occurrence during programming or erasing flash memory and the download of the on-chip program.

Bit :	7	6	5	4	3	2	1	0
	FWE	—	—	FLER	—	—	—	SCO
Initial value :	1/0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	(R)W

- Bit 7—Flash Programming Enable (FWE): Monitors the level which is input to the FWE pin that performs hardware protection of the flash memory programming or erasing. The initial value is 0 or 1 according to the FWE pin state.

Bit 7

FWE	Description
0	When the FWE pin goes low (in hardware protection state)
1	When the FWE pin goes high

- Bits 6 and 5—Reserved: These bits are always read as 0. The write value should always be 0.
- Bit 4—Flash Memory Error (FLER): Indicates an error occurs during programming and erasing flash memory.

When FLER is set to 1, flash memory enters the error protection state.

This bit is initialized at a power-on reset or in hardware standby mode.

When FLER is set to 1, high voltage is applied to the internal flash memory. To reduce the damage to flash memory, the reset signal must be released after the reset period of 100 μs which is longer than normal.

Bit 4

FLER	Description
0	Flash memory operates normally (Initial value) Programming/erasing protection for flash memory (error protection) is invalid. [Clearing condition] At a power-on reset or in hardware standby mode
1	Indicates an error occurs during programming/erasing flash memory. Programming/erasing protection for flash memory (error protection) is valid. [Setting condition] See section 24.6.3, Error Protection.

- Bits 3 to 1—Reserved: These bits are always read as 0. The write value should always be 0.
- Bit 0—Source Program Copy Operation (SCO): Requests the on-chip programming/erasing program to be downloaded to the on-chip RAM.

When this bit is set to 1, the on-chip program which is selected by FPCS/FECS is automatically downloaded in the on-chip RAM area specified by FTDAR.

In order to set this bit to 1, RAM emulation state must be canceled, H'A5 must be written to FKEY, and this operation must be in the on-chip RAM.

Eight NOP instructions must be executed immediately after setting this bit to 1.

For interrupts during download, see section 24.8.2, Interrupts during Programming/Erasing. For the download time, see section 24.8.3, Other Notes.

Since this bit is cleared to 0 when download is completed, this bit cannot be read as 1.

Download by setting the SCO bit to 1 requires a special interrupt processing that performs bank switching to the on-chip program storage area. Therefore, before issuing a download request (SCO = 1), set VBR to H'00000000. Otherwise, the CPU gets out of control. Once download end is confirmed, VBR can be changed to any other value.

Bit 0

SCO	Description
0	Download of the on-chip programming/erasing program to the on-chip RAM is not executed (Initial value) [Clearing condition] When download is completed
1	Request that the on-chip programming/erasing program is downloaded to the on-chip RAM is generated [Clearing conditions] When all of the following conditions are satisfied and 1 is written to this bit • FKEY is written to H'A5 • During execution in the on-chip RAM • Not in RAM emulation mode (RAMS in RAMCR = 0)

(2) Flash Program Code Select Register (FPCS)

FPCS selects the on-chip programming program to be downloaded.

Bit :	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	PPVS
Initial value :	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R/W

- Bits 7 to 1—Reserved: These bits are always read as 0. The write value should always be 0.
- Bit 0—Program Pulse Single (PPVS): Selects the programming program.

Bit 0

PPVS	Description
0	On-chip programming program is not selected (Initial value) [Clearing condition] When transfer is completed
1	On-chip programming program is selected

(3) Flash Erase Code Select Register (FECS)

FECS selects download of the on-chip erasing program.

Bit :	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	EPVB
Initial value :	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R/W

- Bits 7 to 1—Reserved: These bits are always read as 0. The write value should always be 0.
- Bit 0—Erase Pulse Verify Block (EPVB): Selects the erasing program.

Bit 0

EPVB	Description	
0	On-chip erasing program is not selected [Clearing condition] When transfer is completed	(Initial value)
1	On-chip erasing program is selected	

(4) Flash Key Code Register (FKEY)

FKEY is a register for software protection that enables download of the on-chip program and programming/erasing of flash memory. Before setting the SCO bit to 1 in order to download the on-chip program or executing the downloaded programming/erasing program, these processings cannot be executed if the key code is not written.

Bit :	7	6	5	4	3	2	1	0
	K7	K6	K5	K4	K3	K2	K1	K0
Initial value :	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Bits 7 to 0—Key Code (K7 to K0): Only when H'A5 is written, writing to the SCO bit is valid. When a value other than H'A5 is written to FKEY, 1 cannot be written to the SCO bit. Therefore downloading to the on-chip RAM cannot be executed.

Only when H'5A is written, programming/erasing of flash memory can be executed. Even if the on-chip programming/erasing program is executed, flash memory cannot be programmed or erased when a value other than H'5A is written to FKEY.

Bits 7 to 0

K7 to K0	Description
H'A5	Writing to the SCO bit is enabled (The SCO bit cannot be set by a value other than H'A5.)
H'5A	Programming/erasing is enabled (A value other than H'A5 enables software protection state.)
H'00	Initial value

(5) Flash MAT Select Register (FMATS)

FMATS specifies whether user MAT or user boot MAT is selected.

Bit :	7	6	5	4	3	2	1	0	
	MS7	MS6	MS5	MS4	MS3	MS2	MS1	MS0	
Initial value :	0	0	0	0	0	0	0	0	(When not in user boot mode)
Initial value :	1	0	1	0	1	0	1	0	(When in user boot mode)
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Bits 7 to 0—MAT Select (MS7 to MS0): These bits are in user-MAT selection state when a value other than H'AA is written and in user-boot-MAT selection state when H'AA is written.

The MAT is switched by writing a value in FMATS.

When the MAT is switched, follow section 24.8.1, Switching between User MAT and User Boot MAT. (The user boot MAT cannot be programmed in user programming mode if user boot MAT is selected by FMATS. The user boot MAT must be programmed in boot mode or in programmer mode.)

Bits 7 to 0

MS7 to MS0	Description
H'AA	The user boot MAT is selected (in user-MAT selection state when the value of these bits are other than H'AA) Initial value when these bits are initiated in user boot mode.
H'00	Initial value when these bits are initiated in a mode except for user boot mode (in user-MAT selection state)

[Programmable condition] These bits are in the execution state in the on-chip RAM.

(6) Flash Transfer Destination Address Register (FTDAR)

FTDAR specifies the on-chip RAM address to which the on-chip program is downloaded.

Make settings for FTDAR before writing 1 to the SCO bit in FCCS. The initial value is H'00 which points to the start address (H'FFFF0000) in on-chip RAM.

Bit :	7	6	5	4	3	2	1	0
	TDER	TDA6	TDA5	TDA4	TDA3	TDA2	TDA1	TDA0
Initial value :	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Bit 7—Transfer Destination Address Setting Error: This bit is set to 1 when there is an error in the download start address set by bits 6 to 0 (TDA6 to TDA0). Whether the address setting is erroneous or not is judged by checking whether the setting of TDA6 to TDA0 is between the range of H'00 and H'05 after setting the SCO bit in FCCS to 1 and performing download. Before setting the SCO bit to 1 be sure to set the FTDAR value between H'00 to H'05 as well as clearing this bit to 0.

Bit 7

TDER	Description (Return Value after Download)
0	Setting of TDA6 to TDA0 is normal (Initial value)
1	Setting of TDER and TDA6 to TDA0 is H'06 to H'FF and download has been aborted

- Bits 6 to 0—Transfer Destination Address (TDA6 to TDA0): These bits specify the download start address. A value from H'00 to H'05 can be set to specify the download start address in on-chip RAM in 2-Kbyte units.

A value from H'06 to H'FF cannot be set. If such a value is set, the TDER bit (bit 7) in this register is set to 1 to prevent download from being executed.

Bits 6 to 0

TDA6 to TDA0	Description
H'00	Download start address is set to H'FFFF0000
H'01	Download start address is set to H'FFFF0800
H'02	Download start address is set to H'FFFF1000
H'03	Download start address is set to H'FFFF1800
H'04	Download start address is set to H'FFFF2000
H'05	Download start address is set to H'FFFF2800
H'06 to H'FF	Setting prohibited. If this value is set, the TDER bit (bit 7) is set to 1 to abort the download processing.

24.4.3 Programming/Erasing Interface Parameters

The programming/erasing interface parameters specify the operating frequency, user branch destination address, storage place for program data, programming destination address, and erase block and exchanges the processing result for the downloaded on-chip program. This parameter uses the general registers of the CPU (R4, R5, and R0) or the on-chip RAM area. The initial value is undefined at a power-on reset, in hardware standby mode, or in software standby mode.

At download all CPU registers are stored, and at initialization or when the on-chip program is executed, CPU registers except for R0 are stored. The return value of the processing result is written in R0. Since the stack area is used for storing the registers or as a work area, the stack area must be saved at the processing start. (The maximum size of a stack area to be used is 128 bytes.)

The programming/erasing interface parameters are used in the following four items.

(1) Download control
(2) Initialization before programming or erasing
(3) Programming
(4) Erasing

These items use different parameters. The correspondence table is shown in table 24.6.

The processing results of initialization, programming, and erasing are returned, but the bit contents have different meanings according to the processing program. See the description of FPFR for each processing.

Table 24.6 Usable Parameters and Target Modes

Name of Parameter	Abbreviation	Down-load	Initiali-zation	Pro-gram-ming	Erasure	R/W	Initial Value	Allocation
Download pass/fail result	DPFR	O	—	—	—	R/W	Undefined	On-chip RAM*
Flash pass/fail result	FPFR	—	O	O	O	R/W	Undefined	R0 of CPU
Flash programming/ erasing frequency control	FPEFEQ	—	O	—	—	R/W	Undefined	R4 of CPU
Flash user branch address set parameter	FUBRA	—	O	—	—	R/W	Undefined	R5 of CPU
Flash multipurpose address area	FMPAR	—	—	O	—	R/W	Undefined	R5 of CPU
Flash multipurpose data destination area	FMPDR	—	—	O	—	R/W	Undefined	R4 of CPU
Flash erase block select	FEBS	—	—	—	O	R/W	Undefined	R4 of CPU

Note: * One byte of start address of download destination specified by FTDAR

(1) Download Control

The on-chip program is automatically downloaded by setting the SCO bit to 1. The on-chip RAM area to be downloaded is the area as much as 3 Kbytes starting from the start address specified by FTDAR. For the address map of the on-chip RAM, see figure 24.10.

The download control is set by using the programming/erasing interface registers. The return value is given by the DPFR parameter.

(a) Download pass/fail result parameter (DPFR: one byte of start address of on-chip RAM specified by FTDAR)

This parameter indicates the return value of the download result. The value of this parameter can be used to determine if downloading is executed or not. Since the confirmation whether the SCO bit is set to 1 is difficult, the certain determination must be performed by setting one byte of the start address of the on-chip RAM area specified by FTDAR to a value other than the return value of download (for example, H'FF) before the download start (before setting the SCO bit to 1). For the checking method of download results, see section 24.5.2, User Program Mode.

Bit :	7	6	5	4	3	2	1	0
	0	0	0	0	0	SS	FK	SF

- Bits 7 to 3—Unused: Return 0.
- Bit 2—Source Select Error Detect (SS): The on-chip program which can be downloaded can be specified as only one type. When more than two types of the program are selected, the program is not selected, or the program is selected without mapping, an error occurs.

Bit 2

SS	Description
0	Download program can be selected normally
1	Download error occurs (Multi-selection or program which is not mapped is selected)

- Bit 1—Flash Key Register Error Detect (FK): Returns the check result whether the value of FKEY is set to H'A5.

Bit 1

FK	Description
0	FKEY setting is normal (FKEY = H'A5)
1	FKEY setting is abnormal (FKEY = value other than H'A5)

- Bit 0—Success/Fail (SF): Returns the result whether download has ended normally or not.

Bit 0

SF	Description
0	Downloading on-chip program has ended normally (no error)
1	Downloading on-chip program has ended abnormally (error occurs)

(2) Programming/Erasing Initialization

The on-chip programming/erasing program to be downloaded includes the initialization program.

The specified period pulse must be applied when programming or erasing. The specified pulse width is made by the method in which wait loop is configured by the CPU instruction. The operating frequency of the CPU must be set. Since the user branch function is supported, the user branch destination address must be set.

The initial program is set as a parameter of the programming/erasing program which has downloaded these settings.

(2.1) Flash programming/erasing frequency parameter (FPEFEQ: general register R4 of CPU)

This parameter sets the operating frequency of the CPU.

For the range of the operating frequency of this LSI, see section 29.3.2, Clock Timing.

Bit :	31	30	29	28	27	26	25	24
	0	0	0	0	0	0	0	0
Bit :	23	22	21	20	19	18	17	16
	0	0	0	0	0	0	0	0
Bit :	15	14	13	12	11	10	9	8
	F15	F14	F13	F12	F11	F10	F9	F8
Bit :	7	6	5	4	3	2	1	0
	F7	F6	F5	F4	F3	F2	F1	F0

- Bits 31 to 16—Unused: Return 0.
- Bits 15 to 0—Frequency Set (F15 to F0): Set the operating frequency of the CPU. The setting value must be calculated as the following methods.

1. The operating frequency which is shown in MHz units must be rounded in a number to three decimal places and be shown in a number of two decimal places.
2. The centuplicated value is converted to the binary digit and is written to the FPEFEQ parameter (general register R4). For example, when the operating frequency of the CPU is 28.882 MHz, the value is as follows.
   1. The number to three decimal places of 28.882 is rounded and the value is thus 28.88.
   2. The formula that 28.88 × 100 = 2888 is converted to the binary digit and b'0000, 1011, 0100, 1000 (H'0B48) is set to R4.

(2.2) Flash user branch address setting parameter (FUBRA: general register R5 of CPU)

This parameter sets the user branch destination address. The user program which has been set can be executed in specified processing units when programming and erasing.

Bit :	31	30	29	28	27	26	25	24
	UA31	UA30	UA29	UA28	UA27	UA26	UA25	UA24
Bit :	23	22	21	20	19	18	17	16
	UA23	UA22	UA21	UA20	UA19	UA18	UA17	UA16
Bit :	15	14	13	12	11	10	9	8
	UA15	UA14	UA13	UA12	UA11	UA10	UA9	UA8
Bit :	7	6	5	4	3	2	1	0
	UA7	UA6	UA5	UA4	UA3	UA2	UA1	UA0

- Bits 31 to 0—User Branch Destination Address (UA31 to UA0): When the user branch is not required, address 0 (H'00000000) must be set.

The user branch destination must be an area other than the flash memory, an area other than the RAM area in which on-chip program has been transferred, or the external bus space.

Note that the CPU must not branch to an area without the execution code and get out of control. The on-chip program download area and stack area must not be overwritten. If CPU runaway occurs or the download area or stack area is overwritten, the value of flash memory cannot be guaranteed.

The download of the on-chip program, initialization, initiation of the programming/erasing program must not be executed in the processing of the user branch destination. Programming or erasing cannot be guaranteed when returning from the user branch destination. The program data which has already been prepared must not be programmed.

Store general registers R8 to R15 and the control register (GBR). General registers R0 to R7 are available without storing them.

Moreover, the programming/erasing interface registers must not be written to or RAM emulation mode must not be entered in the processing of the user branch destination.

After the processing of the user branch has ended, the programming/erasing program must be returned to by using the RTS instruction.

For the execution intervals of the user branch processing, see note 2 (User branch processing intervals) in section 24.8.3, Other Notes.

(2.3) Flash pass/fail result parameter (FPFR: general register R0 of CPU)

This parameter indicates the return value of the initialization result.

Bit :	31	30	29	28	27	26	25	24
	0	0	0	0	0	0	0	0
Bit :	23	22	21	20	19	18	17	16
	0	0	0	0	0	0	0	0
Bit :	15	14	13	12	11	10	9	8
	0	0	0	0	0	0	0	0
Bit :	7	6	5	4	3	2	1	0
	0	0	0	0	0	BR	FQ	SF

- Bits 31 to 3—Unused: Return 0.
- Bit 2—User Branch Error Detect (BR): Returns the check result whether the specified user branch destination address is in the area other than the storage area of the programming/erasing program which has been downloaded .

Bit 2

BR	Description
0	User branch address setting is normal
1	User branch address setting is abnormal

- Bit 1—Frequency Error Detect (FQ): Returns the check result whether the specified operating frequency of the CPU is in the range of the supported operating frequency.

Bit 1

FQ	Description
0	Setting of operating frequency is normal
1	Setting of operating frequency is abnormal

- Bit 0—Success/Fail (SF): Indicates whether initialization is completed normally.

Bit 0	
SF	**Description**
0	Initialization has ended normally (no error)
1	Initialization has ended abnormally (error occurs)

(3) Programming Execution

When flash memory is programmed, the programming destination address on the user MAT must be passed to the programming program in which the program data is downloaded.

1. The start address of the programming destination on the user MAT is set in general register R5 of the CPU. This parameter is called FMPAR (flash multipurpose address area parameter).
   Since the program data is always in 128-byte units, the lower eight bits (MOA7 to MOA0) must be H'00 or H'80 as the boundary of the programming start address on the user MAT.
2. The program data for the user MAT must be prepared in the consecutive area. The program data must be in the consecutive space which can be accessed by using the MOV.B instruction of the CPU and is not the flash memory space.
   When data to be programmed does not satisfy 128 bytes, the 128-byte program data must be prepared by embedding the dummy code (H'FF).
   The start address of the area in which the prepared program data is stored must be set in general register R4. This parameter is called FMPDR (flash multipurpose data destination area parameter).
   For details on the programming procedure, see section 24.5.2, User Program Mode.

(3.1) Flash multipurpose address area parameter (FMPAR: general register R5 of CPU)

This parameter indicates the start address of the programming destination on the user MAT.

When an address in an area other than the flash memory space is set, an error occurs.

The start address of the programming destination must be at the 128-byte boundary. If this boundary condition is not satisfied, an error occurs. The error occurrence is indicated by the WA bit (bit 1) in FPFR.

Bit :	31	30	29	28	27	26	25	24
	MOA31	MOA30	MOA29	MOA28	MOA27	MOA26	MOA25	MOA24
Bit :	23	22	21	20	19	18	17	16
	MOA23	MOA22	MOA21	MOA20	MOA19	MOA18	MOA17	MOA16
Bit :	15	14	13	12	11	10	9	8
	MOA15	MOA14	MOA13	MOA12	MOA11	MOA10	MOA9	MOA8
Bit :	7	6	5	4	3	2	1	0
	MOA7	MOA6	MOA5	MOA4	MOA3	MOA2	MOA1	MOA0

- Bits 31 to 0—MOA31 to MOA0: Store the start address of the programming destination on the user MAT. The consecutive 128-byte programming is executed starting from the specified start address of the user MAT. The MOA6 to MOA0 bits are always 0 because the start address of the programming destination is at the 128-byte boundary.

(3.2) Flash multipurpose data destination parameter (FMPDR: general register R4 of CPU)

This parameter indicates the start address in the area which stores the data to be programmed in the user MAT. When the storage destination of the program data is in flash memory, an error occurs. The error occurrence is indicated by the WD bit (bit 2) in FPFR.

Bit :	31	30	29	28	27	26	25	24
	MOD31	MOD30	MOD29	MOD28	MOD27	MOD26	MOD25	MOD24
Bit :	23	22	21	20	19	18	17	16
	MOD23	MOD22	MOD21	MOD20	MOD19	MOD18	MOD17	MOD16
Bit :	15	14	13	12	11	10	9	8
	MOD15	MOD14	MOD13	MOD12	MOD11	MOD10	MOD9	MOD8
Bit :	7	6	5	4	3	2	1	0
	MOD7	MOD6	MOD5	MOD4	MOD3	MOD2	MOD1	MOD0

- Bits 31 to 0—MOD31 to MOD0: Store the start address of the area which stores the program data for the user MAT. The consecutive 128-byte data is programmed to the user MAT starting from the specified start address.

(3.3) Flash pass/fail parameter (FPFR: general register R0 of CPU)

This parameter indicates the return value of the program processing result.

Bit :	31	30	29	28	27	26	25	24
	0	0	0	0	0	0	0	0
Bit :	23	22	21	20	19	18	17	16
	0	0	0	0	0	0	0	0
Bit :	15	14	13	12	11	10	9	8
	0	0	0	0	0	0	0	0
Bit :	7	6	5	4	3	2	1	0
	0	MD	EE	FK	0	WD	WA	SF

- Bits 31 to 7—Unused: Return 0.
- Bit 6—Programming Mode Related Setting Error Detect (MD): Returns the check result of whether the signal input to the FWE pin is high and whether the error protection state is entered.

When a low-level signal is input to the FWE pin or the error protection state is entered, 1 is written to this bit. The input level to the FWE pin and the error protection state can be confirmed with the FWE bit (bit 7) and the FLER bit (bit 4) in FCCS, respectively. For conditions to enter the error protection state, see section 24.6.3, Error Protection.

Bit 6

MD	Description
0	FWE and FLER settings are normal (FWE = 1, FLER = 0)
1	FWE = 0 or FLER = 1, and programming cannot be performed

- Bit 5—Programming Execution Error Detect (EE): 1 is returned to this bit when the specified data could not be written because the user MAT was not erased or when flash-memory related register settings are partially changed on returning from the user branch processing.

If this bit is set to 1, there is a high possibility that the user MAT is partially rewritten. In this case, after removing the error factor, erase the user MAT.

If FMATS is set to H'AA and the user boot MAT is selected, an error occurs when programming is performed. In this case, both the user MAT and user boot MAT are not rewritten.

Programming of the user boot MAT must be executed in boot mode or programmer mode.

Bit 5

EE	Description
0	Programming has ended normally
1	Programming has ended abnormally (programming result is not guaranteed)

- Bit 4—Flash Key Register Error Detect (FK): Returns the check result of the value of FKEY before the start of the programming processing.

Bit 4

FK	Description
0	FKEY setting is normal (FKEY = H'A5)
1	FKEY setting is error (FKEY = value other than H'A5)

- Bit 3—Unused: Returns 0.
- Bit 2—Write Data Address Detect (WD): When an address in the flash memory area is specified as the start address of the storage destination of the program data, an error occurs.

Bit 2

WD	Description
0	Setting of write data address is normal
1	Setting of write data address is abnormal

- Bit 1—Write Address Error Detect (WA): When the following items are specified as the start address of the programming destination, an error occurs.

1. The programming destination address is an area other than flash memory
2. The specified address is not at the 128-byte boundary (A6 to A0 are not 0)

Bit 1

WA	Description
0	Setting of programming destination address is normal
1	Setting of programming destination address is abnormal

- Bit 0—Success/Fail (SF): Indicates whether the program processing has ended normally or not.

Bit 0

SF	Description
0	Programming has ended normally (no error)
1	Programming has ended abnormally (error occurs)

(4) Erasure Execution

When flash memory is erased, the erase-block number on the user MAT must be passed to the erasing program which is downloaded. This is set to the FEBS parameter (general register R4).

One block is specified from the block number 0 to 15.

For details on the erasing procedure, see section 24.5.2, User Program Mode.

(4.1) Flash erase block select parameter (FEBS: general register R4 of CPU)

This parameter specifies the erase-block number. Several block numbers cannot be specified.

Bit :	31	30	29	28	27	26	25	24
	0	0	0	0	0	0	0	0

Bit :	23	22	21	20	19	18	17	16
	0	0	0	0	0	0	0	0

Bit :	15	14	13	12	11	10	9	8
	0	0	0	0	0	0	0	0

Bit :	7	6	5	4	3	2	1	0
	EBS7	EBS6	EBS5	EBS4	EBS3	EBS2	EBS1	EBS0

- Bits 31 to 8—Unused: Return 0.
- Bits 7 to 0—Erase Block (EB7 to EB0): Set the erase-block number in the range from 0 to 15. 0 corresponds to the EB0 block and 15 corresponds to the EB15 block. An error occurs when a number other than 0 to 15 (H'00 to H'0F) is set.

(4.2) Flash pass/fail result parameter (FPFR: general register R0 of CPU)

This parameter returns the value of the erasing processing result.

Bit :	31	30	29	28	27	26	25	24
	0	0	0	0	0	0	0	0

Bit :	23	22	21	20	19	18	17	16
	0	0	0	0	0	0	0	0

Bit :	15	14	13	12	11	10	9	8
	0	0	0	0	0	0	0	0

Bit :	7	6	5	4	3	2	1	0
	0	MD	EE	FK	EB	0	0	SF

- Bits 31 to 7—Unused: Return 0.
- Bit 6—Erasure Mode Related Setting Error Detect (MD): Returns the check result of whether the signal input to the FWE pin is high and whether the error protection state is entered.

When a low-level signal is input to the FWE pin or the error protection state is entered, 1 is written to this bit. The input level to the FWE pin and the error protection state can be confirmed with the FWE bit (bit 7) and the FLER bit (bit 4) in FCCS, respectively. For conditions to enter the error protection state, see section 24.6.3, Error Protection.

Bit 6

MD	Description
0	FWE and FLER settings are normal (FWE = 1, FLER = 0)
1	FWE = 0 or FLER = 1, and erasure cannot be performed

- Bit 5—Erasure Execution Error Detect (EE): 1 is returned to this bit when the user MAT could not be erased or when flash-memory related register settings are partially changed on returning from the user branch processing.

If this bit is set to 1, there is a high possibility that the user MAT is partially erased. In this case, after removing the error factor, erase the user MAT.

If FMATS is set to H'AA and the user boot MAT is selected, an error occurs when erasure is performed. In this case, both the user MAT and user boot MAT are not erased.

Erasure of the user boot MAT must be executed in boot mode or programmer mode.

Bit 5

EE	Description
0	Erasure has ended normally
1	Erasure has ended abnormally (erasure result is not guaranteed)

- Bit 4—Flash Key Register Error Detect (FK): Returns the check result of FKEY value before start of the erasing processing.

Bit 4

FK	Description
0	FKEY setting is normal (FKEY = H'5A)
1	FKEY setting is error (FKEY = value other than H'5A)

- Bit 3—Erase Block Select Error Detect (EB): Returns the check result whether the specified erase-block number is in the block range of the user MAT.

Bit 3

EB	Description
0	Setting of erase-block number is normal
1	Setting of erase-block number is abnormal

- Bits 2 and 1—Unused: Return 0.
- Bit 0—Success/Fail (SF): Indicates whether the erasing processing has ended normally or not.

Bit 0

SF	Description
0	Erasure has ended normally (no error)
1	Erasure has ended abnormally (error occurs)

24.4.4 RAM Emulation Register (RAMER)

When the realtime programming of the user MAT is emulated, RAMER sets the area of the user MAT which is overlapped with a part of the on-chip RAM. RAMER is initialized to H'0000 at a power-on reset or in hardware standby mode, or in software standby mode. The RAMER setting must be executed in user mode or in user program mode.

For the division method of the user-MAT area, see table 24.7. In order to operate the emulation function certainly, the target MAT of the RAM emulation must not be accessed immediately after RAMER is programmed. If it is accessed, the normal access is not guaranteed.

Bit :	15	14	13	12	11	10	9	8
	—	—	—	—	—	—	—	—
Initial value :	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R

Bit :	7	6	5	4	3	2	1	0
	—	—	—	—	RAMS	RAM2	RAM1	RAM0
Initial value :	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R/W	R/W	R/W	R/W

- Bits 15 to 4—Reserved: These bits are always read as 0. The write value should always be 0.
- Bit 3—RAM Select (RAMS): Sets whether the user MAT is emulated or not. When RAMS = 1, all blocks of the user MAT are in the programming/erasing protection state.

Bit 3

RAMS	Description
0	Emulation is not selected (Initial value) Programming/erasing protection of all user-MAT blocks is invalid
1	Emulation is selected Programming/erasing protection of all user-MAT blocks is valid

- Bits 2 to 0—User MAT Area Select: These bits are used with bit 3 to select the user-MAT area to be overlapped with the on-chip RAM. (See table 24.7.)

Table 24.7 Overlapping of RAM Area and User MAT Area

RAM Area	Block Name	RAMS	RAM2	RAM1	RAM0
H'FFFF0000 to H'FFFF0FFF	RAM area (4 Kbytes)	0	*	*	*
H'00000000 to H'00000FFF	EB0 (4 Kbytes)	1	0	0	0
H'00001000 to H'00001FFF	EB1 (4 Kbytes)	1	0	0	1
H'00002000 to H'00002FFF	EB2 (4 Kbytes)	1	0	1	0
H'00003000 to H'00003FFF	EB3 (4 Kbytes)	1	0	1	1
H'00004000 to H'00004FFF	EB4 (4 Kbytes)	1	1	0	0
H'00005000 to H'00005FFF	EB5 (4 Kbytes)	1	1	0	1
H'00006000 to H'00006FFF	EB6 (4 Kbytes)	1	1	1	0
H'00007000 to H'00007FFF	EB7 (4 Kbytes)	1	1	1	1

Legend: * Don't care.