

EE 4140

Final Board

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1.0 Introduction

The purpose of this report is to analyze the success of the design, simulation, fabrication, and testing of our EE4140 RF board. The board itself was a combination of all the different labs completed throughout the semester, including the DC Bias Regulator, Amplifier, Oscillator, and Resonator.

2.0 DC Bias Circuit

2.1 Design

The DC bias circuit was designed to provide a regulated voltage to the transistor for the amplifier and oscillator stages. The goal was to have a V_{ce} of 8 V and a collector current of 10 mA. To achieve this, we used a standard resistor divider to set the base voltage. We conducted several parameter sweeps in simulation to determine the optimal resistance values while maintaining compatibility with standard E-series resistor values. The schematic for the DC Bias can be seen below in Figure 1.

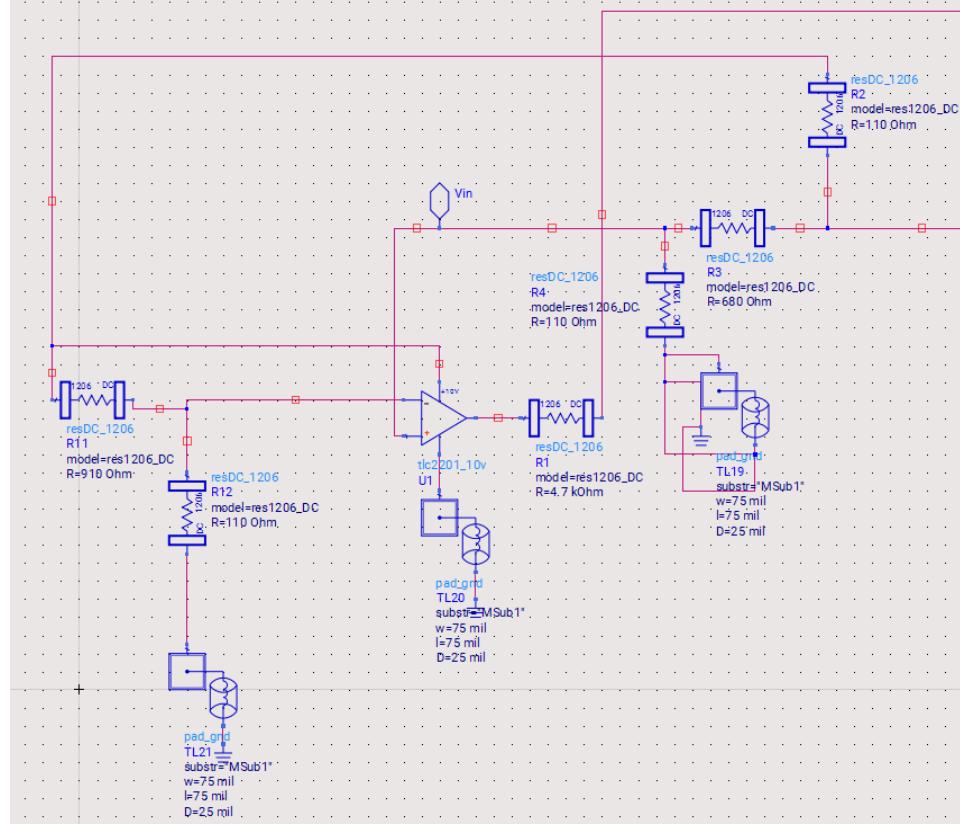


Figure 1: ADS Schematic for the DC Bias Regulator Circuit.

2.2 Simulation

The initial DC simulations proceeded smoothly, and we got 7.735V with 10.69mA on the transistor. Although this does not perfectly meet specifications, we had confidence that the DC Bias would be a for our needs. We also put the DC Bias into the other schematics to ensure there was no odd behavior.

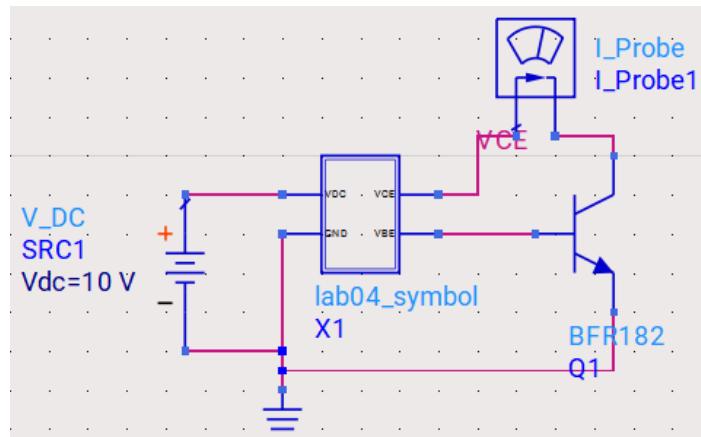


Figure 2: Schematic for testing DC Bias.

freq	I_Probe1.i	VCE
0.0000 Hz	10.69 mA	7.735 V

Figure 3: Results from DC Bias Simulation.

2.3 Testing

To test the values, 10V was applied to the terminal block, and the voltage was measured across the resistor connected directly to the termination network. The goal was to be 8V; however, the estimated value was 8.37V. The 0.37 difference was attributed to resistor tolerance and board-level parasitics. The DC Bias was determined to be stable enough to power the RF sections of the board.

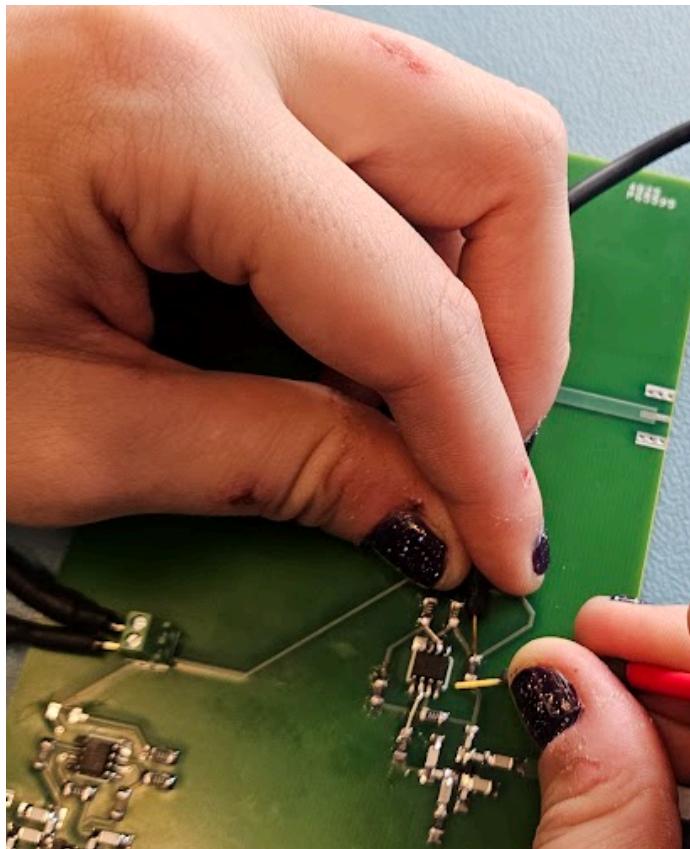


Figure 4: Testing Setup for DC Bias.

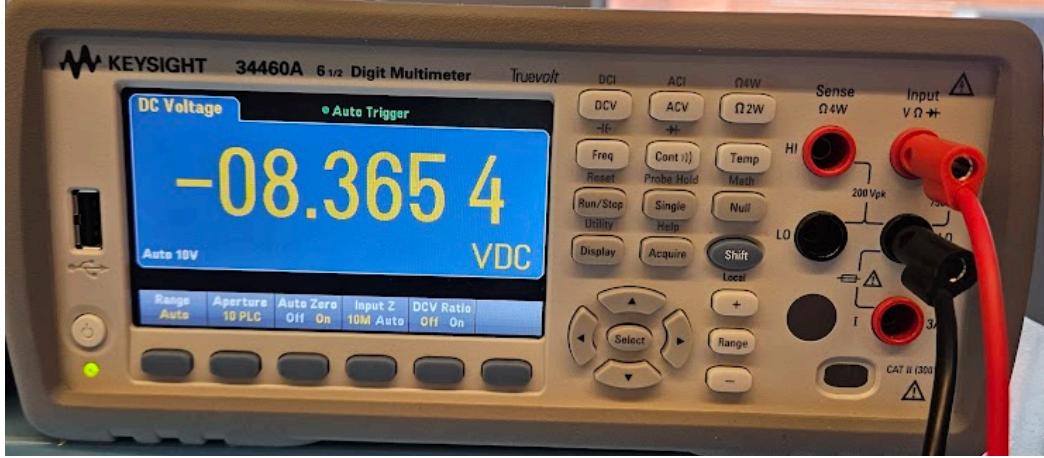


Figure 5: Multimeter Result from DC Bias Testing.

3.0 Amplifier

3.1 Design

The amplifier was designed as a stable, maximum-gain RF amplifier operating at 1 GHz. The design process began by extracting S-parameters at the design frequency and calculating the source and load impedances. Input and output matching networks were synthesized by hand using Smith chart techniques and quality factor calculations, initially using ideal components. Stability was evaluated using source and load stability circles. Once the perfect design met the specifications, non-ideal components and solder pads were incorporated into the final design, as shown in Figure 6 below.

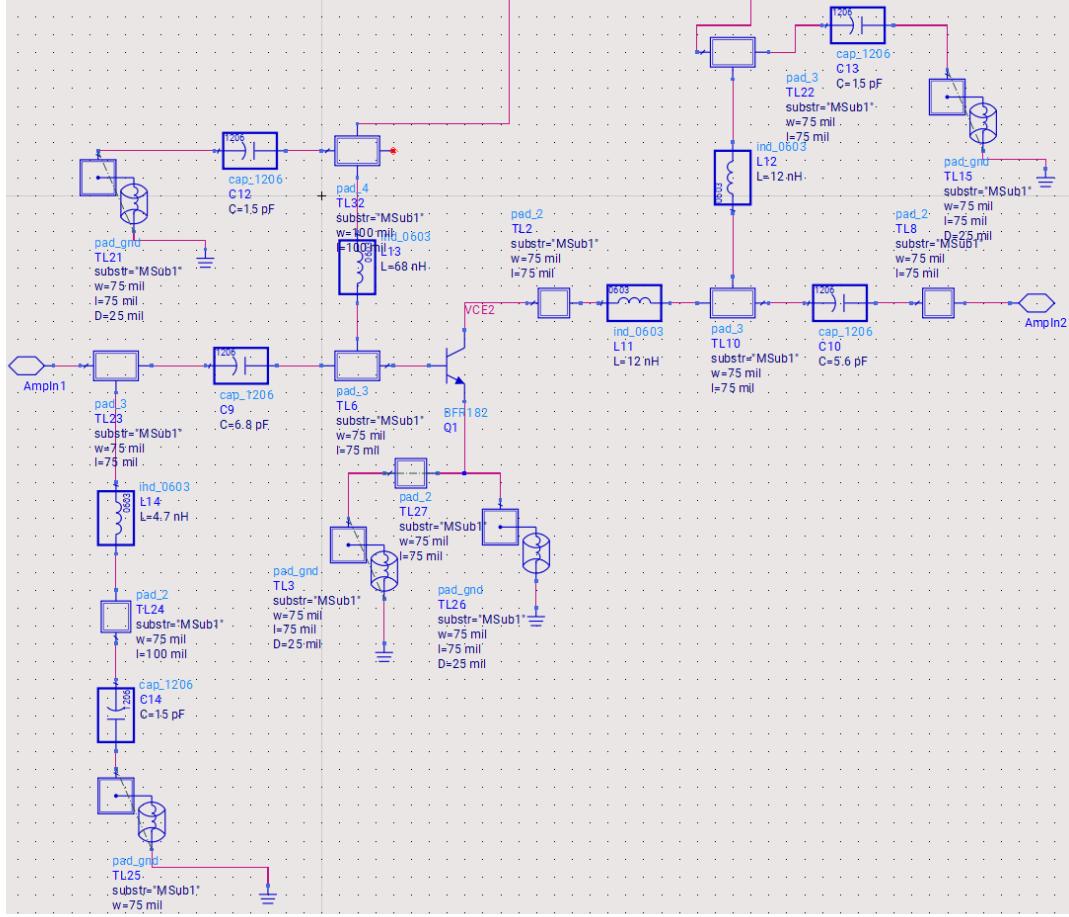


Figure 6: Final Amplifier Schematic.

3.2 Simulation

Simulations with ideal components showed that the amplifier met or exceeded gain and return loss specifications at 1 GHz. As non-ideal components and solder pads were added to the design, component values were adjusted within available E-series values to recover performance while maintaining stability. The final simulated design achieved near-specification gain and acceptable input and output matching, as shown below.

Specification Metric	Specification Requirement	Simulated Performance	DC Bias Simulated Performance
Design Frequency (MHz)	1000	1000	1000
Gain: dB(S(2,1))	13	13.425	13.701
Input Return Loss: dB(S(1,1))	-15	-18.898	-16.919
Output Return Loss: dB(S(2,2))	-15	-22.902	-14.211
Stable ($\mu > 1$) Frequency Range	1	1.001	1.001

Table 1: Amplifier comparison with lab specifications.

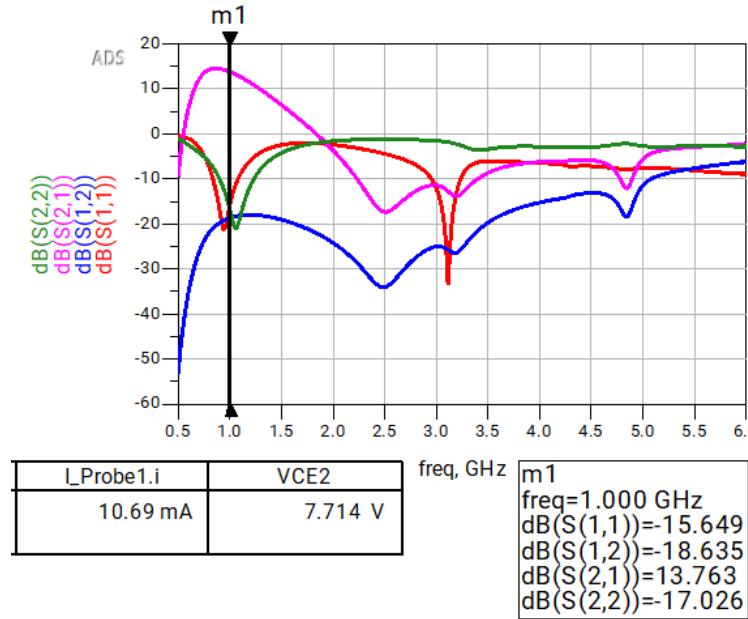


Figure 7: Simulation results from the Amplifier.

3.3 Layout

The PCB layout emphasized controlled-impedance RF traces, short signal paths, and solid grounding to minimize parasitic inductance and capacitance. The goal was to have the shortest traces possible.

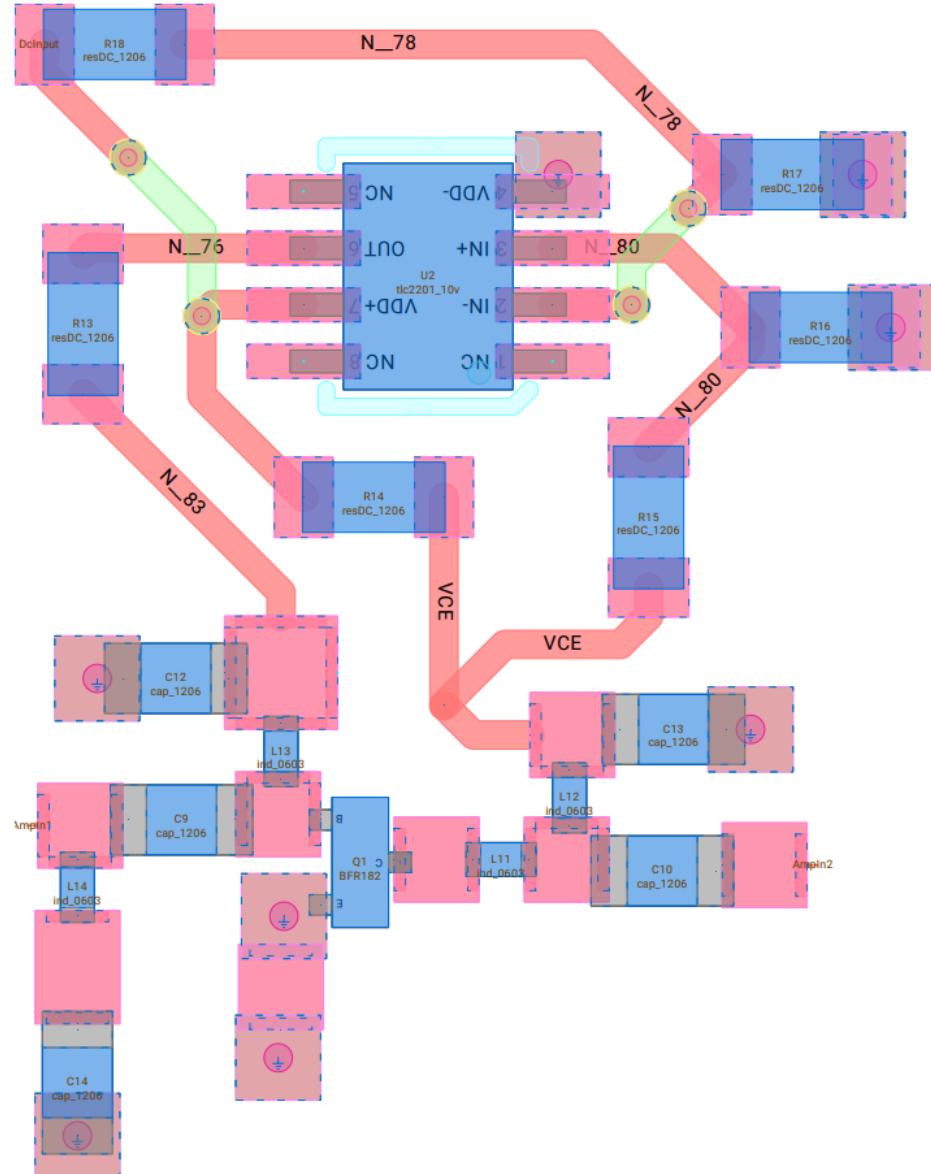


Figure 8: Layout for the Amplifier with the DC Bias Regulator.

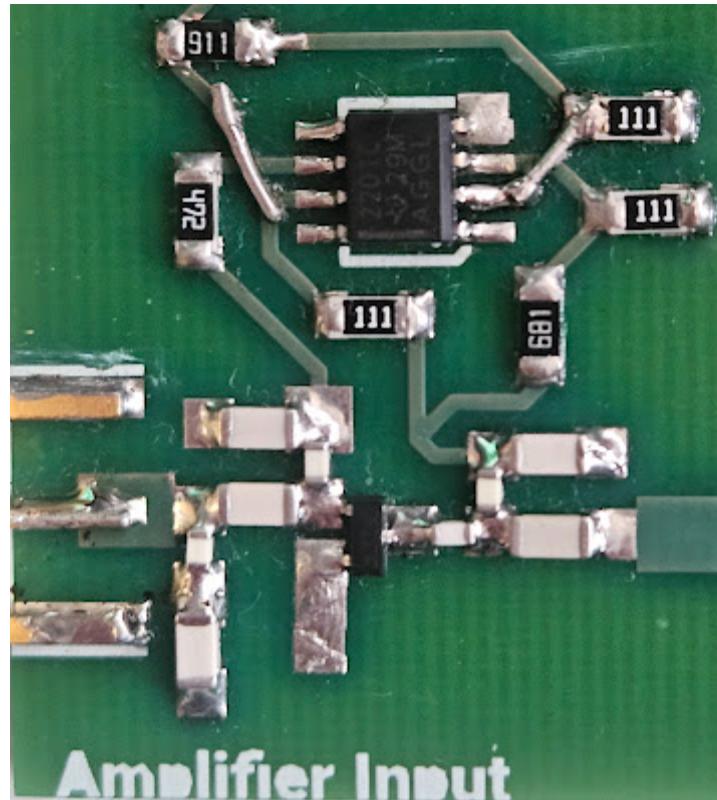


Figure 9: Built-out Amplifier with DC Bias.

3.4 Testing

Measured S-parameters showed an input return loss, $S(1,1)$, of -14.61 dB, which slightly missed the -15 dB specification. The measured forward gain, $S(2,1)$, was 10.81 dB, which is below the 13 dB target. These discrepancies are attributed to losses from non-ideal components and pad parasitics. Although it did not fully meet the specifications, the amplifier operated stably and provided decent gain, so we consider it a success.



Figure 10: Results of testing the Amplifier.

4.0 Oscillator

4.1 Design

The oscillator was designed as a reflection oscillator targeting a center frequency of 1 GHz. The design followed a negative-resistance oscillator design. First, we made our transistor unstable and then chose the correct biasing voltage to obtain the desired current and V_{ce}. Next, we found the feedback network by sweeping the values of a capacitor. Then, we identified the terminating network by plotting Gamma T using the relationship between r and X. We selected a specific power value and determined Z_{in}. We found an L-matching network for the load impedance. Lastly, we used the harmonic balance simulation to see if our oscillations were at the desired frequency and of the desired sinusoidal shape.

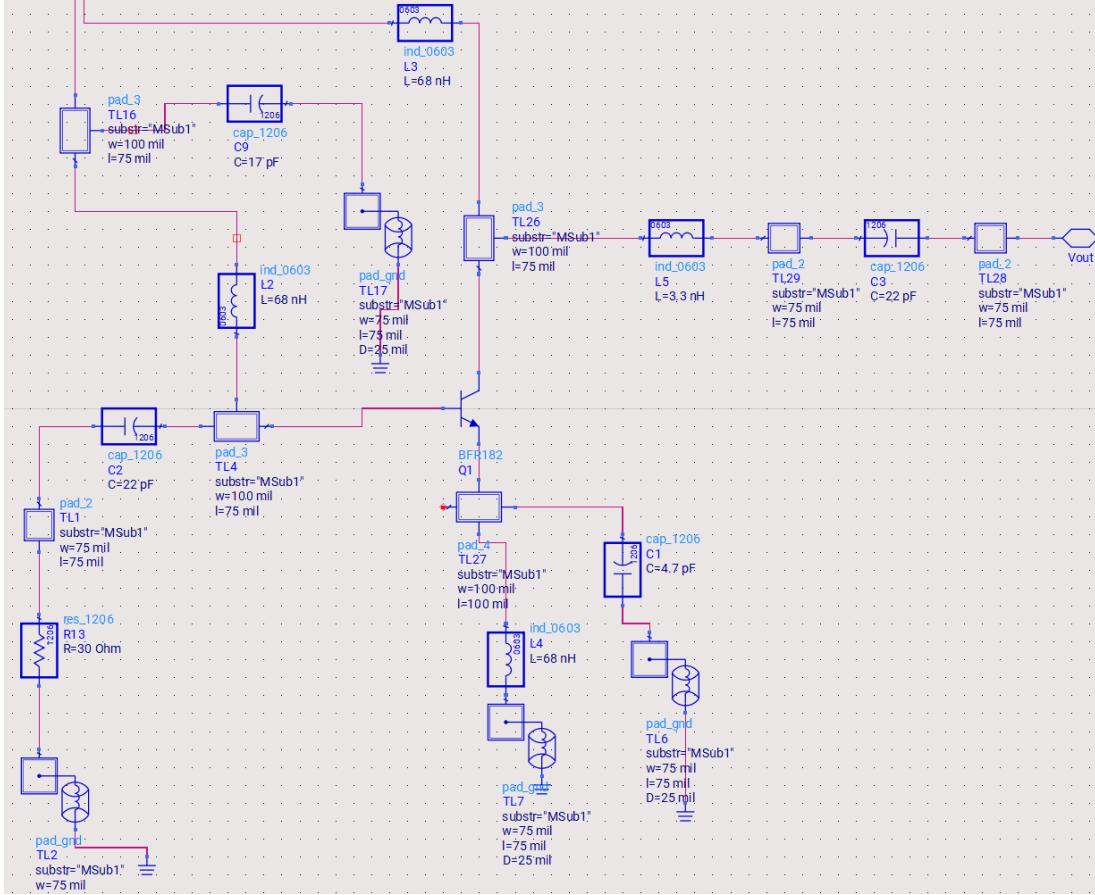


Figure 11: Final schematic of the 1 GHz oscillator.

4.2 Simulation

Harmonic balance simulations confirmed sustained oscillation near 1 GHz with stable amplitude. Stability analysis revealed a loop gain magnitude less than unity at the zero-phase crossing, which satisfies the oscillation conditions. The simulated oscillation frequency was slightly below 1 GHz, consistent with expected sensitivity to component values and parasitics.

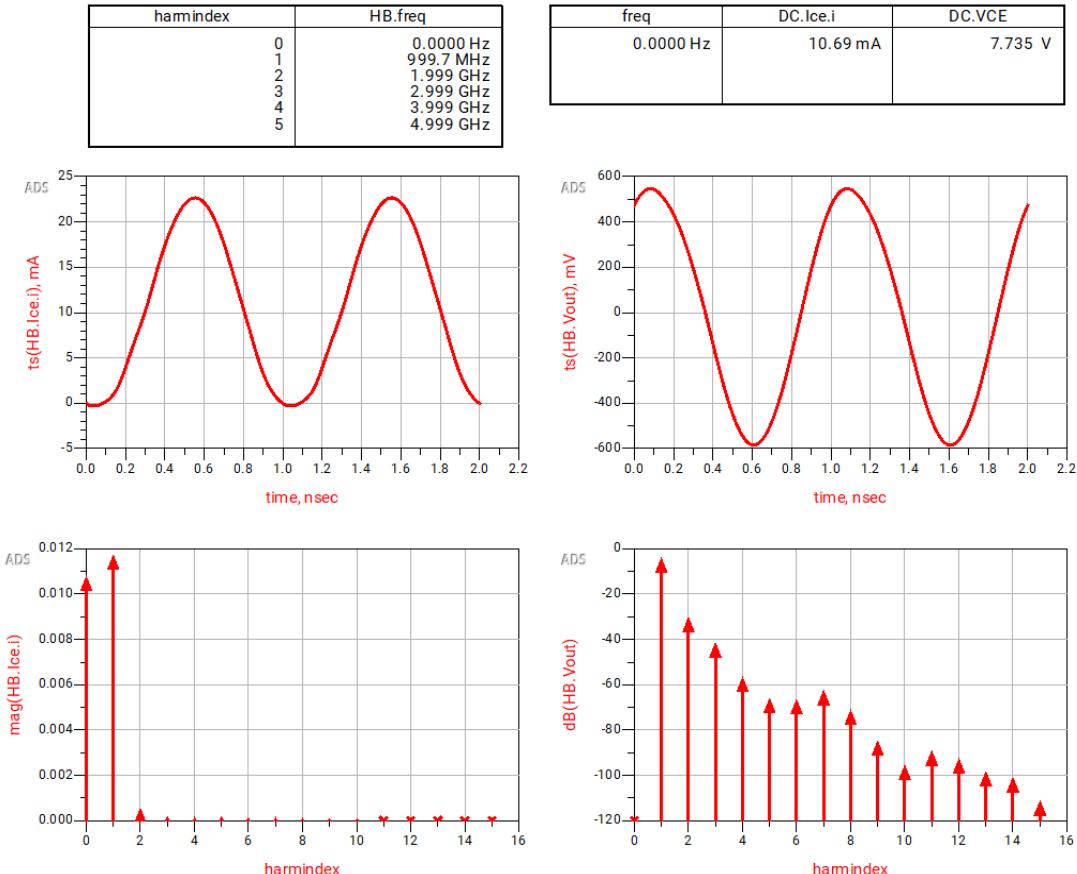


Figure 12: Simulated results of the 1 GHz oscillator.

4.3 Layout

The oscillator layout prioritized symmetry, short feedback paths, and firm grounding to reduce unwanted coupling and phase noise.

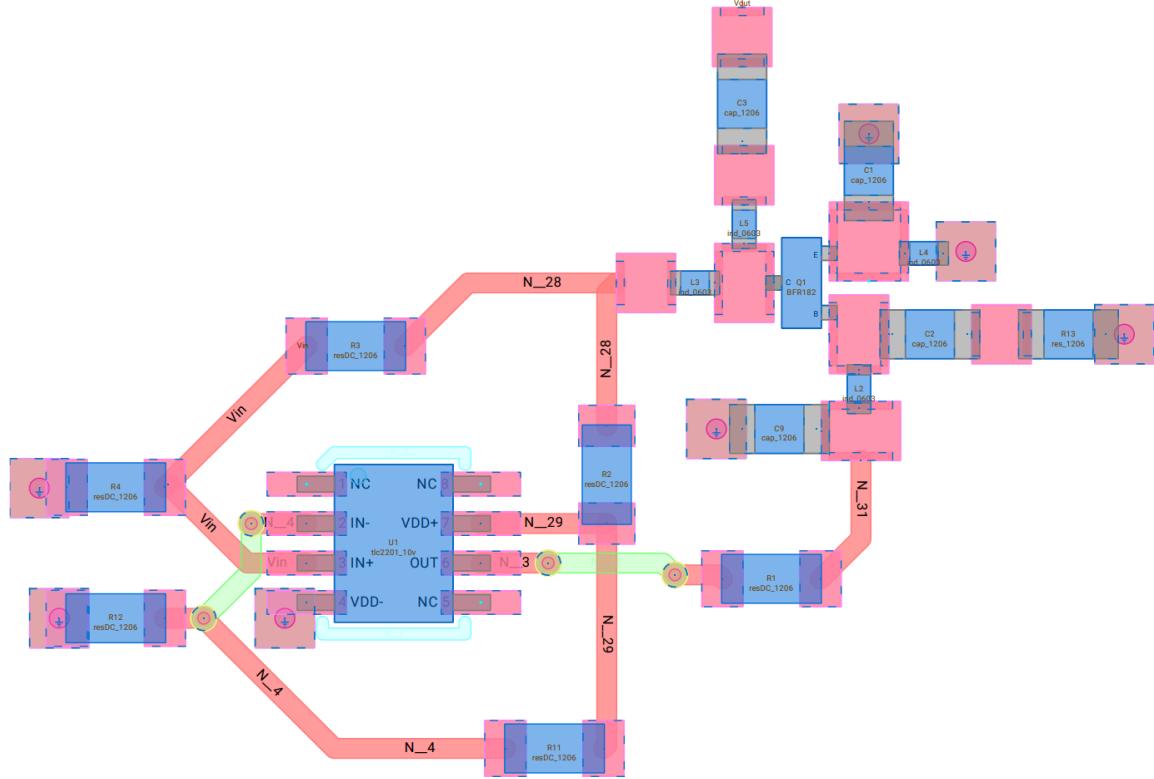


Figure 13: Layout of the oscillator with DC Bias.

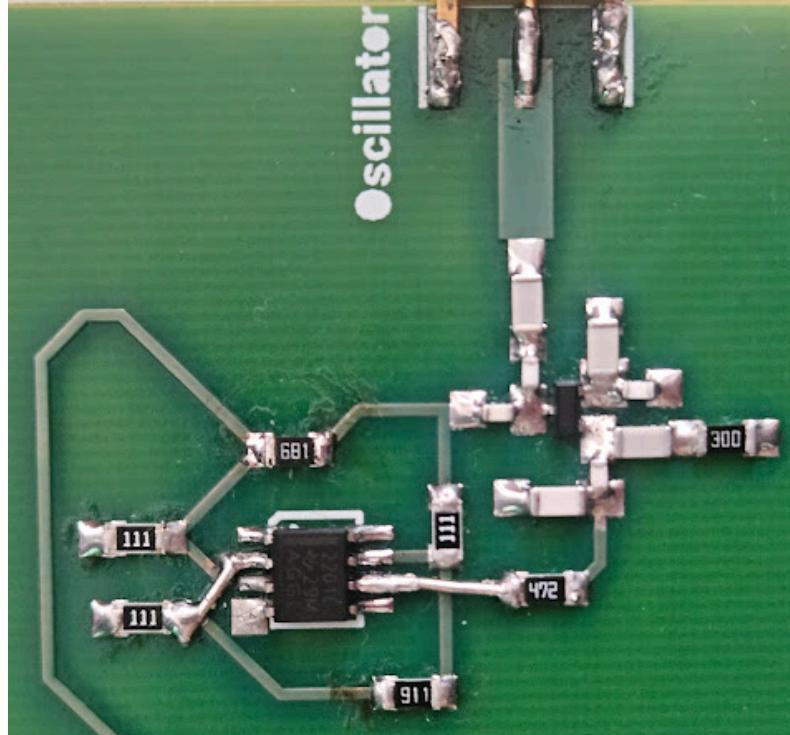


Figure 14: Built-out Oscillator with DC Bias.

4.4 Testing

During initial testing, 5 V was inadvertently applied to the intended 10 V supply input. Although this initially appeared to indicate poor output power, the oscillator still reliably started and oscillated, demonstrating design robustness. With a 5 V supply, the oscillator operated at 952.6 MHz. When the correct 10 V supply was applied, oscillation occurred at 937.6 MHz. While the target frequency of 1 GHz was not achieved, both measurements were within 10% of the design goal. The observed frequency shift is consistent with component tolerances, layout parasitics, and loading effects not fully captured in simulation.

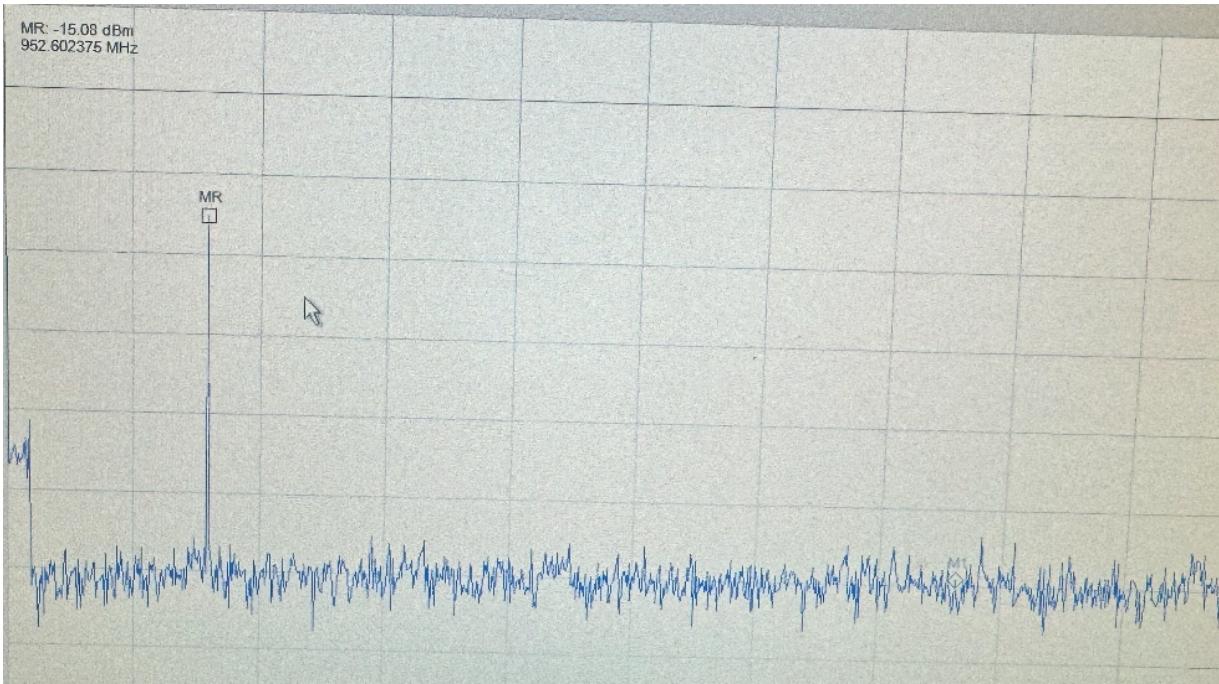


Figure 15: Oscillator Results with 5V input.

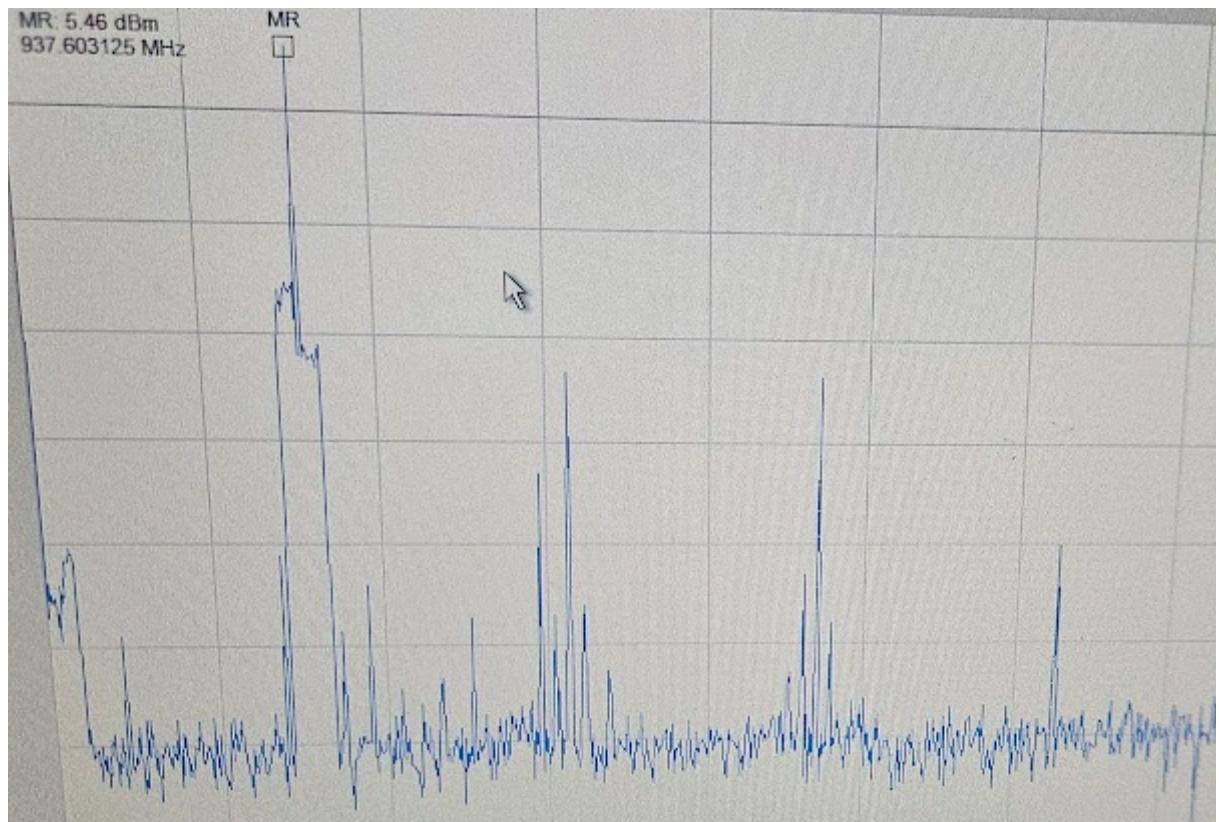


Figure 16: Oscillator results with a 10V input.

5.0 Resonator

5.1 Design

The resonator was designed based on an H-shaped resonator topology. Lumped and distributed effects were both considered in the design, with grounding structures playing a critical role in defining the resonant characteristics.

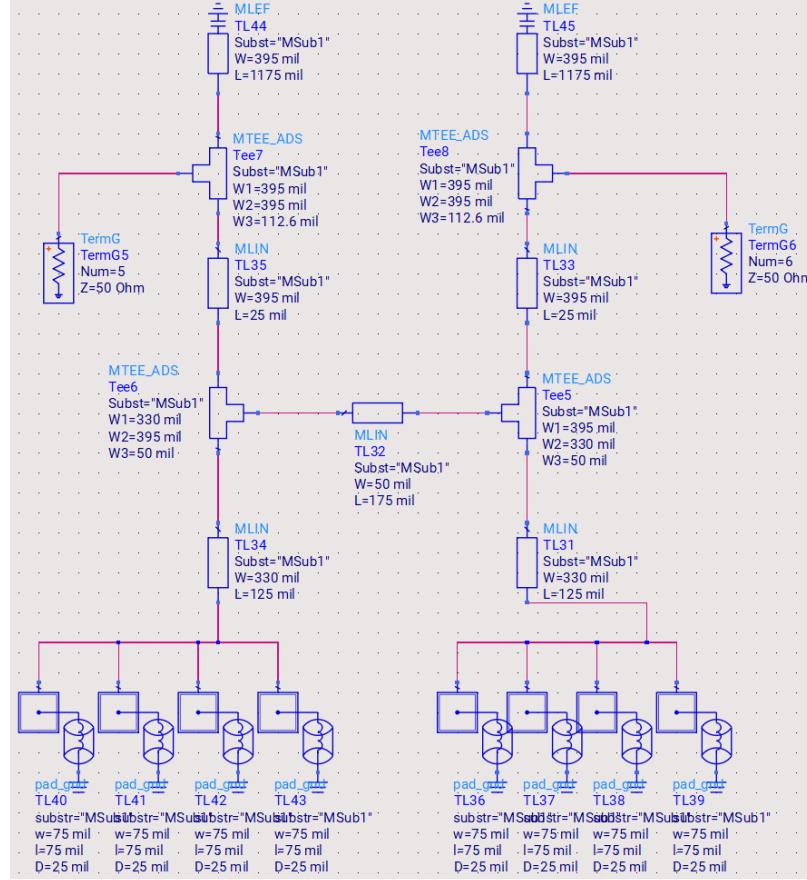


Figure 17: Schematic for the Resonator.

5.2 Simulation

Simulations predicted a resonance near the target frequency, though with limited bandwidth. The expected response indicated sensitivity to grounding, current distribution, and geometric parasitics.

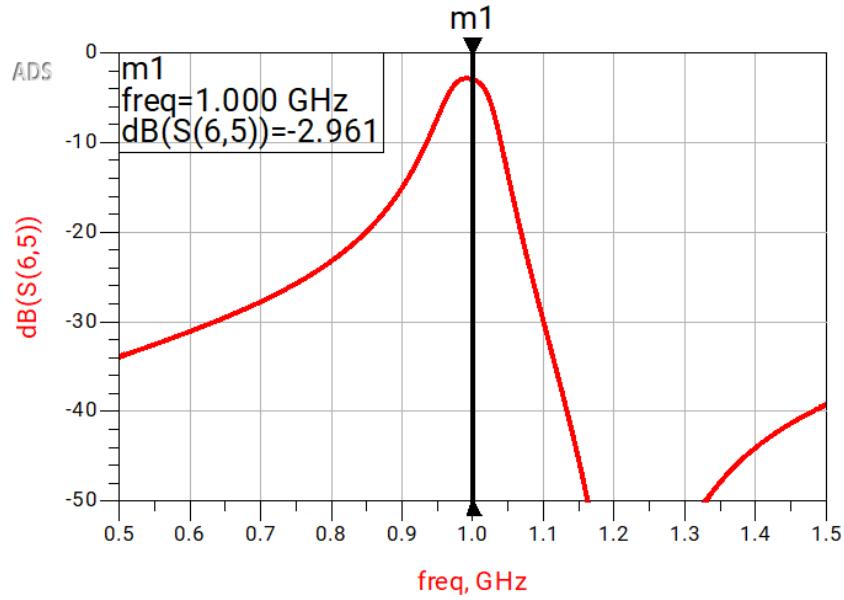


Figure 18: Simulation Results for the Resonator.

5.3 Layout

The resonator layout closely followed the H-shaped geometry used in simulation; however, instead of lining the ground vias along the bottom of the H-shape, we placed the vias on top of each other, which was likely a poor decision.



Figure 19: Layout for the Resonator.

5.4 Testing

Measured results showed a narrow bandwidth and low response magnitude at the target frequency. The discrepancy between simulated and measured performance is likely due to the bad grounding technique. These effects may have disrupted the intended current distribution of the H-shaped resonator, reducing its effective Q and shifting the resonance behavior.

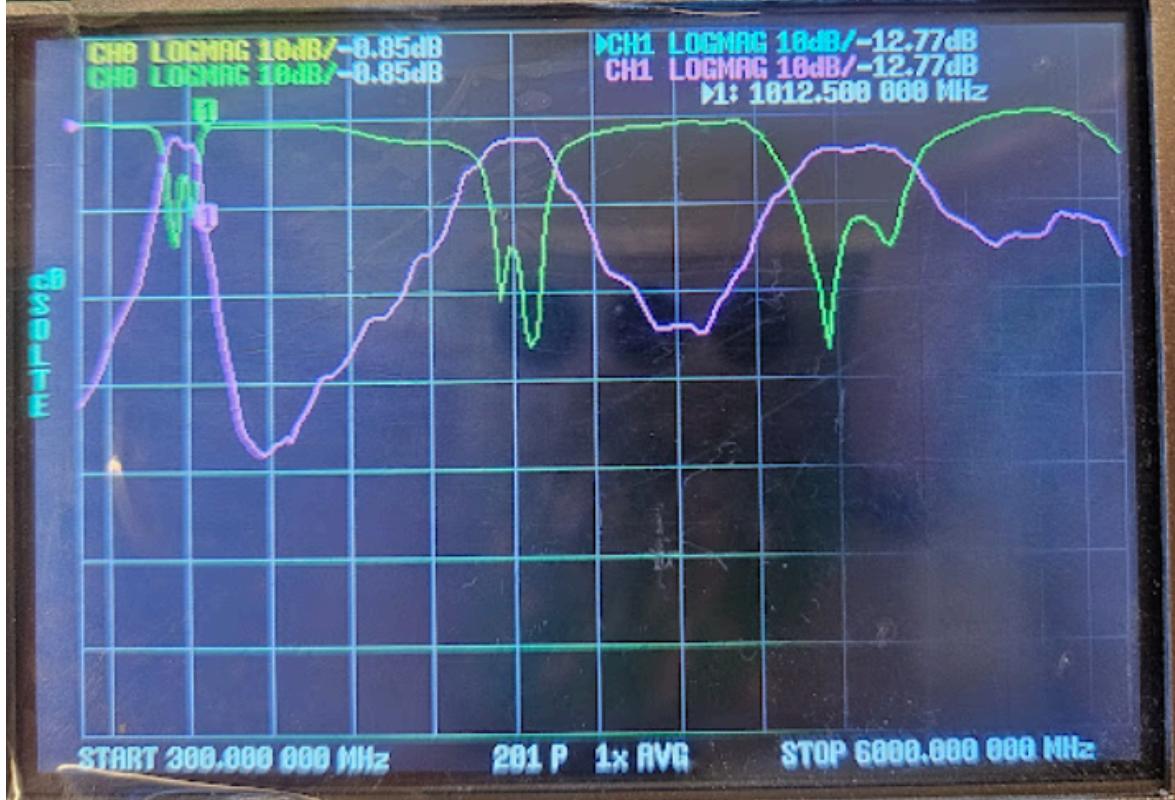


Figure 20: Results of the Resonator.

6.0 Troubleshooting

An error occurred during submission of the drill files, resulting in the absence of backside traces on the fabricated PCB. Because the back layer is our ground plane, all vias intended to connect to back traces were instead tied directly to ground. To resolve this issue, a drill press was used to isolate the affected vias from the ground plane physically. Jumper wires were then added to the top layer to connect the pins. Although this was an unideal build of the board, it did allow for testing and fixed the grounding issue. An image of the drilled-out vias is shown below.



Figure 21: Drilled out vias on the ground plane.

7.0 Conclusion

This project combined all the RF subsystems we built throughout the semester into a single PCB. While not all subsystems fully met their individual specifications, the observed performances were all slightly successful, considering non-ideal components, parasitic effects, and fabrication issues. The DC bias and oscillator circuits demonstrated strong robustness, while the amplifier and resonator taught us the sensitivity of RF performance to layout and grounding decisions. Overall, the project successfully demonstrated the RF design process and provided valuable insights into the challenges of transitioning from simulation results to real-world hardware.