SIS3316
16 Channel VME Digitizer

Neutron/Gamma PSD Application Manual

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Revision Table:

Revision	Date	Modification
1.01	31.10.2015	First official release related to Firmware Versions - VME FPGA: V3316-200B (0x3316200B) - ADC FPGAs: V0250-0201 (0x02500201) This manual is an addendum to the manual SIS3316-M-1-1-V115.pdf

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1 Introduction

The SIS3316 is our first 16 channel digitizer card. It combines high channel density per card with the availability of greatly enhanced FPGA resources per channel and a flexible analog input stage followed by high resolution digitizer/ADC chips. The SIS3316 comes in two base configurations as listed in the table below.

Model	Sampling Speed	Resolution
SIS3316-125-16	125 MSPS	16-bit
SIS3316-250-14	250 MSPS	14-bit

SIS3316

As we are aware, that no manual is perfect, we appreciate your feedback and will incorporate proposed changes and corrections as quickly as possible. The most recent version of this manual can be obtained by email from info@struck.de, the revision dates are online under http://www.struck.de/manuals.html . Feel free to apply for an account for our PDF documentation web page also.

The SIS3316 firmware page is at www.struck.de/sis3316firm.html .

Information on SIS3316 applications, firmware news and other related issues will be posted on our DAQ blog at www.struck.de/blog also.

2 ADC FPGA Application Firmware: Neutron/Gamma PSD

The implemented FPGA firmware of the SIS3316 has the following features:

- Internal Trigger generation for each channel (FIR filter with CFD feature, baseline independent)
- 4 Accumulators/Integrals (4 x 24-bit) for each channel
- 48-bit Timestamp
- Global start/time reset input for generation of a "TOF Active Window"

- Two per channel, internal Shape 2-D histograms (512 x 512)
  - one 2-D histogram is used for particle type mapping (PSD value)
  - one 2-D histogram is used as the discrimination look up table (LUT) for Neutron/Gamma/Unclassified types
  - two Methods are implemented to discriminate the pulses

- Two per channel, internal TOF (time of flight) histograms (1M)
  - one TOF histogram will be for Gamma ray events
  - one TOF histogram will be for Neutron events

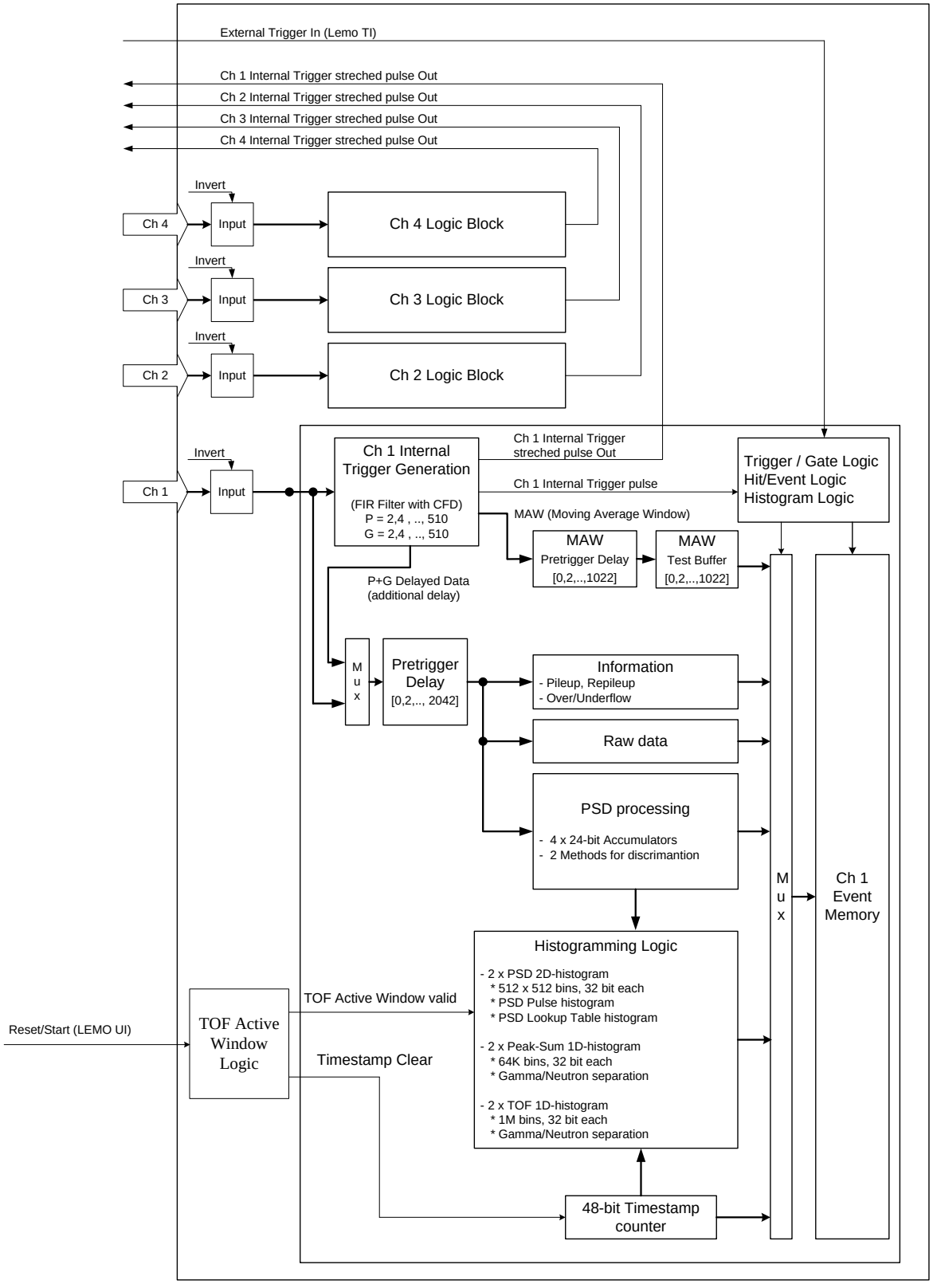
- Two per channel, internal Peak Sum (Peak-Height) histograms (64K)
  - one Peak Sum histogram will be for Gamma ray events
  - one Peak Sum histogram will be for Neutron events

- Eleven statistic counter per channel

It is possible to histogram the events/hits and sample the events/hits (save the events/hits in the Memory) in parallel !

- Double Bank / Multi event operation
- 16 channel asynchronous (internal trigger generation) and synchronous (external trigger, global trigger) operation
- Flexible Hit/Event storage (additional raw data, FIR Trigger trapezoidal MAW values, Accumulator values)

2.1 Four Channel group blockdiagram



2.2 Hit/Event Logic

The Hit/Event (sample) logic starts with a "Ch x trigger pulse" and executes the following steps provided the Sample Control logic is armed:

1. starts the "Active Trigger Gate Window" and latches the 48-bit timestamp.
2. writes the 16-bit programmable Channel Header ID and the latched 48-bit Timestamp into the Event Memory.
3. writes a programmable number of Ch x Raw Values into Event Memory
4. writes at the end of the "Active Trigger Gate Window" the Pileup information, the 4 accumulator values.
5. writes the buffered MAW data into the Event Memory if enabled.

The Hit/Event Logic parameters, related to the following illustration, are:

- *P1: FIR Filter Trigger parameters: see FIR Trigger Setup registers
- *P2: FIR Filter Trigger Threshold: see FIR Trigger Threshold registers

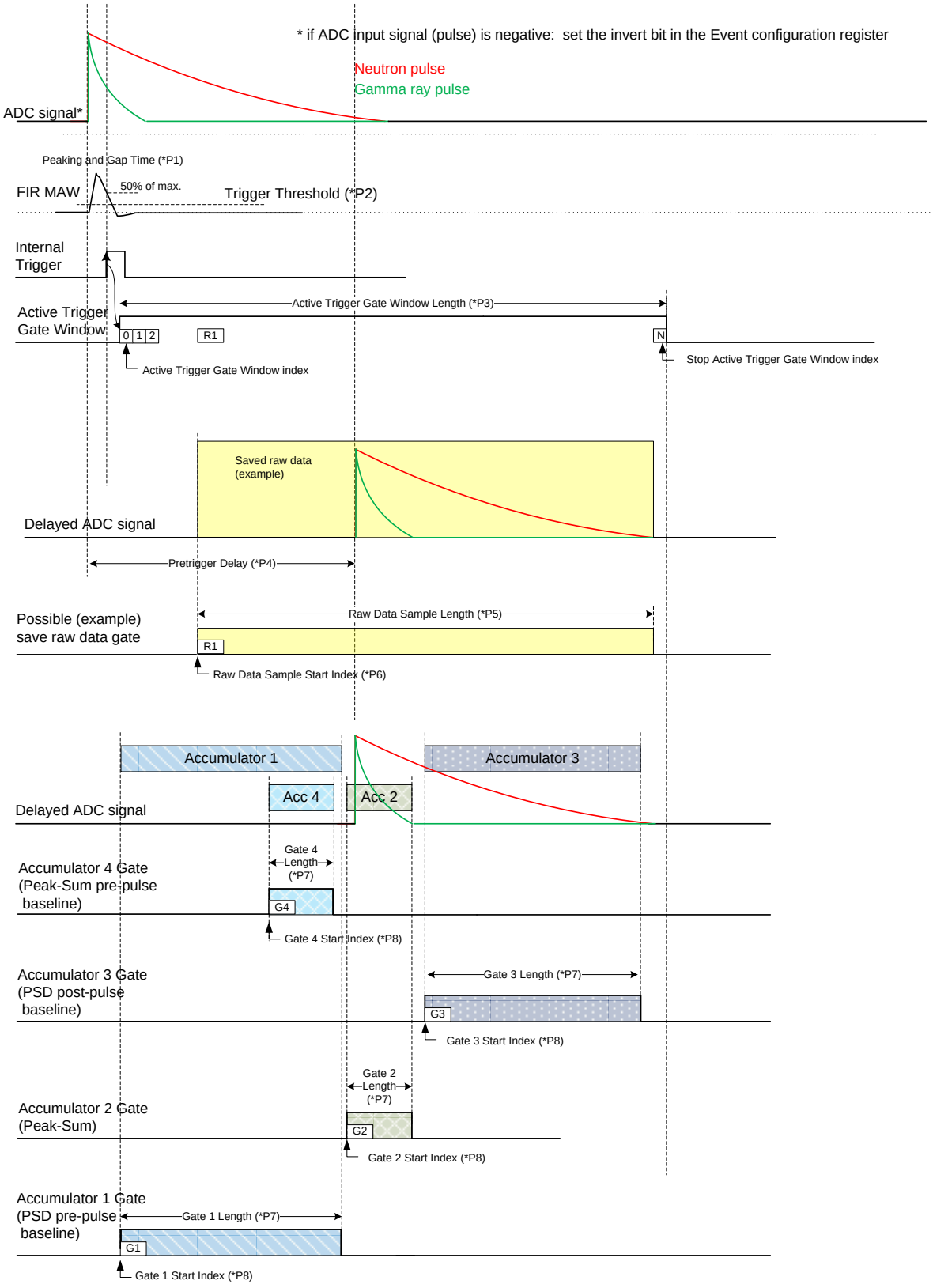
- *P3: Active Trigger Gate Window Length: see Active Trigger Gate Window Length registers
- *P4: Pre Trigger Delay: see Pre Trigger Delay registers

- *P5: Raw Data Sample Length: see Raw Data Buffer Configuration registers
- *P6: Raw Data Sample Start Index: see Raw Data Buffer Configuration registers

- *P7: Gate Length: see Accumulator Gate X Configuration registers
- *P8: Gate Start Index: see Accumulator Gate X Configuration registers

- *P9: Gate Length: see Accumulator Gate X Configuration registers
- *P10: Gate Start Index: see Accumulator Gate X Configuration registers

Hit/Event Logic parameter illustration:



2.3 Internal Trigger Generation

A trapezoidal FIR filter is implemented for each ADC Channel to generate a trigger signal. This Trigger Signal can be used to trigger the gate/sample logic immediately (asynchronous sample mode) or it can be routed to SIS3316 LEMO output.
This Trigger Signal will be also used to generate the "Pileup and Re-Pileup" information, to build coincidence windows and to feed the Statistic Counter.

Features for each ADC channel:

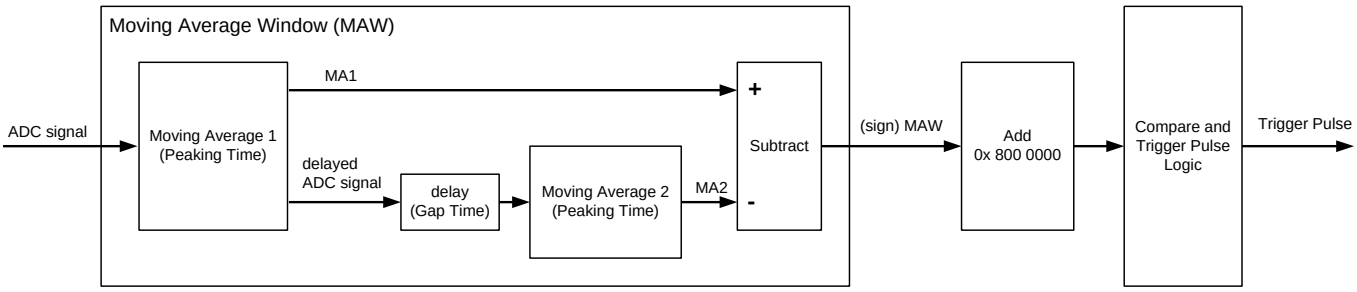
- Programmable Peaking Time (2, 4, 6, ….510)
- Programmable Gap Time (2, 4, 6, ….510)
- Programmable Trigger pulse out length (2, 4, 6, ….254)
- Programmable Trigger Threshold
- Programmable High Energy Suppress Trigger Threshold
- Programmable Trigger Mode (CFD)
- Programmable Trigger OUT (Enable, Disable)

See "FIR Trigger Setup", "Trigger Threshold" and "High Energy Suppress Trigger Threshold" registers.

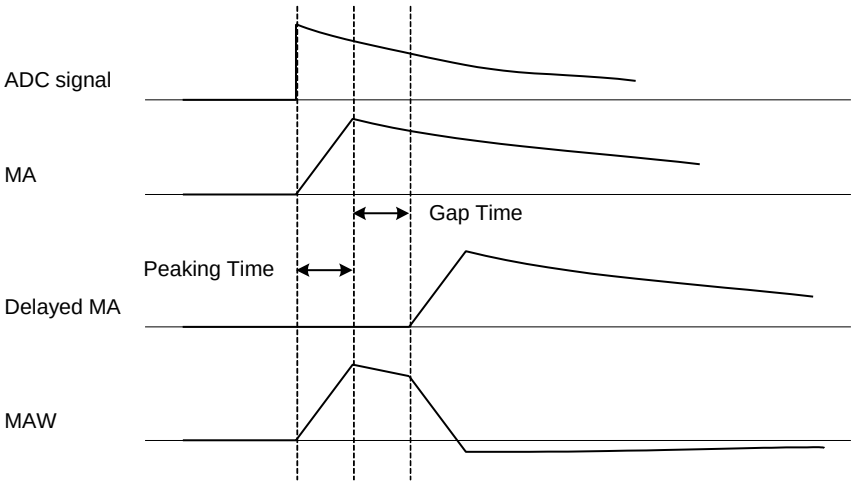
2.3.1.1 Block diagram of the Trigger MAW unit

Explanation:

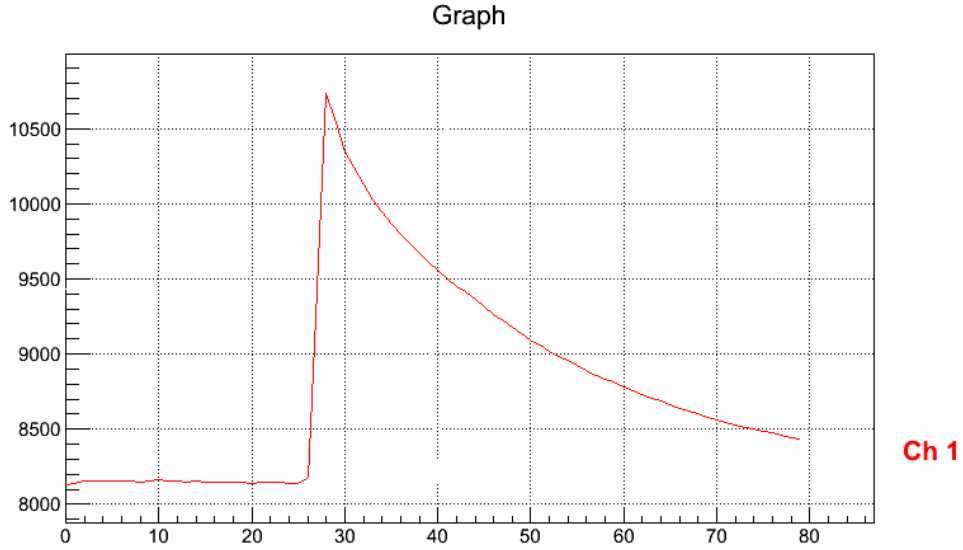
- MAW: moving average window
- MA: moving average
- Peaking Time: the length of the MA for moving average unit
- Gap Time: the differentiation time of the mowing window average unit



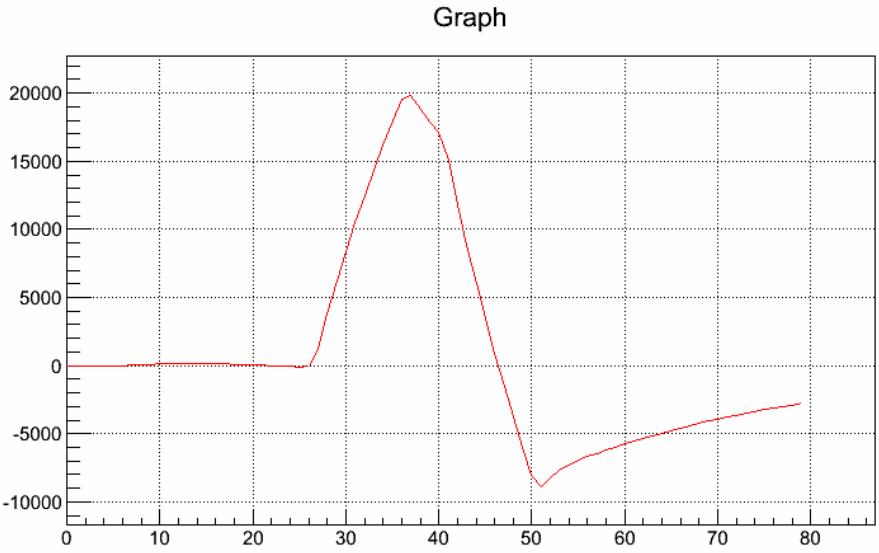
2.3.1.2 Signal diagram of the Trigger MAW unit



ADC Signal:

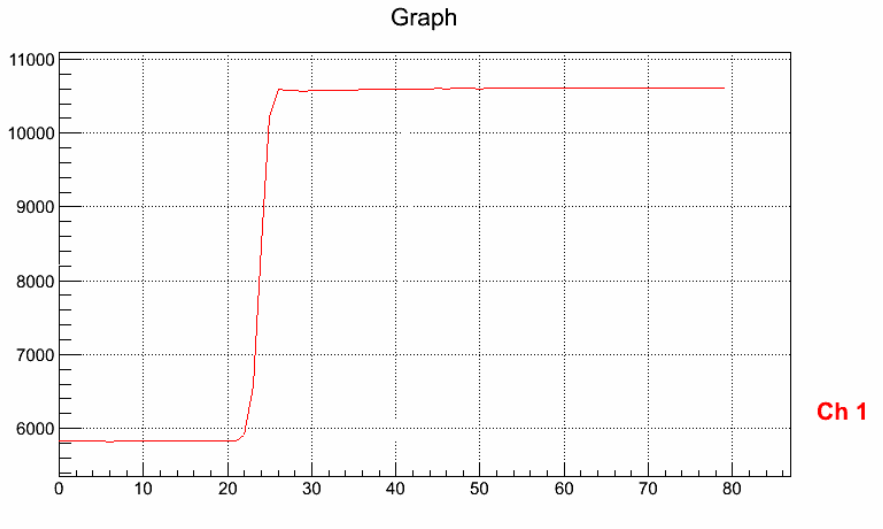


MAW Trapezoid:
P = 10, G = 4



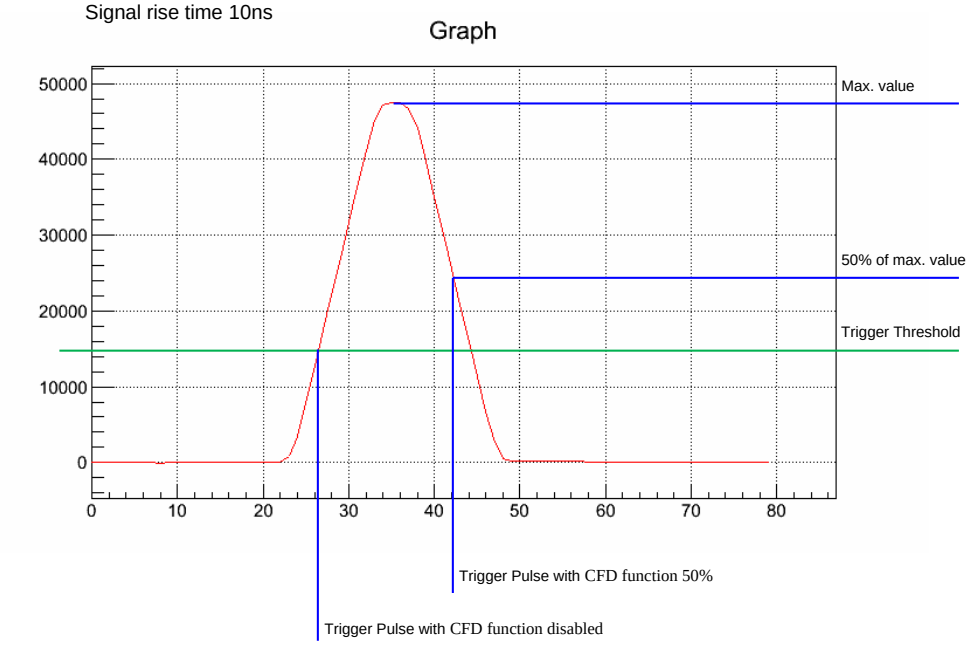
2.3.1.3 CFD Trigger Feature

ADC Signal:



P = 10, G = 4
Signal rise time 10ns

MAW:



CFD is disabled:

A trigger pulse will be issued if the actual trapezoidal value (MAW) goes above the programmable threshold value.

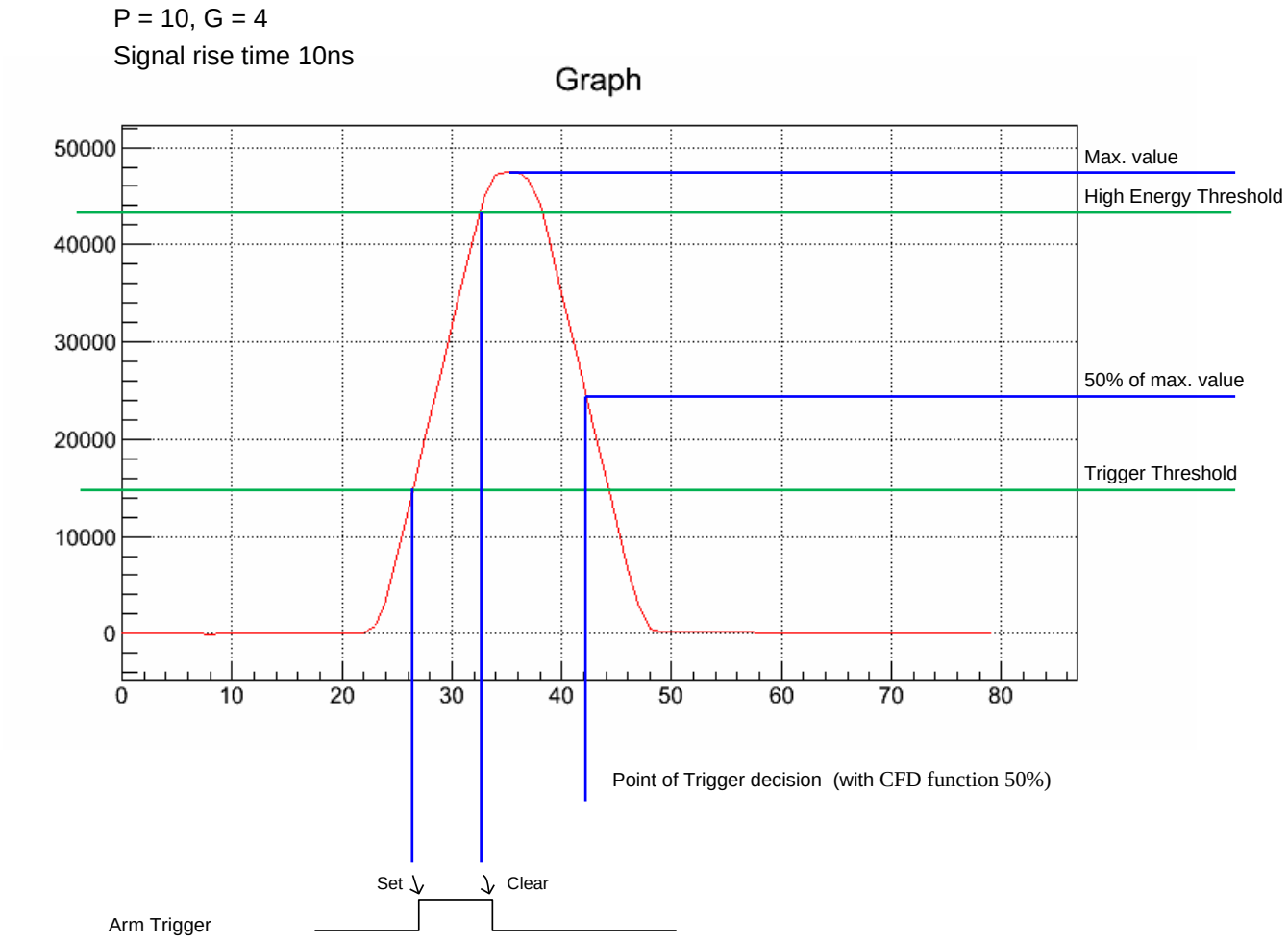
CFD is enabled:

The trigger logic will be armed if the actual trapezoidal value (MAW) goes above the programmable threshold value. The logic generates a trigger pulse if the trigger logic is armed and the actual trapezoidal value falls below the half of its maximum value (50%).

The 50% crossing of this digital CFD can be compared to the zero crossing of an analog CFD. The moment of the trigger doesn't depend on the pulse amplitude (provided that the rise times of the signals are identical).
The time resolution of the CFD trigger feature is limited by the sampling frequency.

2.3.1.4 High Energy Suppress Trigger Mode

A High Energy Suppress Trigger Mode is implemented to suppress triggers. A trigger will be suppressed if the running sum of the trapezoidal filter goes above the value of the High Energy Threshold register.



The Trigger Logic will be armed if the trapezoidal filter value (red) goes above the Trigger Threshold value and it will be disarmed if the trapezoidal filter value goes above the High Energy Threshold value. The trigger will be generated only if the "Arm Trigger" signal is valid at the point of trigger decision.

Note: This mode works only with the CFD function enabled!

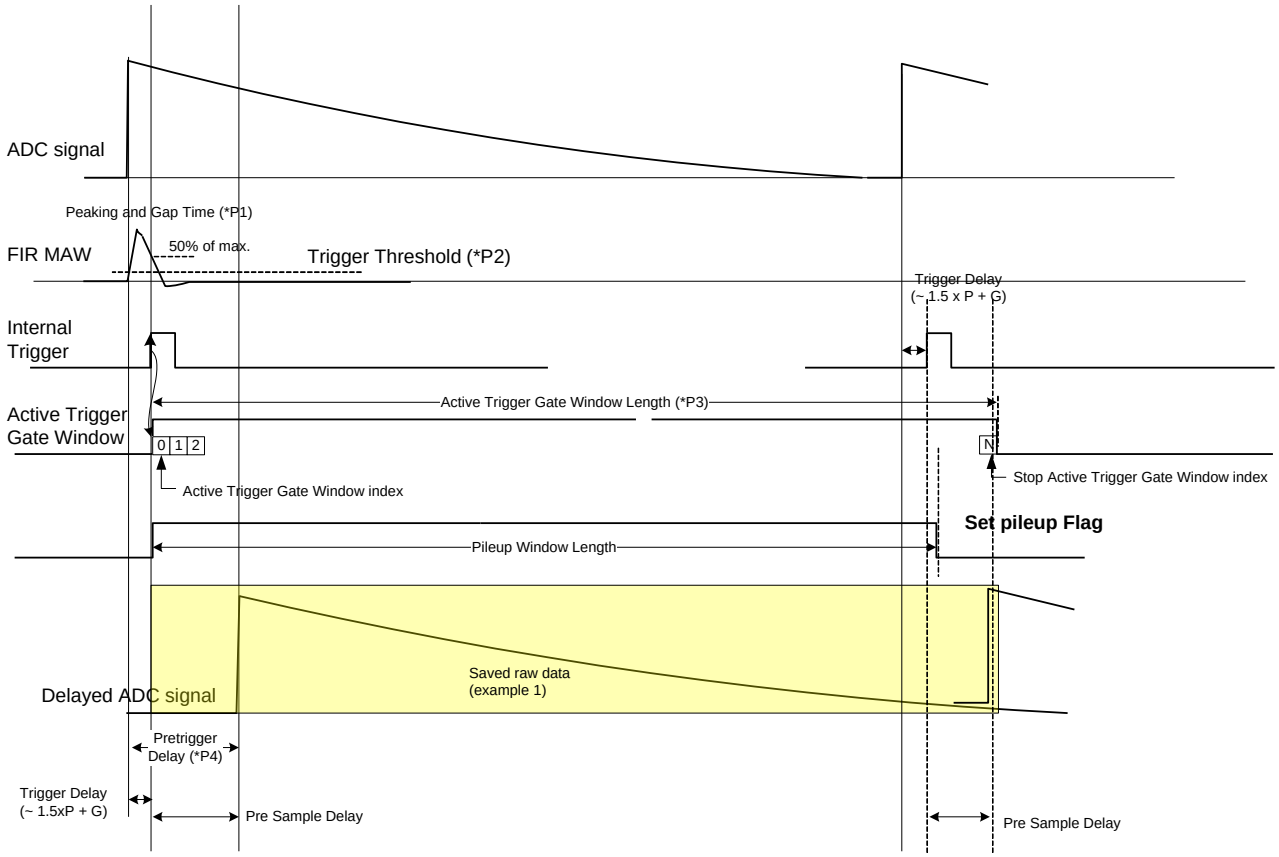
2.4 Pileup Detection Logic

A pileup detection logic is implemented for each channel. This logic allows for the definition of two windows (time slots):
1. after the hit (trigger starts the "Active Trigger Gate Window") → detect Pileups
2. before the hit (trigger starts the "Active Trigger Gate Window") → detect Re-Pileups (or Pre-Pileup)

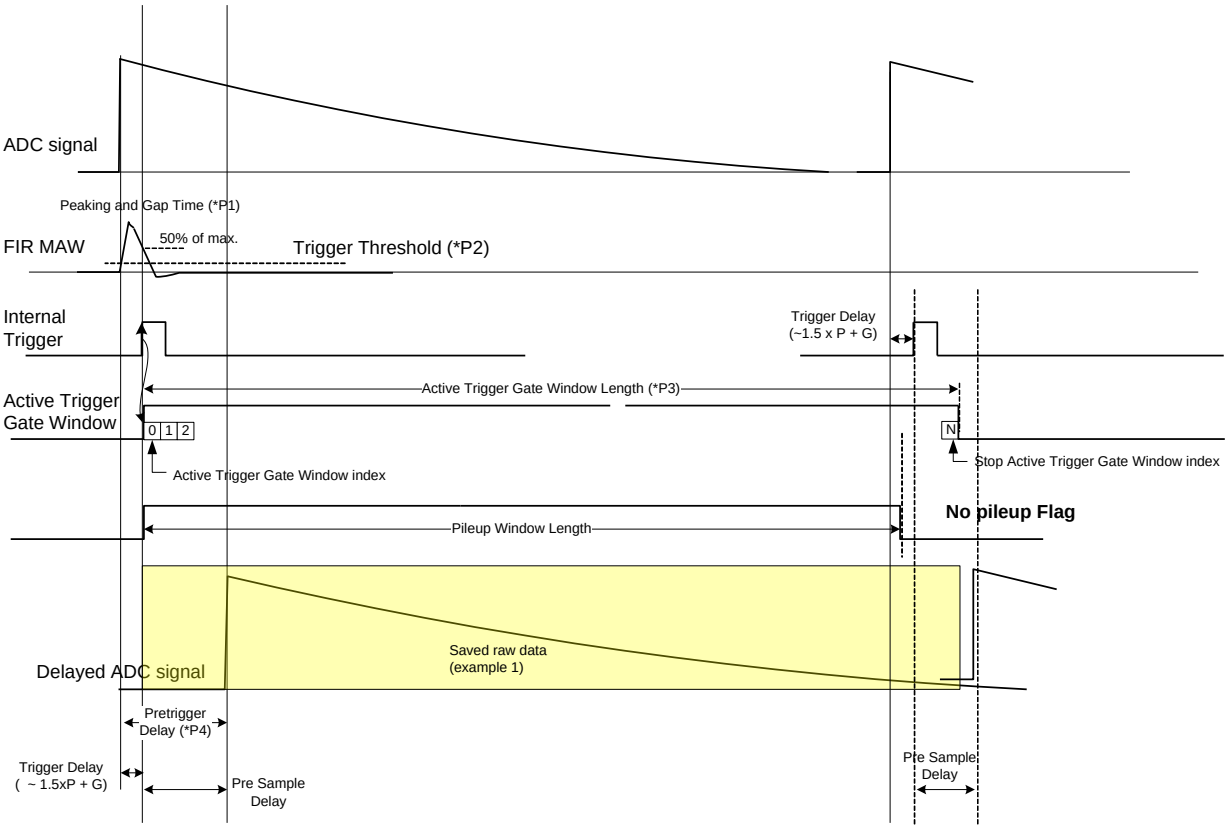
2.4.1 Pileup Window

The "Pileup Window" starts with the start of the "Active Trigger Gate Window". The Length of the "Pileup Window" is programmed with the Pileup Configuration registers.
A Pileup Flag will be set if the "Pileup Window" is active and a further internal trigger pulse appears (see below).

Set Pileup Flag Illustration:

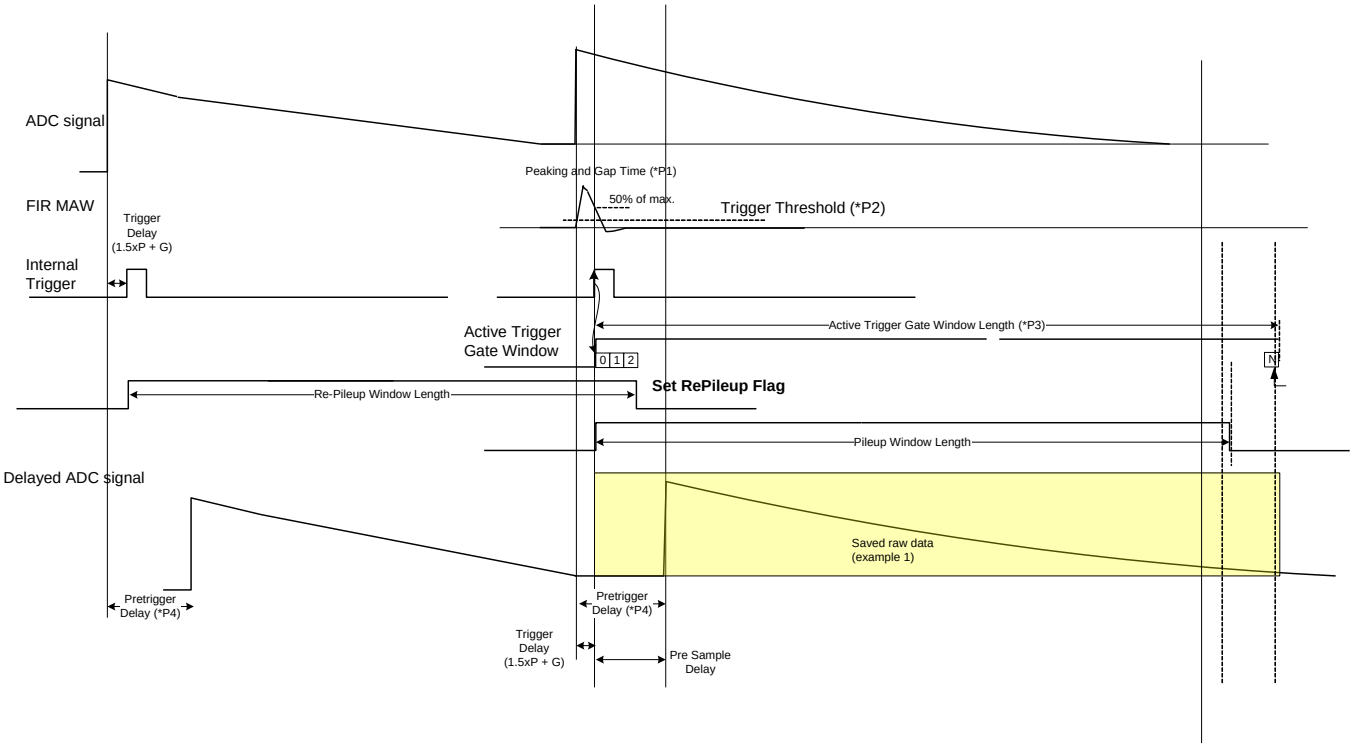


Not set Pileup Flag Illustration:



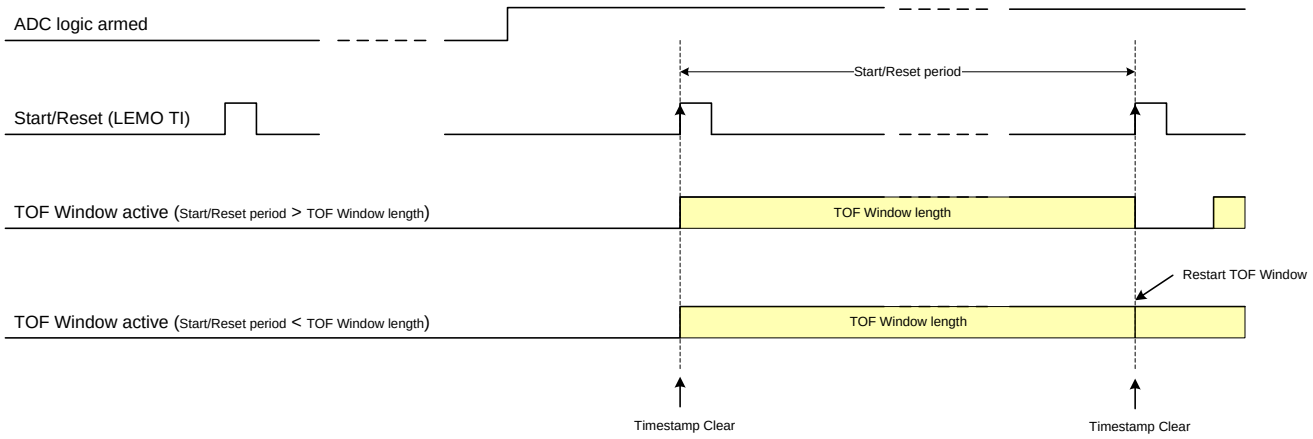
2.4.2 Re-Pileup (Pre-Pileup) Window

The “Re-Pileup Window” starts (restarts) with each internal trigger pulse. The length of the “Re-Pileup Window” is programmed with the Pileup Configuration registers.
A Re-Pileup Flag will be set if the “Re-Pileup Window” is active and a further internal trigger pulse triggers the start of the “Active Trigger Gate Window” (see below).
.



2.5 TOF Window Logic

TOF Window logic illustration:



After the ADC sample logic is armed a next Start/Reset pulse on LEMO TI starts the TOF Window Active and clears the timestamp. Depend on the configuration of the histogram logic the logic will histogram only if the TOF Window is active or not.

See TOF Window configuration register(s).

2.6 Histogram Logic

The Histogram logic holds six histograms for each channel inside of the SIS3316 Memory:

- PSD 2D-histogram 1 (PSD value versus Peak-Sum)
- PSD lookup table 2D-histogram 2 (PSD Lookup table)
- Peak-Sum 1D-histogram 1 (Gamma ray)
- Peak-Sum 1D-histogram 2 (Neutron)
- TOF 1D-histogram 1 (Gamma ray)
- TOF 1D-histogram 1 (Neutron)

The histogram logic takes the four Accumulator values and calculates the PSD value (y-axis) and the Peak-Sum (x-axis). For the calculation of the PSD value are two methods implemented. Two configuration registers (x- and y-axis) are implemented to adapt the PSD and Peak-Sum values to the x and y-axis of the histogram.

If the calculated x-axis index and y-axis index are valid (between 0 and 511) then the logic reads the value with the calculated axis indexes from the PSD Lookup table histogram. The reading value will classify the pulse:

- 0: ignore (unclassified)
- 1: Gamma ray
- 2: Neutron

If the type of the pulse is a “Gamma” then the Gamma-Peak-Sum and the Gamma-TOF histogram will be incremented.
If the type of the pulse is a “Neutron” then the Neutron-Peak-Sum and the Neutron -TOF histogram will be incremented.

In case of Pileups and/or Overflows it is programmable (enable/disable) whether the logic increments the histograms or not.

The “histogram rate” of the Histogram logic is 1 MHz per channel.

2.6.1 PSD Histograms

The PSD 2D-Histogram logic is configured with the Shape Histogram X-axis Configuration register(s) and the Shape Histogram Y-axis Configuration register(s).
The Histogram size is 512 x 512 bins.

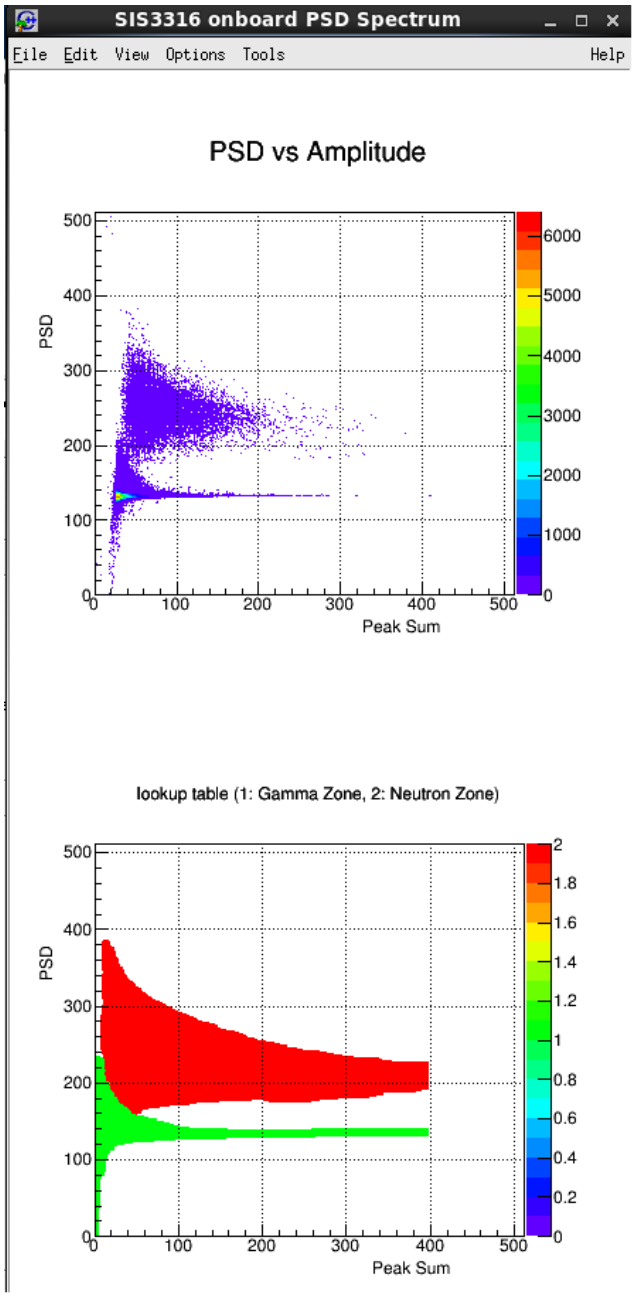
2.6.1.1 PSD Histogram using Method 1

PSD value (y-axis index) =
(((Acc. 3 – Acc. 1) * 0x10000) / (Acc. 2 – Acc. 4)) / y-axis-divider*) + y-axis-offset*

*Shape 2-D Histogram Y-axis Configuration registers

Peak-Sum value (x-axis index*) =
((Acc. 2 – Acc. 4) / x-axis-divider*)
+ x-axis-offset*

**Shape 2-D Histogram X-axis Configuration registers



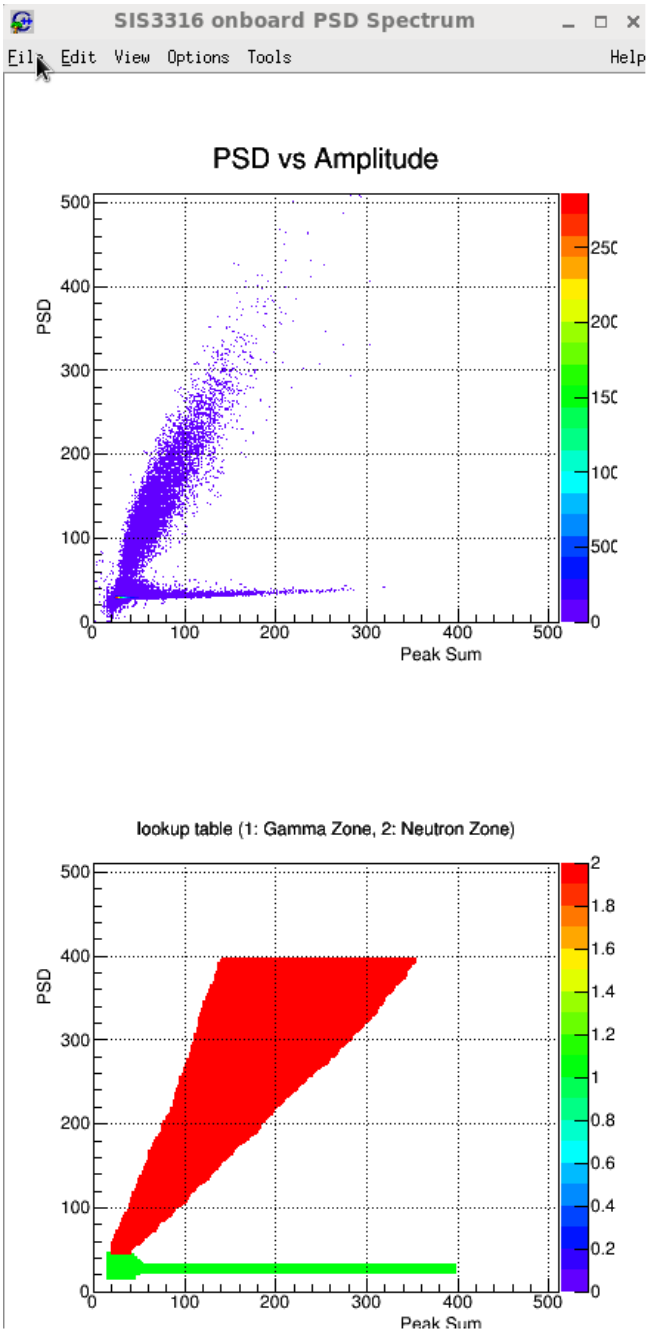
2.6.1.2 PSD Histogram using Method 2

PSD value (y-axis index) =
((Acc. 3 – Acc. 1) / y-axis-divider*)
+ y-axis-offset*

*Shape 2-D Histogram Y-axis Configuration registers

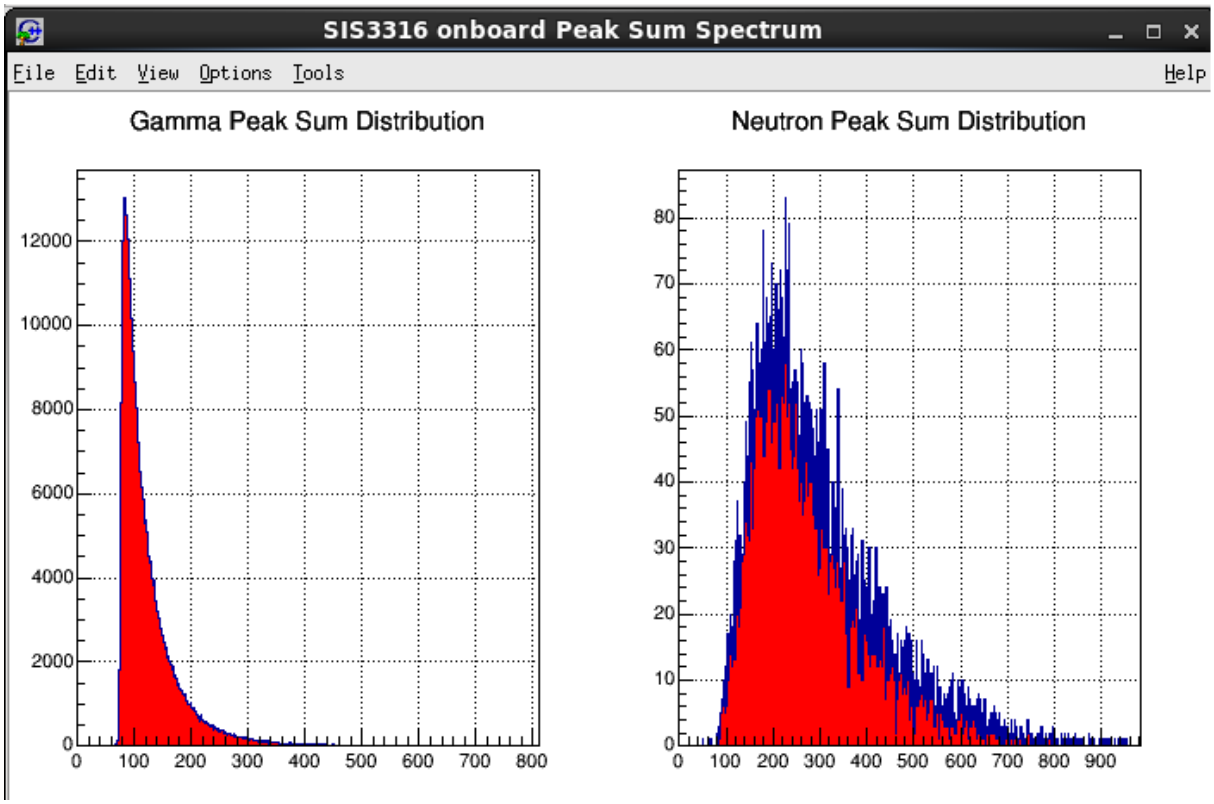
Peak-Sum value (x-axis index) =
((Acc. 2 – Acc. 4) / x-axis-divider**)
+ x-axis-offset**

**Shape 2-D Histogram X-axis Configuration registers



2.6.2 Peak-Sum Histograms

The Peak-Sum 1D-Histogram logic is configured with the Peak-Sum Histogram Configuration register(s).



The Histogram size is 64 K bins.

The 24-bit Peak-Sum value (Accumulator Sum Gate 2 - Accumulator Sum Gate 4) can be divided by a 12-bit programmable value to map the Peak-Sum value to the X-axis bin.

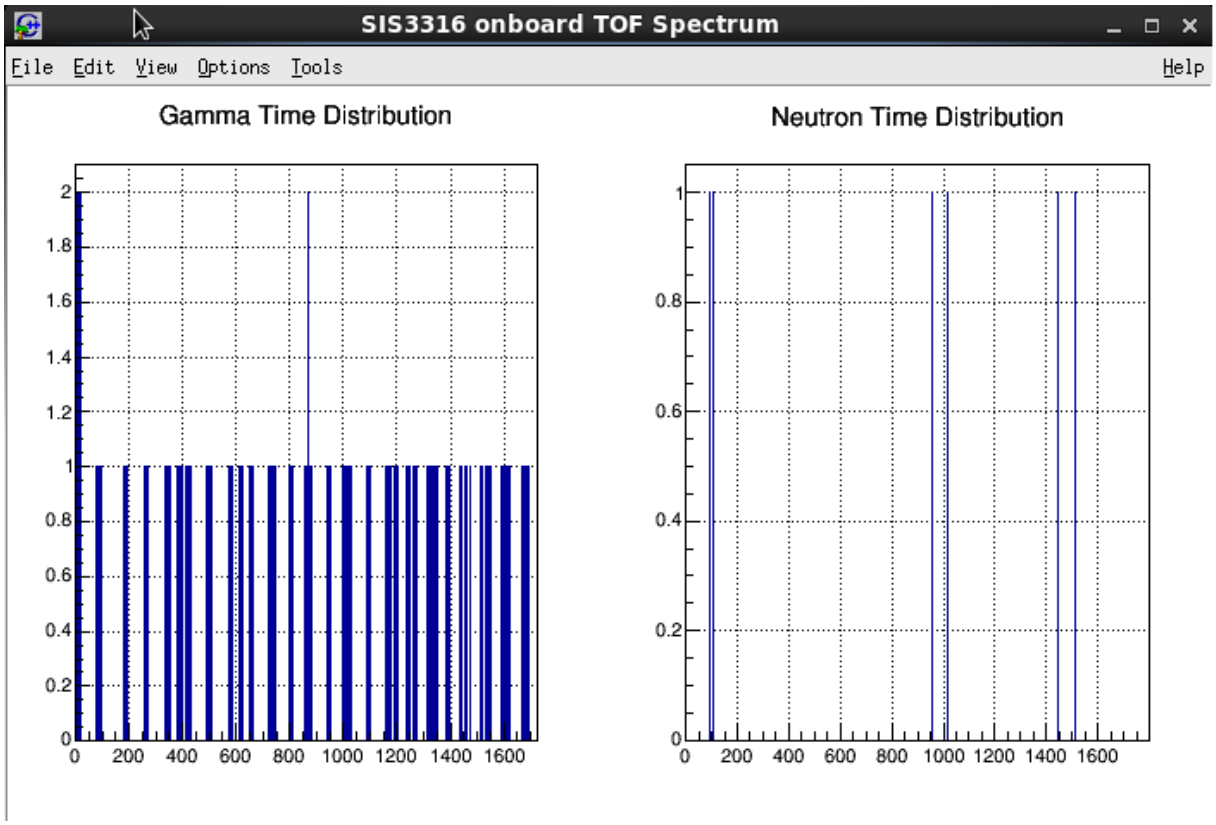
Values which are higher than 64 K will be ignored.

Peak-Sum value (x-axis index) =
((Acc. 2 – Acc. 4) / x-axis-divider*) + x-axis-offset*

*Peak Sum Histogram Configuration registers

2.6.3 TOF Histograms

The TOF (time of flight) 1D-Histogram logic is configured with the TOF Histogram Configuration register(s).



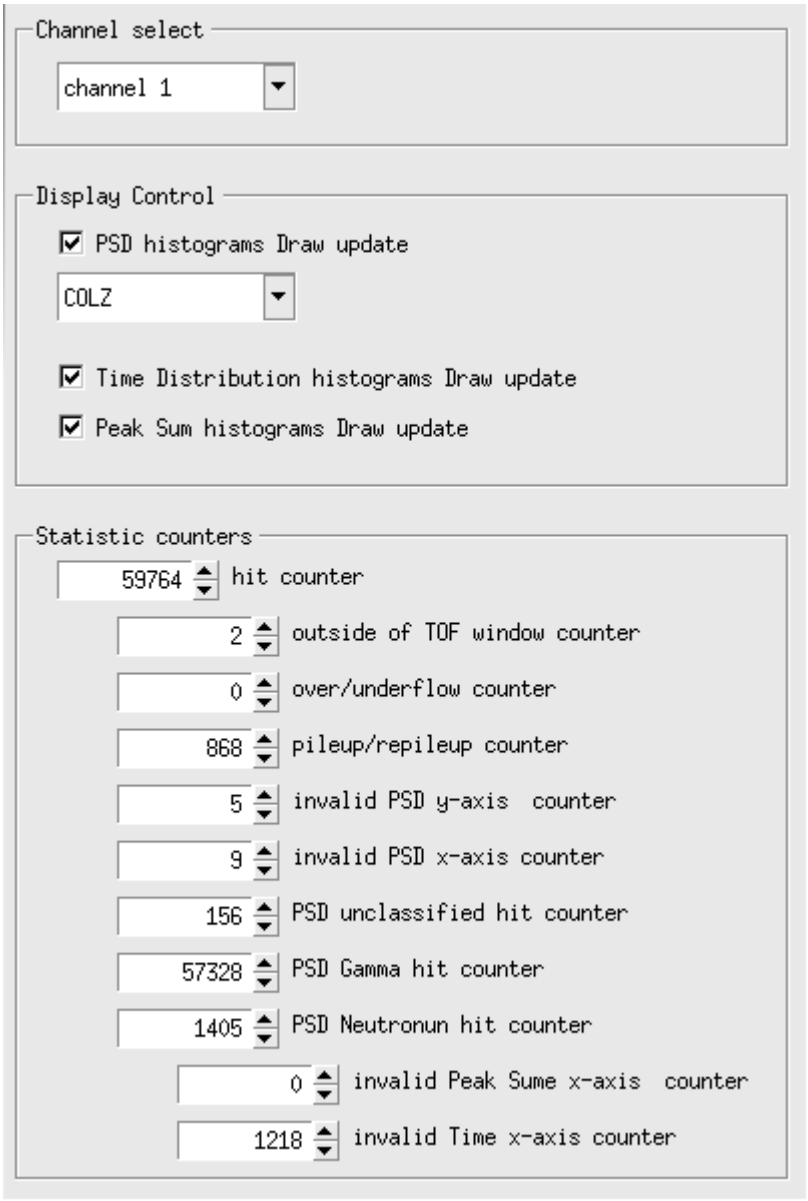
The Histogram size is 1 M bins.

The 40-bit timestamp (4 ns / 250 MHz) can be divided by a 24-bit programmable value to map the timestamp value to the X-axis bin.

Values higher than 1 M will be ignored.

2.6.4 Statistic counters

Eleven statistic counters are implemented for each channel:



All counters will be cleared with a “Histogram-Clear” command.

Statistic Counter Data Format:

Ch1 hit counter[31:0]
Ch1 outside of TOF Window counter[31:0]
Ch1 over/underflow counter[31:0]
Ch1 pIleup/repileup trigger counter[31:0]
Ch1 invalid PSD y-axis counter[31:0]
Ch1 invalid PSD x-axis counter[31:0]
Ch1 PSD unclassified hit counter[31:0]
Ch1 PSD Gamma hit counter[31:0]
Ch1 PSD Neutron hit counter[31:0]
Ch1 invalid Peak-Sum x-axis counter[31:0]
Ch1 invalid Peak-Sum y-axis counter[31:0]
reserved
reserved
reserved
reserved
reserved

Ch2 hit counter[31:0]
Ch2 outside of TOF Window counter[31:0]

• •
• •
• •

Ch4 invalid Peak-Sum x-axis counter[31:0]
Ch4 invalid Peak-Sum y-axis counter[31:0]

The “ADC FPGA Data Transfer” Logic has to be used to read/get the Statistic Counters.

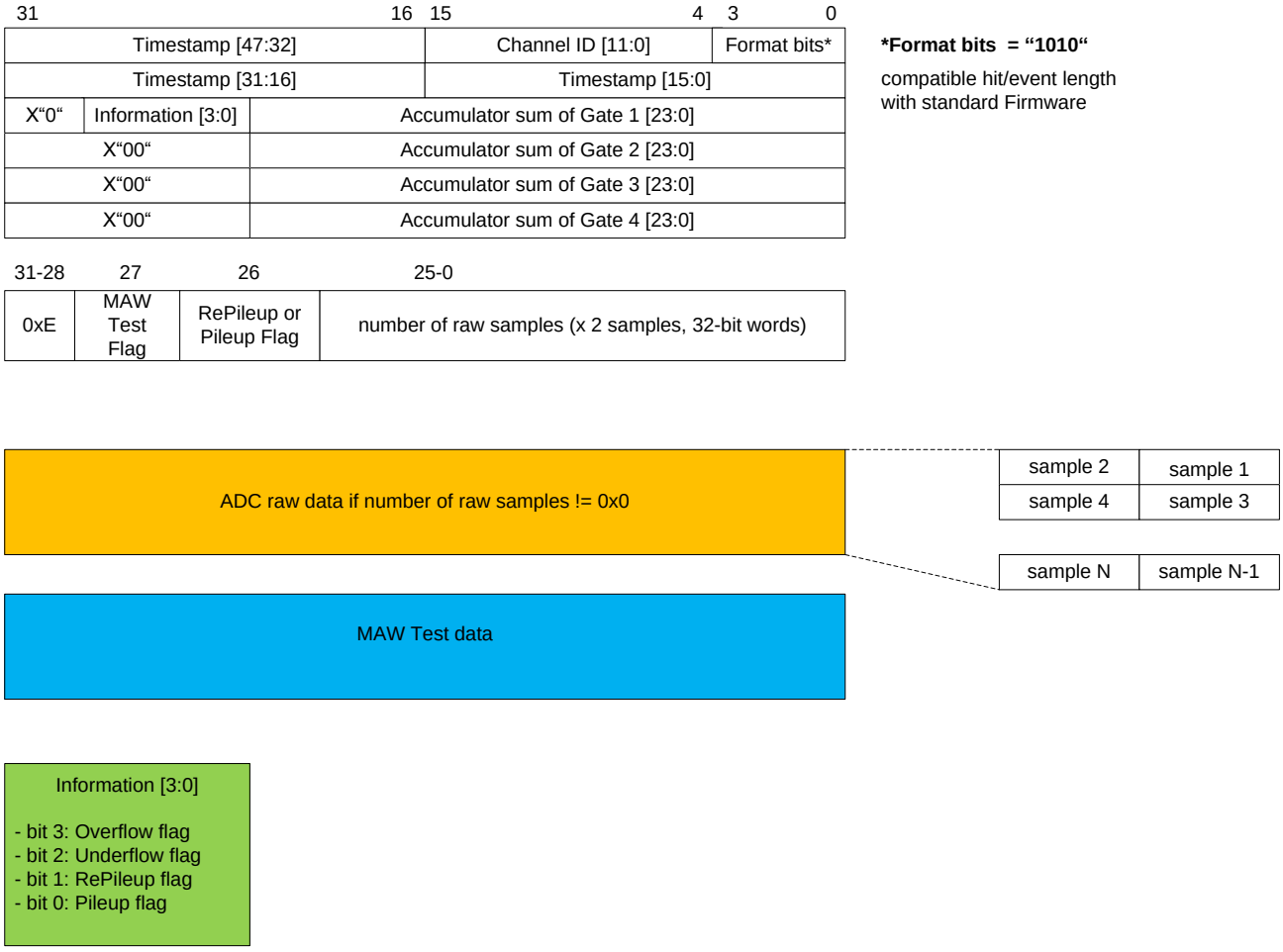
Example: read Trigger Statistic Counter

```
// start readout FSM
i_adc=0; // only channel 1 to ch4
vme_crate->vme_A32D32_write ( module_base_addr +
                              SIS3316_DATA_TRANSFER_CH1_4_CTRL_REG + (i_adc*4) ,
                              0x80000000 +  0x30000000 );  //  Space = Statistic counter
// read from FIFO
req_nof_32bit_words = 24 ;
vme_crate->vme_A32BLT32FIFO_read ( module_base_addr
                              +SIS3316_FPGA_ADC1_MEM_BASE
                              + (i_adc*SIS3316_FPGA_ADC_MEM_OFFSET), gl_rblt_data,
                              req_nof_32bit_words, &got_nof_32bit_words);  //
```

2.7 Hit/Event Data Format

The data format is illustrated below. You have the option to get raw data besides integrals (Accumulator sums), if you choose a non zero value for the number of raw samples The timestamp information is stored with the leading edge of the "Active Trigger Gate window".

The Hits/Events are stored to Bankx memory with the following data format:



2.8 Memory Organization

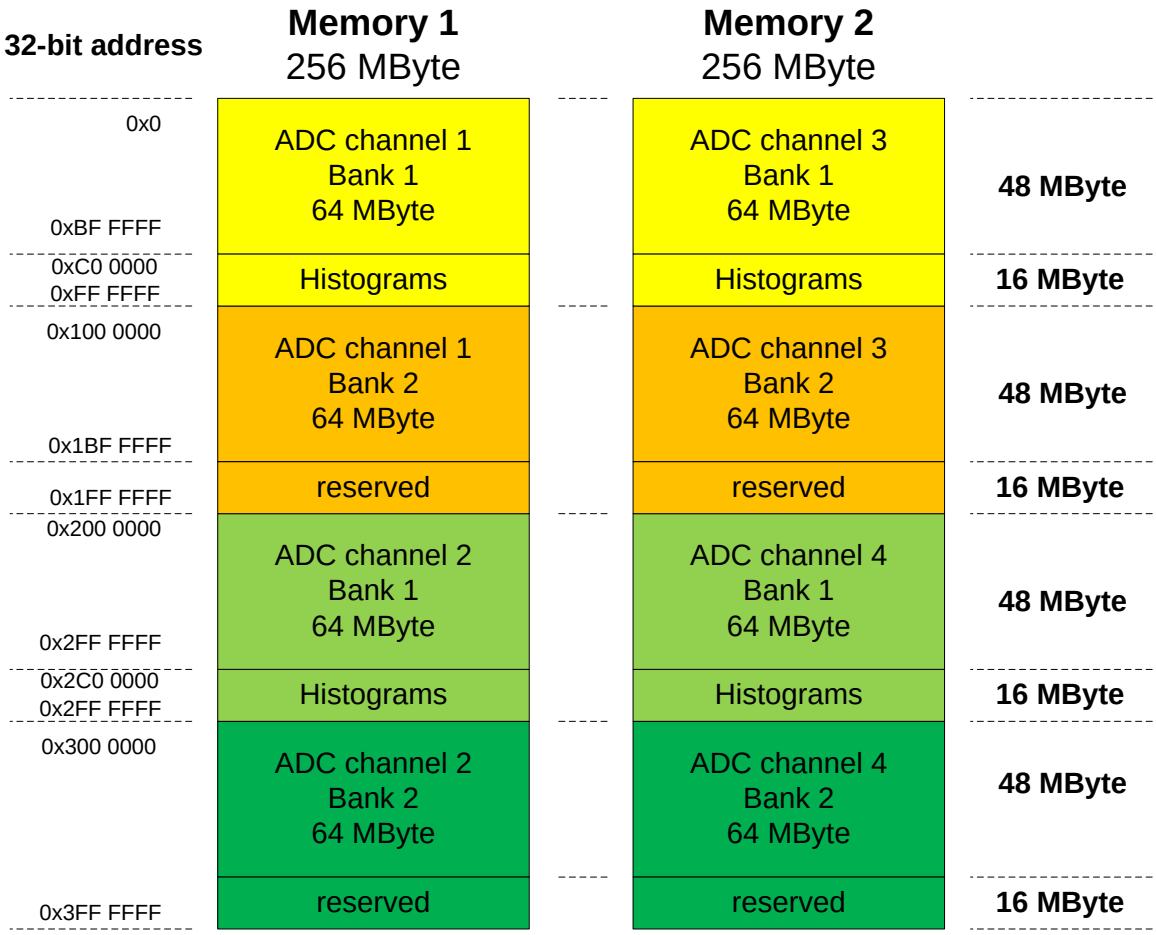
Each ADC FPGA group (4 ADC channels) has two physical DDR3-memory-chips of 256MByte each → 512 MByte for four channels → 128 MByte per channel.

Two ADC data storage modes (hits/events) are foreseen:

- Double Bank mode
- Single Bank mode (reserved, not implemented yet)

2.8.1 Double Bank mode

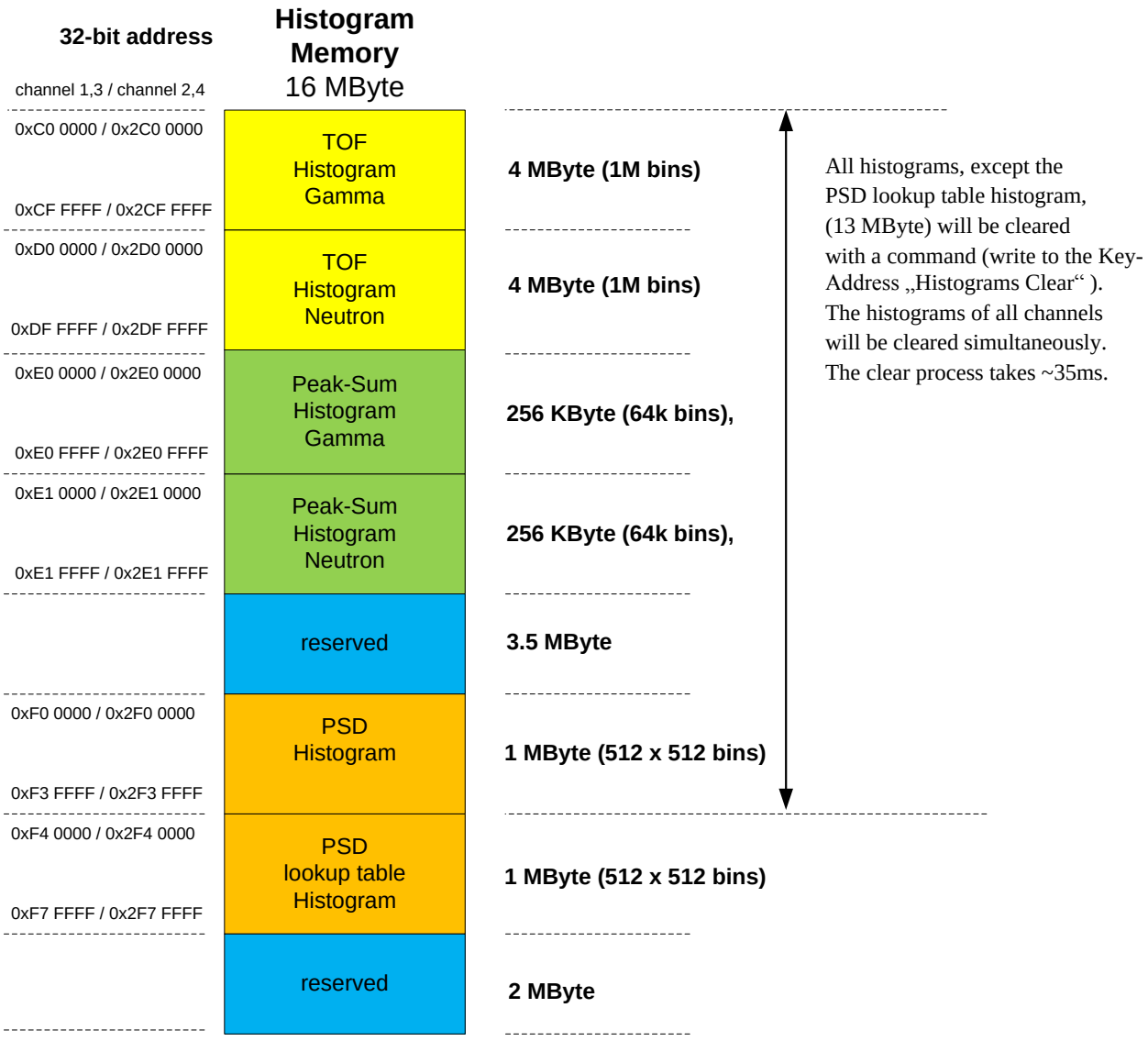
In Double Bank mode two banks of 64 MByte each are dedicated to each ADC channel.



The sample logic writes the Hits/Events with each trigger (internal or external) to the "armed Bank" continuously. The memory address logic generates a veto signal if the 48 MByte Bank is almost full (48 MByte – 512 KByte). In this case the logic ignores following triggers to suppress an overwriting of the following memory space (next Bank or channel Bank).

2.8.1.1 Histogram Memory

16 MByte of each Channel Memory Bank is used for histogramming.
The Histograms are divided as shown below:



3 VME Addressing

The base address is defined by the selected addressing mode, which is selected by jumper array SW80 and SW1 and SW2 (in non geographical mode).

The table below summarises the possible base address settings.

SW80 Setting		Bits							
EN_A32	EN_GEO	31	30	29	28	27	26	25	24
x		SW1				SW2			
	x	To be implemented							

Shorthand	Explanation
SW1/SW2	Setting of rotary switch SW1 or SW2 respective

Notes:

- This concept allows the use of the SIS3316 in standard VME as well as in VME64x environments, i.e. the user does not need to use a VME64x backplane.
- The factory default setting is EN_A32 closed, SW1=4, SW2=1 (i.e. the module will react to A32 addressing under address 0x41000000). With more than one unit shipped in one batch a set of addresses (like 0x41000000, 0x42000000, 0x43000000,...) may be used also.

3.1 Address Map Overview

The SIS3316 resources and their locations are listed in the tables below.

Offset	BLT	Access	Function
0x000000 – 0x00001C	-	W/R	VME FPGA interface registers
0x000020 – 0x0000FC	-	W/R	VME FPGA registers
0x000400 – 0x00043C	-	W only	VME FPGA key addresses (with Broadcast functionality)
0x001000 – 0x001FFC	-	R/W	ADC FPGA 1: ch1-ch4 registers
0x002000 – 0x002FFC	-	R/W	ADC FPGA 2: ch5-ch8 registers
0x003000 – 0x003FFC	-	R/W	ADC FPGA 3: ch9-ch12 registers
0x004000 – 0x004FFC	-	R/W	ADC FPGA 4: ch13-ch16 registers
0x100000 – 0x1FFFFC	x	R/W	ADC FPGA 1: ch1-ch4 Memory Data FIFO
0x200000 – 0x2FFFFC	x	R/W	ADC FPGA 2: ch5-ch8 Memory Data FIFO
0x300000 – 0x3FFFFC	x	R/W	ADC FPGA 3: ch9-ch12 Memory Data FIFO
0x400000 – 0x4FFFFC	x	R/W	ADC FPGA 4: ch13-ch16 Memory Data FIFO

Note 1:
- Read/Write access to the VME FPGA interface register space is always possible.
- Read access to the VME FPGA register space is always possible.
- Write access to the VME FPGA register and "key address" space is only possible if the "Link" interface has no grant.
- Read/Write access to the ADC FPGA register and memory space is only possible if the "Link" interface has no grant.

Note 2: Write access to a key address (KA) with arbitrary datum invokes the respective action

Note 3: Only the yellow marked registers/key addresses are described in this manual.

0x00000404	4	-	KA W	VME Key Histograms Clear (35 ms)

3.1.1 VME FPGA interface registers

Offset	Access	Function
0x00000000	W/R	Control/Status Register (J-K register)
0x00000004	R only	Module Id. and Firmware Revision register
0x00000008	R/W	Interrupt configuration register
0x0000000C	R/W	Interrupt control register
0x00000010	R/W	Interface Access Arbitration control/status register
0x00000014	R/W	CBLT/Broadcast Setup register
0x00000018	R/W	Internal test
0x0000001C	R/W	Hardware Version register

3.1.2 VME FPGA registers

Offset	Access	Function
0x00000020	R	Temperature register
0x00000024	R/W	Onewire control/status register (EEPROM DS2430)
0x00000028	R	Serial number register
0x0000002C	R/W	reserved
0x00000030	R/W	ADC FPGAs Boot Controller
0x00000034	R/W	SPI Flash Control/Status
0x00000038	R/W	SPI Flash Data
0x0000003C	R/W	Reserved for FlashPROM programming
0x00000040	R/W	Programmable ADC Clock: Oscillator I2C register
0x00000044	R/W	Programmable MGT1 Clock: Oscillator I2C register
0x00000048	R/W	Programmable MGT2 Clock: Oscillator I2C register (option, not used)
0x0000004C	R/W	Programmable DDR3 Clock: Oscillator I2C register (option, not used)
0x00000050	R/W	ADC Sample Clock distribution control register
0x00000054	R/W	External NIM Clock Multiplier (Si5325) SPI register
0x00000058	R/W	FP-Bus control register
0x0000005C	R/W	NIM-IN Control/Status register
0x00000060	R/W	Acquisition control/status register
0x00000064	R/W	reserved
0x00000068	R/W	reserved
0x0000006C	R/W	reserved

0x00000070	R/W	LEMO Out “CO” Select register
0x00000074	R/W	LEMO Out “TO” Select register
0x00000078	R/W	LEMO Out “UO” Select register
0x0000007C	R/W	reserved
0x00000080	R/W	ADC FPGA 1: ch1-ch4 FPGA Data Transfer Control register
0x00000084	R/W	ADC FPGA 2: ch5-ch8 FPGA Data Transfer Control register
0x00000088	R/W	ADC FPGA 3: ch9-ch12 FPGA Data Transfer Control register
0x0000008C	R/W	ADC FPGA 4: ch13-ch16 FPGA Data Transfer Control register
0x00000090	R only	ADC FPGA 1: ch1-ch4 FPGA Data Transfer Status register
0x00000094	R only	ADC FPGA 2: ch5-ch8 FPGA Data Transfer Status register
0x00000098	R only	ADC FPGA 3: ch9-ch12 FPGA Data Transfer Status register
0x0000009C	R only	ADC FPGA 4: ch13-ch16 FPGA Data Transfer Status register
0x000000A0	R/W	VME FPGA – ADC FPGAs Data Link Status register
0x000000A4	R only	ADC FPGA SPI Busy Status register
0x000000A8	R/W	reserved
0x000000AC	R/W	reserved
0x000000B0	R/W	SFP I2C Interface Test (for internal use)
0x000000B4	R/W	SFP Interface Test (for internal use)
0x000000B8	R/W	VXS-Bus Line IN/OUT Test (for internal use)
0x000000BC	R/W	ADC Control SGL Line Out Test (for internal use)
0x000000C0	R/W	Link Interface Test (for internal use)
0x000000C4	R/W	reserved
0x000000C8	R/W	reserved
0x000000CC	R/W	reserved
0x000000D0	R/W	ADC Trigger Line IN and Status Out Test (for internal use)
0x000000D4	R/W	External and ADC Trigger Line IN (clocked) Test (for internal use)
0x000000D8	R/W	FP-Bus Line IN/OUT Test (for internal use)
0x000000DC	R/W	reserved

3.1.3 Key address registers

Offset	Size in Bytes	BLT	Access	Function
0x00000400	4	-	KA W	VME Key Register Reset
0x00000404	4	-	KA W	VME Key Histograms Clear (35 ms)
0x00000408	4	-	KA W	reserved
0x0000040C	4	-	KA W	reserved
0x00000410	4	-	KA W	VME Key Arm Sample Logic (Single Bank Mode)
0x00000414	4	-	KA W	VME Key Disarm Sample Logic
0x00000418	4	-	KA W	VME Key Trigger
0x0000041C	4	-	KA W	VME Key Timestamp Clear
0x00000420	4	-	KA W	VME Key Disarm Bankx and Arm Bank1
0x00000424	4	-	KA W	VME Key Disarm Bankx and Arm Bank2
0x00000428	4	-	KA W	VME Key Enable “Sample Bank Swap Control with NIM Input TI/UI” Logic
0x0000042C	4	-	KA W	reserved
0x00000430	4	–	KA W	reserved
0x00000434	4	–	KA W	VME Key Reset ADC-FPGA-Logic (DDR3-Memory, FPGA-Link Interface)
0x00000438	4	–	KA W	VME Key ADC Clock DCM /PLL Reset
0x0000043C	4	–	KA W	reserved

3.1.4 FPGA ADC group 1 registers (Ch1 to Ch4)

Offset	Size in Bytes	Access	Function
0x01000	4	R/W	ADC Input Tap Delay register ch1-ch4
0x01004	4	R/W	ADC Gain/Termination Control register ch1-ch4
0x01008	4	R/W	ADC Offset (DAC) Control register
0x0100C	4	R/W	ADC SPI Control register
0x01010	4	R/W	Event Configuration register ch1-ch4
0x01014	4	R/W	Channel Header ID register
0x01018	4	R/W	End Address Threshold register ch1-ch4
0x0101C	4	R/W	Active Trigger Gate Window Length register
0x01020	4	R/W	Raw Data Buffer Configuration register
0x01024	4	R/W	Pileup Configuration register
0x01028	4	R/W	Pre Trigger Delay register
0x0102C	4	R/W	reserved
0x01030	4	R/W	Data Format Configuration register
0x01034	4	R/W	MAW Test Buffer Configuration register
0x01038	4	R/W	Internal Trigger Delay Configuration register
0x0103C	4	R/W	Internal Gate Length Configuration register (Coincidence)
0x01040	4	R/W	FIR Trigger Setup Ch1
0x01044	4	R/W	Trigger Threshold Ch1
0x01048	4	R/W	High Energy Suppress Trigger Threshold Ch1
0x0104C	4	R/W	reserved
0x01050	4	R/W	FIR Trigger Setup Ch2
0x01054	4	R/W	Trigger Threshold Ch2
0x01058	4	R/W	High Energy Suppress Trigger Threshold Ch2
0x0105C	4	R/W	reserved
0x01060	4	R/W	FIR Trigger Setup Ch3
0x01064	4	R/W	Trigger Threshold Ch3
0x01068	4	R/W	High Energy Suppress Trigger Threshold Ch3
0x0106C	4	R/W	reserved
0x01070	4	R/W	FIR Trigger Setup Ch4
0x01074	4	R/W	Trigger Threshold Ch4
0x01078	4	R/W	High Energy Suppress Trigger Threshold Ch4
0x0107C	4	R/W	reserved

Offset	Size in Bytes	Access	Function
0x01080	4	R/W	reserved
0x01084	4	R/W	reserved
0x01088	4	R/W	reserved
0x0108C	4	R/W	reserved
0x01090	4	R/W	Trigger Statistic Counter Mode register [Ch1..Ch4]
0x01094	4	R/W	reserved
0x01098	4	R/W	reserved
0x0109C	4	R/W	reserved
0x010A0	4	R/W	Accumulator Gate 1 Configuration register
0x010A4	4	R/W	Accumulator Gate 2 Configuration register
0x010A8	4	R/W	Accumulator Gate 3 Configuration register
0x010AC	4	R/W	Accumulator Gate 4 Configuration register
0x010B0	4	R/W	reserved
0x010B4	4	R/W	reserved
0x010B8	4	R/W	reserved
0x010BC	4	R/W	reserved
0x010C0	4	R/W	TOF Active Window Configuration register [Ch1..Ch4]
0x010C4	4	R/W	reserved
0x010C8	4	R/W	reserved
0x010CC	4	R/W	General Histogram Configuration register [Ch1..Ch4]
0x010D0	4	R/W	TOF Histogram Configuration register [Ch1..Ch4]
0x010D4	4	R/W	Shape 2-D Histogram X-axis Configuration register [Ch1..Ch4]
0x010D8	4	R/W	Shape 2-D Histogram Y-axis Configuration register [Ch1..Ch4]
0x010DC	4	R/W	Peak-Sum Histogram Configuration register [Ch1..Ch4]

Offset	Size in Bytes	Access	Function
0x01100	4	R	ADC FPGA Version register
0x01104	4	R	ADC FPGA Status register
0x01108	4	R	ADC Offset (DAC) readback register
0x0110C	4	R	ADC SPI readback register
0x01110	4	R	Actual Sample address register Ch1
0x01114	4	R	Actual Sample address register Ch2
0x01118	4	R	Actual Sample address register Ch3
0x0111C	4	R	Actual Sample address register Ch4
0x01120	4	R	Previous Bank Sample address register Ch1
0x01124	4	R	Previous Bank Sample address register Ch2
0x01128	4	R	Previous Bank Sample address register Ch3
0x0112C	4	R	Previous Bank Sample address register Ch4
0x01130	4	R	Test: readback register 0x01010
0x01134	4	R	Test: readback register 0x01014
0x01138	4	R	Test: readback register 0x01018
0x0113C	4	R	Test: readback register 0x0101C

4 Register Description

The function of the yellow marked registers is described in detail in this section, while the non marked registers are covered in the “standard manual”.
The first line after the subsection header (in Courier font) like:

```
#define SIS3316_CONTROL_STATUS            0x0         /* read/write; D32 */
```

refers to the SIS3316.h header file

4.1 Event configuration registers

```
#define SIS3316_ADC_CH1_4_EVENT_CONFIG_REG                0x1010
#define SIS3316_ADC_CH5_8_EVENT_CONFIG_REG                0x2010
#define SIS3316_ADC_CH9_12_EVENT_CONFIG_REG               0x3010
#define SIS3316_ADC_CH13_16_EVENT_CONFIG_REG              0x4010
```

This register is implemented for each four channel group.

Bit	Function
31	reserved
30	reserved
29	reserved
28	reserved
27	CH4 External Trigger Enable bit
26	CH4 Internal Trigger Enable bit
25	reserved
24	CH4 Input Invert bit
23	reserved
22	reserved
21	reserved
20	reserved
19	CH3 External Trigger Enable bit
18	CH3 Internal Trigger Enable bit
17	reserved
16	CH3 Input Invert bit
15	reserved
14	reserved
13	reserved
12	reserved
11	CH2 External Trigger Enable bit
10	CH2 Internal Trigger Enable bit
9	reserved
8	CH2 Input Invert bit
7	reserved
6	reserved
5	reserved
4	reserved
3	CH1 External Trigger Enable bit
2	CH1 Internal Trigger Enable bit
1	reserved
0	CH1 Input Invert bit

CHx input invert bit = 0: used for positive signals
CHx input invert bit = 1: used for negative signals

ADCx Trigger enable bits

external trigger enable	internal trigger enable	Function
0	0	No triggering
0	1	internal channel based trigger (asynchronous mode)
1	0	external trigger (synchronous mode)
1	1	Or of internal channel based trigger and external trigger

4.2 Data Format Configuration registers

```
#define SIS3316_ADC_CH1_4_DATAFORMAT_CONFIG_REG          0x1030
#define SIS3316_ADC_CH5_8_DATAFORMAT_CONFIG_REG          0x2030
#define SIS3316_ADC_CH9_12_DATAFORMAT_CONFIG_REG         0x3030
#define SIS3316_ADC_CH13_16_DATAFORMAT_CONFIG_REG        0x4030
```

Bit	Function
31	reserved
30	reserved
29	reserved
28	Ch4 Save MAW Test Buffer Enable bit
27	reserved
26	reserved
25	reserved
24	reserved
23	Reserved
22	Reserved
21	Reserved
20	Ch3 Save MAW Test Buffer Enable bit
19	Reserved
18	Reserved
17	Reserved
16	reserved
15	reserved
14	Reserved
13	Reserved
12	Ch2 Save MAW Test Buffer Enable bit
11	Reserved
10	Reserved
9	Reserved
8	reserved
7	Reserved
6	reserved
5	Reserved
4	Ch1 Save MAW Test Buffer Enable bit
3	reserved
2	reserved
1	reserved
0	reserved

4.3 Accumulator Gate X Configuration registers

```
#define SIS3316_ADC_CH1_4_ACCUMULATOR_GATE1_CONFIG_REG          0x10A0
#define SIS3316_ADC_CH5_8_ACCUMULATOR_GATE1_CONFIG_REG          0x20A0
#define SIS3316_ADC_CH9_12_ACCUMULATOR_GATE1_CONFIG_REG         0x30A0
#define SIS3316_ADC_CH13_16_ACCUMULATOR_GATE1_CONFIG_REG        0x40A0

#define SIS3316_ADC_CH1_4_ACCUMULATOR_GATE2_CONFIG_REG          0x10A4
#define SIS3316_ADC_CH5_8_ACCUMULATOR_GATE2_CONFIG_REG          0x20A4
#define SIS3316_ADC_CH9_12_ACCUMULATOR_GATE2_CONFIG_REG         0x30A4
#define SIS3316_ADC_CH13_16_ACCUMULATOR_GATE2_CONFIG_REG        0x40A4

#define SIS3316_ADC_CH1_4_ACCUMULATOR_GATE3_CONFIG_REG          0x10A8
#define SIS3316_ADC_CH5_8_ACCUMULATOR_GATE3_CONFIG_REG          0x20A8
#define SIS3316_ADC_CH9_12_ACCUMULATOR_GATE3_CONFIG_REG         0x30A8
#define SIS3316_ADC_CH13_16_ACCUMULATOR_GATE3_CONFIG_REG        0x40A8

#define SIS3316_ADC_CH1_4_ACCUMULATOR_GATE4_CONFIG_REG          0x10AC
#define SIS3316_ADC_CH5_8_ACCUMULATOR_GATE4_CONFIG_REG          0x20AC
#define SIS3316_ADC_CH9_12_ACCUMULATOR_GATE4_CONFIG_REG         0x30AC
#define SIS3316_ADC_CH13_16_ACCUMULATOR_GATE4_CONFIG_REG        0x40AC
```

These registers define the length and the Start Index of the Accumulator Gates.

D31:25	D24:16	D15:0
0	Gate Length	Gate Start Index (Address)

Value of Gate Length register	Number of sample(s)
0	1
1	2
2	3
..	..
0x1FF	0x200 (512)

Si : Sum of (input sample stream)

$$\sum_{i=\text{start index}}^{\text{start index + length}} Si$$

4.4 TOF Window Configuration registers

```
#define SIS3316_ADC_CH1_4_TOF_WINDOW_CONFIG_REG            0x10C0
#define SIS3316_ADC_CH5_8_TOF_WINDOW_CONFIG_REG            0x20C0
#define SIS3316_ADC_CH9_12_TOF_WINDOW_CONFIG_REG           0x30C0
#define SIS3316_ADC_CH13_16_TOF_WINDOW_CONFIG_REG          0x40C0
```

These registers define the length of the TOF (time of flight) Window.

D31:0
TOF Window Length value

The power up default value is 0

Calculation of the TOF Window length:
TOF Window length = (TOF Window Length value + 1) * (sample clock period * 128)

Example with sample clock period = 4ns (250MHz):
sample clock period * 128 = 512 ns

For a desired TOF Window of 40ms:
→ preset the registers to 0x0001312C (40.000.000 ns / 512 ns = 78125 -> 0x1312D)

For a desired TOF Window of 1 sec:
→ preset the registers to 0x001DCD64 (1.000.000.000 ns / 512 ns = 1953125 -> 0x1DCD65)

For a desired TOF Window of 1000 sec:
→ preset the registers to 0x746A5287 (1.000.000.000.000 ns / 512 ns = 1953125000 -> 0x746A5288)

4.5 General Histogram Configuration registers

```
#define SIS3316_ADC_CH1_4_GENERAL_HISTOGRAM_CONFIG_REG          0x10CC
#define SIS3316_ADC_CH5_8_GENERAL_HISTOGRAM_CONFIG_REG          0x20CC
#define SIS3316_ADC_CH9_12_GENERAL_HISTOGRAM_CONFIG_REG         0x30CC
#define SIS3316_ADC_CH13_16_GENERAL_HISTOGRAM_CONFIG_REG        0x40CC
```

Bit	Function
31	reserved
..	..
8	reserved
7	reserved
6	histogramming “if TOF Window is active“ Enable bit
5	histogramming “if Over/Underflow“ Enable bit
4	histogramming “if Pileup/Repileup“ Enable bit
3	PSD Method select bit
2	Histogram clear Disable bit
1	Writing Hits/Events into Event Memory Disable bit
0	Histograming Enable bit

The power up default value reads 0x0

Bit6:
“if TOF Window is active” Enable bit = 0: increment histograms if logic is enabled
“if TOF Window is active” Enable bit = 1: increment histograms if logic is enabled and the TOF Window is active

Bit5:
“if Over/Underflow” Enable bit = 0: don’t increment histograms in case of Over/Underflow*
“if Over/Underflow” Enable bit = 1: increment histograms in case of Over/Underflow*
* ADC Over/Underflow input detection

Bit4:
“if Pileup/Repileup” Enable bit = 0:
don’t increment histograms in case of pileup/repileup
“if Pileup/Repileup” Enable bit = 1:
increment histograms in case of pileup/repileup

Bit3:
PSD Method select bit = 0:
Select PSD method 1

PSD Method select bit = 1:
Select PSD method 2

Bit2:
Histogram clear Disable bit = 0:
The Histograms are cleared with a Key-Histogram-clear command

Histogram clear Disable bit = 1:
The Histograms are not cleared with a Key-Histogram-clear command

Bit1:
Writing Hits/Events into Event Memory Disable bit = 0:
The Sample logic writes Hits/Events to the Event Memory Ch x and the Histogram logic increments the Histogram simultaneously, if the Sample logic is armed on Bank1 or Bank2 and if the Histogram logic is enabled.

Writing Hits/Events into Event Memory Disable bit = 1
Disables writing of Hits/Events to the Event Memory. The Hits/Events are histogrammed, only, if the Sample logic is armed on Bank1 or Bank2 and if the Histogram logic is enabled.

Bit0:
Histograming Enable bit = 0: the Histogram logic is disabled
Histograming Enable bit = 1: the Histogram logic is enabled

4.6 Shape 2-D Histogram X-axis Configuration registers

```
#define SIS3316_ADC_CH1_4_SHAPE_HISTOGRAM_X_CONFIG_REG          0x10D4
#define SIS3316_ADC_CH5_8_SHAPE_HISTOGRAM_X_CONFIG_REG          0x20D4
#define SIS3316_ADC_CH9_12_SHAPE_HISTOGRAM_X_CONFIG_REG         0x30D4
#define SIS3316_ADC_CH13_16_SHAPE_HISTOGRAM_X_CONFIG_REG        0x40D4
```

These read/write registers configure the scaling of the x-axis of the Shape histogram.

Bit	Function
31	reserved
..	..
24	reserved
23	Shape X-axis Offset bit 7
..	..
17	Shape X-axis Offset bit 1
16	Shape X-axis Offset bit 0
15	reserved
14	reserved
13	reserved
12	reserved
11	Shape X-axis Divider bit 11
..	..
1	Shape X-axis Divider bit 1
0	Shape X-axis Divider bit 0

The power up default value reads 0x0
Note: a Divider value of 0 will be set to 1 internally to prevent a division by 0.

4.6.1 Calculation of the “Peak Sum” to the Shape Histogram X-axis Histogram index (bin):

The Shape Histogram memory has a length of 512 x 512 bins (32-bit unsigned integer) and it is implemented in the Event Memory ADC channel x Bank1.

Shape Histogram1:
- Event Memory 1/2 Channel 1/3/5/../15 32-bit address offset = 0x00E00000 to 0x00E3FFFF
- Event Memory 1/2 Channel 2/4/6/../16 32-bit address offset = 0x02E00000 to 0x02E3FFFF

Shape Histogram2:
- Event Memory 1/2 Channel 1/3/5/../15 32-bit address offset = 0x00E40000 to 0x00E7FFFF
- Event Memory 1/2 Channel 2/4/6/../16 32-bit address offset = 0x02E40000 to 0x02E7FFFF

Shape Histogram X-axis Index (Peak-Sum) =
((Acc. 2 – Acc. 4) / x-axis-divider) + x-axis-offset

4.7 Shape 2-D Histogram Y-axis Configuration registers

```
#define SIS3316_ADC_CH1_4_SHAPE_HISTOGRAM_Y_CONFIG_REG          0x10D8
#define SIS3316_ADC_CH5_8_SHAPE_HISTOGRAM_Y_CONFIG_REG          0x20D8
#define SIS3316_ADC_CH9_12_SHAPE_HISTOGRAM_Y_CONFIG_REG         0x30D8
#define SIS3316_ADC_CH13_16_SHAPE_HISTOGRAM_Y_CONFIG_REG        0x40D8
```

These read/write registers configure the scaling of the y-axis of the Shape histogram.

Bit	Function
31	reserved
..	..
24	reserved
23	Shape Y-axis Offset bit 7
..	..
17	Shape Y-axis Offset bit 1
16	Shape Y-axis Offset bit 0
11	Shape Y-axis Divider bit 15
..	..
1	Shape Y-axis Divider bit 1
0	Shape Y-axis Divider bit 0

The power up default value reads 0x0

Note: a Divider value of 0 will be set to 1 internally to prevent a division by 0.

4.7.1 Calculation of the “PSD value” to the Shape Histogram Y-axis Histogram index (bin):

Method 1:
Shape Histogram Y-axis Index (PSD) =
(((Acc. 3 – Acc. 1) * 0x10000) / (Acc. 2 – Acc. 4)) / y-axis-divider) + y-axis-offset

Method 2:
Shape Histogram Y-axis Index (PSD) =
((Acc. 3 – Acc. 1) / y-axis-divider) + y-axis-offset

4.8 Peak Sum Histogram Configuration registers

```
#define SIS3316_ADC_CH1_4_PEAK_SUM_HISTOGRAM_CONFIG_REG          0x10DC
#define SIS3316_ADC_CH5_8_PEAK_SUM_HISTOGRAM_CONFIG_REG          0x20DC
#define SIS3316_ADC_CH9_12_PEAK_SUM_HISTOGRAM_CONFIG_REG         0x30DC
#define SIS3316_ADC_CH13_16_PEAK_SUM_HISTOGRAM_CONFIG_REG        0x40DC
```

These read/write registers configure the scaling of the x-axis of the Peak Sum histogram.

Bit	Function
31	reserved
..	..
..	..
24	reserved
23	Peak Sum X -axis Offset bit 7
..	..
17	Peak Sum X -axis Offset bit 1
16	Peak Sum X -axis Offset bit 0
15	reserved
14	reserved
13	reserved
12	reserved
11	Peak Sum X-axis Divider bit 11
..	..
..	..
1	Peak Sum X-axis Divider bit 1
0	Peak Sum X-axis Divider bit 0

The power up default value reads 0x0

The “calculated Peak Sum“ bin of each Hit/Event will be histogramed in the Peak Sum histogram space of the Event Memory Ch x if the Sample logic is armed on Bank1 or Bank2.

4.8.1 Calculation of the “Peak Sum” value to the Peak Sum (bin) Histogram Index:

The Peak-Height/Charge Histogram memory has a length of 1 K (reserved 64K) bins (32-bit unsigned integer) and it is implemented in the Event Memory ADC channel x Bank1.

Peak-Height/Charge Histogram1:
- Event Memory 1/2 Channel 1/3/5/../15 32-bit address offset = 0x00F00000 to 0x00F003FF
- Event Memory 1/2 Channel 2/4/6/../16 32-bit address offset = 0x02F10000 to 0x02F103FF

Peak-Height/Charge Histogram2:
- Event Memory 1/2 Channel 1/3/5/../15 32-bit address offset = 0x00F00000 to 0x00F003FF
- Event Memory 1/2 Channel 2/4/6/../16 32-bit address offset = 0x02F10000 to 0x02F103FF

Peak-Sum Histogram X-axis Index (Peak-Sum) =
((Acc. 2 – Acc. 4) / x-axis-divider) + x-axis-offset

4.9 TOF Histogram Configuration registers

```
#define SIS3316_ADC_CH1_4_TOF_HISTOGRAM_CONFIG_REG              0x10D0
#define SIS3316_ADC_CH5_8_TOF_HISTOGRAM_CONFIG_REG              0x20D0
#define SIS3316_ADC_CH9_12_TOF_HISTOGRAM_CONFIG_REG             0x30D0
#define SIS3316_ADC_CH13_16_TOF_HISTOGRAM_CONFIG_REG            0x40D0
```

These read/write registers configure the scaling of the x-axis of the TOF (time of flight) histogram.

Bit	Function
31	reserved
..	..
24	reserved
23	Divider bit 23
..	..
1	Divider bit 1
0	Divider bit 0

The power up default value reads 0x0
Note: a Divider value of 0 will be set to 1 internally to prevent a division by 0.

4.9.1 Calculation of the “Time” to the TOF Histogram (bin) Index:

Each TOF Histogram memory has a length of 1M bins (32-bit unsigned integer).

TOF Histogram1 (Gamma):
- Event Memory 1/2 Channel 1/3/5/../15 32-bit address offset = 0x00C00000 to 0x00CFFFFF
- Event Memory 1/2 Channel 2/4/6/../16 32-bit address offset = 0x02C00000 to 0x02CFFFFF

TOF Histogram2 (Neutron):
- Event Memory 1/2 Channel 1/3/5/../15 32-bit address offset = 0x00D00000 to 0x00DFFFFF
- Event Memory 1/2 Channel 2/4/6/../16 32-bit address offset = 0x02D00000 to 0x02DFFFFF

TOF Histogram Index = (40-bit Timestamp / TOF Histogram Divider)

The minimal bin width is 4ns by 250MHz.

divider value	bin width	size of histogram (bin width * 1 048 576)
0	4 ns	4,194304 ms
1	4 ns	4,194304 ms
250	1 us	1,048576 sec
250 000 (0x61A8)	1 ms	1048,576 sec
2 500 000 (0x2625A0)	10 ms	10 048,576 sec
..	..	..
10485755 (0xffffff)	41,94302ms	~43 980 sec (appr. 12 hours)

4.10 ADC FPGA Firmware Version Register

```
#define SIS3316_ADC_CH1_4_FIRMWARE_REG              0x1100 /* rd only */
#define SIS3316_ADC_CH5_8_FIRMWARE_REG              0x2100 /* rd only */
#define SIS3316_ADC_CH9_12_FIRMWARE_REG             0x3100 /* rd only */
#define SIS3316_ADC_CH13_16_FIRMWARE_REG            0x4100 /* rd only */
```

This register reflects the ADC FPGA Firmware Version and Revision number.
The Version level will be used to distinguish between substantial design differences and experiment specific designs, while the Revision level will be used to mark user specific adaptations.

Bits	31 - 16	15 - 8	7 - 0
	Firmware Type	Firmware Version	Firmware Revision

Example:

Firmware Type	= 0x0250 :	250 MHz ADC
Firmware Version	= 0x02:	Neutron/Gamma PSD
Firmware Revision	= 0x01:	1. official Revision from 15.10.2015

4.1 ADC FPGA Status register

```
#define SIS3316_ADC_CH1_4_STATUS_REG            0x1104 /* rd only */
#define SIS3316_ADC_CH5_8_STATUS_REG            0x2104 /* rd only */
#define SIS3316_ADC_CH9_12_STATUS_REG           0x3104 /* rd only */
#define SIS3316_ADC_CH13_16_STATUS_REG          0x4104 /* rd only */
```

This register holds the ADC FPGA Status of the Data Link between the ADC FPGA and the VME FPGA , the Status of the both Memory Controller and the Status of the ADC-Clock DCM.

Bit	Read
31	0
…	0…
24	Histogram Clear logic Busy
23	0
22	0
21	ADC-Clock DCM RESET flag
20	ADC-Clock DCM OK flag
19	0
18	0
17	Memory 2 OK flag (ch3 and ch4)
16	Memory 1 OK flag (ch1 and ch2)
15	0
14	0
13	0
12	0
11	0
10	0
9	0
8	Data Link Speed flag
7	VME FPGA : Frame_error_latch
6	VME FPGA : Soft_error_latch
5	VME FPGA : Hard_error_latch
4	VME FPGA : Lane_up_flag
3	VME FPGA : Channel_up_flag
2	VME FPGA : Frame_error_flag
1	VME FPGA : Soft_error_flag
0	VME FPGA : Hard_error_flag

The latched error bits may be set after power up. After a write with 0x400 (i.e. setting bit 10) to the corresponding ADC Input tap delay register the contents should read 0x30018.

Note: The “Histogram Clear logic Busy” flag is ored to the “ADC FPGA n Busy” flags in the “ADC FPGA SPI BUSY Status” register, also.

4.2 Key addresses (0x400 – 0x43C write only)

Write access (with Broadcast functionality) to a key address (KA) with arbitrary data invokes a respective action.

4.2.1 Key address: Histograms Clear

```
#define SIS3316_KEY_HISTOGRAMS_CLEAR          0x404   /* write only; D32
*/
```

A write with arbitrary data to this register (key address) clears the Histograms except the "PSD lookup table" Histogram.
This clear process takes appr. 35 ms.

4.3 Software

A ready to run example ROOT GUI (Graphical User Interface) comes with the SIS3316.
The CERN ROOT home page can be found at http://root.cern.ch
At this point in time code for the VC++10 Windows version is distributed with the product DVD.

4.3.1 Firmware Upgrade over VME

One section of the –to be expanded- SIS3316-M-Software-root-gui-1-Vxxx.doc software manual describes the firmware upgrade procedure.

4.3.2 Ethernet operation

Ethernet based operation of the SIS3316 is described in the Ethernet addendum to this manual. The SIS3316_test_gui_ethernet program is available as executable for Windows and in source code.

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