SIS3316
Global Clock Distribution
Addendum

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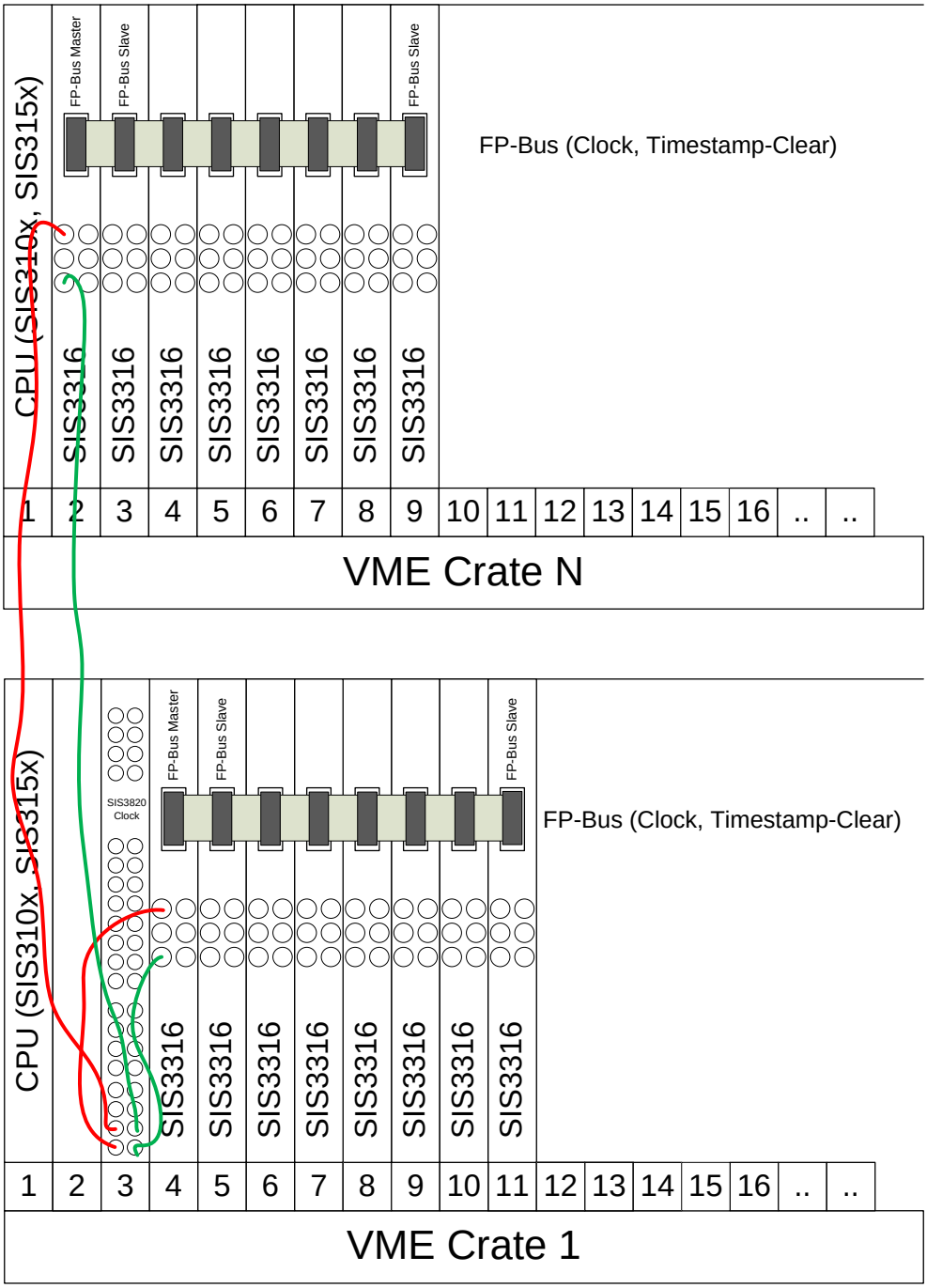
Revision Table:

Revision	Date	Modification
1.00	10.02.2017	First release

1 Table of contents

2 Introduction

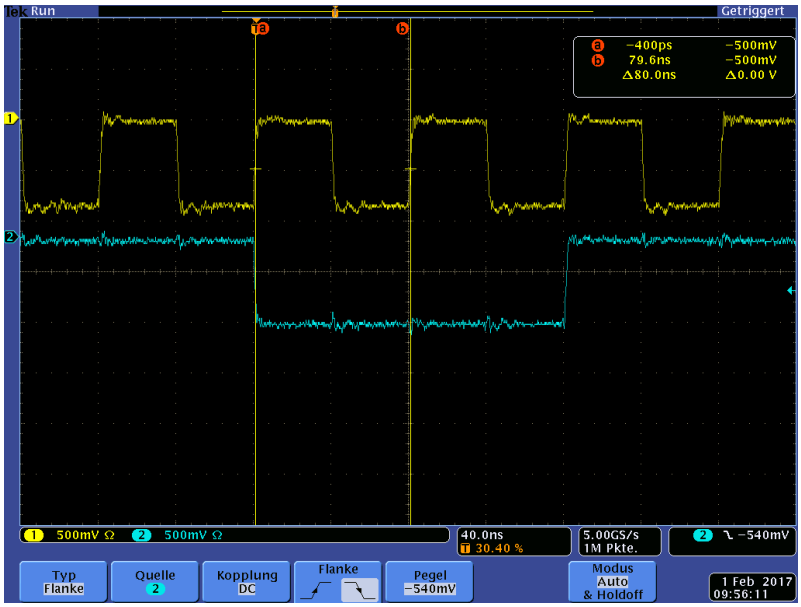
The front panel LVDS Bus (FP-Bus) can be used for synchronized operation of multiple SIS3316s in a single VME Crate.
For synchronized operation of multiple SIS3316s in multiple VME Crates a combination of using the FP-Bus (local Crate distribution) and a SIS3820-Clock distribution module can be used.



Red LEMO cable: 12.5 MHz global Clock, the length of all cables **should** be equal !
Green LEMO cable: Timestamp-Clear pulse, the length of all cables **must** be equal !

3 Global Clock and Timestamp-Clear distribution

The SIS3820-Clock provides after configuration 16 clock outputs (left side column) and two groups of 8 strobe outputs (right side column). The lower 8 strobe outputs are used as Timestamp-Clear.



Ch1 (yellow): 12.5 MHz measured at Data Output 1 (3, 5, .., 31 are identical) of the SIS3820
Ch2 (blue): Strobe 1 pulse with a width of 2 Clock cycles measured at Data Output 2 (4, 6, ..,16 are identical)

The frequency of the Global Clock is configured with 12.5 MHz, which can be distributed over a long distance via a LEMO cable (NIM signal). It was tested with a length of 20 meter.

The “SIS3316 FP-Bus Master” multiplies the 12.5 MHz global clock to 250MHz (or 125MHz) and distributes it to the FB-Bus (LVDS) which will be used as sample clock on all modules in the Crate.
The “SIS3316 FP-Bus Master” distributes the Timestamp-Clear pulse over the FP-Bus to all modules, also.

4 SIS3316 Sample clock and synchronized Timestamp-Clear pulse

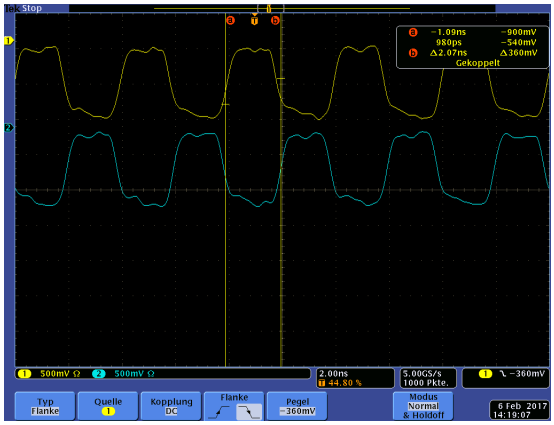
The “SIS3316 FP-Bus Master” multiplies the Global Clock 12.5 MHz to the Sample Clock of 250MHz (125MHz). The multiplied Sample Clock can be monitored at the NIM output CO (if it is selected).

Ch1 (yellow): 250 MHz measured at CO of the “SIS3316 FP-Bus Master” in Crate 1
Ch2 (blue): 250 MHz measured at CO of the “SIS3316 FP-Bus Master” in Crate 2

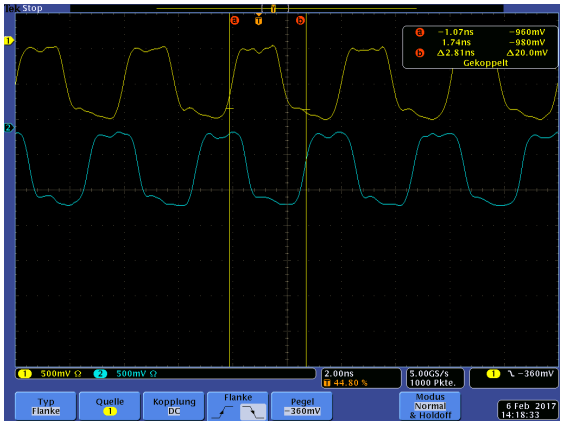
Four different correlations between the Sample Clocks of “SIS3316 FP-Bus Master” in Crate 1 and “SIS3316 FP-Bus Master” in Crate 2 are possible (depends on the Multiplier IC):

0 ns delay between Sample Clock 1 and 2

1 ns delay between Sample Clock 1 and 2



2 ns delay between Sample Clock 1 and 2

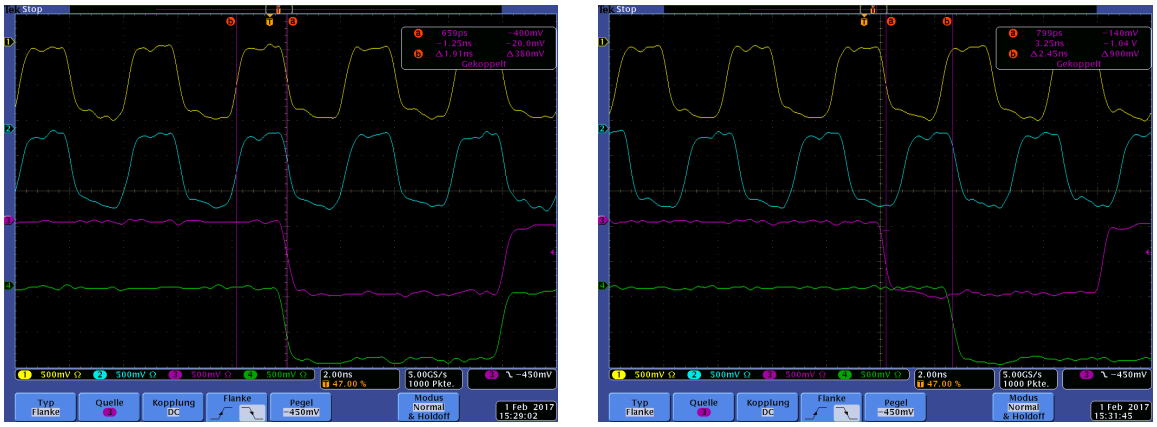


3 ns delay between Sample Clock 1 and 2

Note: After the clocks are configured the “delay” will be constant.
A new clock configuration can change the “delay”.

The internal Timestamp-Clear pulse, which is synchronized with the Sample Clock, can be monitored at the NIM output UO (if it is selected).

We can observe that the synchronized internal Timestamp-Clear pulses are not always synchronous between the “SIS3316 FP-Bus Master” in Crate 1 and Crate 2 (and Crate N):



Ch1 (yellow): 250 MHz measured at CO of the “SIS3316 FP-Bus Master” in Crate 1
Ch2 (blue): 250 MHz measured at CO of the “SIS3316 FP-Bus Master” in Crate 2
Ch3 (magenta): Timestamp-Clear measured at UO of the “SIS3316 FP-Bus Master” in Crate 1
Ch4 (green): Timestamp-Clear measured at UO of the “SIS3316 FP-Bus Master” in Crate 2

Both SIS3316s receive the Timestamp-Clear signal at exact the same moment (same length of Timestamp-Clear cable) but the internal synchronization with the internal Sample Clocks will/can generate a “delay” between the both outputs UO. The left scope picture shows a delay of ~0 ns and the right scope picture shows a delay of ~2.4 ns.

Note: After the sample clocks are configured the “delay” will be constant.
A new clock configuration can change the “delay”.

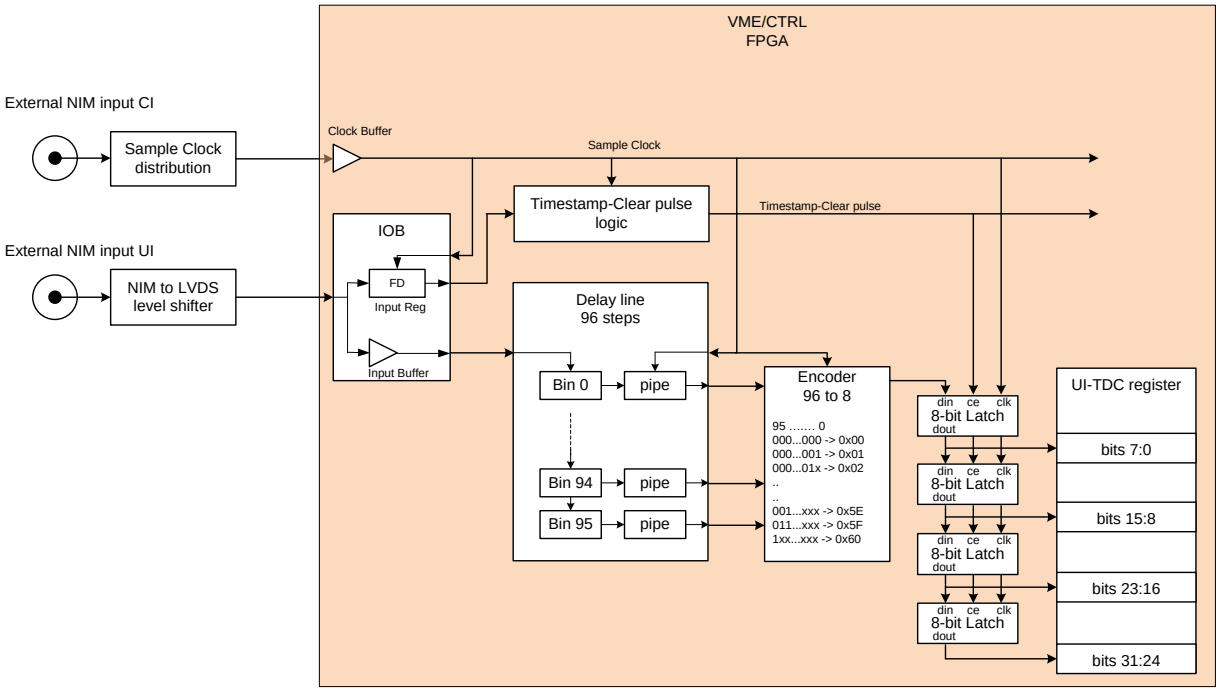
The “delay” between these both output signals (UI) corresponds to the delay between the Timestamp-Clear commands and/or the Timestamp-Counters of the both modules (crate 1 and crate 2).

With other words it describes a time displacement between the Timestamps (Timestamp-Counter values) of the modules in different crates.

To determine this “delay” (time displacement) a TDC-logic for the UI input path is implemented in the SIS3316 Firmware. This TDC-logic calculates the delay of the UI input signal to an internal synchronized signal UI with the sample clock. The relative resolution is appr. +/- 80 ps.

5 SIS3316 UI-TDC logic

A new “UI-TDC” logic is implemented in the SIS3316 with the VME FPGA Firmware “sis3316vme_top_V-200D”. With this “UI-TDC” logic it is possible to measure the delay of the “real” external Timestamp-Clear signal to the internal Timestamp-Clear pulse, which is synchronized with the sample clock.



Each delay step of the Delay line represents appr. 80ps. This is a typically value, only, and it could be vary from module to module. It depends on temperature, also.

Please have a look to the UI-TDC measurement examples.

```
#define SIS3316_UI_TDC_REG          0xB4       /* read  D32 */
```

Bits	31 - 24	23 - 16	15 - 8	7 - 0
Function	TDC delay value Latch-Pipeline 4	TDC delay value Latch-Pipeline 3	TDC delay value Latch-Pipeline 2	TDC delay value Latch-Pipeline 1
Time offset	3 x sample periode	2 x sample periode	1 x sample periode	0 ns

Valid TDC delay values are 0x0 to 0x60.
0x0 represents that no bins in the delay line are set.
0x10 represents that bin 0 to 15 are 1 and the following bins are 0.
0x60 represents that all bins in the delay line are set.

The Latch-Pipelines have a time offset of the sample period.

Note: once-only latched values have an inaccuracy of +/- 1 !

Example with a sample clock of 250MHz (4ns): register value = 0 x 00 11 46 60

Simple delay calculation (assume that Pipeline 4 is 0x00 and Pipeline 1 is 0x60):

```
unsigned int latch_Pipeline[4];
unsigned int tdc_ui_time_ps;

tdc_ui_time_ps =  ((tdc_ui_register_val & 0x00ff0000) >> 16) * 80 ;
if (tdc_ui_time_ps != 0) {
       tdc_ui_time_ps =  tdc_ui_time_ps + 8000 ; // 250 MHz
}
else {
       tdc_ui_time_ps =  (((tdc_ui_register_val & 0x0000ff00) >> 8) * 80) + 4000   ;
}
```

Example:

```
tdc_ui_time_ps  = (17 * 80ps) + 8000ps =  9260 ps ;
```

"Calibrated" delay calculation

```
unsigned int latch_Pipeline[4];
unsigned int n;
unsigned int n;
float sample_periode_ps ;
float delay_step_ps ;
float delay_ps ;
sample_periode_ps = 4000.0 ;
n = 4 ;
for (i=0; i<3; i++) {
   if (latch_Pipeline[n] == 0) {
       n=n-1;
   }
   else {  // found first value != 0
       delay_step_ps = sample_periode_ps / (float(latch_Pipeline[n-1] - latch_Pipeline[n]) ) ;
       delay_ps = ((n-1) * sample_periode_ps) + (latch_Pipeline[n] * delay_step_ps ) ;
       break ;
   }
}
```

Example:

```
delay_step_ps = 4000 / (0x46 - 0x11 ) = 4000 / (70-17) =  appr. 75.5 ps
delay_ps = (2 * 4000) + (17 * 75.5) =  9283 ps ;
```

6 UI-TDC measurement Examples

The Clock and Timestamp-Clear distribution is shown in chapter “Introduction”. Clock and Timestamp-Clear cables are 20m long. External Trigger pulses and “Signal” pulses at channel 1 are provided to both “SIS3316 FP-Bus Master” modules in Crate 1 and 2. These signals are generated with the SIS3820-Clock at the 8 “Strobe 2” outputs. These pulses are synchronous.

The delay calculation of the program based on the “Simple Delay calculation” with an offset difference of one sample clock period (4000ps). The example program generates only one time the Timestamp-Clear pulse and takes the UI-TDC value. For a real “module specified calibration” it is reasonable to build a histogram of the delay (generate N Timestamp-Clear pulse).
After Clock configuration (only one time) the program generates a Timestamp-Clear pulse (Strobe 1) and it takes 100 events by generating 100 “Strobe 2” pulses (External Triggers and Signals at channel 1) in a loop.
The Graph shows the 100 signals of channel 1 of SIS3316 in Crate 1 (red) and the 100 signals of channel 1 of SIS3316 in Crate 2 (green).
This (Timestamp-Clear, take 100 Events) runs in an endless loop.

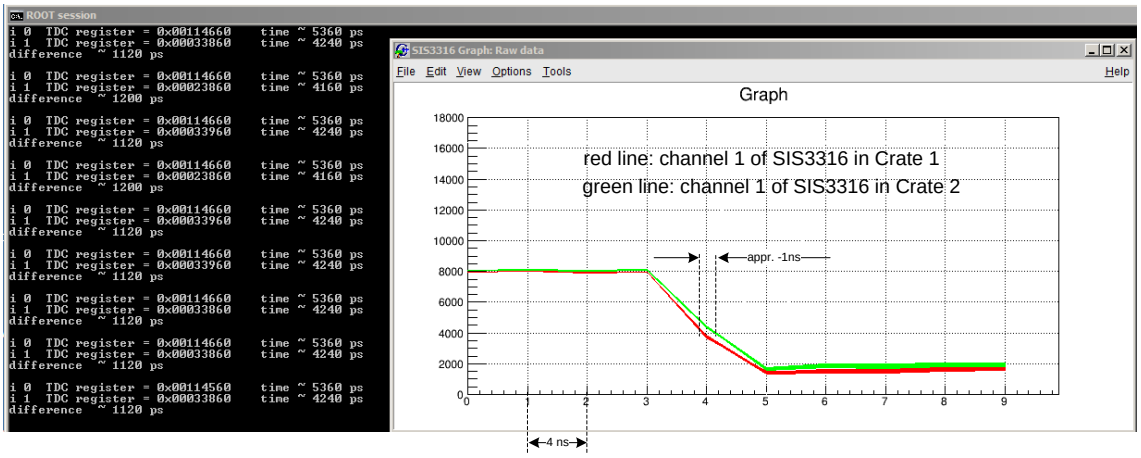
6.1 UI-TDC measurement Example 1

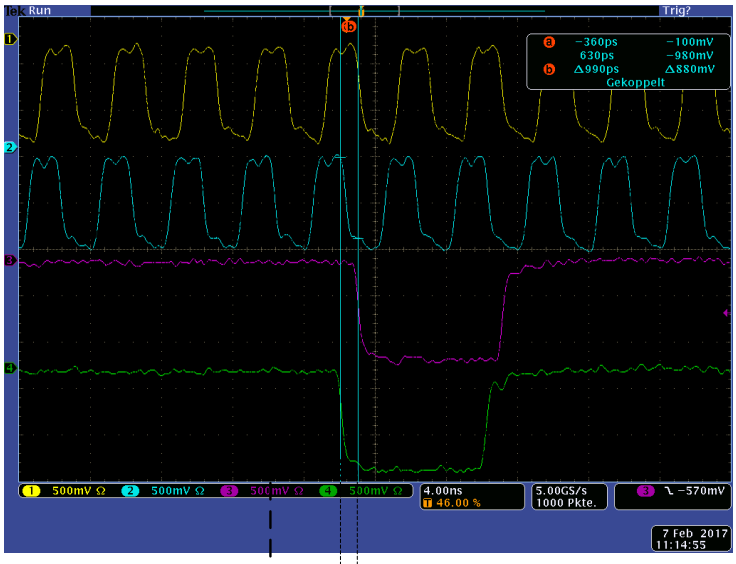
The program calculates the difference of both UI-TDC delay values. The printed value represents not an exact delay in ps:

1. it is calculated with the "Simple calculation"
2. measured only one time
3. module specified delays (ICs)

So, a printed difference of +1120ps have to interpreted as +960ps to +1280ps (+/-2 bins).

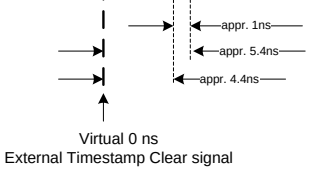
A positive difference means that the SIS3316 in Crate 1 generates the internal Timestamp-Clear pulse later than the SIS3316 in Crate 2. This shows the scope picture, also. The delay from the green pulse to the magenta pulse is appr. 1ns.
The consequence of a positive difference is that the red sampled traces (100 traces) of SIS3316 in Crate 1 are plotted appr. 1 ns earlier than the traces (green) of SIS3316 in Crate 2.





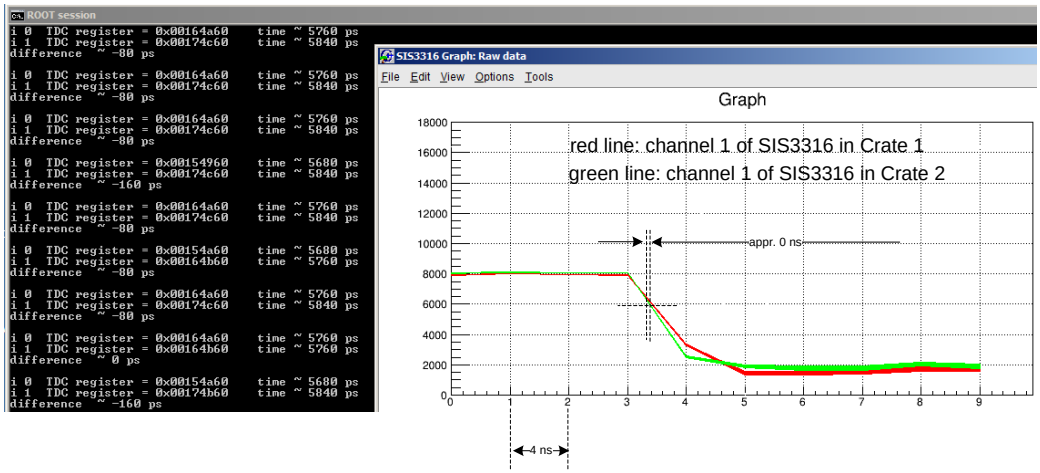
Ch3 (magenta):
Timestamp-Clear measured at UO of the "SIS3316 FP-Bus Master" in Crate 1

Ch4 (green):
Timestamp-Clear measured at UO of the "SIS3316 FP-Bus Master" in Crate 2



6.2 UI-TDC measurement Example 2

A printed difference of -80ps have to interpreted as -240ps to +80ps (+/-2 bins).

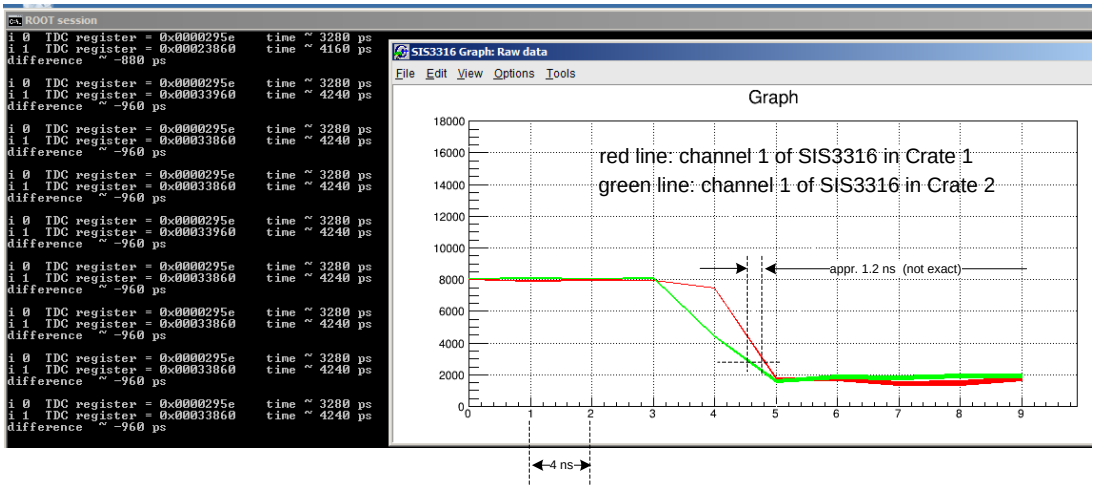


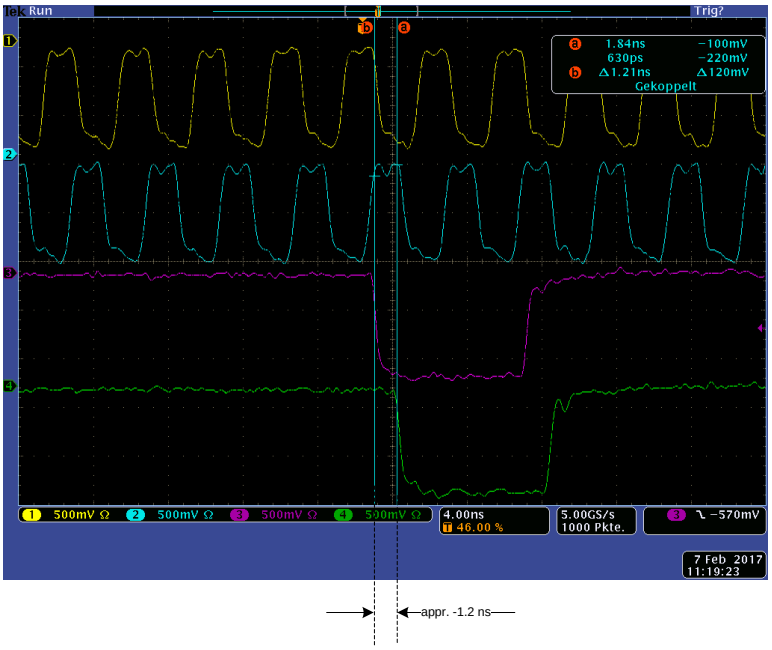
Ch3 (magenta):
Timestamp-Clear measured at UO of the "SIS3316 FP-Bus Master" in Crate 1

Ch4 (green):
Timestamp-Clear measured at UO of the "SIS3316 FP-Bus Master" in Crate 2

6.3 UI-TDC measurement Example 3

A printed difference of -960ps have to interpreted as -800ps to -1120ps (+/-2 bins).



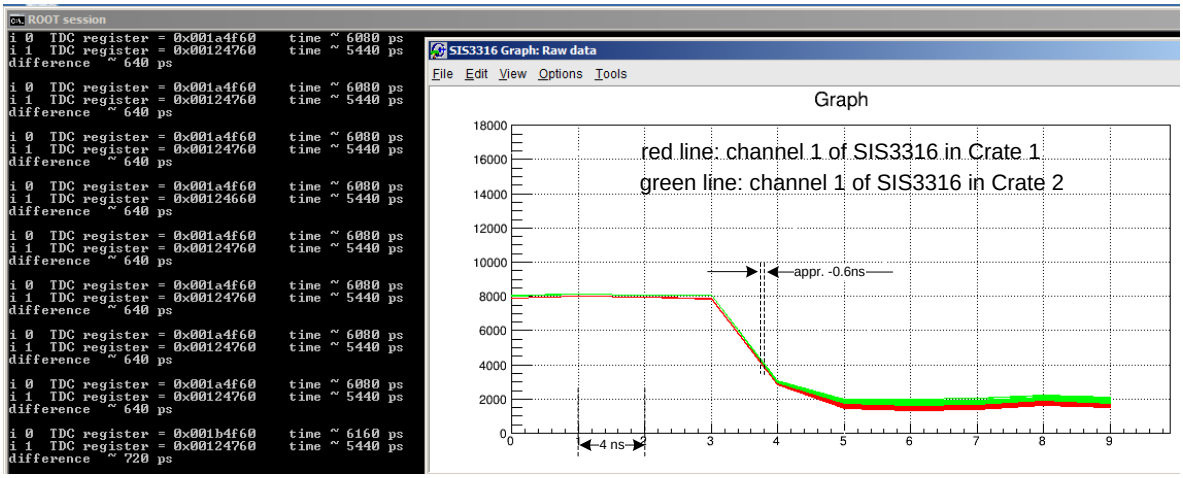


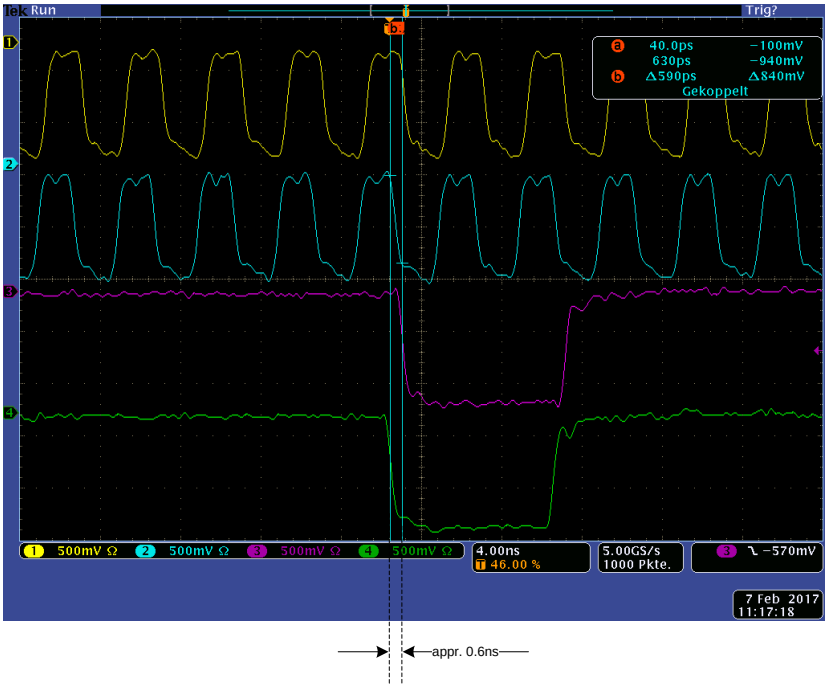
Ch3 (magenta):
Timestamp-Clear measured at UO of the "SIS3316 FP-Bus Master" in Crate 1

Ch4 (green):
Timestamp-Clear measured at UO of the "SIS3316 FP-Bus Master" in Crate 2

6.4 UI-TDC measurement Example 4

A printed difference of +640ps have to interpreted as +480ps to +800ps (+/-2 bins).



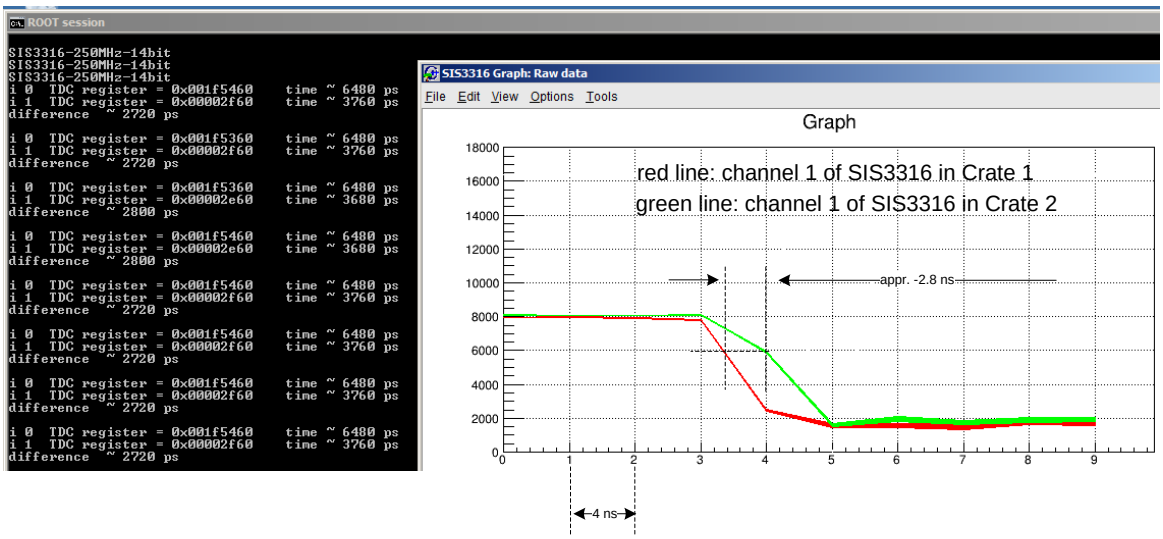


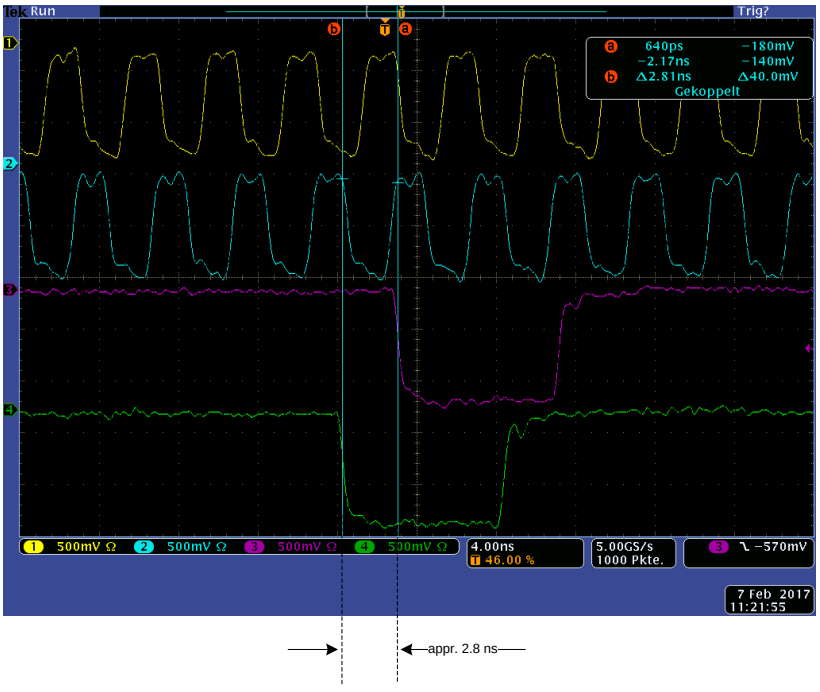
Ch3 (magenta):
Timestamp-Clear measured at UO of the "SIS3316 FP-Bus Master" in Crate 1

Ch4 (green):
Timestamp-Clear measured at UO of the "SIS3316 FP-Bus Master" in Crate 2

6.5 UI-TDC measurement Example 5

A printed difference of +2720ps have to interpreted as +2560ps to +2880ps (+/-2 bins).





Ch3 (magenta):
Timestamp-Clear measured at UO of the "SIS3316 FP-Bus Master" in Crate 1

Ch4 (green):
Timestamp-Clear measured at UO of the "SIS3316 FP-Bus Master" in Crate 2