DESCRIPTION

The Hynix HY57V653220B is a 67,108,864-bit CMOS Synchronous DRAM, ideally suited for the memory applications which require wide data I/O and high bandwidth. HY57V653220B is organized as 4banks of 524,288x32.

HY57V653220B is offering fully synchronous operation referenced to a positive edge of the clock. All inputs and outputs are synchronized with the rising edge of the clock input. The data paths are internally pipelined to achieve very high bandwidth. All input and output voltage levels are compatible with LVTTL.

Programmable options include the length of pipeline (Read latency of 2 or 3), the number of consecutive read or write cycles initiated by a single control command (Burst length of 1,2,4,8 or full page), and the burst count sequence(sequential or interleave). A burst of read or write cycles in progress can be terminated by a burst terminate command or can be interrupted and replaced by a new burst read or write command on any cycle. (This pipelined design is not restricted by a `2N` rule.)

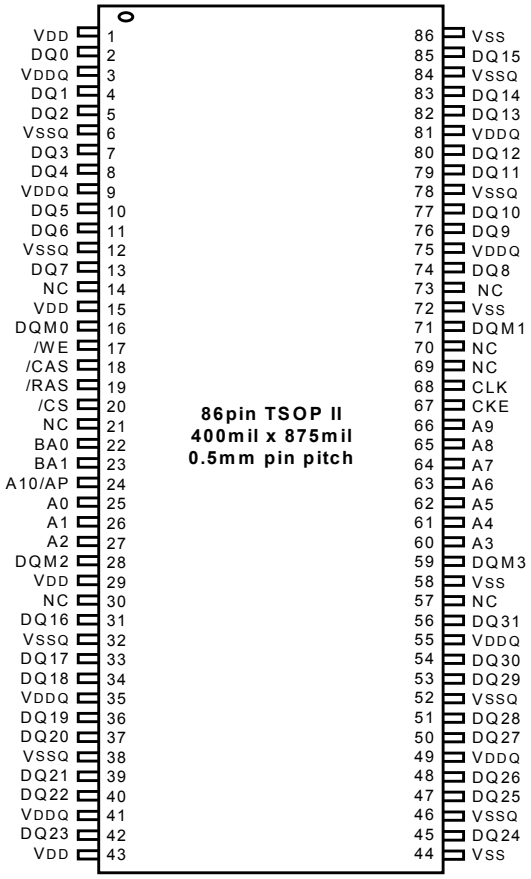
FEATURES

- JEDEC standard 3.3V power supply
- All device pins are compatible with LVTTL interface
- JEDEC standard 400mil 86pin TSOP-II with 0.5mm of pin pitch
- All inputs and outputs referenced to positive edge of system clock
- Data mask function by DQM0,1,2 and 3
- Internal four banks operation
- Auto refresh and self refresh
- 4096 refresh cycles / 64ms
- Programmable Burst Length and Burst Type
  - 1, 2, 4, 8 or full page for Sequential Burst
  - 1, 2, 4 or 8 for Interleave Burst
- Programmable $\overline{CAS}$ Latency ; 2, 3 Clocks
- Burst Read Single Write operation

ORDERING INFORMATION

Part No.	Clock Frequency	Power	Organization	Interface	Package
HY57V653220BTC-5	200MHz	Normal	4Banks x 512Kbits x32	LVTTL	400mil 86pin TSOP II
HY57V653220BTC-55	183MHz				
HY57V653220BTC-6	166MHz				
HY57V653220BTC-7	143MHz				
HY57V653220BTC-8	125MHz				
HY57V653220BTC-10P	100MHz				
HY57V653220BTC-10	100MHz				

PIN CONFIGURATION

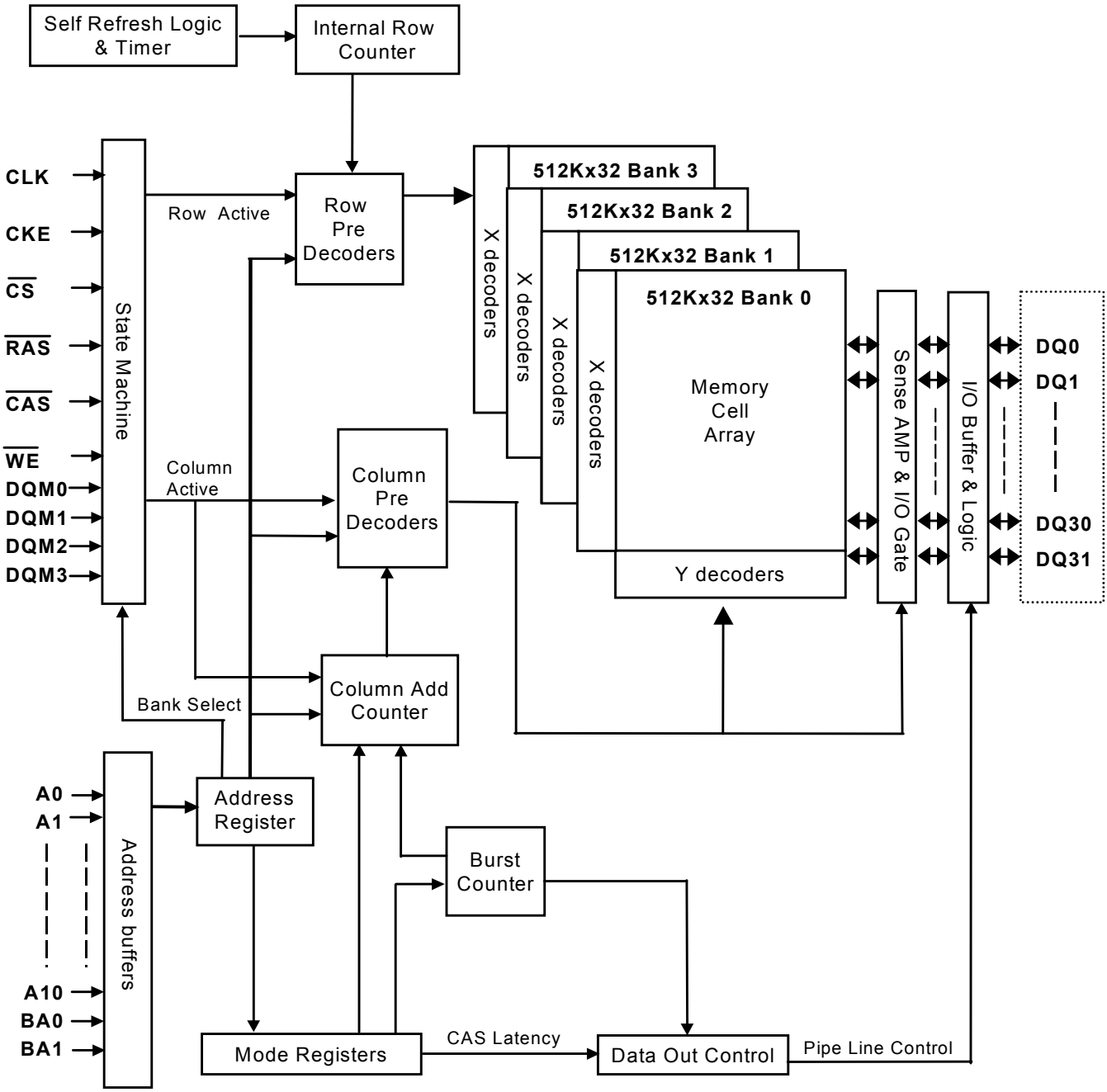


PIN DESCRIPTION

PIN	PIN NAME	DESCRIPTION
CLK	Clock	The system clock input. All other inputs are registered to the SDRAM on the rising edge of CLK.
CKE	Clock Enable	Controls internal clock signal and when deactivated, the SDRAM will be one of the states among power down, suspend or self refresh
$\overline{CS}$	Chip Select	Enables or disables all inputs except CLK, CKE and DQM
BA0, BA1	Bank Address	Selects bank to be activated during $\overline{RAS}$ activity Selects bank to be read/written during $\overline{CAS}$ activity
A0 ~ A10	Address	Row Address : RA0 ~ RA10, Column Address : CA0 ~ CA7 Auto-precharge flag : A10
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Row Address Strobe, Column Address Strobe, Write Enable	$\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ define the operation Refer function truth table for details
DQM0~3	Data Input/Output Mask	Controls output buffers in read mode and masks input data in write mode
DQ0 ~ DQ31	Data Input/Output	Multiplexed data input / output pin
VDD/VSS	Power Supply/Ground	Power supply for internal circuits and input buffers
VDDQ/VSSQ	Data Output Power/Ground	Power supply for output buffers
NC	No Connection	No connection

FUNCTIONAL BLOCK DIAGRAM

512Kbit x 4banks x 32 I/O Synchronous DRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Ambient Temperature	TA	0 ~ 70	°C
Storage Temperature	TSTG	-55 ~ 125	°C
Voltage on Any Pin relative to VSS	VIN, VOUT	-1.0 ~ 4.6	V
Voltage on VDD relative to VSS	VDD, VDDQ	-1.0 ~ 4.6	V
Short Circuit Output Current	IOS	50	mA
Power Dissipation	PD	1	W
Soldering Temperature · Time	TSOLDER	260 · 10	°C · Sec

Note : Operation at above absolute maximum rating can adversely affect device reliability

DC OPERATING CONDITION (TA=0 to 70°C)

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Power Supply Voltage	VDD, VDDQ	3.0	3.3	3.6	V	1,2
Input high voltage	VIH	2.0	3.0	VDDQ + 0.3	V	1,3
Input low voltage	VIL	VSSQ - 0.3	0	0.8	V	1,4

Note :
1.All voltages are referenced to VSS = 0V
2.VDD/VDDQ(min) is 3.15V for HY57V653220BTC-5/55/6
3.VIH (max) is acceptable 5.6V AC pulse width with ≤3ns of duration with no input clamp diodes
4.VIL (min) is acceptable -2.0V AC pulse width with ≤3ns of duration with no input clamp diodes

AC OPERATING CONDITION (TA=0 to 70°C, 3.0V ≤VDD ≤3.6V, VSS=0V - Note1)

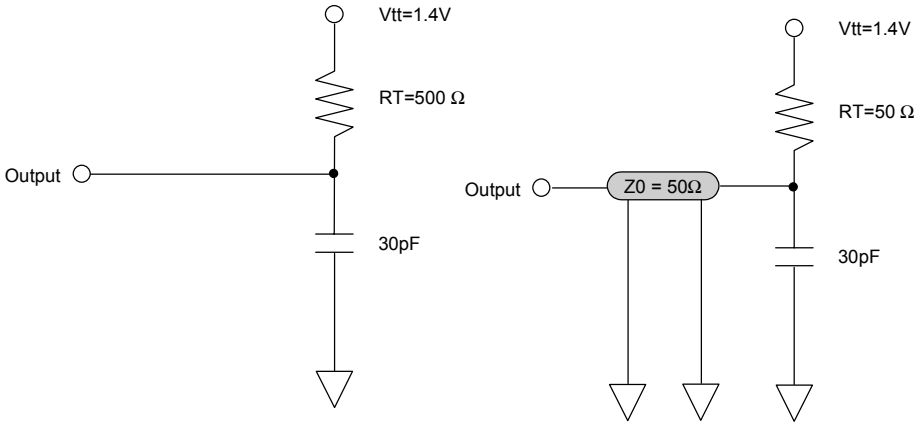
Parameter	Symbol	Value	Unit	Note
AC input high / low level voltage	VIH / VIL	2.4/0.4	V	
Input timing measurement reference level voltage	Vtrip	1.4	V	
Input rise / fall time	tR / tF	1	ns	
Output timing measurement reference level	Voutref	1.4	V	
Output load capacitance for access time measurement	CL	30	pF	2

Note :
1.3.15V ≤VDD ≤3.6V is applied for HY57V653220BC-5/55/6
2.Output load to measure access times is equivalent to two TTL gates and one capacitor (30pF)
For details, refer to AC/DC output load circuit

CAPACITANCE (TA=25°C, f=1MHz, VDD=3.3V)

Parameter	Pin	Symbol	Min	Max	Unit
Input capacitance	CLK	C_{I1}	2.5	4	pF
	A0 ~ A10, BA0, BA1, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM0~3	C_{I2}	2.5	5	pF
Data input / output capacitance	DQ0 ~ DQ31	$C_{I/O}$	4	6.5	pF

OUTPUT LOAD CIRCUIT



DC Output Load Circuit AC Output Load Circuit

DC CHARACTERISTICS I (DC operating conditions unless otherwise noted)

Parameter	Symbol	Min.	Max	Unit	Note
Input leakage current	I_{LI}	-1	1	uA	1
Output leakage current	I_{LO}	-1.5	1.5	uA	2
Output high voltage	V_{OH}	2.4	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	0.4	V	I_{OL} = +2mA

Note :
1.V_{IN} = 0 to 3.6V, All other pins are not under test = 0V
2.D_{OUT} is disabled, V_{OUT}=0 to 3.6V

DC CHARACTERISTICS II (DC operating conditions unless otherwise noted)

Parameter	Symbol	Test Condition		Speed							Unit	Note
				-5	-55	-6	-7	-8	-10P	-10		
Operating Current	IDD1	Burst Length=1, One bank active tRAS ≥ tRAS(min), tRP ≥ tRP(min), IOL=0mA		200	190	180	170	150	150	150	mA	1
Precharge Standby Current in power down mode	IDD2P	CKE ≤ VIL(max), tCK = 15ns		2							mA	
	IDD2PS	CKE ≤ VIL(max), tCK = ∞		2								
Precharge Standby Current in non power down mode	IDD2N	CKE ≥ VIH(min), $\overline{CS}$ ≥ VIH(min), tCK = 15ns Input signals are changed one time during 2clks. All other pins ≥ VDD-0.2V or ≤ 0.2V		15							mA	
	IDD2NS	CKE ≥ VIH(min), tCK = ∞ Input signals are stable.		10								
Active Standby Current in power down mode	IDD3P	CKE ≤ VIL(max), tCK = 15ns		3							mA	
	IDD3PS	CKE ≤ VIL(max), tCK = ∞		3								
Active Standby Current in non power down mode	IDD3N	CKE ≥ VIH(min), $\overline{CS}$ ≥ VIH(min), tCK = 15ns Input signals are changed one time during 2clks. All other pins ≥ VDD-0.2V or ≤ 0.2V		40							mA	
	IDD3NS	CKE ≥ VIH(min), tCK = ∞ Input signals are stable		25								
Burst Mode Operating Current	IDD4	tCK ≥ tCK(min), tRAS ≥ tRAS(min), IOL=0mA All banks active	CL=3	280	260	240	210	180	180	160	mA	1
			CL=2	160	160	160	160	160	160	140		
Auto Refresh Current	IDD5	tRRC ≥ tRRC(min), All banks active		250	235	220	210	190	190	190	mA	2
Self Refresh Current	IDD6	CKE ≤ 0.2V		2							mA	

Note :

1.I_{DD1} and I_{DD4} depend on output loading and cycle rates. Specified values are measured with the output open

2.Min. of tRRC (Refresh $\overline{RAS}$ cycle time) is shown at AC CHARACTERISTICS II

AC CHARACTERISTICS I (AC operating conditions unless otherwise noted)

Parameter		Symbol	-5		-55		-6		-7		-8		-10P		-10		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
System clock cycle time	$\overline{CAS}$ Latency = 3	tCK3	5	1000	5.5	1000	6	1000	7	1000	8	1000	10	1000	10	1000	ns	
	$\overline{CAS}$ Latency = 2	tCK2	10		10		10		10		10		10		12		ns	
Clock high pulse width		tCHW	2	-	2.25	-	2.5	-	3	-	3	-	3	-	3.5	-	ns	1
Clock low pulse width		tCLW	2	-	2.25	-	2.5	-	3	-	3	-	3	-	3.5	-	ns	1
Access time from clock	$\overline{CAS}$ Latency = 3	tAC3	-	4.5	-	5	-	5.5	-	5.5	-	6	-	6	-	6	ns	2
	$\overline{CAS}$ Latency = 2	tAC2	-	6	-	6	-	6	-	6	-	6	-	6	-	6	ns	
Data-out hold time		tOH	1.5	-	2	-	2	-	2	-	2	-	2	-	2	-	ns	3
Data-Input setup time		tDS	1.5	-	1.5	-	1.5	-	1.75	-	2	-	2	-	2.5	-	ns	1
Data-Input hold time		tDH	1	-	1	-	1	-	1	-	1	-	1	-	1	-	ns	1
Address setup time		tAS	1.5	-	1.5	-	1.5	-	1.75	-	2	-	2	-	2.5	-	ns	1
Address hold time		tAH	1	-	1	-	1	-	1	-	1	-	1	-	1	-	ns	1
CKE setup time		tCKS	1.5	-	1.5	-	1.5	-	1.75	-	2	-	2	-	2.5	-	ns	1
CKE hold time		tCKH	1	-	1	-	1	-	1	-	1	-	1	-	1	-	ns	1
Command setup time		tCS	1.5	-	1.5	-	1.5	-	1.75	-	2	-	2	-	2.5	-	ns	1
Command hold time		tCH	1	-	1	-	1	-	1	-	1	-	1	-	1	-	ns	1
CLK to data output in low Z-time		tOLZ	1	-	1	-	1	-	1	-	1	-	1	-	1	-	ns	
CLK to data output in high Z-time	$\overline{CAS}$ Latency = 3	tOHZ3	-	4.5	-	5	-	5.5	-	5.5	-	6	-	6	-	6	ns	
	$\overline{CAS}$ Latency = 2	tOHZ2	-	6	-	6	-	6	-	6	-	6	-	6	-	6	ns	

Note :

1.Assume tR / tF (input rise and fall time) is 1ns

2.Access times to be measured with input signals of 1v/ns edge rate, 0.8v to 2.0v

3.Data-out hold time to be measured under 30pF load condition, without Vt termination

AC CHARACTERISTICS II (AC operating conditions unless otherwise noted)

Parameter		Symbol	-5		-55		-6		-7		-8		-10P		-10		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{RAS}$ cycle time	Operation	tRC	55	-	55	-	60	-	63	-	68	-	70	-	70	-	ns	
	Auto Refresh	tRRC	55	-	55	-	60	-	63	-	68	-	70	-	70	-	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD	15	-	16.5	-	18	-	20	-	20	-	20	-	20	-	ns	
$\overline{RAS}$ active time		tRAS	40	100K	38.5	100K	42	100K	42	100K	48	100K	50	100K	50	100K	ns	
$\overline{RAS}$ precharge time		tRP	15	-	16.5	-	18	-	20	-	20	-	20	-	20	-	ns	
$\overline{RAS}$ to $\overline{RAS}$ bank active delay		tRRD	10	-	11	-	12	-	14	-	16	-	20	-	20	-	ns	
$\overline{CAS}$ to $\overline{CAS}$ delay		tCCD	1	-	1	-	1	-	1	-	1	-	1	-	1	-	CLK	
Write command to data-in delay		tWTL	0	-	0	-	0	-	0	-	0	-	0	-	0	-	CLK	
Data-in to precharge command		tDPL	1	-	1	-	1	-	1	-	1	-	1	-	1	-	CLK	
Data-in to active command		tDAL	4	-	4	-	4	-	4	-	4	-	4	-	4	-	CLK	
DQM to data-out Hi-Z		tDQZ	2	-	2	-	2	-	2	-	2	-	2	-	2	-	CLK	
DQM to data-in mask		tDQM	0	-	0	-	0	-	0	-	0	-	0	-	0	-	CLK	
MRS to new command		tMRD	2	-	2	-	2	-	2	-	2	-	2	-	2	-	CLK	
Precharge to data output Hi-Z	$\overline{CAS}$ Latency = 3	tPROZ3	3	-	3	-	3	-	3	-	3	-	3	-	3	-	CLK	
	$\overline{CAS}$ Latency = 2	tPROZ2	2	-	2	-	2	-	2	-	2	-	2	-	2	-	CLK	
Power down exit time		tPDE	1	-	1	-	1	-	1	-	1	-	1	-	1	-	CLK	
Self refresh exit time		tSRE	1	-	1	-	1	-	1	-	1	-	1	-	1	-	CLK	1
Refresh Time		tREF	-	64	-	64	-	64	-	64	-	64	-	64	-	64	ms	

Note :

1. A new command can be given tRRC after self refresh exit

DEVICE OPERATING OPTION TABLE

HY57V653220B-5

	$\overline{CAS}$ Latency	tRCD	tRAS	tRC	tRP	tAC	tOH
200MHz(5ns)	3CLKs	3CLKs	8CLKs	11CLKs	3CLKs	4.5ns	1.5ns
183MHz(5.5ns)	3CLKs	3CLKs	8CLKs	11CLKs	3CLKs	5ns	2ns
166MHz(6ns)	3CLKs	3CLKs	7CLKs	10CLKs	3CLKs	5.5ns	2ns

HY57V653220B-55

	$\overline{CAS}$ Latency	tRCD	tRAS	tRC	tRP	tAC	tOH
183MHz(5.5ns)	3CLKs	3CLKs	7CLKs	10CLKs	3CLKs	5ns	2ns
166MHz(6ns)	3CLKs	3CLKs	7CLKs	10CLKs	3CLKs	5.5ns	2ns
143MHz(7ns)	3CLKs	3CLKs	6CLKs	9CLKs	3CLKs	5.5ns	2ns

HY57V653220B-6

	$\overline{CAS}$ Latency	tRCD	tRAS	tRC	tRP	tAC	tOH
166MHz(6ns)	3CLKs	3CLKs	7CLKs	10CLKs	3CLKs	5.5ns	2ns
143MHz(7ns)	3CLKs	3CLKs	6CLKs	9CLKs	3CLKs	5.5ns	2ns
125MHz(8ns)	3CLKs	3CLKs	6CLKs	9CLKs	3CLKs	6ns	2.5ns

HY57V653220B-7

	$\overline{CAS}$ Latency	tRCD	tRAS	tRC	tRP	tAC	tOH
143MHz(7ns)	3CLKs	3CLKs	6CLKs	9CLKs	3CLKs	5.5ns	2ns
125MHz(8ns)	3CLKs	3CLKs	6CLKs	9CLKs	3CLKs	6ns	2.5ns
100MHz(10ns)	2CLKs	2CLKs	5CLKs	7CLKs	2CLKs	6ns	2.5ns

HY57V653220B-8

	$\overline{CAS}$ Latency	tRCD	tRAS	tRC	tRP	tAC	tOH
125MHz(8ns)	3CLKs	3CLKs	6CLKs	9CLKs	3CLKs	6ns	2.5ns
100MHz(10ns)	2CLKs	2CLKs	5CLKs	7CLKs	2CLKs	6ns	2.5ns
83MHz(12ns)	2CLKs	2CLKs	4CLKs	6CLKs	2CLKs	6ns	2.5ns

HY57V653220B-10P

	$\overline{CAS}$ Latency	tRCD	tRAS	tRC	tRP	tAC	tOH
100MHz(10ns)	2CLKs	2CLKs	5CLKs	7CLKs	2CLKs	6ns	2.5ns
83MHz(12ns)	2CLKs	2CLKs	5CLKs	7CLKs	2CLKs	6ns	2.5ns
66MHz(15ns)	2CLKs	2CLKs	4CLKs	6CLKs	2CLKs	6ns	2.5ns

HY57V653220B-10

	$\overline{\text{CAS}}$ Latency	tRCD	tRAS	tRC	tRP	tAC	tOH
100MHz(10ns)	3CLKs	2CLKs	5CLKs	7CLKs	2CLKs	6ns	2.5ns
83MHz(12ns)	2CLKs	2CLKs	5CLKs	7CLKs	2CLKs	6ns	2.5ns
66MHz(15ns)	2CLKs	2CLKs	4CLKs	6CLKs	2CLKs	6ns	2.5ns

COMMAND TRUTH TABLE

Command		CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	ADDR	A10/ AP	BA	Note
Mode Register Set		H	X	L	L	L	L	X	OP code			
No Operation		H	X	H	X	X	X	X	X			
				L	H	H	H					
Bank Active		H	X	L	L	H	H	X	RA		V	
Read		H	X	L	H	L	H	X	CA	L	V	
Read with Autoprecharge										H		
Write		H	X	L	H	L	L	X	CA	L	V	
Write with Autoprecharge										H		
Precharge All Banks		H	X	L	L	H	L	X	X	H	X	
Precharge selected Bank										L	V	
Burst Stop		H	X	L	H	H	L	X	X			
DQM		H	X					V	X			
Auto Refresh		H	H	L	L	L	H	X	X			
Burst-READ-Single-WRITE		H	X	L	L	L	L	X	A9 Pin High (Other Pins OP code)			
Self Refresh[1]	Entry	H	L	L	L	L	H	X	X			
	Exit	L	H	H	X	X	X	X				
				L	H	H	H					
Precharge power down	Entry	H	L	H	X	X	X	X	X			
				L	H	H	H					
	Exit	L	H	H	X	X	X	X				
				L	H	H	H					
Clock Suspend	Entry	H	L	H	X	X	X	X	X			
				L	V	V	V					
	Exit	L	H	X				X				

Note :
1. Exiting Self Refresh occurs by asynchronously bringing CKE from low to high
2. X = Don't care, H = Logic High, L = Logic Low. BA =Bank Address, RA = Row Address, CA = Column Address, Opcode = Operand Code, NOP = No Operation

PACKAGE INFORMATION

400mil 86pin Thin Small Outline Package