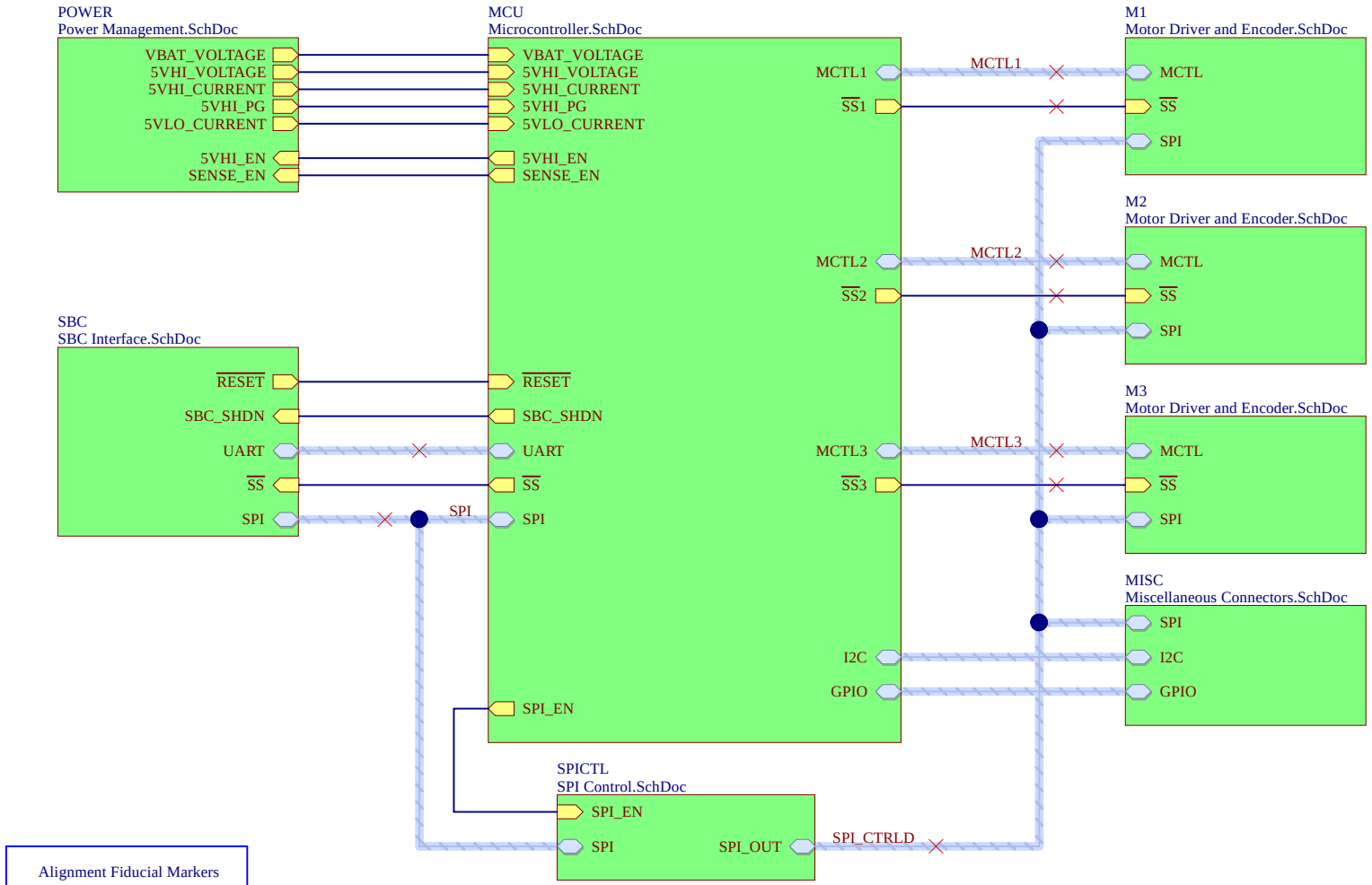
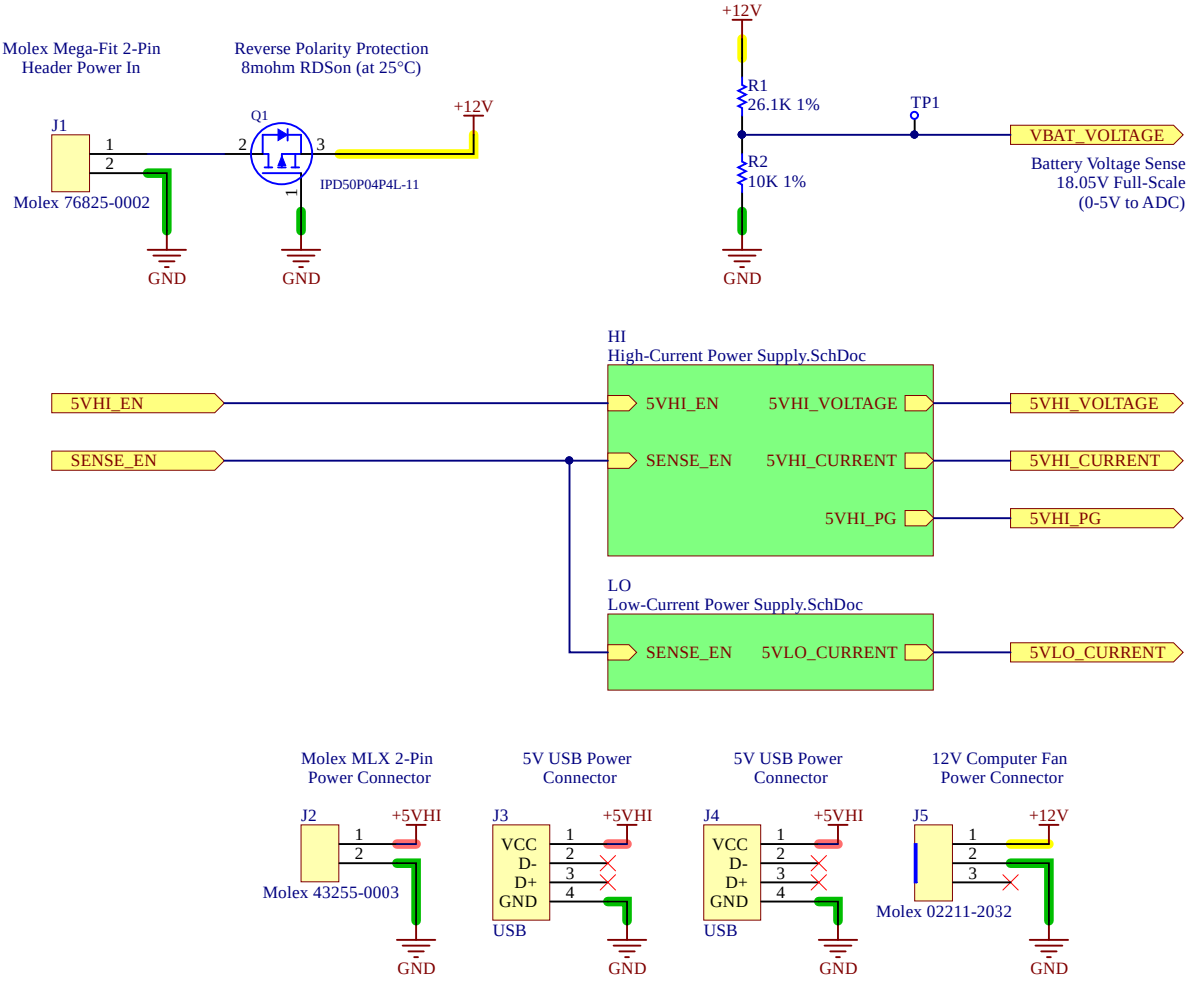


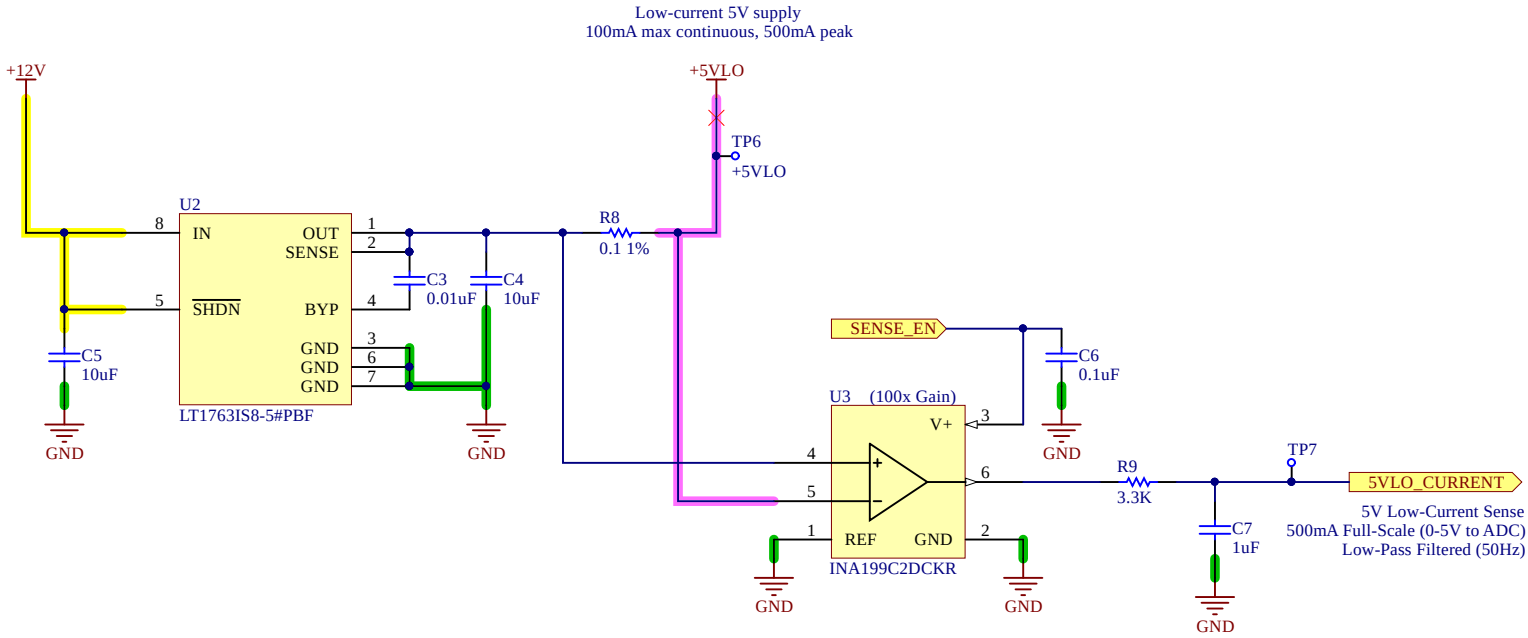
Title: Tennis Butler Top Level		Rev: 1.0
Size: Letter	Drawn By: Joseph Riesen	
Date: 5/1/2019	Time: 11:23:01 AM	Sheet 1 / 10

Tennis Butler



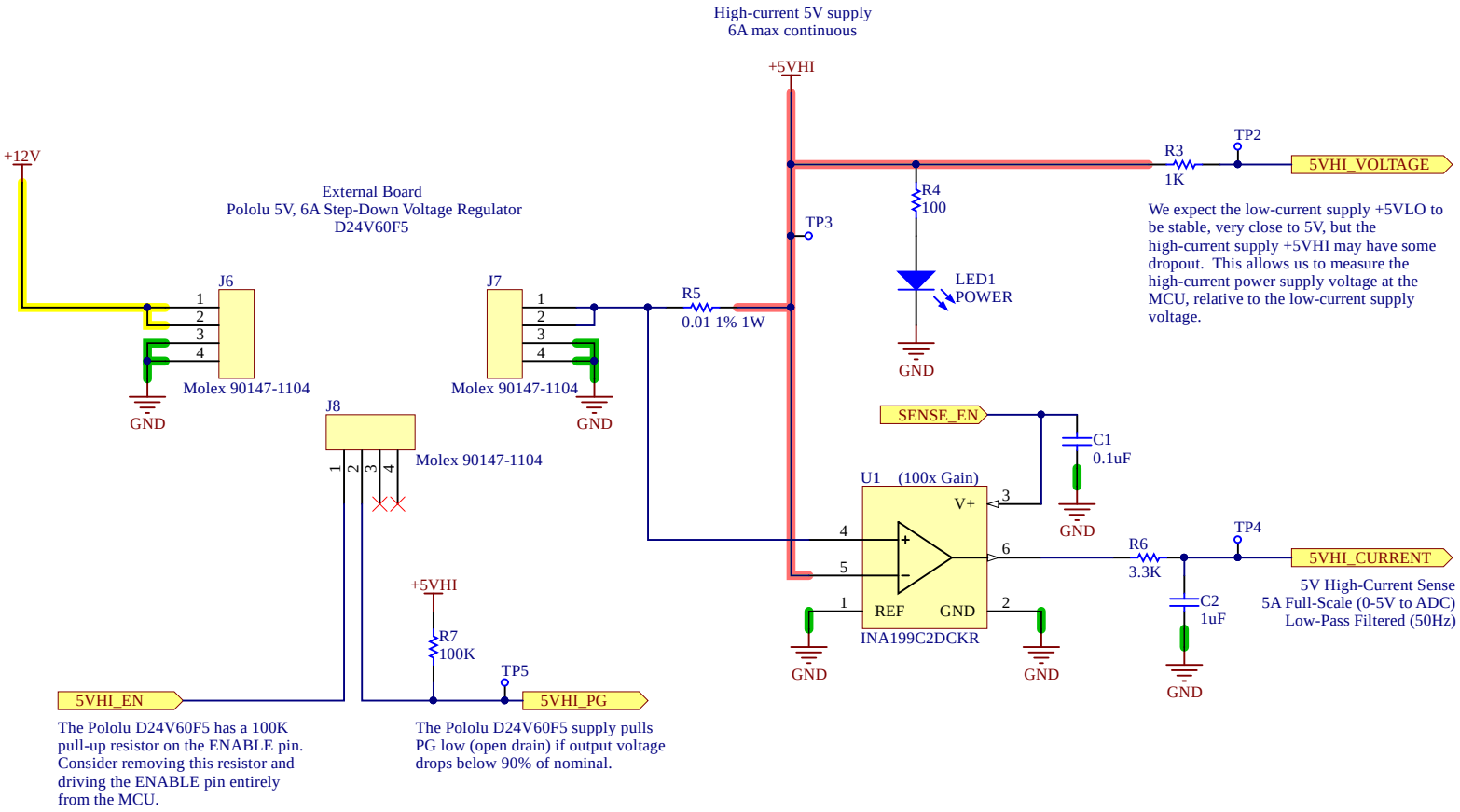
Title: Power Management			Rev: 1.0
Size: Letter	Drawn By: Joseph Riesen		
Date: 5/1/2019	Time: 11:23:01 AM	Sheet 2 / 10	

Tennis Butler



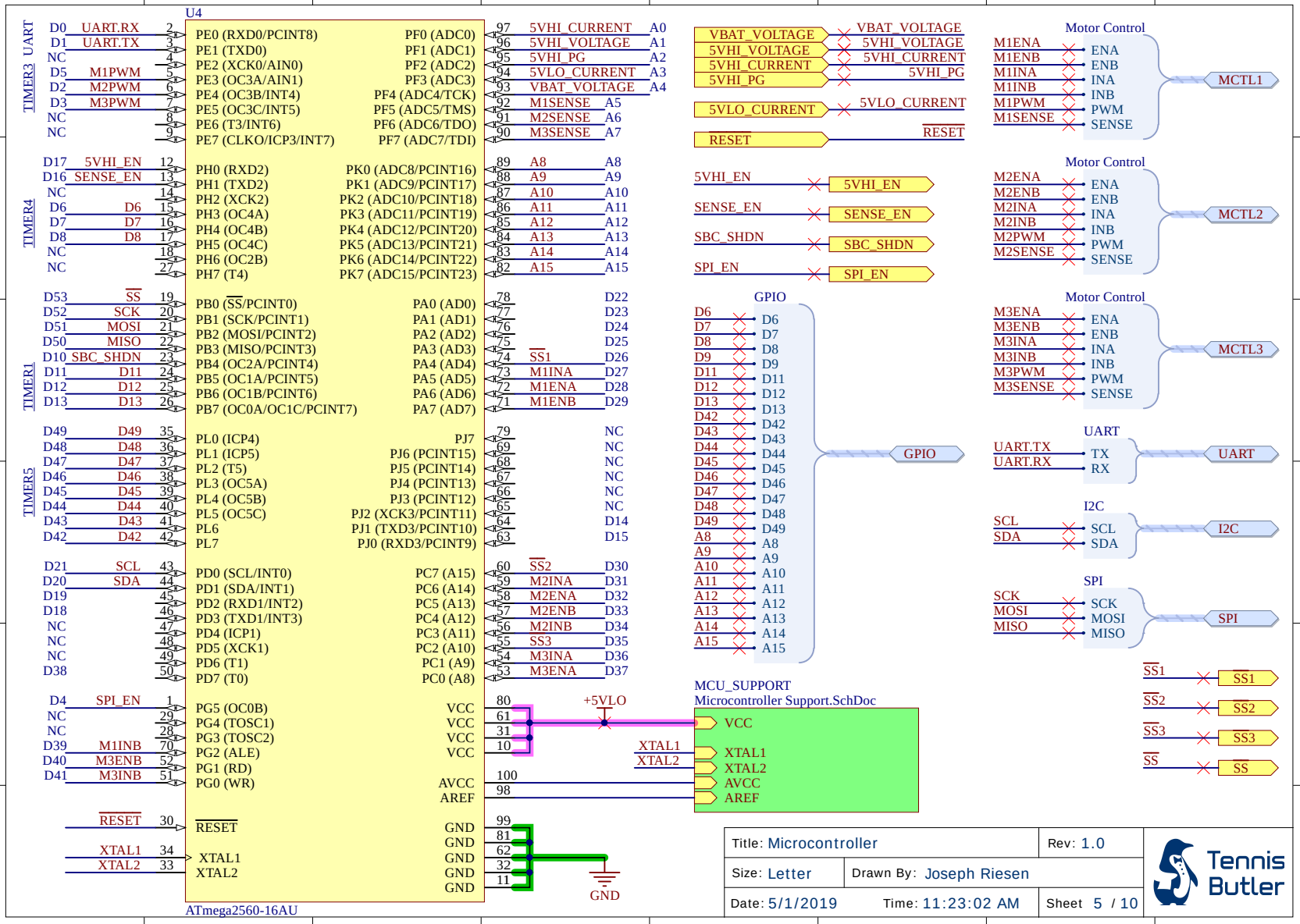
Title: Low-Current Power Supply			Rev: 1.0
Size: Letter	Drawn By: Joseph Riesen		
Date: 5/1/2019	Time: 11:23:01 AM	Sheet 3 / 10	

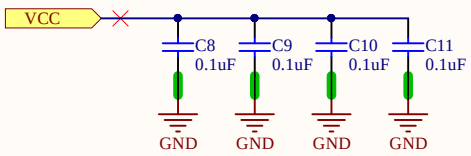
Tennis Butler

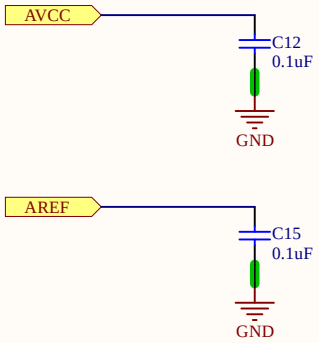


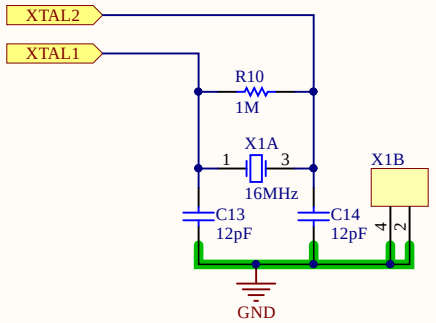
Title: High-Current Power Supply			Rev: 1.0
Size: Letter	Drawn By: Joseph Riesen		
Date: 5/1/2019	Time: 11:23:01 AM	Sheet 4 / 10	

Tennis Butler

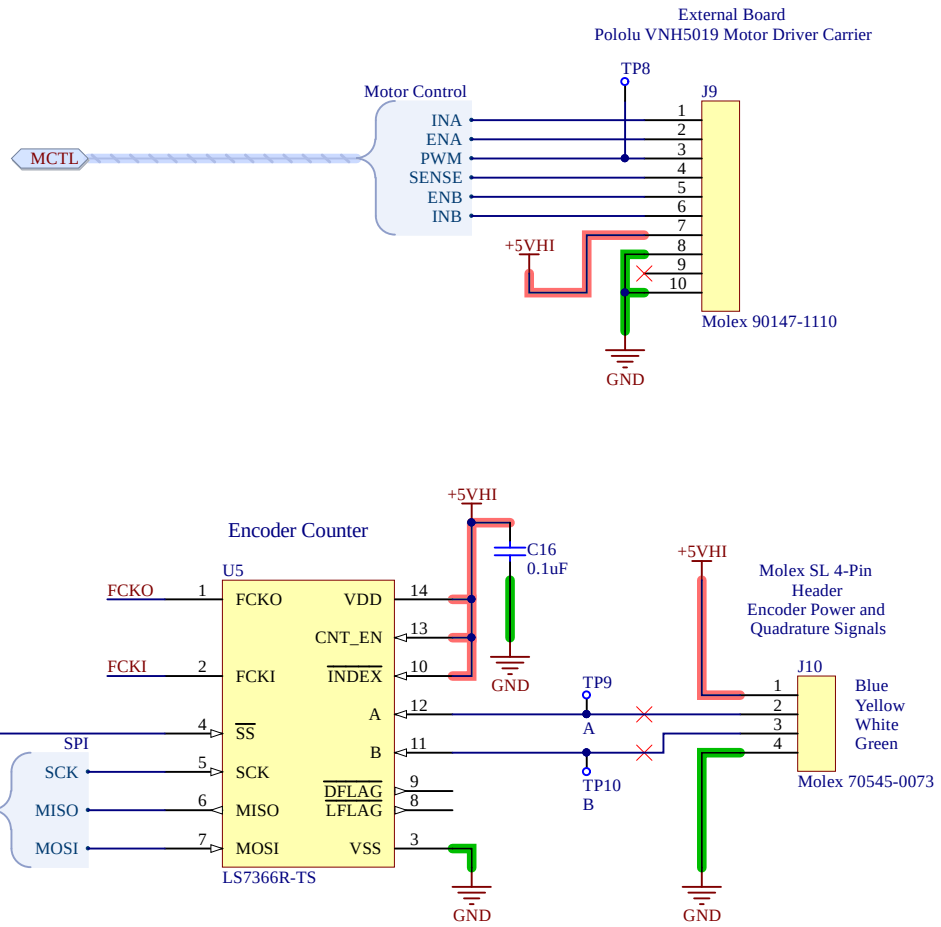

U4
ATmega2560-16AU
PE0 (RXD0/PCINT8)
PE1 (TXD0)
PE2 (XCK0/AIN0)
PE3 (OC3A/AIN1)
PE4 (OC3B/INT4)
PE5 (OC3C/INT5)
PE6 (T3/INT6)
PE7 (CLKO/ICP3/INT7)
PH0 (RXD2)
PH1 (TXD2)
PH2 (XCK2)
PH3 (OC4A)
PH4 (OC4B)
PH5 (OC4C)
PH6 (OC2B)
PH7 (T4)
PB0 (SS/PCINT0)
PB1 (SCK/PCINT1)
PB2 (MOSI/PCINT2)
PB3 (MISO/PCINT3)
PB4 (OC2A/PCINT4)
PB5 (OC1A/PCINT5)
PB6 (OC1B/PCINT6)
PB7 (OC0A/OC1C/PCINT7)
PL0 (ICP4)
PL1 (ICP5)
PL2 (T5)
PL3 (OC5A)
PL4 (OC5B)
PL5 (OC5C)
PL6
PL7
PD0 (SCL/INT0)
PD1 (SDA/INT1)
PD2 (RXD1/INT2)
PD3 (TXD1/INT3)
PD4 (ICP1)
PD5 (XCK1)
PD6 (T1)
PD7 (T0)
PG5 (OC0B)
PG4 (TOSC1)
PG3 (TOSC2)
PG2 (ALE)
PG1 (RD)
PG0 (WR)
RESET
XTAL1
XTAL2
PF0 (ADC0)
PF1 (ADC1)
PF2 (ADC2)
PF3 (ADC3)
PF4 (ADC4/TCK)
PF5 (ADC5/TMS)
PF6 (ADC6/TDO)
PF7 (ADC7/TDI)
PK0 (ADC8/PCINT16)
PK1 (ADC9/PCINT17)
PK2 (ADC10/PCINT18)
PK3 (ADC11/PCINT19)
PK4 (ADC12/PCINT20)
PK5 (ADC13/PCINT21)
PK6 (ADC14/PCINT22)
PK7 (ADC15/PCINT23)
PA0 (AD0)
PA1 (AD1)
PA2 (AD2)
PA3 (AD3)
PA4 (AD4)
PA5 (AD5)
PA6 (AD6)
PA7 (AD7)
PJ7
PJ6 (PCINT15)
PJ5 (PCINT14)
PJ4 (PCINT13)
PJ3 (PCINT12)
PJ2 (XCK3/PCINT11)
PJ1 (TXD3/PCINT10)
PJ0 (RXD3/PCINT9)
PC7 (A15)
PC6 (A14)
PC5 (A13)
PC4 (A12)
PC3 (A11)
PC2 (A10)
PC1 (A9)
PC0 (A8)
VCC
AVCC
AREF
GND
UART
TIMER3
TIMER4
TIMER1
TIMER5
5VHI_CURRENT
5VHI_VOLTAGE
5VHI_PG
5VLO_CURRENT
VBAT_VOLTAGE
M1SENSE
M2SENSE
M3SENSE
SS1
SS2
SS3
+5VLO
MCU_SUPPORT
Microcontroller Support.SchDoc
GPIO
Motor Control
MCTL1
MCTL2
MCTL3
UART
I2C
SPI
ENA
ENB
INA
INB
PWM
SENSE
Title: Microcontroller
Rev: 1.0
Size: Letter
Drawn By: Joseph Riesen
Date: 5/1/2019
Time: 11:23:02 AM
Sheet 5 / 10
Tennis Butler





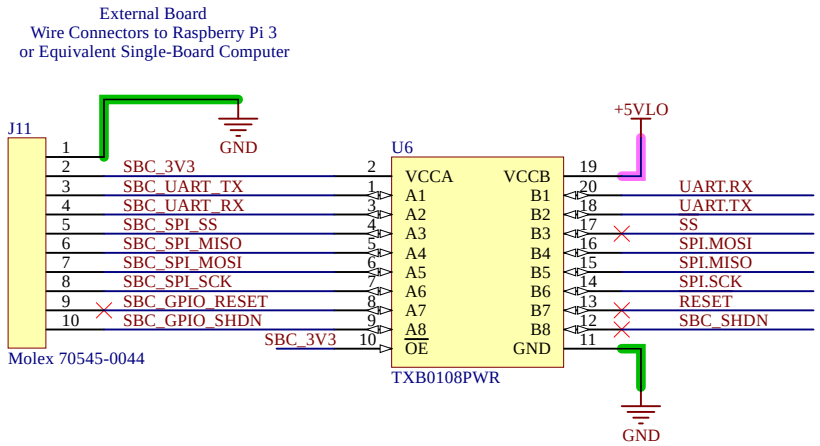


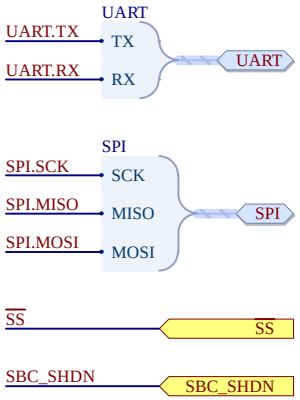
Title		
Size: Letter	Number	Revision
Date: 5/1/2019		Sheet of
File: C:\Users\..\Microcontroller Support.SchDoc		Drawn By:

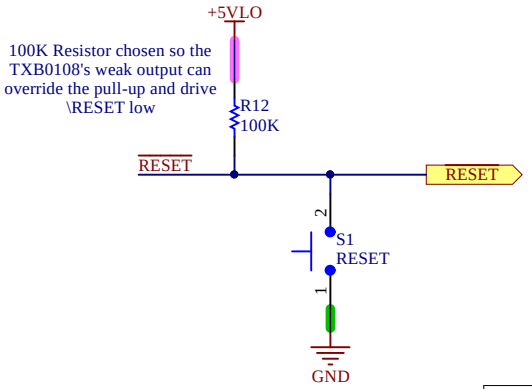


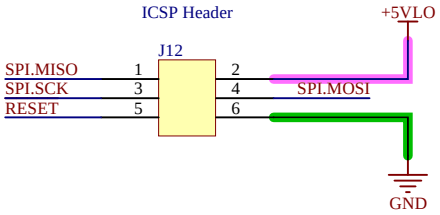
Title: Motor Driver and Encoder Counter			Rev: 1.0
Size: Letter	Drawn By: Joseph Riesen		
Date: 5/1/2019	Time: 11:23:02 AM	Sheet 7 / 10	

Tennis Butler



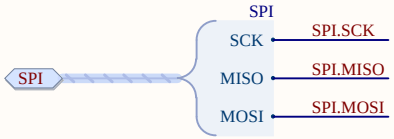


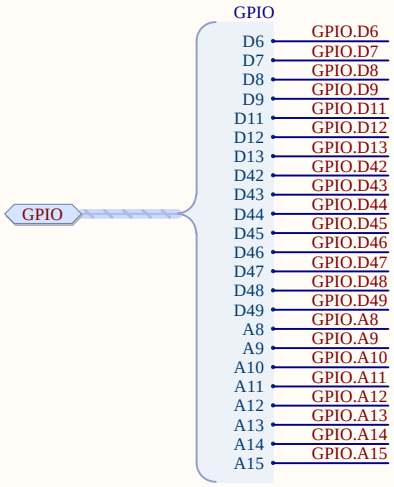




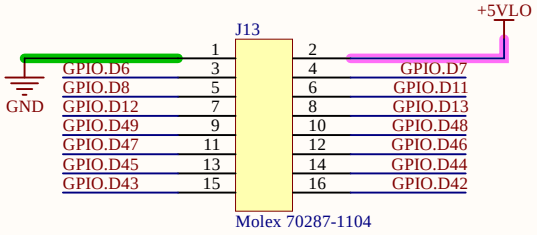
Title: Single Board Computer Interface			Rev: 1.0
Size: Letter	Drawn By: Joseph Riesen		
Date: 5/1/2019	Time: 11:23:02 AM	Sheet 8 / 10	

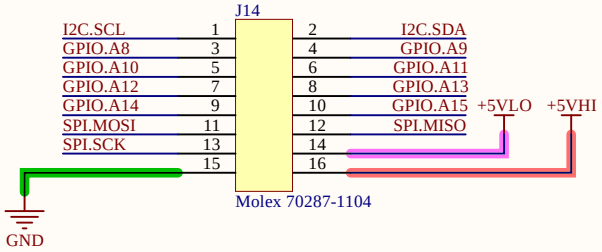
Tennis Butler



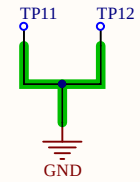


General-Purpose Headers

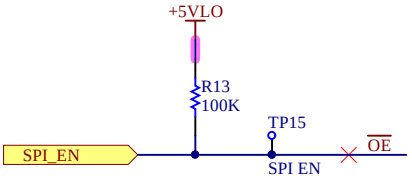


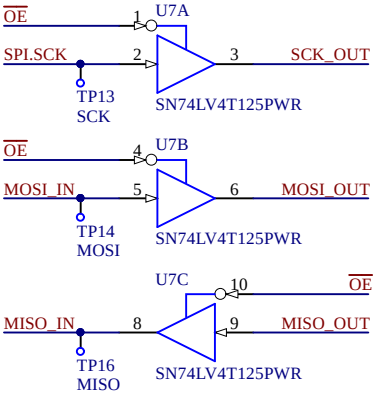


Ground Probe
Test Points



Title		
Size: Letter	Number	Revision
Date: 5/1/2019	Sheet of	
File: C:\Users\..\Miscellaneous Connectors.SchDoc	Drawn By:	



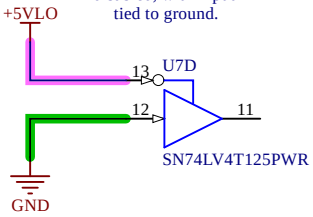


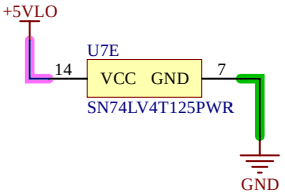
The SPI bus is disabled by default (save for the ICSP and SBC interface) to protect devices that may not be powered if we are using an external programmer and the +5VHI supply is disabled.

For example, the LS7366R cannot tolerate signals above VDD+0.3V, which precludes SPI activity if the ICs are not powered. However, each LS7366R requires 0.8mA at all times and cannot be put in standby mode, which precludes adding them to the +5VLO supply.

The MCU pulls SPI_EN low to enable communication with the rest of the SPI bus when +5VHI is enabled and stable.

Unused buffer is disabled, with input tied to ground.





Title: SPI Control			Rev: 1.0
Size: Letter	Drawn By: Joseph Riesen		
Date: 5/1/2019	Time: 11:23:02 AM		Sheet 10 / 10

Tennis Butler