Computer Architecture I

Grading Option II - Semester Project

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CS6133

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Project Goals

1. **Implementation - 10%**: Implement OR1K based SoC on a FPGA development kit.
2. **Enhancement - 25%**: Propose and perform some hardware improvement in the processing system to increase performance, reduce power and/or implementation size.
3. **Performance Analysis 25%**: Develop a plan to analyse stock system with the enhanced system and execute it.

Implement?

Processing Systems: OpenCore's OpenRISC Processor OR1K in DE0-Nano development board

- OpenCore's OpenRISC (OR1K) Processor[1]
  - A very successful open source processor
  - Compact and easy to customize
  - Supported by GNU tool-chain and Linux Kernel
  - Used as a reference design by many popular EDA tools vendors (Cadence for example)
- DE0-Nano: Altera's FPGA Development and Education Board[2]
  - Compact and robust development platform
  - Price reduced for students and faculty
  - Could host OR1K processor and run Linux
  - Expandable to increase capabilities

[1] www.opencores.org/or1k/Main_Page

[2] www.altera.com/education/univ/materials/boards/de0-nano/unv-de0-nano-board.html

What could I Enhance?

1. **ALU**: Most FPGA have fast multipliers and adders. Perhaps you could replace slow ALU in the processing system with fast once.
2. **CACHE**: Increase the CACHE size or change the cache scheme to minimize fault rate.
3. **Smart Branch**: Implement a new branch predication scheme.
4. **DSP Co-Processor**: Augment the processing system with a DSP Co-Processor. Most FPGAs have ultra fast DSP engines built in.
5. **I/O speed enhancement**: FPGAs have built-in FIFOs, take advantage of these FIFOs in some way to increase I/O performance.

What to Analyse?

1. **Base Line**: Before you make any modification to the stock system you should do a performance analyses of the component that you will be enhancing.
2. **Improvement**: After implementing the enhancements you should perform the same analysis and compare the results with the base line.

Why choose the project option?

1. **YOU**: The skills, confidence and discipline you acquire by doing the project will increase your value.
2. **Opportunity**: This project is an opportunity for you to explore, experiment and extended your boundaries.

Semester Project Schedule

1. **Implementation Phase (I)**: 02/12 - 02/26
   - Progress report 1 due on 02/12
   - Phase I milestone report and demonstration due by 02/26
2. **Enhancement Phase (II)**: 02/26 - 04/09
   - Progress report 2 due on 03/12
   - Progress report 3 due on 03/26
   - Phase II milestone report and demonstration due by 04/09
3. **Performance Analysis Phase (III)**: 04/09 - 05/07
   - Progress report 4 due on 04/23
   - Phase III milestone report and demonstration due by 05/07

Progress Report 1 Goals

Due - 02/12/14

1. Install and test development environment:
   - Quartus II 13.1, update 2
   - OR1K corsscompiler - GCC and associated build tools for bare-metal and Linux environment
   - OR1K debugger - GDB and on-dhip debugger (openocd)
2. Install appropriate Linux kernel source with patches for OR1K processor
3. Install and test OR1K simulator

Your report should contain information about how you accomplished the above tasks and results and should be less than two pages.

Phase I Milestone Goals

Due - 02/26/14

1. Video/Live demonstration:
   - Linux running in OR1K simulator. Upon successful boot you should display "CS6133-*your name*-Spring14" in the console.
   - Linux running in DE0-Nano. Upon successful boot you should display "CS6133-*your name*-Spring14" and contents /proc/cpuinfo in the console
   - Ability to control 8 LEDs in DE0-Nano through Linux. You are allowed to remap GPIO to LEDs
   - Ability to transfer files to and from Linux running in DE0-Nano using Xmodem protocol
   - Ability to boot Linux from SPI flash
2. Your Report should contain:
   1. Details of OR1K SoC top level and peripherals connected to OR1K processor
   2. Details of OR1K boot sequence
   3. Written documentation of the above demonstration

Progress Report 2 Goals

Due - 03/12/14

1. **Enhancement Selection**: The component that you have selected to enhance in OR1K SoC with architectural details
2. Ability to use the component without modification
3. Performance analysis tools you are planning to use for baseline performance analysis
4. Baseline performance Analysis of the component you will be enhancing

Goals for progress report 3 & 4 and phase II & III will be based on your performance and component you selected to enhance.

Fall Back

- Could I change my mind in middle or towards the end of the semester to discontinue with the project and go back to grading option 1?
  Yes, but you have to complete mid term and final project.
- Would I get partial credit for the project?
  May be