

Mid Term Project

Part 1: MIPS Registers (10 Points)

Instruction Set
Architecture
(ISA) - Part V

Vikram
Padman

Mid Term

Part 1

Part 2

Part 3

Part 4

Part 5

Part 6

Extra Credit

- ① MIPS CPU provided 32 general purpose registers.
Registers access is faster than memory access. (5 Points)
 - ① Does it make sense to increase the number of registers?
 - ② List and discuss advantages and disadvantages of having many registers
 - ③ How does an architect come up with the optimal number of registers and what are the driving factors?
- ② Read Appendix-A and answer the following questions: (5 Points)
 - ① What is the difference between the “Opcode” and “funct” in MIPS R-Type instructions?
 - ② You are designing a CPU that is required to support 200+ instructions and functions. How many “opcode” and “funct” bits would you need? Support your answer with details.

Mid Term Project

Part 2: Analyse of AVR32 ISA

Instruction Set
Architecture
(ISA) - Part V

Vikram
Padman

Mid Term

Part 1

Part 2

Part 3

Part 4

Part 5

Part 6

Extra Credit

Atmel's AVR family of micro controllers are widely used in small embedded control system, power supplies, real time systems and embraced by hobbyist. Its popularity is due to lower cost, simplistic design, flexible interface and supported by many compilers. AVR32 is extension of the original AVR instruction set and was created to support real time operating systems. AVR32 processors are comparatively cheap and its development environment is well supported by the open source community and industry.

AVR32 Architecture Document could be found here:

<http://www.atmel.com/Images/doc32000.pdf>

Mid Term Project

Part 2: Analyse of AVR32 ISA (15 Points)

Instruction Set
Architecture
(ISA) - Part V

Vikram
Padman

Mid Term

Part 1

Part 2

Part 3

Part 4

Part 5

Part 6

Extra Credit

For Part 1, study AVR instruction set and answer the following questions:

- Classify AVR32's ISA. Use week 4, 5, 6 lectures and Appendix A as a guide for classification. (10 Points)
- From your analysis determine if AVR32 processor could be used for: (5 Points)
 - Digital Signal Processing application
 - Server class operating system (Linux/Unix, Solaris, Windows Server).

You must provide justification.

please try to limit your report size to 10 pages for this part.

Mid Term Project

Part 3: Understanding Simple CPU (mips_ss.qar) (15 Points)

Instruction Set
Architecture
(ISA) - Part V

Vikram
Padman

Mid Term

Part 1

Part 2

Part 3

Part 4

Part 5

Part 6

Extra Credit

Understanding Simple CPU (mips_ss) is important to complete the rest of the midterm project. In this part you will write couple of assembly programs in binary and execute it in mips_ss CPU running in DE0-Nano.

- ① Write a counter program that would count from 0 to 15 and decrement to 10. Once it decrements to 10 the counter should reset to 0 and restart. (5 points)
- ② Write a program to write the following the string “Your Name, CS6133, FALL2013” somewhere in the data memory (10 points)

For this part you must submit the programs you wrote and signal tap II capture file.

Mid Term Project

Part 4: Program Counter (mips_ss.qar) (20 Points)

Instruction Set
Architecture
(ISA) - Part V

Vikram
Padman

Mid Term

Part 1

Part 2

Part 3

Part 4

Part 5

Part 6

Extra Credit

- ① Consider the program counter in AVR32 and Simple CPU.
 - ① How many different methods are there to change PC in AVR32 and Simple CPU? (5 Points)
 - ② Suppose you were asked to redesign Simple CPU's PC to mimic AVR32's PC. How would you change Simple CPU's control set-up and data path to accomplish this task? Describe in detail with pictures. (10 Points)
- ② Implement and demonstrate your new PC in Simple CPU implemented in DE0-Nano. (5 Points) ¹

¹Partial credit (2.5 points) will awarded for a reasonable non-functional implementation.

Mid Term Project

Part 5: Jump/Branch and Link (mips_ss.qar) (20 Points)

Instruction Set
Architecture
(ISA) - Part V

Vikram
Padman

Mid Term

Part 1

Part 2

Part 3

Part 4

Part 5

Part 6

Extra Credit

- ① Consider the return pointer register in AVR32.
 - ① How could you implement a jump/branch and link instruction, similar to the once in AVR32, in Simple CPU? Describe in detail with pictures. (15 Points)
- ② Modify the branch instruction to branch and link in Simple CPU implemented in DE0-Nano. (5 Points) ²

²Partial credit (2.5 points) will awarded for a reasonable non-functional implementation.

Mid Term Project

Part 6: OUT instruction (mips_ss.qar) (20 Points)

Instruction Set
Architecture
(ISA) - Part V

Vikram
Padman

Mid Term

Part 1

Part 2

Part 3

Part 4

Part 5

Part 6

Extra Credit

- ① You are asked to design and implement a new instruction, called “OUT”, in Simple CPU. The OUT instruction has one source register operand and it outputs lower 8-bits to LEDs in DE0-Nano board. For example; assembly instruction “out \$16” would output the lower 8-bits to DE0-Nano’s LEDs.
 - ① What type of instruction format would you use for the “OUT” instruction? and why? (2 Points)
 - ② How would you encode “OUT” instruction? and why? (3 Points)
 - ③ Design the “OUT” instruction in paper (8 Points)
 - ④ Assume that you have designed and implemented the “OUT” instruction as described above. A software engineer is questioning how she could use this new instruction to output data memory’s contents. How would you answer her question?(2 Points)
- ② Implement and demonstrate “OUT” in DE0-Nano. (5 Points)³

³Partial credit (2.5 points) will awarded for a reasonable non-functional implementation

Mid Term Project

Extra Credit: Jump instruction (mips_ss.qar) (25 Points)

Instruction Set
Architecture
(ISA) - Part V

Vikram
Padman

Mid Term

Part 1
Part 2
Part 3
Part 4
Part 5
Part 6

Extra Credit

- ① Design and implement, in paper, direct jump instruction explained in “Computer Organization and Design” pg 328 in 4th edition or pg 313 in 3rd edition. (15 Points)
- ② Implement and demonstrate jump instruction in DE0-nano (10 Points)