Computer Architecture I

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CS6133

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Instructor: Vikram Padman

Experience:

- Over 10 years of experience in hardware design
- Work for a defence contractor in NJ
  - Design high speed DSP hardware and related control systems
  - Evaluate COTS processors and software

Education:

- BS and MS from NYU:Poly

Contact Information:

- **E-mail:** vikram@poly.edu or vikram@computer.org or vikram.padman@nyu.edu
- **Live Q & A:** For online session only, every Wednesday 10PM to 11PM(EST) using NYU classes (TBA)

Course Logistics

- **Textbooks:** You will be asked to read selected chapters from the following textbooks.
  1. Computer Architecture - A Quantitative Approach, Fourth or Fifth Edition. Hennesy and Patterson
  2. Digital Design and Computer Architecture, First or Second Edition. David Money and Sarah L. Harris
  3. Computer Organization and Design, Third or Fourth Edition. Patterson and Hennesy
- **Conference Papers and Technical Articles :** In addition to the above textbooks you will be asked to read conference/journal papers, technical articles, and user guides.

Course Logistics

- **DE0-Nano :** Altera DE0-Nano FPGA Development and Education Board. You are required to **buy** this board, it costs around $60 to $70. This board will be used in weekly activities, course projects and semester project.
  `http://www.altera.com/education/univ/materials/boards/de0-nano/unv-de0-nano-board.html`
- **Lecture format for on-line sessions:** One to four short video lectures per week

Course Logistics

This is a GRADUATE COURSE and that means it is YOUR responsibility to:

- Ask questions
- Fulfil course requirements on-time without reminders
- Manage your time
- Manage course load
- Understand course expectations
- Exercise honest and ethical behaviour
- Report unethical behaviour to faculty and/or course staff.
- Have the DESIRE TO LEARN
- Comply with "Departmental Policy on Collaboration on Programming Assignments" [1]

[1] http://cis.poly.edu/policies/

Grading Option I

Default

- **Weekly Activities :** Two to four activity sets per week. Expect to spend around 2 to 3 hours per activity set
- **Course Project :** Mid-Term Project
- **Exam :** Final Exam (Open Book)
- **Course Participation :** Active participation in discussion forums are required
- **Course Grade :**
  - Weekly Activities - 10%
  - Discussion Forums - 10%
  - Mid-Term Project - 30%
  - Final Project - 30%
  - Final Exam - 20

Grading Option II

Advanced, Instructor's Approval Required

- **Weekly Activities :** Two to four activity sets per week. Expect to spend around 2 to 3 hours per activity set
- **Course Participation :** Active participation in discussion forums and project presentation is required
- **Course Grade :**
  - Weekly Activities - 10%
  - Discussion Forums - 10%
  - Semester Project - 80%
- **Semester Project (80%)**
  Based on OR1K Processor `http://opencores.org/or1k/Main_Page`
  - Implementation - 20%
  - Enhancement - 30%
  - Performance analysis - 30%

Final Grade Policy

93% to 100%	A
90% to 92.9%	A-
87% to 89.9%	B+
83% to 86.9%	B
80% to 82.9%	B-
77% to 79.9%	C+
55% to 76.9%	C
54.9% or below	F

Computer Architecture

Course Objectives / Syllabus

- **Digital Computer**
  - Computing Machinery And Intelligence – A.M.Turing
  - The First Draft Report on the EDVAC – John von Neumann
- **Digital Electronics**
  - Managing Complexity
  - Numbering System
  - Binary Arithmetic
  - Logic Gates
  - Digital Abstraction
  - Combinatorial Logic
    - Boolean Equations
    - Boolean Algebra
    - Karnaugh Maps
    - Timing Analysis

Computer Architecture

Course Objectives / Syllabus

- **Digital Electronics** (Continued)
  - Sequential Logic
    - Latches and Flip-Flops
    - Synchronous Logic Design
    - Finite State Machines
    - Timing Analysis
    - Parallelism
  - Physical Constraints
- **CPU**
  - Instruction Set Architecture
  - Building Blocks
  - Hardware Architecture - Single Cycle CPU
    - Data and Control Path
    - Instructions
    - Performance Analysis
- **Midterm Project**

Computer Architecture

Course Objectives / Syllabus

- **CPU** (Continued)
  - Hardware Architecture - Pipelined CPU
    - Data and Control Path
    - Hazards
    - Pipelined CPU Implementation
- **Memory Subsystem**
  - Memory Basics
  - Memory Hierarchy
    - Cache
    - Virtual Memory
    - Performance Analysis and Measurements
- **Final Exam**

Q: What are Grading Options?

- This course has two grading options as explained before. You, as student, could select grading option I or II. However, admission into grading option II will be approved by the staff after an initial screening.

Q: What will I be doing in weekly activities?

In weekly activities you will be asked to:

1. Read selected chapters from course textbook and answer questions
2. Read technical articles and research papers and answer questions
3. Implement sections of a simple MIPS CPU using schematics and test it in DE0-Nano
4. On average students spent around 12.5 hours per week on activities, projects and discussion forums for this course in previous semesters.

Q: How and when do I submit weekly activities and projects?

1. You will submit your weekly activities and projects through Blackboard
2. E-mail submissions are invalid and not acceptable
3. Submission deadlines will be posted and late submissions are not allowed
4. Submission format for weekly activities and projects are:
   - File 1: **Report** in pdf format with the following file name: lastname_firstname_week_x.pdf
   - File 2: **Quartus II** project archive (.qar) file, if applicable, with the following file name lastname_firstname_week_x.qar
   - No other files are acceptable
5. Your reports should to concise and clear

Q: How are discussion forums graded?

1. There will be around 11 to 12 discussion forums this semester and your could get up to 10 point from each discussion forum.
2. To get those 10 points every week you have to:
   1. Post 2 to 3 unique question threads related to concepts covered in lectures or assigned reading materials from a particular week.
   2. Answer 3 to 4 questions threads started by other.
   3. You may get points for posting technical problems and solutions related to DE0-Nano.
   4. You may get points for posting in general threads posted by the staff.
3. Discussion forums will be graded every week. Grade changes cannot be made once a forum is graded.

Q: What portion of the syllabus is tested in the Final Exam? And how is it conducted?

Final Exam:

- Covers the entire course syllabus
- Conducted through ProctorU
- Open-Book: You are allowed to bring in any printed material. Electronic references are not allowed
- Around 3 hours

Q: What will I be doing in midterm project?

In midterm project you will:

1. Integrate, improve and test simple MIPS CPU in DE0-Nano using schematics. You are not required to use any HDL languages. However, if you already know VHDL, Verilog or AHDL you are welcome to use your knowledge. You will be graded the same way and will not get any extra point for using HDLs.
2. Read selected chapters from course text book, research papers and answer questions
3. Prove or disprove a theory. Reference material will be supplied.

Q: What will I be doing if I select grading option II?

1. You will **implement** OR1K processor in DE0-Nano, test and do a base line **performance analysis**.
2. You will analyse the stock OR1K implementation and **enhance** some portion/component in the stock CPU to improve performance, reduce power and/or increase reliability.
3. Finally, you will perform a detailed **performance analysis** of stock implementation and enhanced CPU and write a final report.

a) You should have working knowledge in VHDL/Verilog or AHDL to be accepted in grading option II. If you like to be grading option II contact me within two weeks from the course start date.
b) I will provide necessary technical guidance to you in all three stages. I will also let you know what your report should contain and how much details I expect to see.

Q: Should I know VHDL, Verilog or AHDL to get an "A" in this course?

- **NO** you do not need to know any HDL languages to get an "A" in this course
- HDLs are a requirement only for grading option II.
  - Most of the students who got an "A" last semester are from grading option I.
  - Grading option II is for students who wants to take the extra challenge in exchange for real world experience.

Q: Does DE0-Nano use any special software? If yes, what is it and how could I learn to use it?

- We will be using Altera's free Quartus II Web Edition software to program and analyse logic in DE0-Nano.
  - You could download Quartus II from Altera's web site (`http://dl.altera.com/?edition=web`)
  - This semester we will be using version 13.1 (Update 1)
- You could learn how to use Quartus II software from free on-line training video provided by Altera.
  - A comprehensive list of those videos and links are listed in the following slides.

Altera's Quartus-II Training

Free Online Training

1. **Read Me First!** (ORMF1000, 0.5 Hour)
   - English: `http://www.altera.com/education/training/courses/ORMF1000`
   - Chinese: `http://www.altera.com/education/training/courses/OCRMF1000`
   - Japanese: `http://www.altera.com/education/training/courses/OJRMF1000`
2. **Basics of Programmable Logic** (ODSW1005, 1.5 Hours)
   - English: `http://www.altera.com/education/training/courses/ODSW1005`
   - Chinese: `http://www.altera.com/education/training/courses/OCDSW1005`
   - Japanese: `http://www.altera.com/education/training/courses/OJDSW1005`
3. **How to Begin a Simple FPGA Design** (ODSW1010, 1 Hour)
   - English: `http://www.altera.com/education/training/courses/ODSW1010`
   - Chinese: `http://www.altera.com/education/training/courses/OCDSW1010`
   - Japanese: `http://www.altera.com/education/training/courses/OJDSW1010`
4. **Quartus II Software: An Introduction** (ODSW1100, 1.5 Hours)
   - English: `http://www.altera.com/education/training/courses/ODSW1100`
   - Chinese: `http://www.altera.com/education/training/courses/OCDSW1100`

Altera's Quartus-II Training

Free Online Training

5. **Quartus II Software: Schematic Design** (ODSW1105, 0.5 Hours)
   - English: `http://www.altera.com/education/training/courses/ODSW1105`
   - Chinese: `http://www.altera.com/education/training/courses/OCDSW1105`
6. **SignalTap II Logic Analyzer** (ODSW1164, 2 Hours)
   - English: `http://www.altera.com/education/training/courses/ODSW1164`
   - Chinese: `http://www.altera.com/education/training/courses/OCDSW1164`
7. **Configuring Altera FPGAs** (ODEV1100, 2 Hours)
   - English: `http://www.altera.com/education/training/courses/ODEV1100`
   - Chinese: `http://www.altera.com/education/training/courses/OCDEV1100`