

ECE4904 Lecture 8

pn Junction Diode: Forward, Reverse Bias (5.2)

Ideal Diode V-I Characteristic (6.1)
Carrier Concentration

Real Diode V-I: Deviations from the Ideal (6.2)
Reverse bias breakdown (6.2.2)
High current effects (6.2.4)

BJT (Ch. 10, 11)
Construction

Handouts

Ch. 5, 6 Figures
Ch. 10, 11 Figures

$$Q = CV$$

$$C = \frac{Q}{V}$$

JUNCTION CAPACITANCE

$$C_j = \frac{\Delta Q}{\Delta V}$$

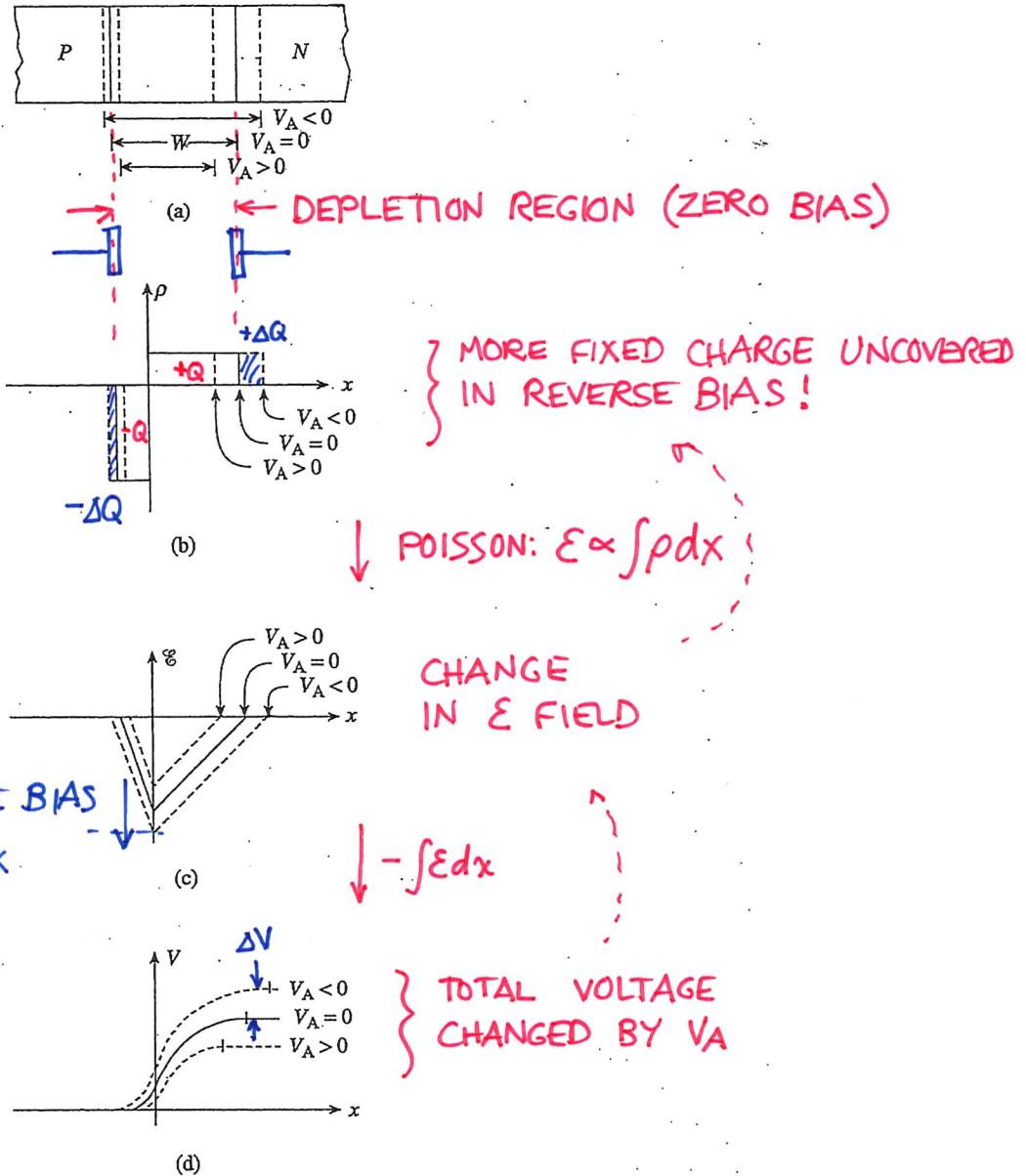
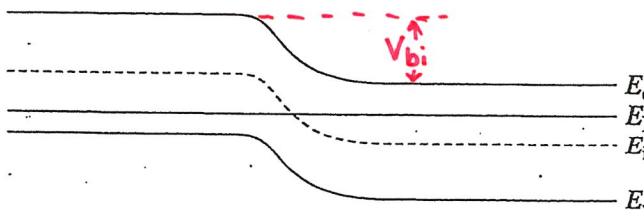
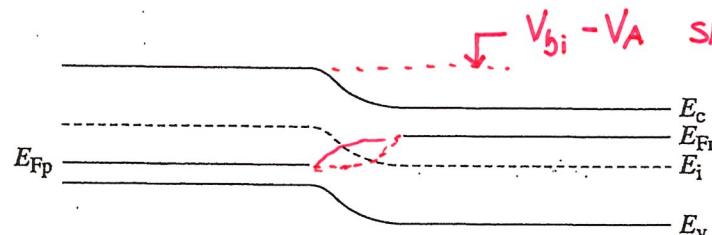


Figure 5.11 Effect of forward and reverse biasing on the (a) depletion width, (b) charge density, (c) electric field, and (d) electrostatic potential inside a *pn* junction diode.



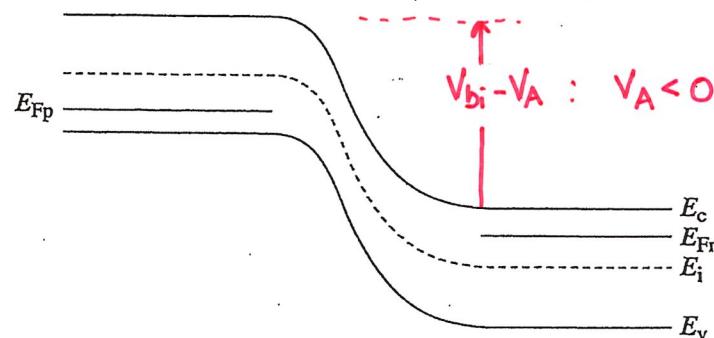
(a) Equilibrium ($V_A = 0$)



(b) Forward bias ($V_A > 0$)

$$\Rightarrow \frac{1}{n} \propto \frac{1}{p} \propto \frac{1}{n_i^2}$$

E_F NOT REALLY DEFINED
IN DEPLETION REGION
(NONEQUILIBRIUM)



(c) Reverse bias ($V_A < 0$)

Figure 5.12 pn junction energy band diagrams. (a) Equilibrium ($V_A = 0$), (b) forward (0), and (c) reverse bias ($V_A < 0$).

KNOWN FWD BIAS $V_A = 0.33V$

- EXCESS MINORITY CARRIERS AT EDGE OF DEPL REGION HOW MUCH IS INCREASE?

LAW OF THE JUNCTION:

$$np = n_i^2 e^{qV_A/kt}$$

$$\approx 1E+20 e^{(0.33/0.0259)}$$

$$3.4E+5$$

$np = 3.4E+25$ AT EDGE OF DEPL REG

IDEAL DIODE EQUATION

$$I = qA \left[\frac{D_n n_i^2}{L_n N_A} + \frac{D_p n_i^2}{L_p N_D} \right] (e^{qV_A/kt} - 1)$$

$$\frac{D}{M} = \frac{kT}{q} \quad M_p (N_D = 1E+15) \quad 460 \text{ cm}^2/\text{V}\cdot\text{s}$$

$$M_n (N_A = 1E+16) \quad 1250 \text{ cm}^2/\text{V}\cdot\text{s}$$

$$I = (1.67E-15 A) [e^{qV_A/kt} - 1]$$

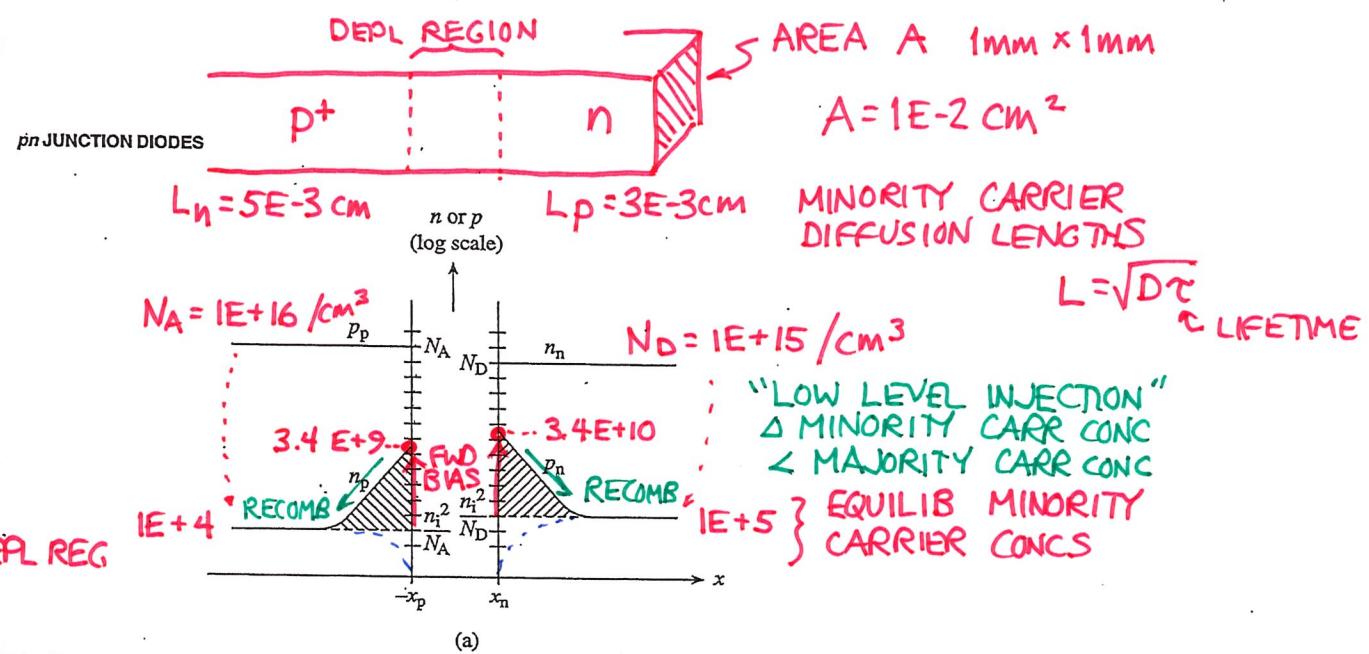
I_s

V_A

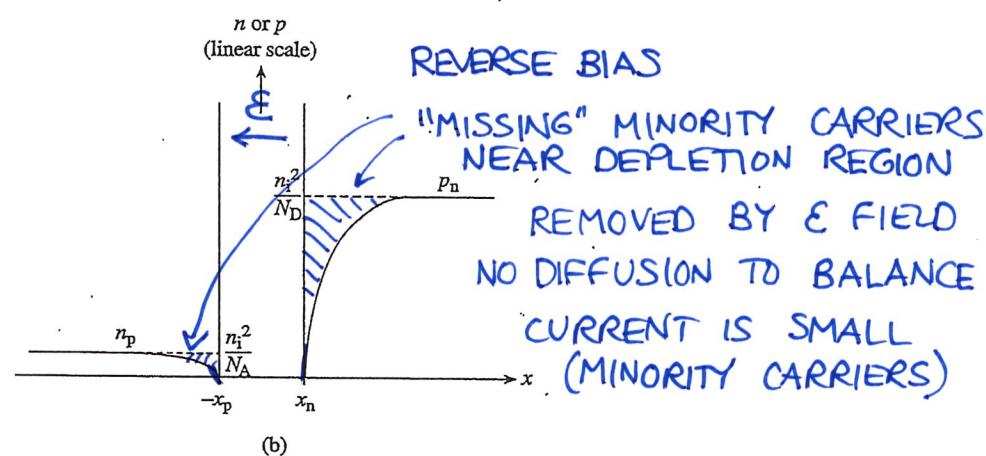
I

$$0.33V \quad 0.57 \text{ nA}$$

$$60mV \downarrow \begin{cases} 0.66V \\ 0.72V \end{cases} \quad \begin{cases} 195 \text{ mA} \\ 1.95 \text{ mA} \end{cases} \quad \begin{cases} 10X \\ 10X \end{cases}$$



(a)



(b)

Figure 6.8 Carrier concentrations inside a pn junction diode under (a) forward biasing and (b) reverse biasing. The cross-hatching identifies excess minority carriers. Note that (a) is a semilog plot while (b) is a linear plot. $N_A > N_D$ was assumed in constructing the sample plots.

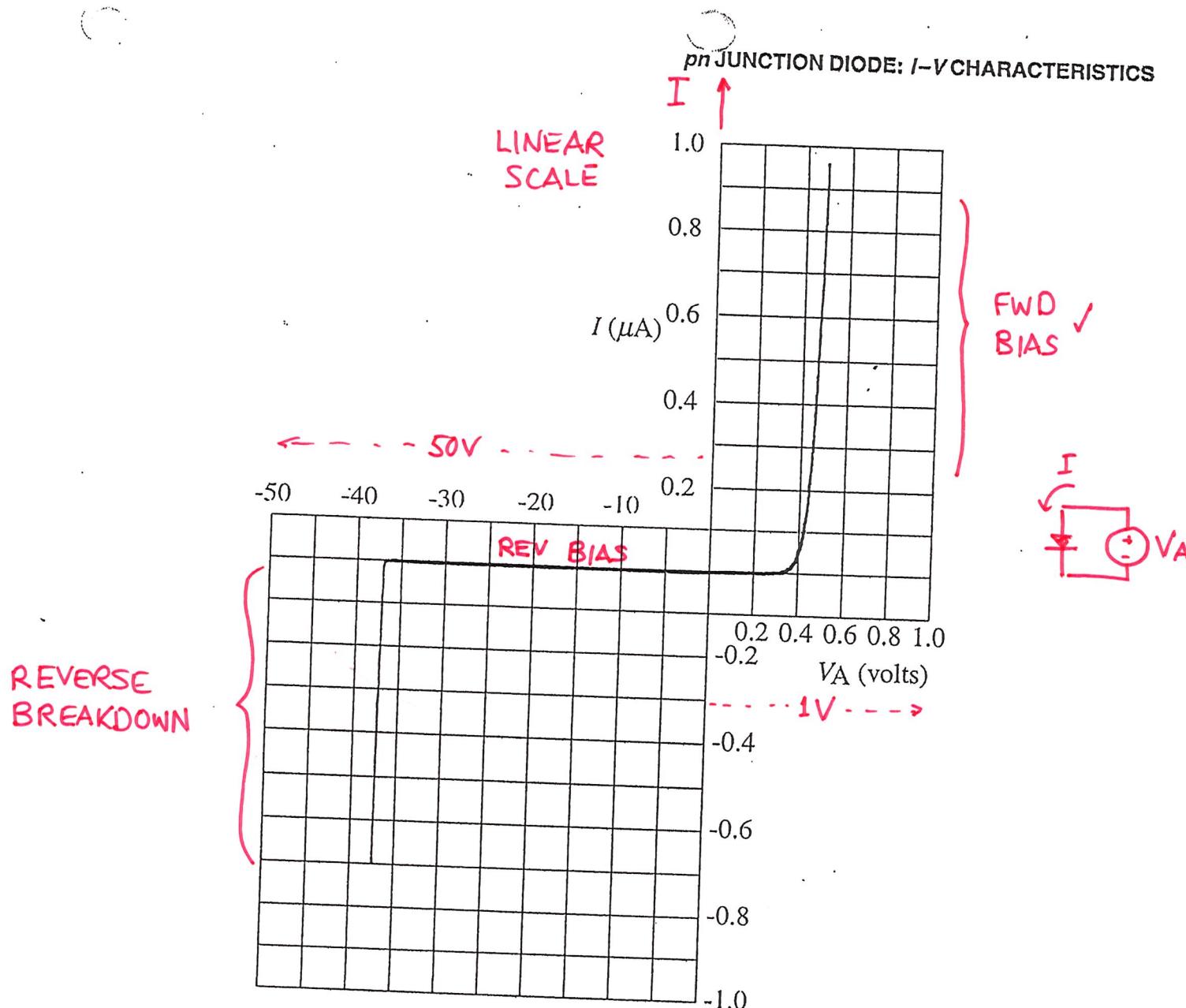


Figure 6.9 Linear plot of the measured I - V characteristic derived from a commercially available Si pn junction diode maintained at room temperature.

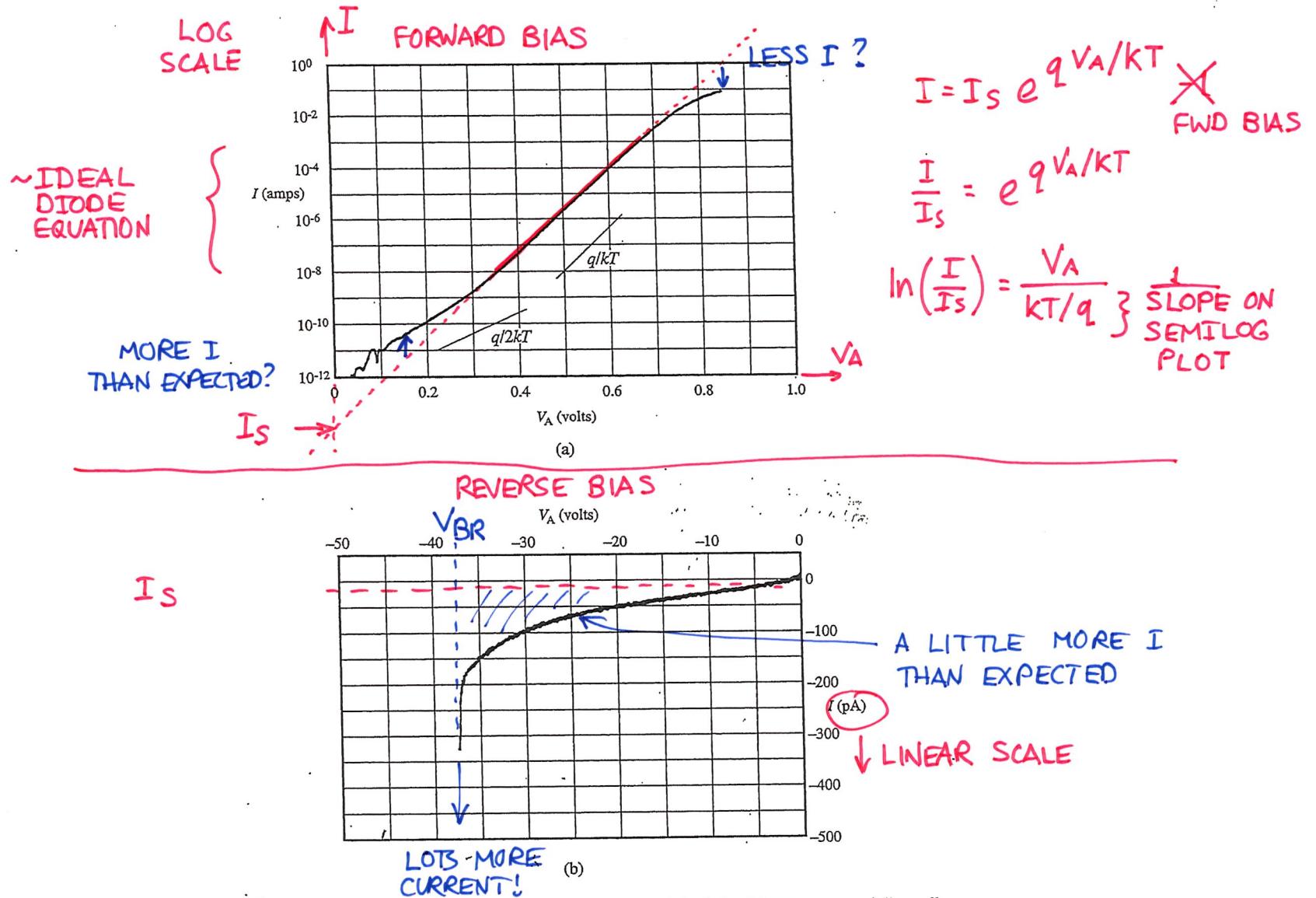


Figure 6.10 Detailed plots of the measured I - V characteristic derived from a commercially available Si p n junction diode maintained at room temperature. The Fig. 6.9 and Fig. 6.10 characteristics are from the same device. (a) Semilog plot of the forward-bias current versus voltage. (b) Expanded scale plot of the reverse-bias current versus voltage.

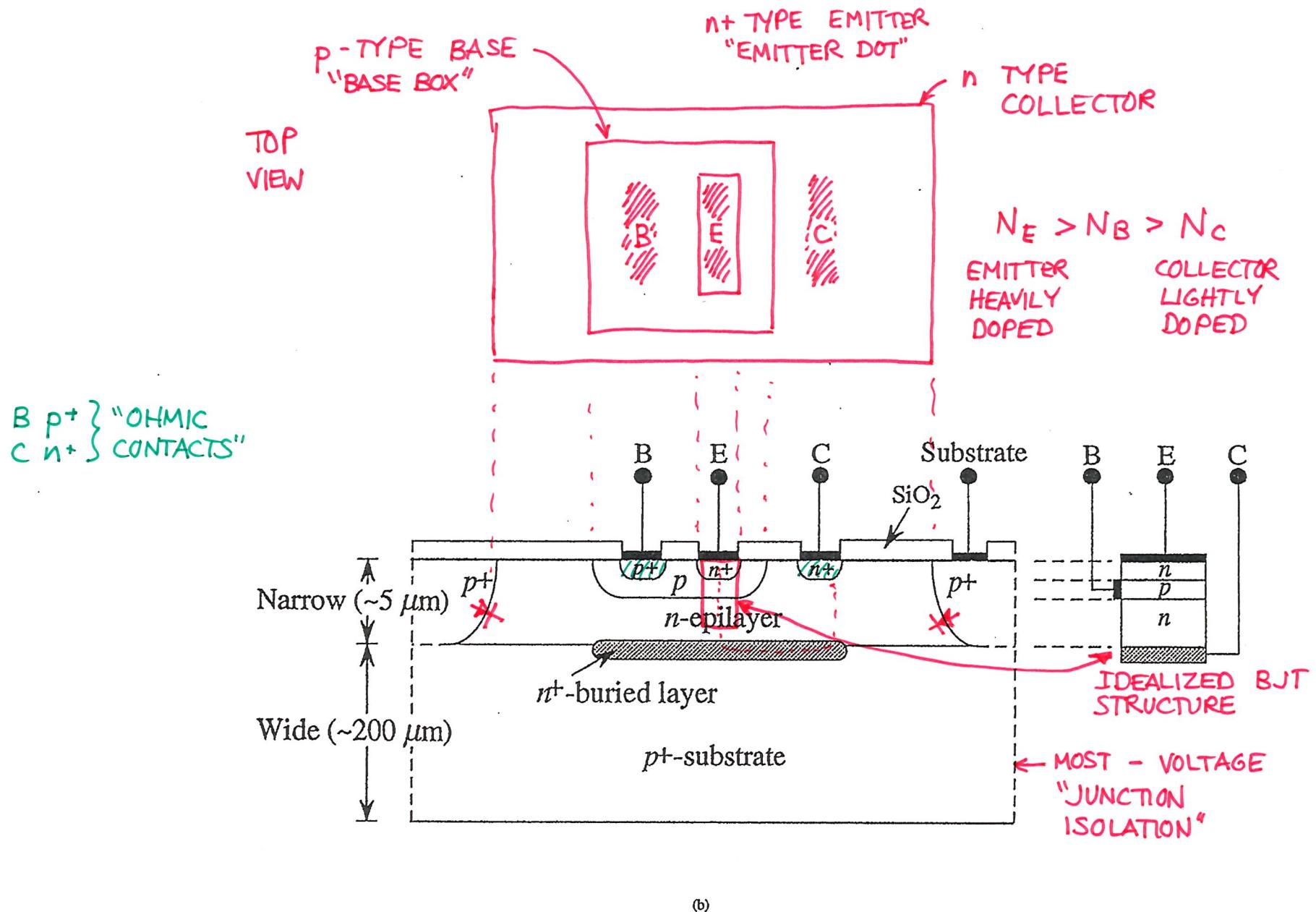


Figure 10.6 Cross sections and simplified models for (a) a typical discrete, double-diffused pnp BJT and (b) an integrated circuit npn BJT.

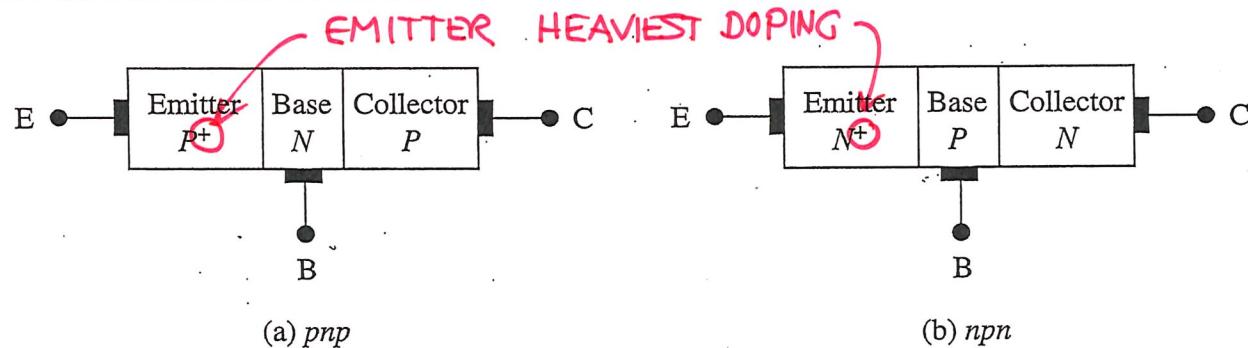
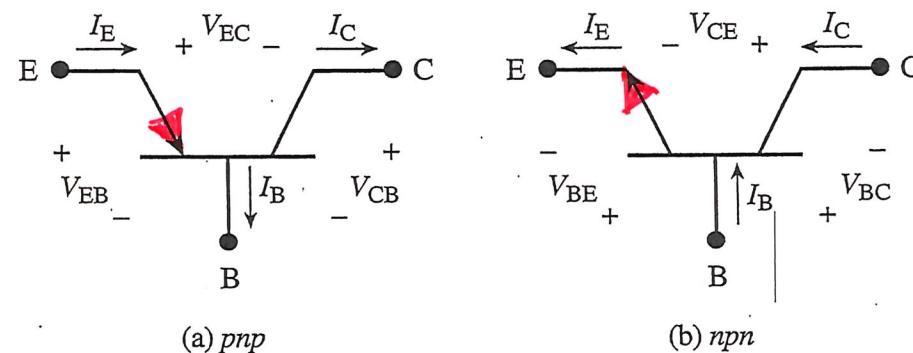


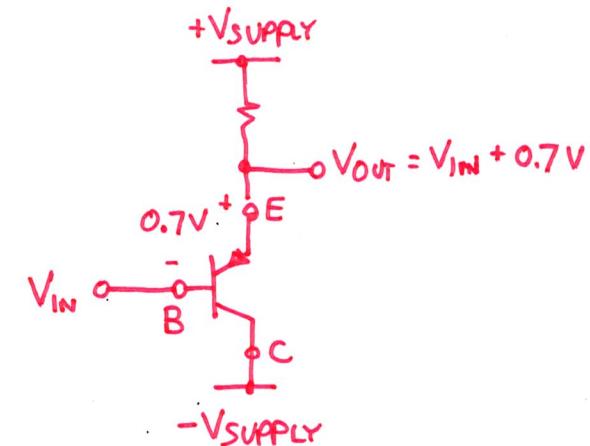
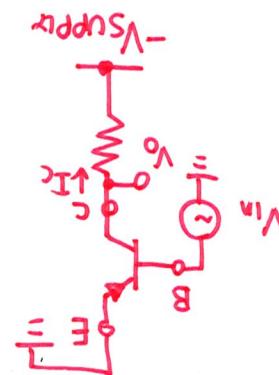
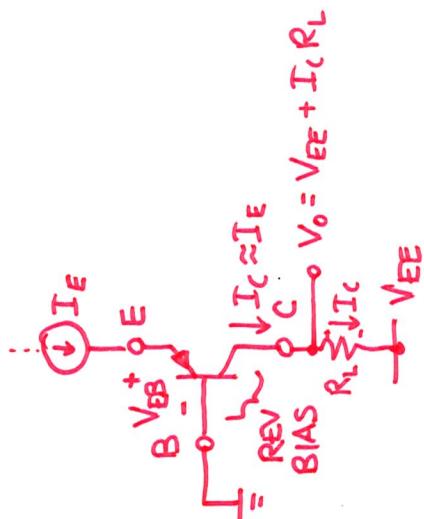
Figure 10.1 Schematic representation of the (a) *pnp* and (b) *npn* BJT showing device regions and the terminal designations.

ARROW: PN OF B-E JUNCTION



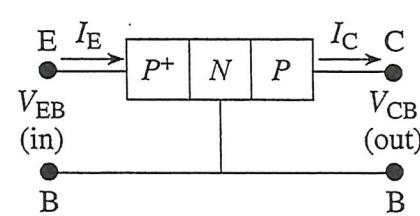
KVL, KCL
 $I_E = I_C + I_B$
 GIVEN ANY 2
 WE KNOW 3rd

Figure 10.2 (a) *pnp* and (b) *npn* BJT circuit symbols. The d.c. terminal currents, voltages, and reference polarities are also noted in the figure.

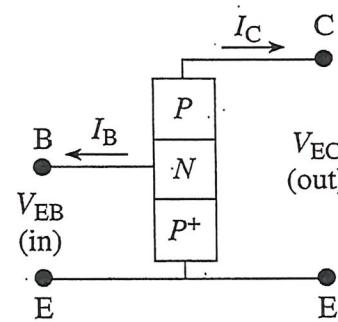


BJT FUNDAMENTALS

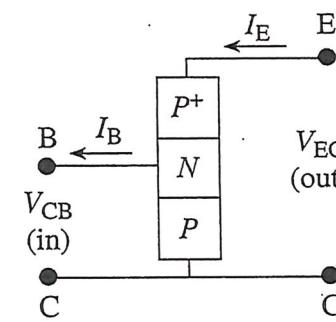
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(a) Common base



(b) Common emitter



(c) Common collector

FOR ALL:
WANT $I_B \approx 0$

~~$I_C = \beta I_B$~~

$V_{BE} \rightarrow I_C$

$$I_B = \frac{I_C}{\beta} \quad \} \rightarrow \infty$$

Figure 10.3 Circuit configurations: (a) common base; (b) common emitter; and (c) common collector.

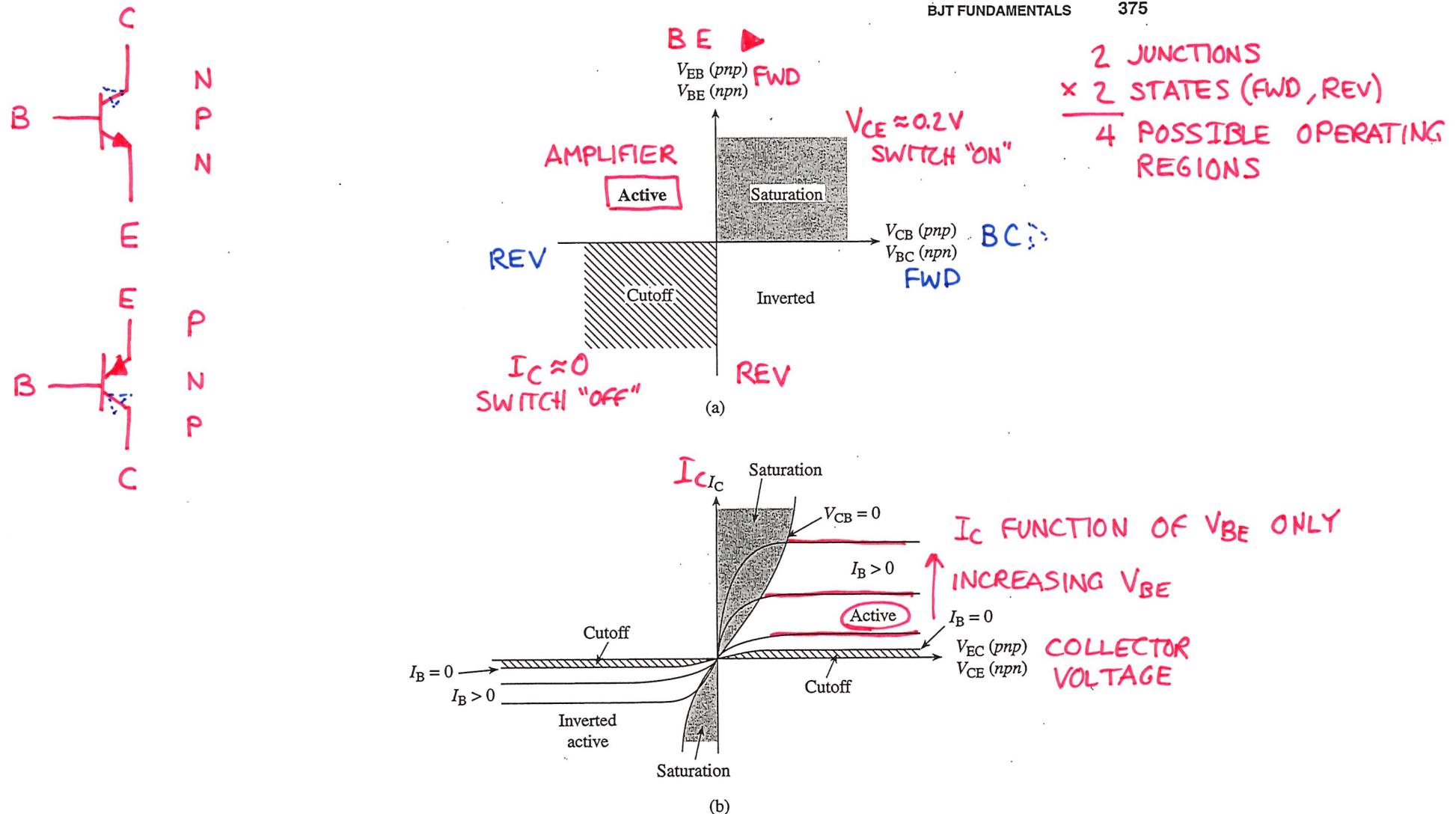


Figure 10.5 (a) Combinations of the BJT input and output voltages resulting in the four biasing modes. (b) Regions of the BJT common emitter output characteristics associated with the four biasing modes.

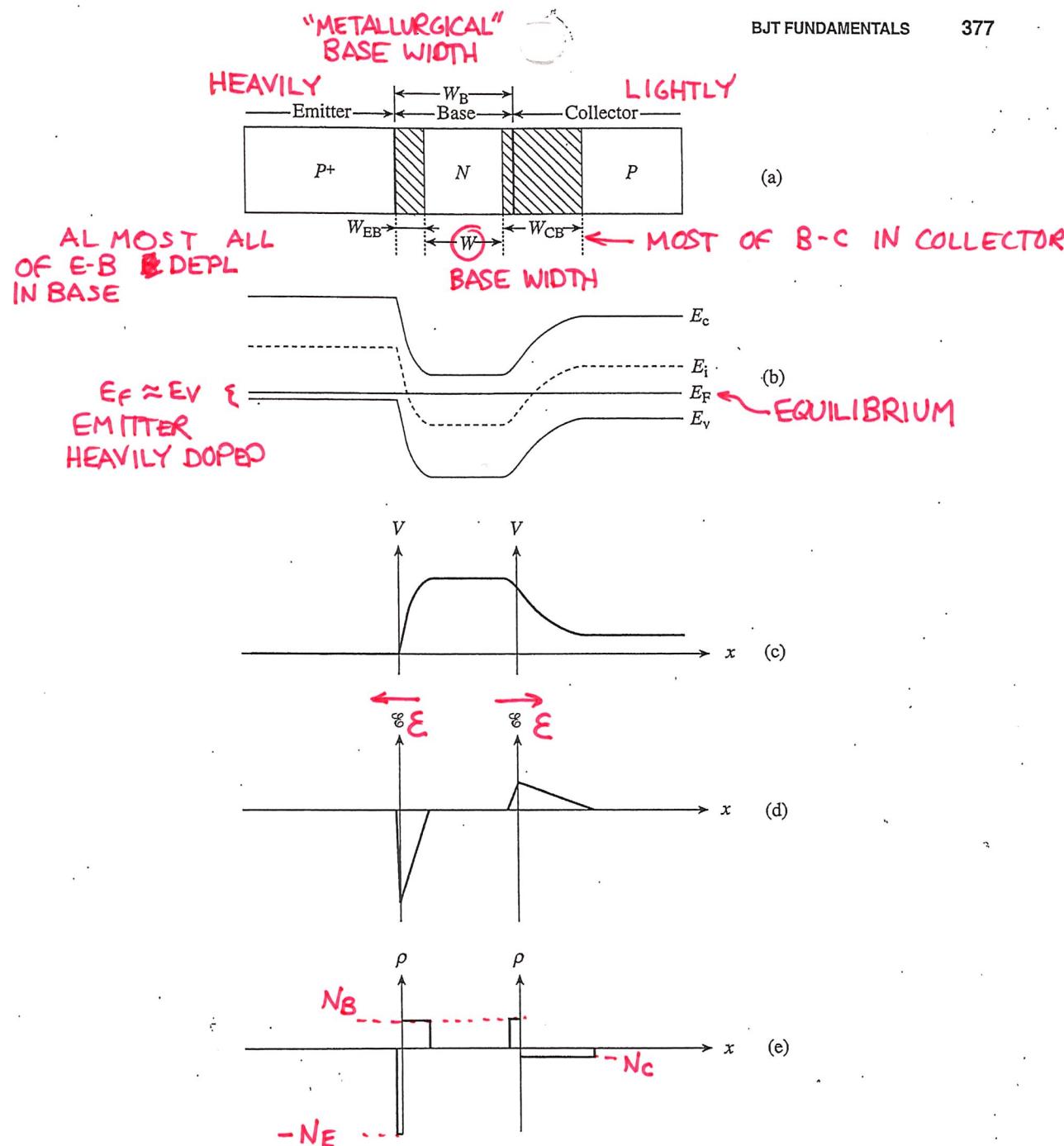


Figure 10.7 Sketches of the electrostatic variables in a *pnp* BJT under equilibrium conditions. (a) Depletion regions, (b) energy band diagram, (c) electrostatic potential, (d) electric field, and (e) charge density. The transistor regions are assumed to be uniformly doped with $N_{AE} \gg N_{DB} > N_{AC}$.

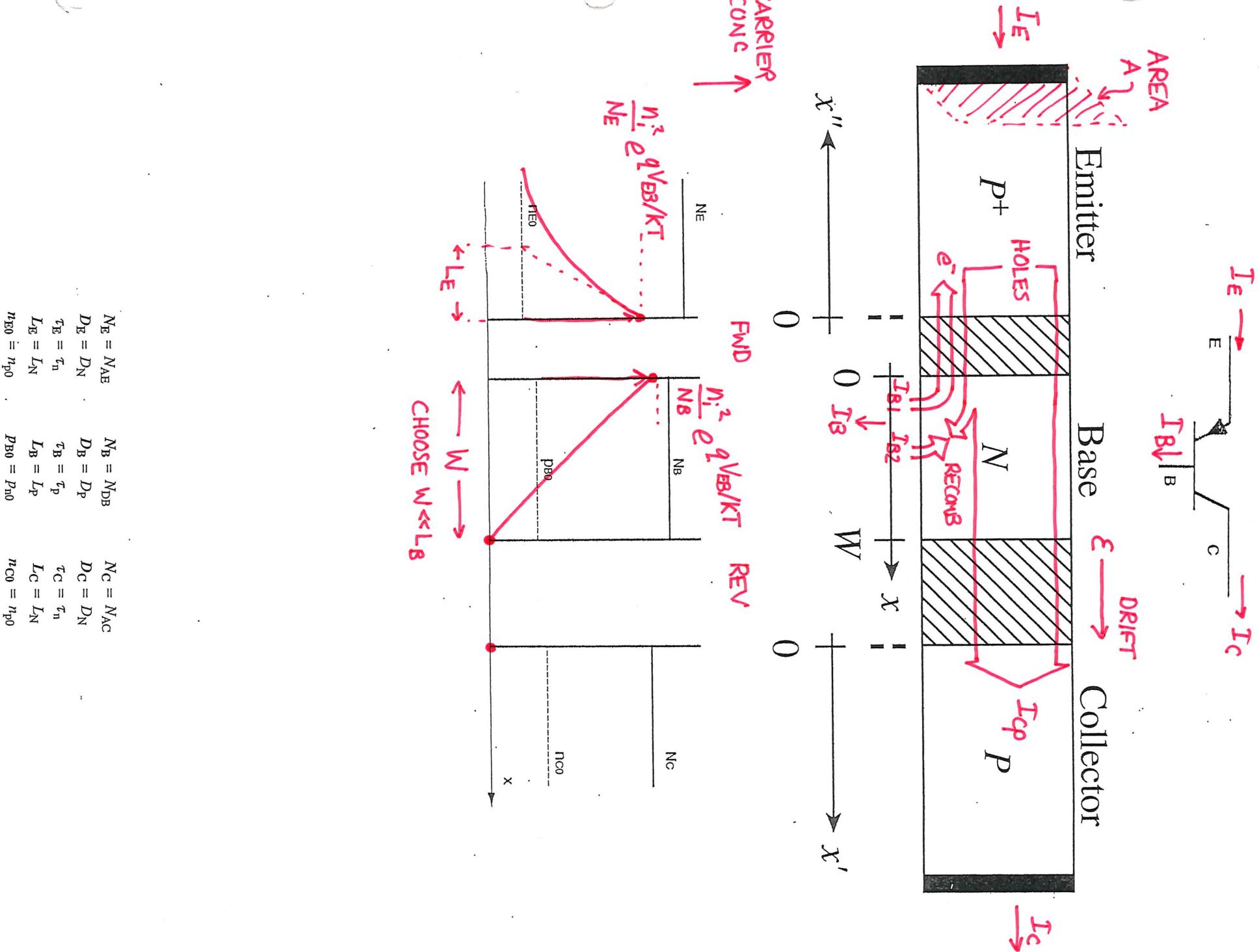


Figure 11.1 Coordinate systems and material parameter symbols (in bold) employed in the ideal transistor analysis.