

## **ECE4904 Lecture 10**

**Finish Ch. 11 BJT topics**

**MOSFET Terminology (Ch. 16)**

**MOSFET Basics (17.1)**

**Construction**

**Qualitative Operation**

**Accumulation - Depletion - Inversion**

**Handouts**

**Ch. 17 MOSFET Construction Figure**

**Accumulation - Depletion - Inversion**

**Ch. 16 MOS Capacitor Figures**

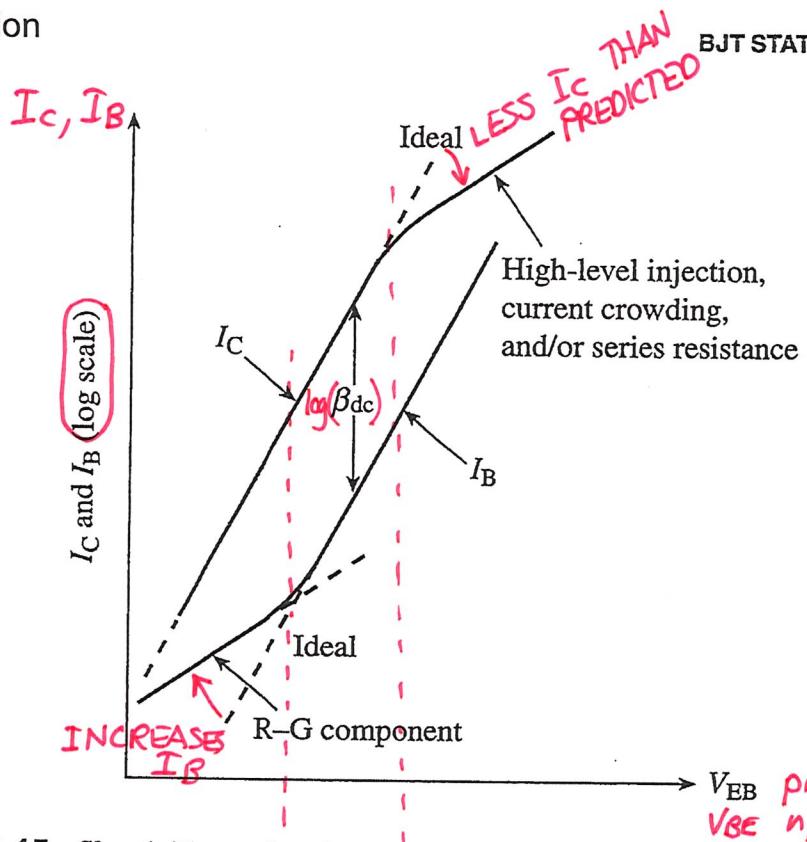
**MOSFET Energy Band Diagram**

**Hand In: HW 4**

**HW 5 (online) due Thu 12/6**

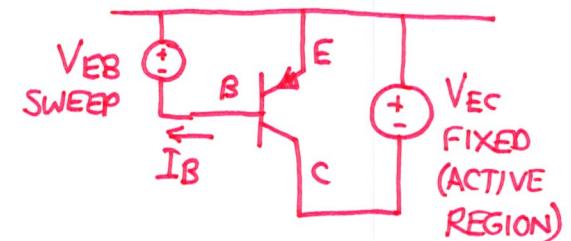
## Nonideal Effects: Real BJT (11.2):

Base width modulation  
Geometrical Effects  
Graded Base  
Gummel Plot



BJT STATIC CHARACTERISTICS

425

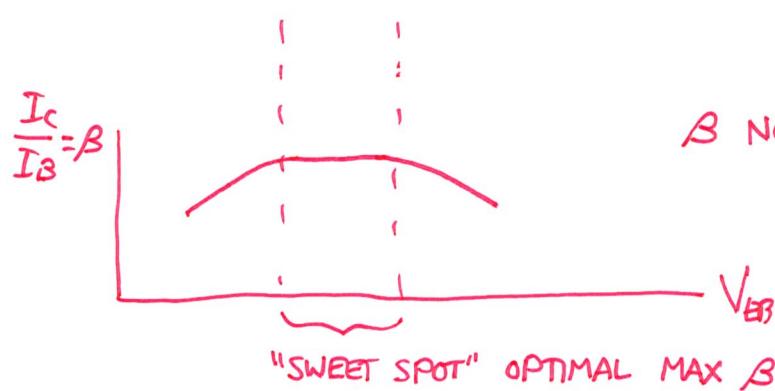


$$\beta = \frac{I_C}{I_B}$$

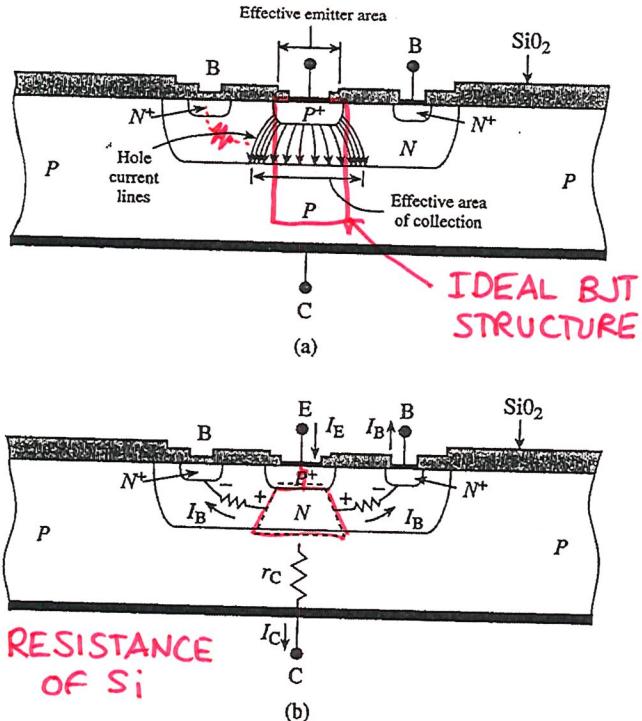
↓ log plot

$$\log(\beta) = \log(I_C) - \log(I_B)$$

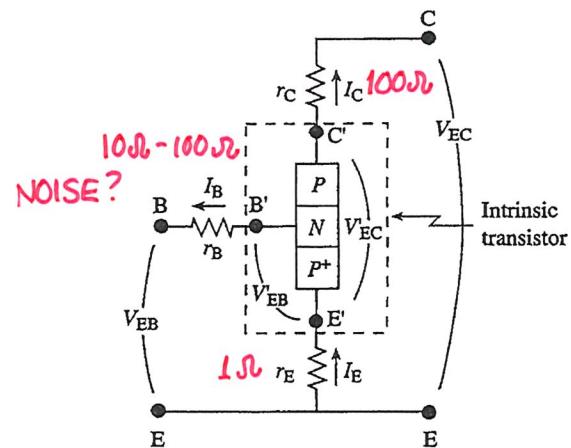
Figure 11.15 Sketch illustrating the usual form and interpretation of the Gummel plot.



~~$$I_C = \beta I_B$$~~

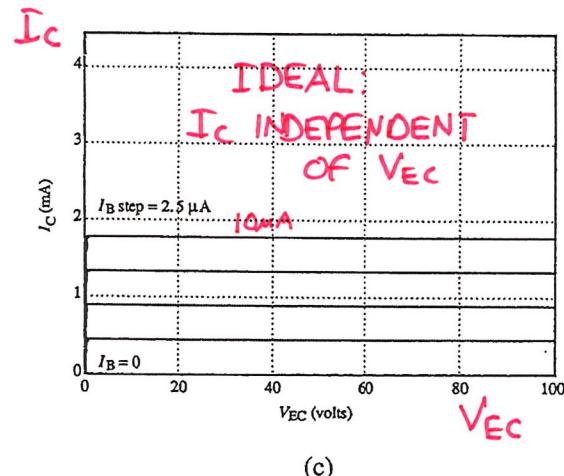


**Figure 11.11** Illustration of geometrical effects in a discrete planar transistor. (a) Current spreading and crowding. (b) Base and collector series resistances. The dashed line region in (b) identifies the “intrinsic transistor,” the “heart” of the device.



**Figure 11.12** BJT equivalent circuit including the emitter ( $r_E$ ), base ( $r_B$ ), and the collector ( $r_C$ ) series resistances.

"BASE WIDTH MODULATION"



APPROX LINEAR  
DEPENDENCE  $I_C \leftrightarrow V_{EC}$

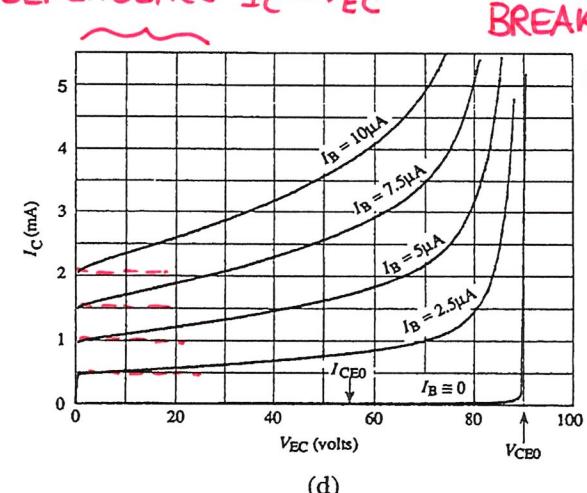


Figure 11.5 Common emitter pnp BJT characteristics: (a) ideal theory and (b) experimental input characteristics; (c) ideal theory and (d) experimental output characteristics. Room temperature data derived from a 2N2605 pnp BJT and recorded employing a Hewlett-Packard 4145B Semiconductor Parameter Analyzer. The theoretical curves were generated assuming  $W = W_B$  and utilizing the computer program constructed for Exercise 11.7.

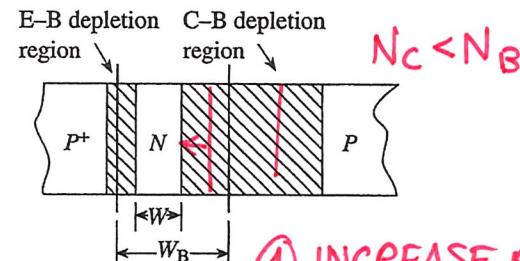
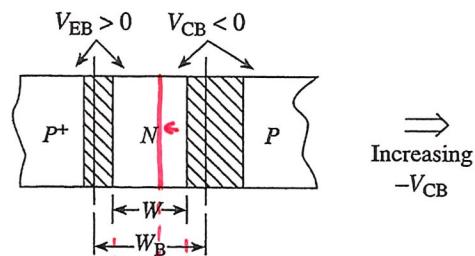
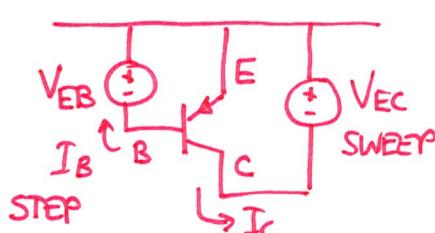
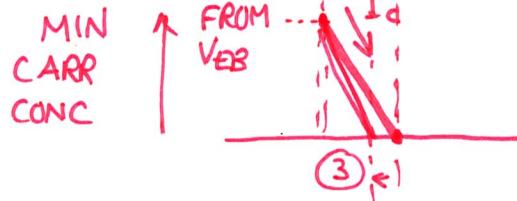


Figure 11.6 Base width modulation. Decrease in  $W$  resulting from an increase in the reverse bias applied across the C-B junction.



- ① INCREASE REVERSE BIAS ON B-C JCT
- ② INCREASE SIZE OF DEPLETION REGION
- ③ STEEPER GRADIENT
- ④  $\Rightarrow$  HIGHER  $I_c$

"GRADED BASE"

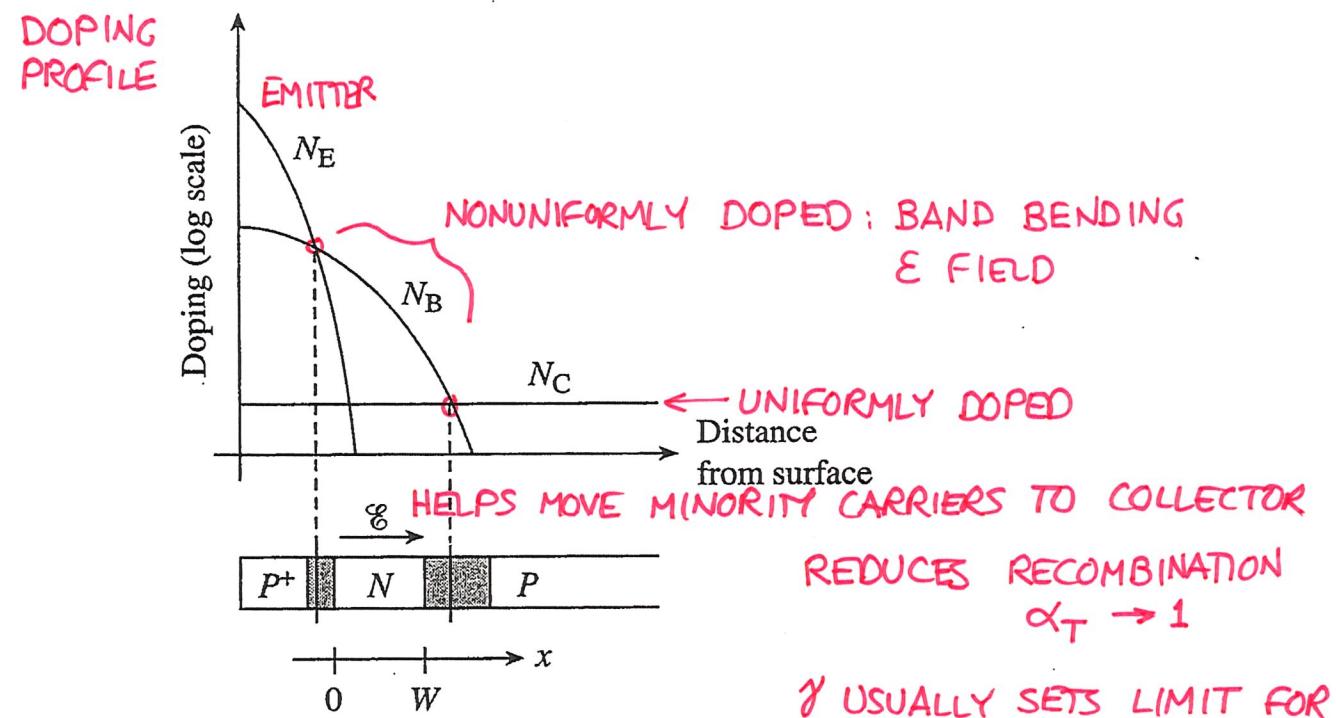


Figure 11.14 Sketch of the doping profiles inside a double-diffused transistor.

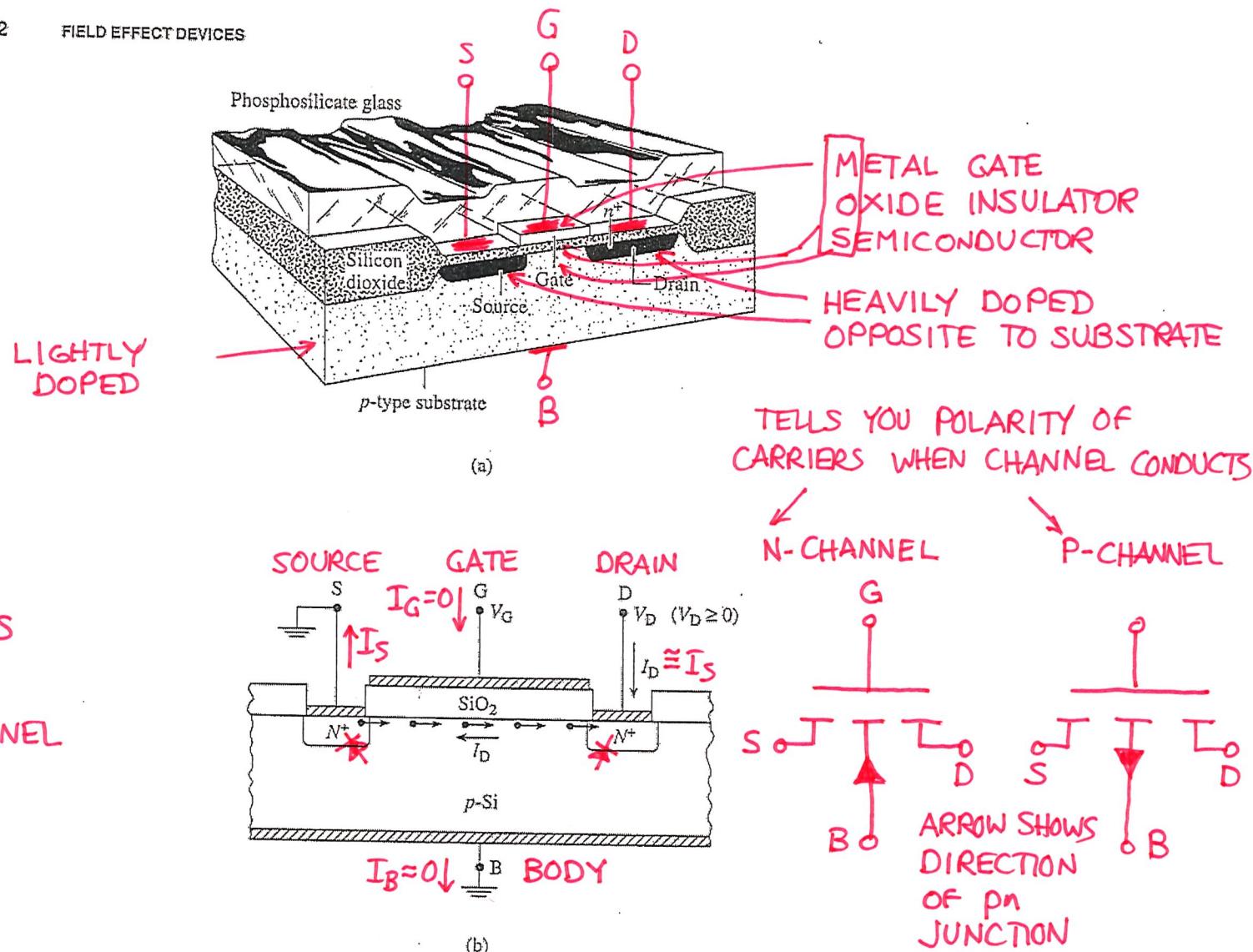
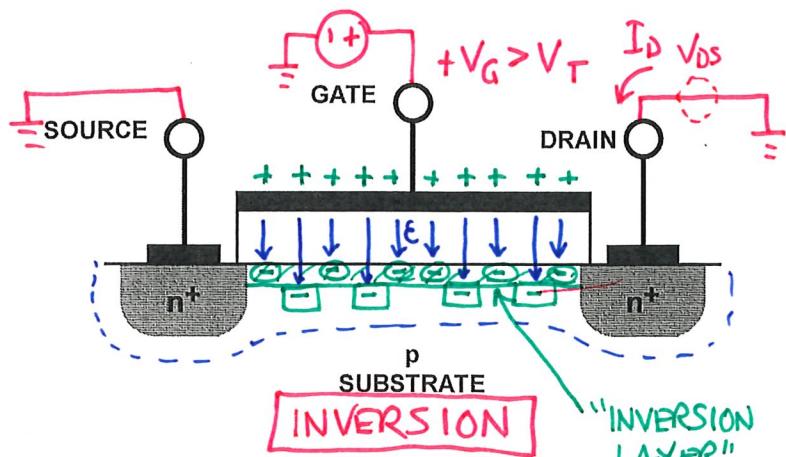


Figure 17.1 The basic MOSFET structure. (a) Idealized cut-away view of a p-bulk (n-channel) MOSFET. (b) Simplified cross-sectional view of the p-bulk (n-channel) structure showing the terminal designations, carrier and current flow directions, and standard biasing conditions. [(a) From Beadle, Tsai, and Plummer<sup>[15]</sup>. Reprinted with permission of AT&T.]

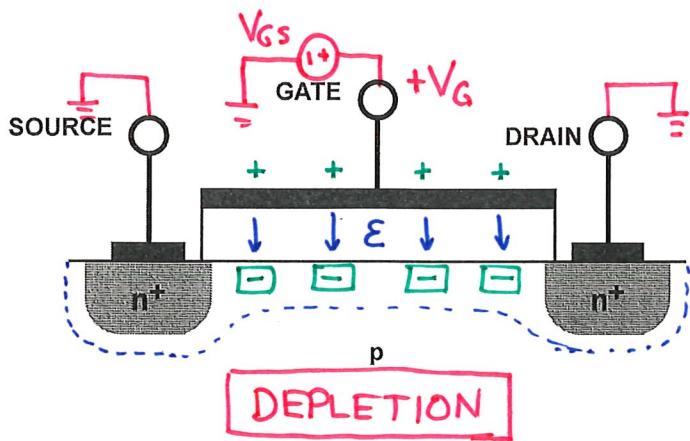


$V_{GS} > V_T$  "THRESHOLD VOLTAGE"

MORE + CHARGE ON GATE  
 $\epsilon$  ATTRACTS MOBILE  $e^-$  TO SURFACE  $-$   
 LAYER OF MOBILE  $e^-$  AT SURFACE

"INVERTED" SENSE OF Si FROM p TO n AT SURFACE

APPLY  $V_{DS} \neq 0$ : CONTINUOUS n-TYPE REGION S  $\rightarrow$  D:  $I_D > 0$

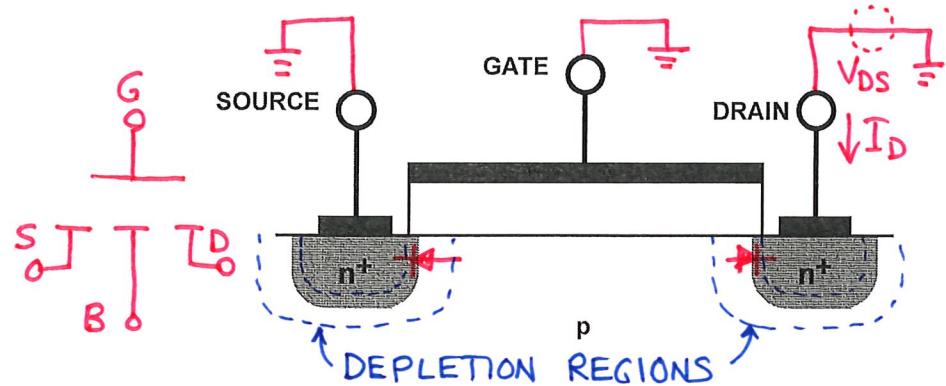


$V_{GS} > 0$

+ CHARGE ON GATE  
 $\epsilon$  FIELD PUSH HOLES AWAY  
 [ ] FIXED NEGATIVE CHARGES "UNCOVERED"

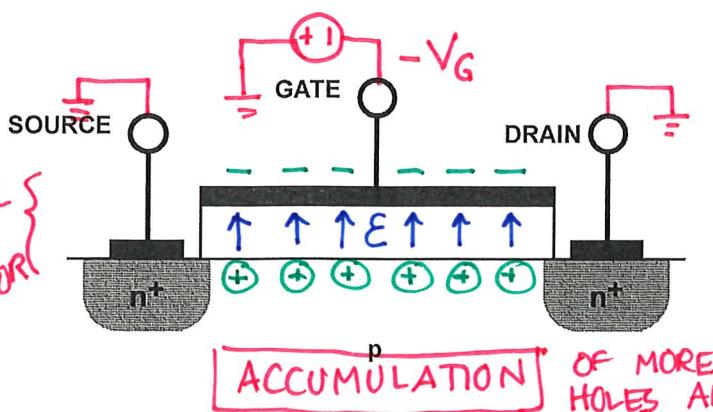
DEPLETION REGION EXTENDS S-D  $I_D = 0$

BUT: DEPLETED S-D OF "WRONG" CARRIERS



$V_{GS} = 0$

DRAIN-TO-SOURCE PATH BACK-TO-BACK DIODES EVEN IF  $V_{DS} \neq 0$   
 ONE DIODE REV BIAS  $\Rightarrow I_D = 0$  "OFF"



$V_{GS} < 0$

- CHARGE ON GATE  
 $\epsilon$  FIELD IN GATE OXIDE (INSULATOR)  
 (+) MOBILE HOLES PILE UP ON SURFACE; BALANCE Q EVEN MORE p-TYPE!

$I_D = 0$

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ACCUMULATION - DEPLETION - INVERSION

PARALLEZ PLATE CAPACITOR!

## ASSUMPTIONS

NEED: ENERGY  
BAND DIAGRAM  
ALONG  $x$   
DIMENSION

OXIDE  
THICKNESS  
 $t_{ox}$

SURFACE  
--- 0 ---  
1-D  
STRUCTURE

SUBSTRATE  
UNIFORMLY  
DOPED

THICK, CONDUCTIVE;  
SAME  $V_G$  EVERYWHERE

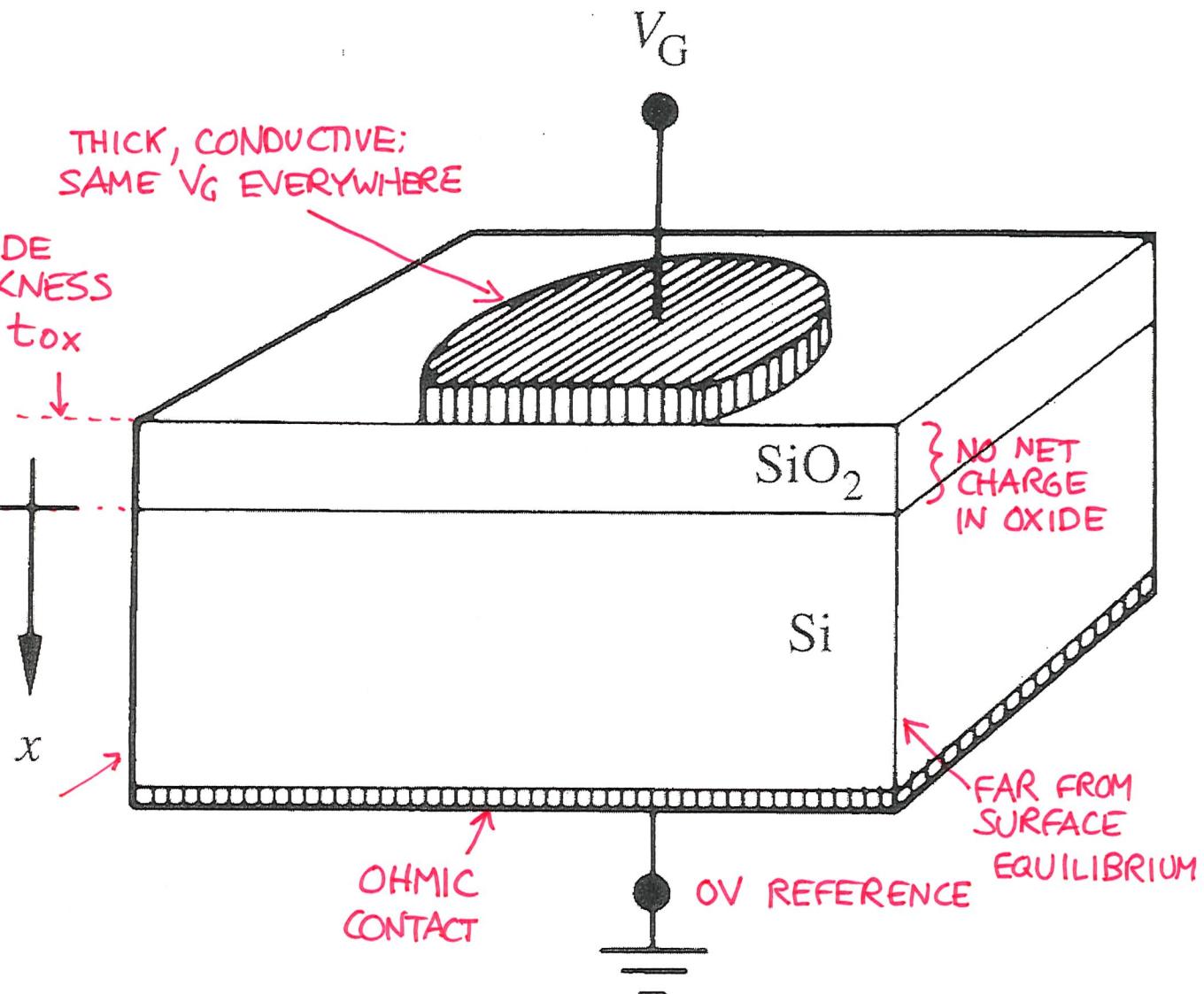


Figure 16.1 The metal-oxide-semiconductor capacitor.

$\Phi_M$  METAL  
WORKFUNCTION  $e^-$  FROM  
 $E_F \uparrow$

FOR SIMPLICITY  
ASSUME  $\Phi_M = \Phi_S$

EQUILIBRIUM  
 $V_G = 0$

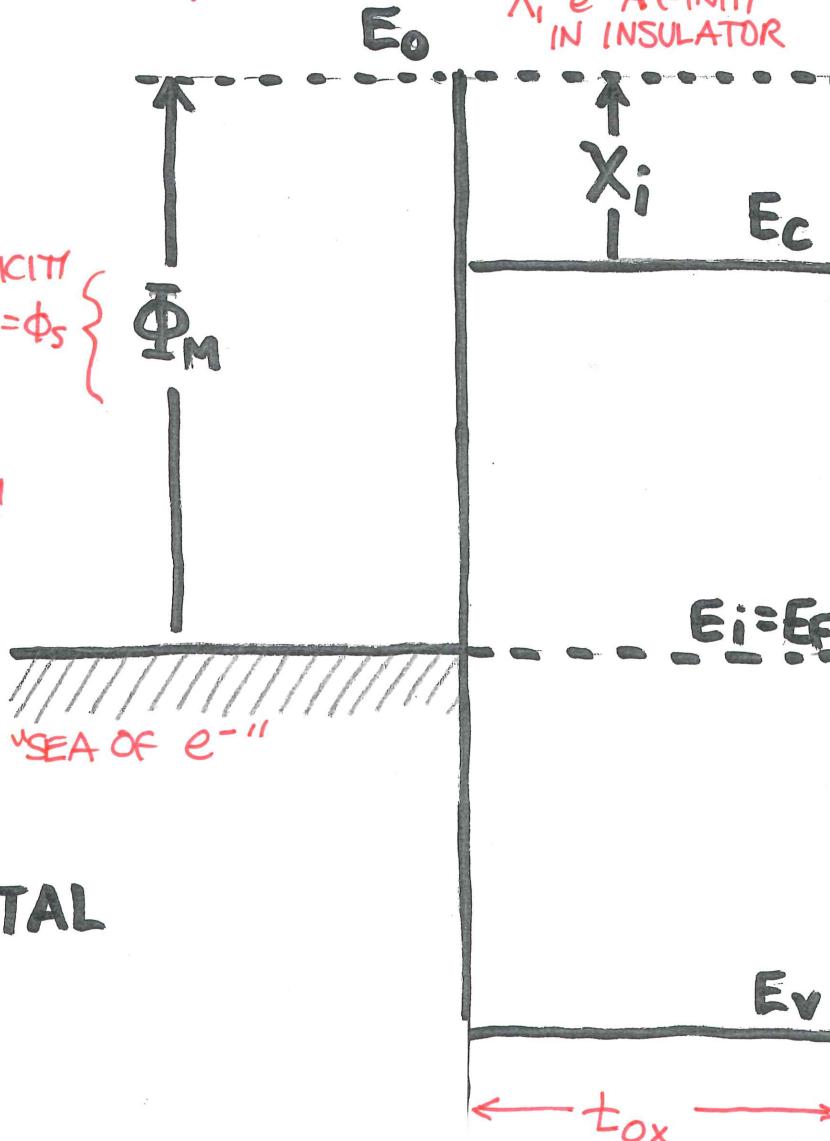
FLAT  $\{ E_F$

METAL

MODEL AS INTRINSIC  
WITH BIG  $E_G$

INSULATOR

$X_i$   $e^-$  AFFINITY  
IN INSULATOR



$X$   $e^-$  AFFINITY  $E_C \uparrow$  OUT

$\Phi_S$  SEMICONDUCTOR  
WORK FUNCTION  $E_F \uparrow$  OUT

INCREASING  
 $e^-$  ENERGY

"VACUUM LEVEL"  
COMPLETELY REMOVE  
 $e^-$  FROM MATERIAL

(DOPED  
P TYPE)

SEMICONDUCTOR

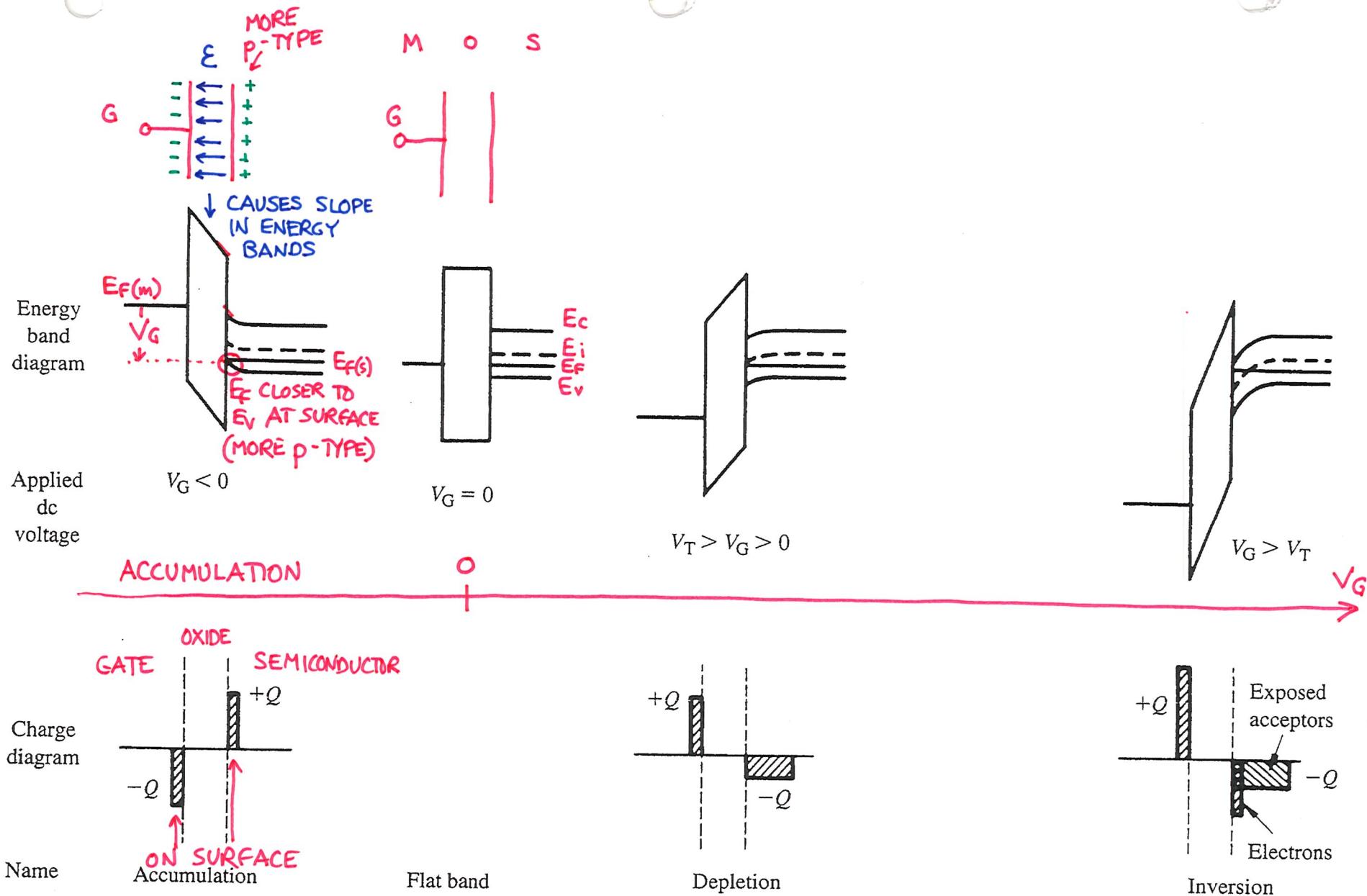


Figure 16.6 Energy band and block charge diagrams for a p-type device under flat band, accumulation, depletion, and inversion conditions.