ECE4904 Lecture 4

Energy Band Diagram Review (3.1.5)
- E_F flat in equilibrium

Carrier Motion: Review Drift (3.1), Diffusion (3.2)
- Total current expression

Nonuniformly doped semiconductor (3.2.4)
- "Band bending" (Text Fig. 3.14)
- Slope of energy bands: E field
- Einstein relationship

Recombination / Generation (3.3)
- Text Fig. 3.15

Basics of Fabrication
- Text Figs. 4.2, 4, 5, 11, 12, 13, 15

Handouts
- Text Figures

DRIFT DIFF

$$\mathbf{J}_P = \mathbf{J}_{P|\text{drift}} + \mathbf{J}_{P|\text{diff}} = q\mu_p p\mathscr{E} - qD_P \nabla p \tag{3.18a}$$

HOLE

$\updownarrow$ drift $\updownarrow$ diffusion

$$\mathbf{J}_N = \mathbf{J}_{N|\text{drift}} + \mathbf{J}_{N|\text{diff}} = q\mu_n n\mathscr{E} + qD_N \nabla n \tag{3.18b}$$

e^-

$$\boxed{\mathbf{J} = \underbrace{\mathbf{J}_N}_{e^- \text{ IN CONDUCTION BAND}} + \underbrace{\mathbf{J}_P}_{\text{HOLES IN VALENCE BAND}}} \tag{3.19}$$

AT EQUILIBRIUM: MUST HAVE E_F FLAT

NO NET CURRENT FLOWING BUT...

$J_N|_{drift} \neq 0$ AND $J_N|_{diff} \neq 0$

MUST CANCEL IN EQUILIBRIUM $J_N|_{drift} + J_N|_{diff} = 0$ [1]

$$q\mu_n n \mathcal{E} + qD_N \frac{dn}{dx} = 0 \quad [2]$$

DRIFT: $\mathcal{E} = \frac{-dV}{dx}$ (DEF'N OF $\mathcal{E}$ FIELD) [3]

FROM ENERGY BAND DIAGRAM

$$V = \frac{-1}{q} E_i \quad [4]$$

SUB [4] INTO [3] FOR $\mathcal{E}$ FIELD

$\mathcal{E} = \frac{1}{q}\frac{dE_i}{dx}$ } STEEPER SLOPE E_i HIGHER $\mathcal{E}$ FIELD [5]

DIFFUSION:

$$n = n_i e^{(E_F-E_i)/kT} \quad [6]$$

GRADIENT IN 1-D ⇒ SLOPE d/dx

$$\frac{dn}{dx} = \frac{-n_i}{kT} e^{(E_F-E_i)/kT} \frac{dE_i}{dx} \qquad \underbrace{\cancel{\frac{dE_F}{dx}} = 0}_{\text{EQUILIBRIUM}} \quad [7]$$

MULTIPLY ~~FOR~~ TOP, BOTTOM BY q

$$\frac{dn}{dx} = \frac{-q}{kT} \underbrace{n_i e^{(E_F-E_i)/kT}}_{n} \underbrace{\frac{1}{q}\frac{dE_i}{dx}}_{\mathcal{E}\text{ FROM [5]}} = \frac{-q}{kT} n\mathcal{E} \quad [8]$$

SUB [8] [5] INTO [2]

$$\underbrace{\cancel{q}\mu_n \cancel{n\mathcal{E}}}_{\text{DRIFT}} = \underbrace{\cancel{q} D_N \frac{q}{kT} \cancel{n\mathcal{E}}}_{\text{DIFF}} \qquad \boxed{\frac{D_n}{\mu_n} = \frac{kT}{q}}$$

"EINSTEIN RELATIONSHIP"

$E_F - E_i = kT \ln\left(\frac{n}{n_i}\right)$

AT x=0

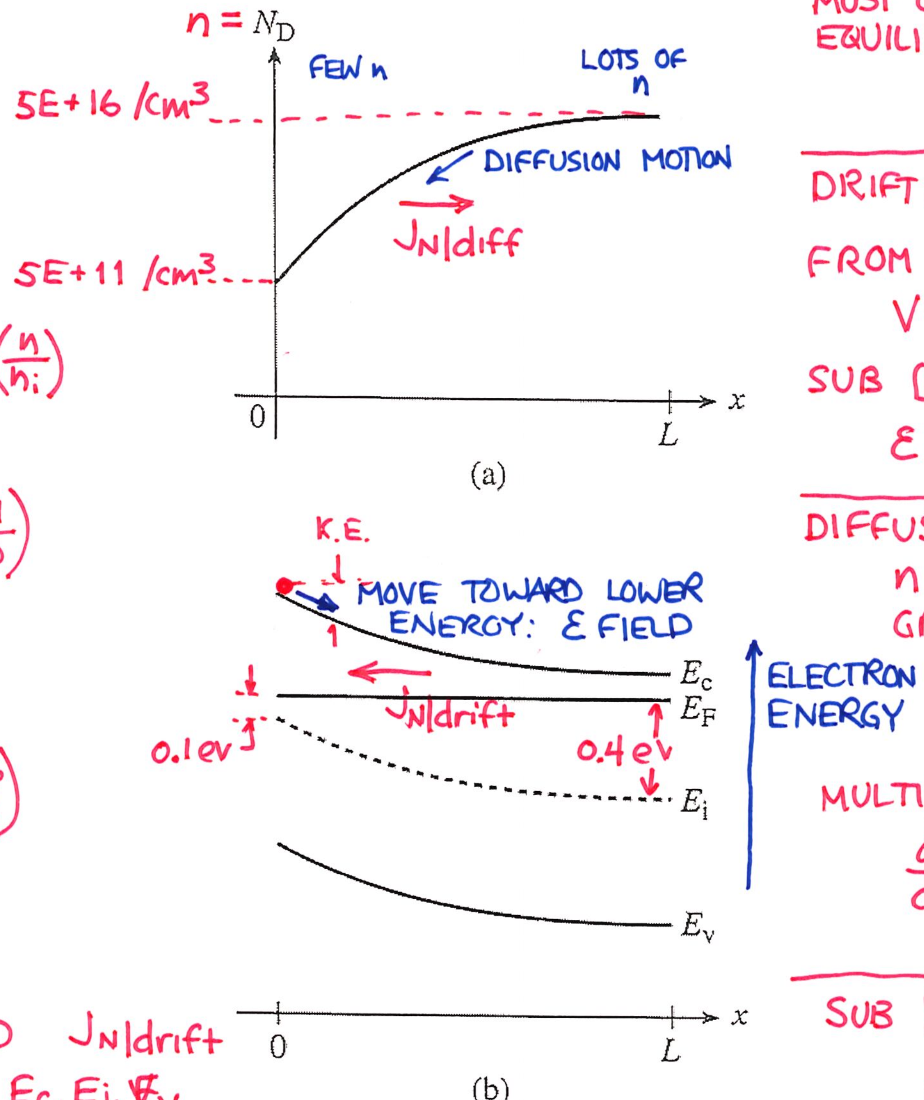
$.0259 \ln\left(\frac{5E+11}{1E+10}\right)$

$= 0.1 eV$

AT x=L

$.0259 \ln\left(\frac{5E+16}{1E+10}\right)$

$= 0.4 eV$



⇒ $\mathcal{E}$ FIELD $J_N|_{drift}$

SLOPE FOR E_c, E_i, E_v

Figure 3.14 Nonuniformly doped semiconductor: (a) assumed doping variation with position; (b) corresponding equilibrium energy band diagram.

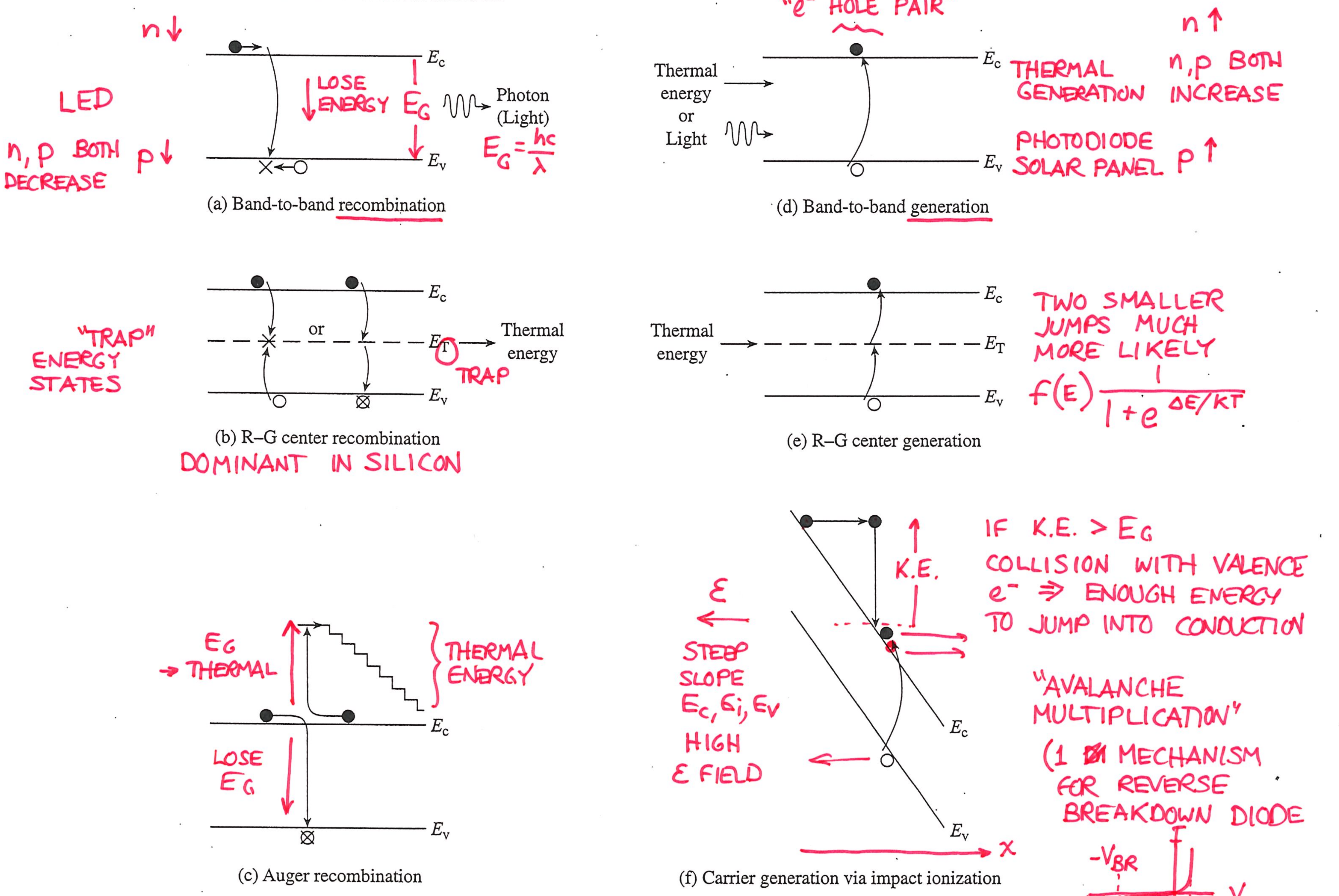


Figure 3.15 Energy band visualization of recombination and generation processes.

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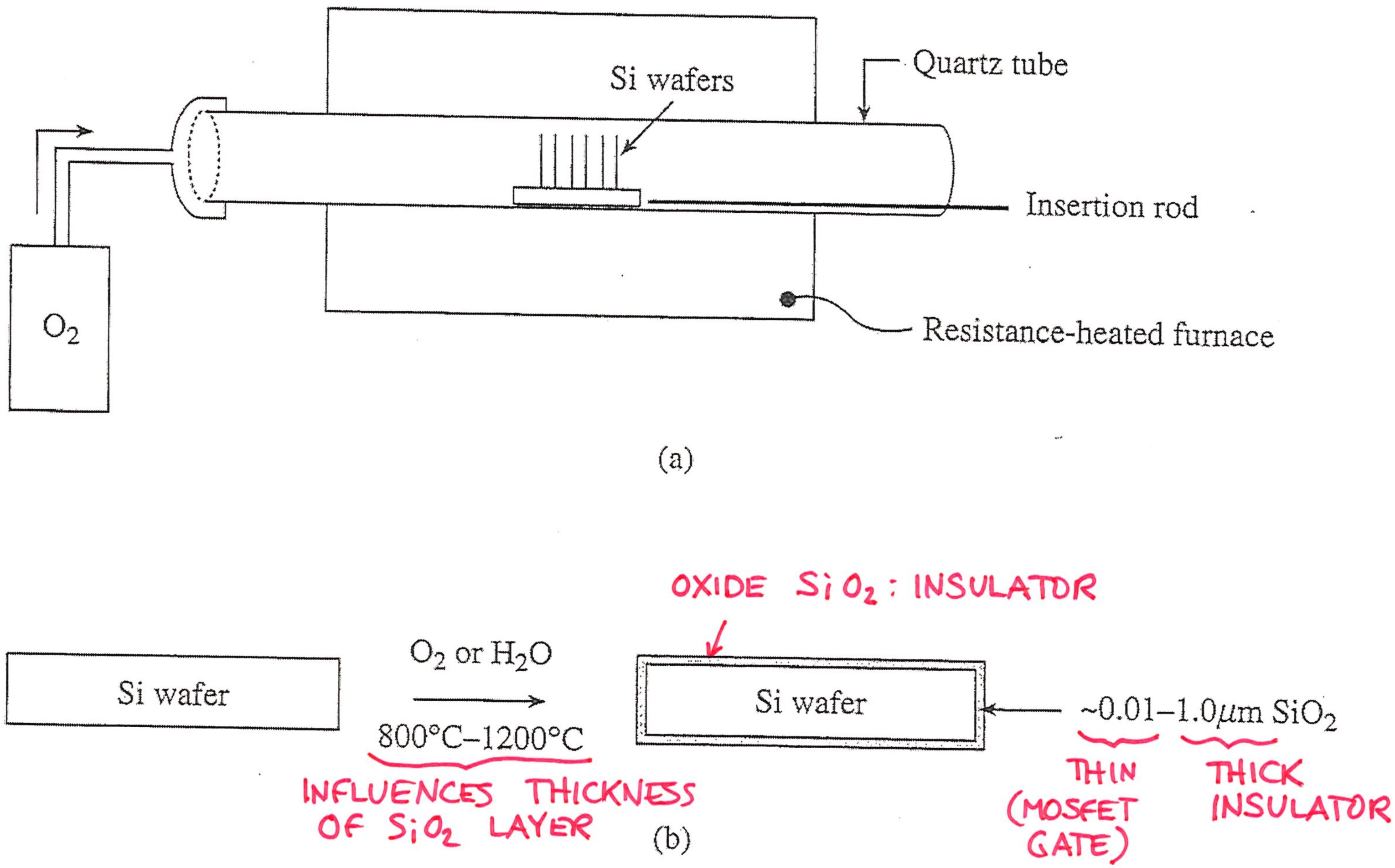
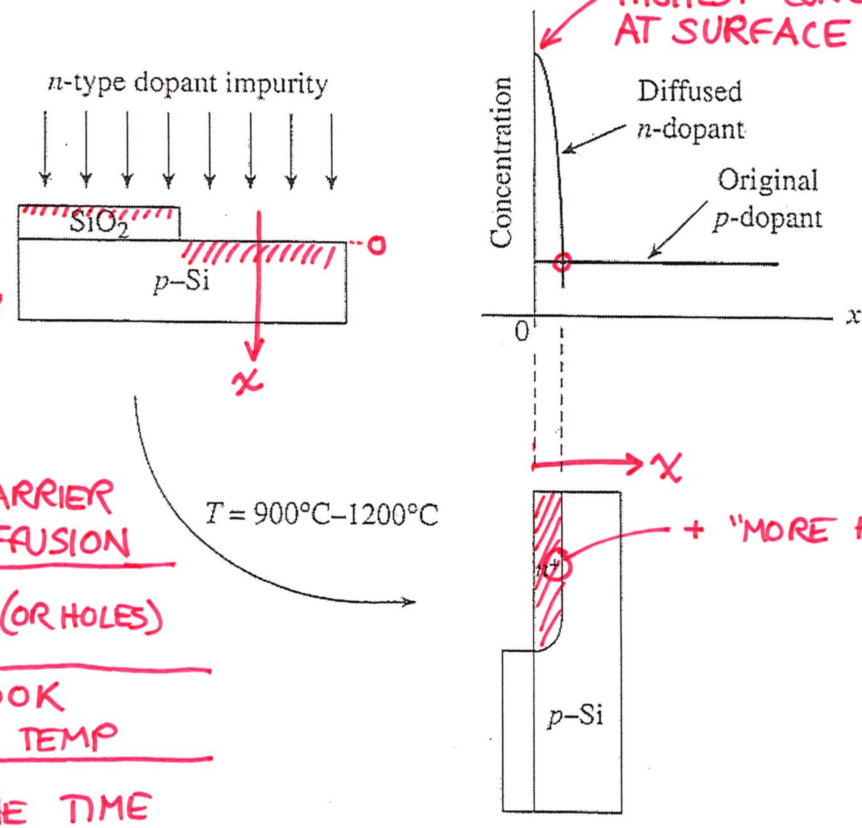


Figure 4.2 (a) Simplified schematic illustration of an oxidation system. (b) Short pictorial description of the oxidation process.

OXIDE: COVERS (PROTECTS) AREAS YOU DON'T WANT DOPED WITH IMPURITY ATOMS

Si WAFER GROWN WITH p-TYPE IMPURITIES



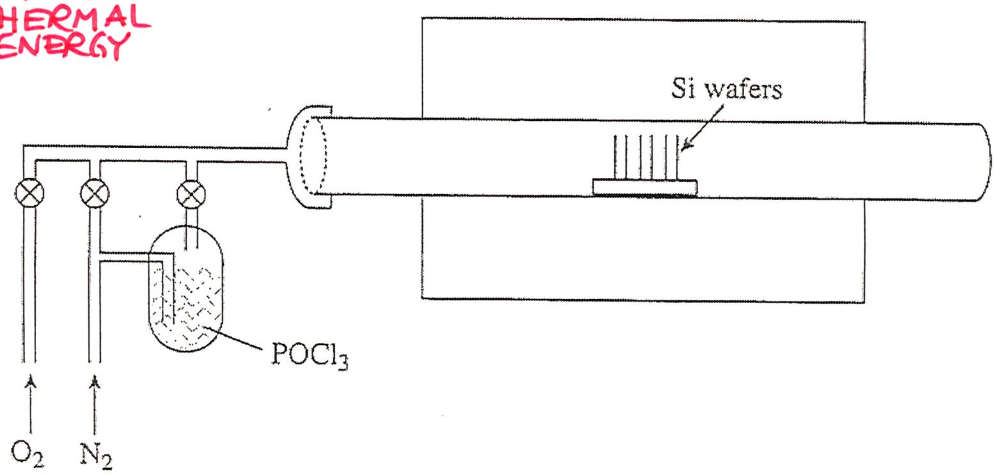
HIGHEST CONCENTRATION AT SURFACE

RELATED TO "DOPING PROFILE"

+ "MORE HEAVILY DOPED

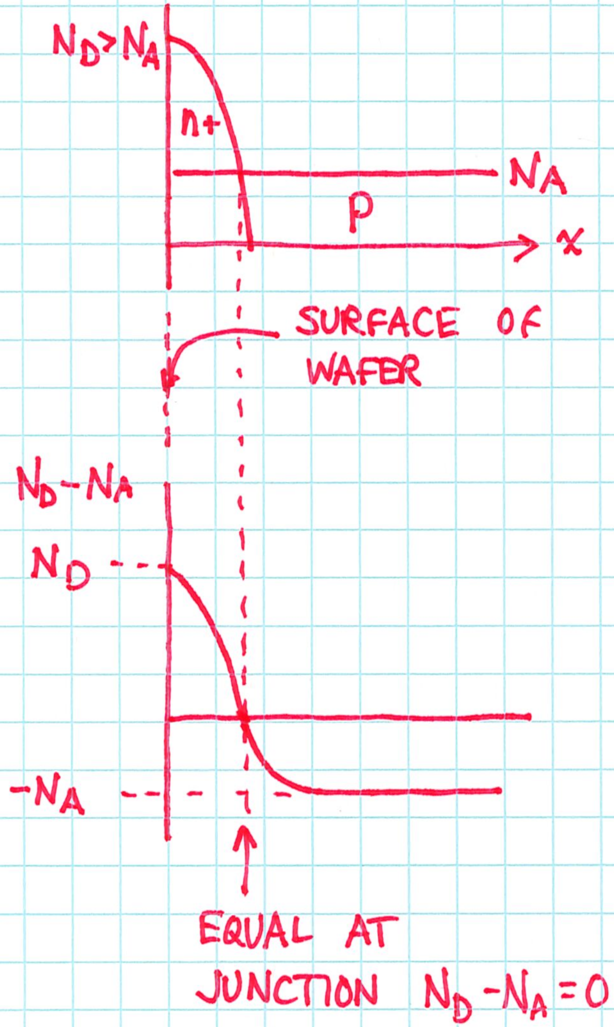
	* "SOLID-STATE DIFFUSION" *	CARRIER DIFFUSION
WHAT IS MOVING?	DOPANT ATOMS DISPLACING Si	e^- (OR HOLES)
TEMP	900°C - 1200°C 1200 K - 1500 K	> 100 K ROOM TEMP
WHEN	ONCE, AT DEVICE FABRICATION	ALL THE TIME
WHY	DOPING	RANDOM THERMAL ENERGY

Figure 4.4 The basic diffusion* process.



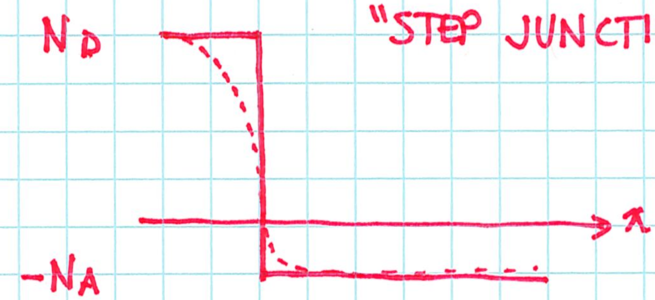
FABRICATION: "DOPING PROFILE" PLOT OF $N_D - N_A$ VS. x

DISTANCE INTO Si FROM SURFACE



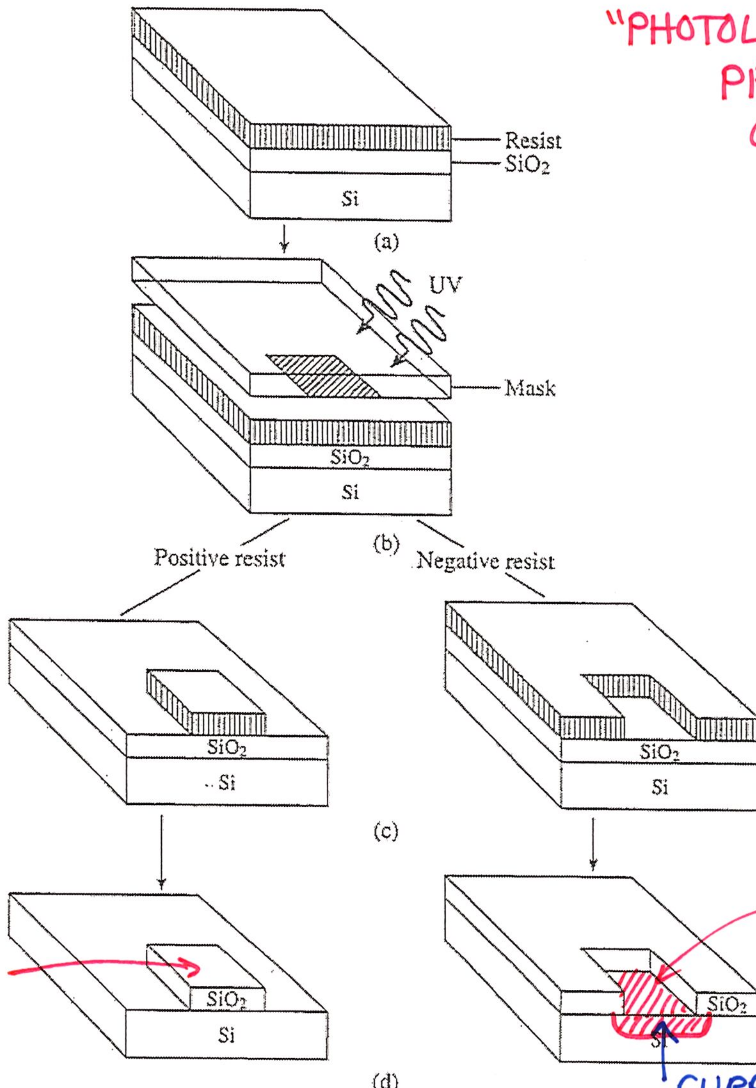
APPROXIMATION NEAR JUNCTION

"STEP JUNCTION"



"LINEARLY GRADED" JUNCTION

"PHOTOLITHOGRAPHY"
PRINTING PATTERNS
ON Si WAFER

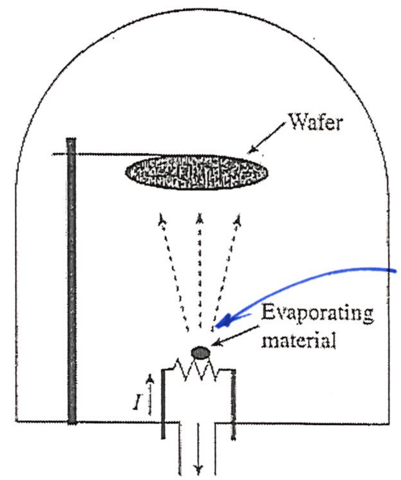


MOSFET
GATE

JUNCTION AREA

CURRENT FLOW PERPENDICULAR
TO SURFACE

Figure 4.11 Major steps in the lithography process: (a) Application of resist; (b) resist exposure through a mask; (c) after development; (d) after oxide etching and resist removal. (From Jaeger[8], © 1988 by Addison-Wesley Publishing Co., Inc. Reprinted by permission of the publisher.)



ALUMINUM: DEPOSIT
CONDUCTORS

Figure 4.12 Hot-filament evaporation.

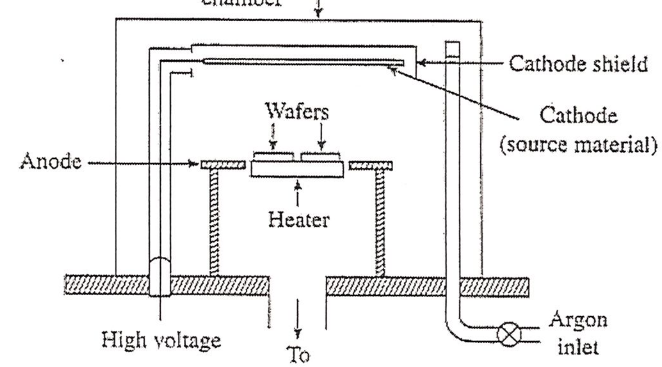


Figure 4.13 Schematic of a d.c. sputtering system. The source material covers the cathode while the wafer is mounted on the system anode. (From Jaeger[8], © 1988 by Addison-Wesley Publishing Co., Inc. Reprinted by permission of the publisher.)

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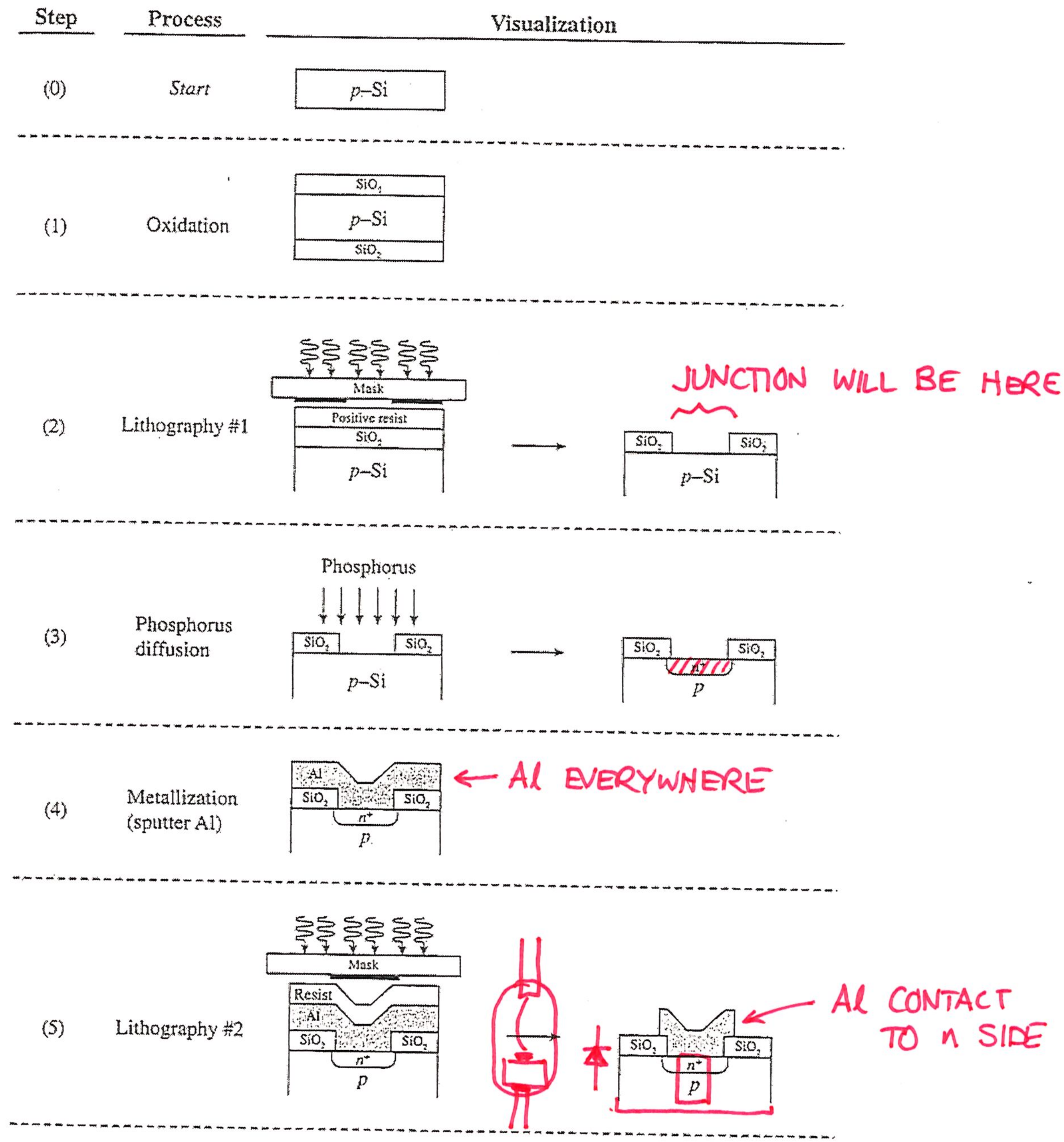

Figure 4.15 Graphical summary of the major processing steps in the formation of a *pn* junction diode.

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