

ECE4904 Lecture 13 (12/10/18)

MOSFET Dynamic (Ch. 17.2, 3)

Gate capacitance: CMOS Inverter delay

Fundamental Limit to CMOS Inverter speed?

MOSFET V-I Characteristics

Small signal model (Fig. 17.12)

pn Junction Dynamic: Small signal model (Fig. 7.3)

SPICE Modeling

MOS-BJT Comparison (handout)

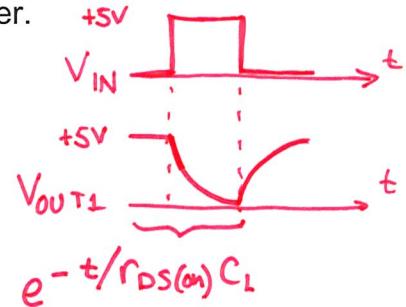
Second Order Effects

Subthreshold conduction (Fig. 17.11)

All late work due by 5pm Friday Dec 14th

Find the propagation delay for a square wave from V_{IN} to V_{OUT1} through a CMOS inverter constructed from MC14007 MOSFETs.

The load driven by the inverter is the input of another CMOS inverter.



$$e^{-t/r_{DS(on)}C_L}$$

$$r_{DS(on)} = \frac{1}{\bar{\mu} C_0 \frac{Z}{L} (V_G - V_T)}$$

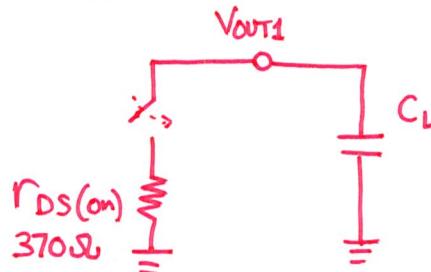
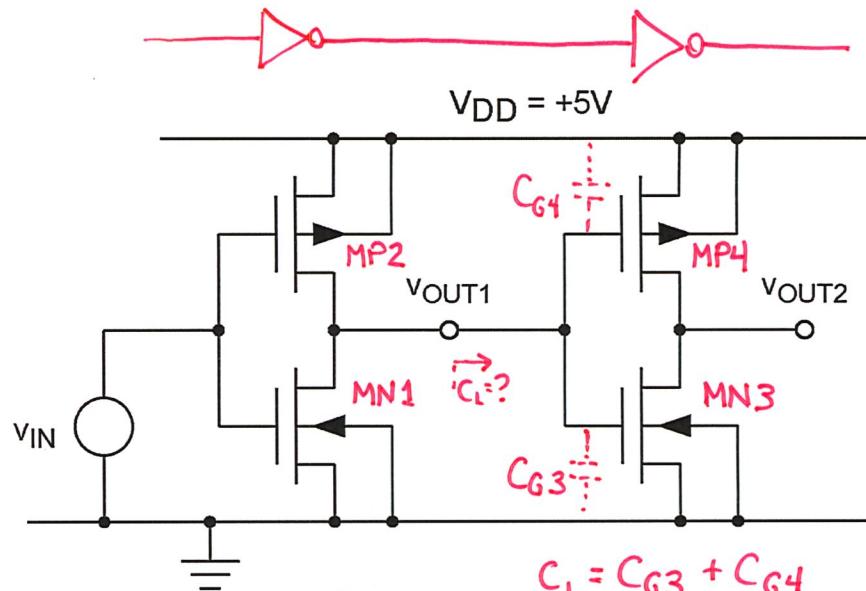
$$= \left(600 \frac{\text{cm}^2}{\text{V}\cdot\text{s}}\right) \left(4.31 \times 10^{-8} \frac{\text{F}}{\text{cm}^2}\right) \left(\frac{300}{10}\right) (5 - 1.5)$$

$$r_{DS(on)} = 370 \Omega$$

$$\tau = r_{DS(on)} C_L$$

$$(370\Omega)(5.17 \text{ pF}) = \underbrace{1.9 \text{ nsec}}$$

ESTIMATED APPROXIMATION



FOR C_{G3}

$$C_{G3} = \underbrace{C_0}_{\frac{C}{\text{AREA}}} W L$$

$$= 4.31 \times 10^{-8} \frac{\text{F}}{\text{cm}^2}$$

$$= 0.43 \frac{\text{fF}}{\text{mm}^2} (300 \text{ mm})(10 \text{ mm}) = 1.29 \text{ pF}$$

$$C_{G4} = 0.43 \frac{\text{fF}}{\text{mm}^2} (900 \text{ nm})(10 \text{ nm}) = \cancel{5.17 \text{ pF}} \quad 3.88 \text{ pF}$$

$$C_L \text{ TOTAL} = C_{G3} + C_{G4} = 5.17 \text{ pF}$$

C_0 FROM OXIDE THICKNESS

$$C_0 = \frac{K_0 \epsilon_0}{X_0}$$

$$\frac{(3.9)(8.85 \times 10^{-14} \text{ F/cm})}{(8 \times 10^{-6} \text{ cm})}$$

$$C_0 = 4.31 \times 10^{-8} \frac{\text{F}}{\text{cm}^2}$$

$$1 \mu\text{m} = 10^{-6} \text{ cm}$$

MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

MC14007UB

**Dual Complementary Pair
Plus Inverter**

The MC14007UB multi-purpose device consists of three N-channel and three P-channel enhancement mode devices packaged to provide access to each device. These versatile parts are useful in inverter circuits, pulse-shapers, linear amplifiers, high input impedance amplifiers, threshold detectors, transmission gating, and functional gating.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4007A or CD4007UB
- This device has 2 outputs without ESD Protection. Anti-static precautions must be taken.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	- 0.5 to + 18.0	V
V _{in} , V _{out}	Input or Output Voltage (DC or Transient)	- 0.5 to V _{DD} + 0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P _D	Power Dissipation, per Package†	500	mW
T _{stg}	Storage Temperature	- 65 to + 150	°C
T _L	Lead Temperature (8-Second Soldering)	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

† Temperature Derating:

Plastic "P and D/DW" Packages: - 7.0 mW/°C From 65°C To 125°C

Ceramic "L" Packages: - 12 mW/°C From 100°C To 125°C



L SUFFIX
CERAMIC
CASE 632



P SUFFIX
PLASTIC
CASE 646



D SUFFIX
SOIC
CASE 751A

ORDERING INFORMATION

MC14XXXUBCP Plastic
MC14XXXUBCL Ceramic
MC14XXXUBD SOIC

T_A = - 55° to 125°C for all packages.

PIN ASSIGNMENT

D-PB	1	14	V _{DD}
S-PB	2	13	D-PA
GATEB	3	12	OUTC
S-NB	4	11	S-PC
D-NB	5	10	GATEC
GATEA	6	9	S-NC
V _{SS}	7	8	D-NA

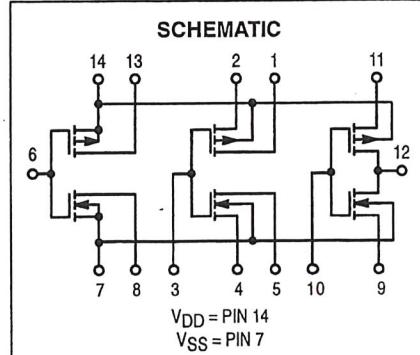
D = DRAIN
S = SOURCE

OXIDE THICKNESS $X_0 = 0.08 \mu\text{m}$ } 8E-6 cm

PARAMETER

N-ch P-ch

SURFACE MOBILITY	$\bar{\mu}$	600	200	$\frac{\text{cm}^2}{\text{V}\cdot\text{sec}}$
THRESHOLD VOLTAGE	V _T	+ 1.5	- 1.5	V
WIDTH LENGTH	$\frac{Z}{L}$	300	900	μm
		10	10	L = 10 μm



WHY ARE C_{G3} , C_{G4} IN PARALLEL?

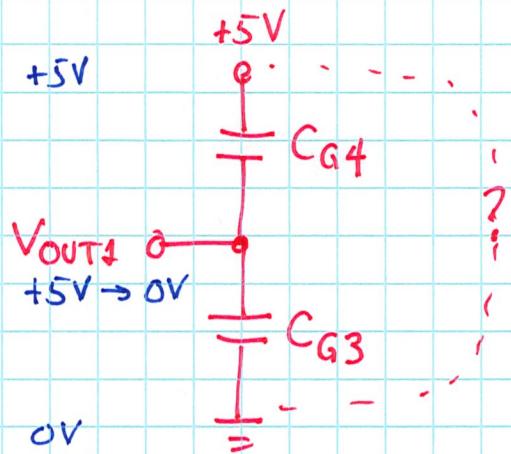
$$I = C \frac{dV}{dt}$$

CHANGE IN
VOLTAGE IS
WHAT MATTERS

WHAT IS CHARGE NEEDED BY EACH CAP?

	C_{G4}	C_{G3}
START	0	5V
FINISH	5V	0

} BOTH SEE ΔV OF 5V



Improving speed of CMOS inverter?

HOW TO REDUCE $\tau = r_{DS(on)} C_L$?

$$r_{DS(on)} = \frac{1}{\bar{\mu} C_0 \frac{Z}{L} (V_G - V_T)}$$

$$C_L = C_0 Z L$$

$$r_{DS(on)} E_L = \frac{\cancel{\bar{\mu}} \cancel{Z} L}{\cancel{\bar{\mu}} \cancel{Z} \frac{L}{L} (V_G - V_T)}$$

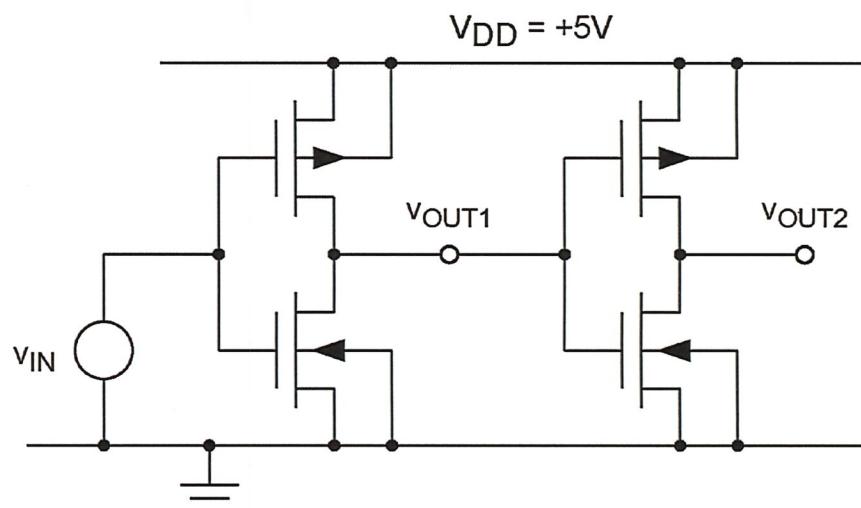
$$r_{DS(on)} C_L \approx \frac{L^2}{\bar{\mu} (V_G - V_T)} \quad \left. \right\} \text{SHORTER } L \checkmark$$

HIGHER $\bar{\mu}$
(n-CH) DRIVE $V_G \uparrow$

REDUCE V_T ? BUT... SUBTHRESHOLD CURRENT...

→ ✓ IMPROVE SPEED

✗ INCREASES STATIC POWER



I_D
LOG SCALE

SUBTHRESHOLD CURRENT $1nA$

$(1nA)(1E+9 \text{ MOSFET}) = 1A$

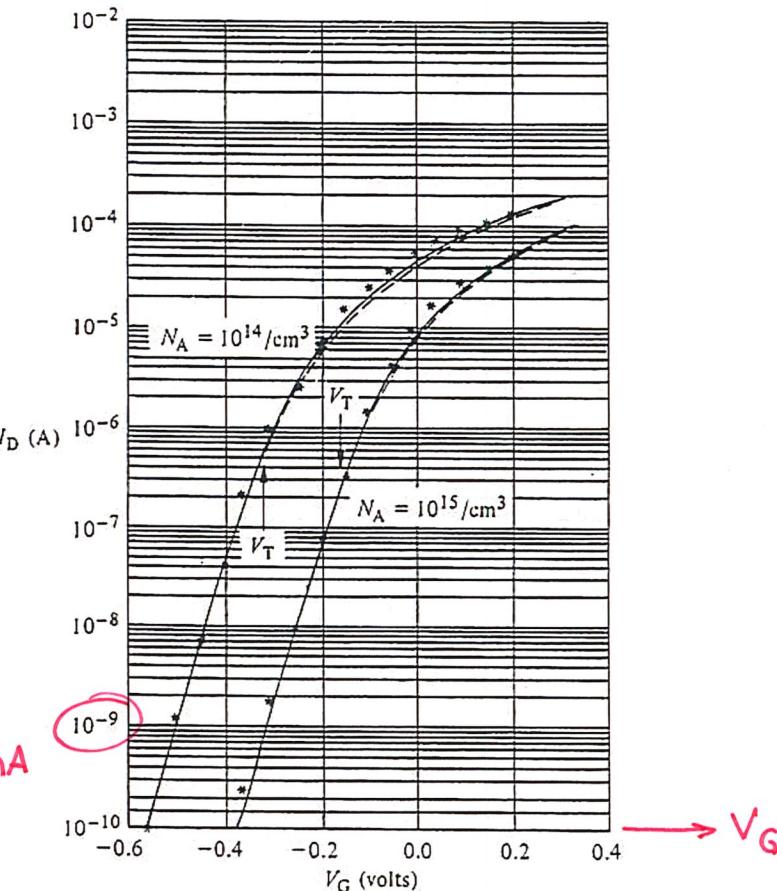
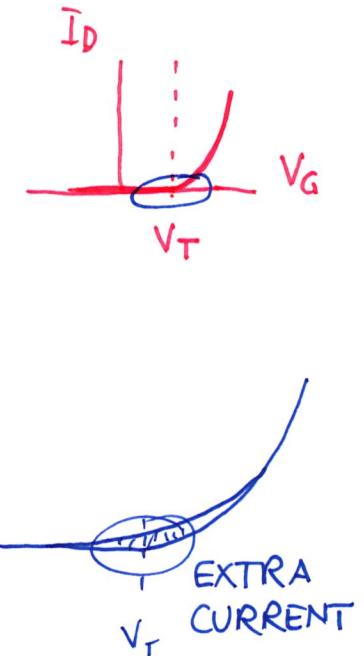
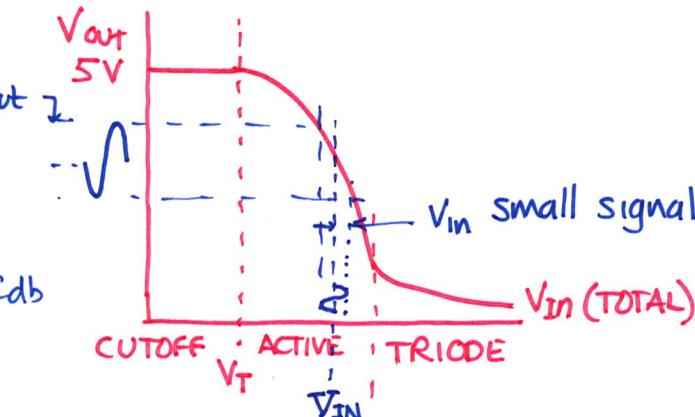
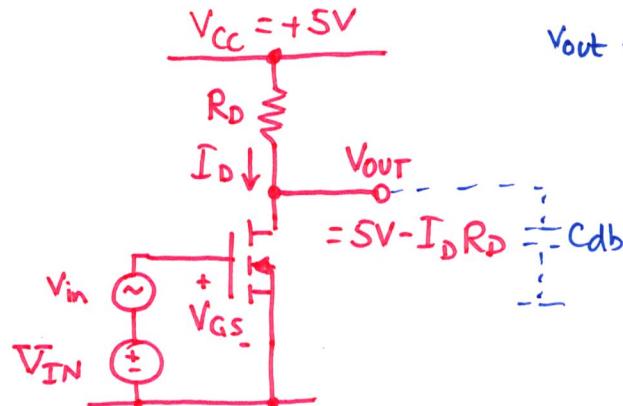


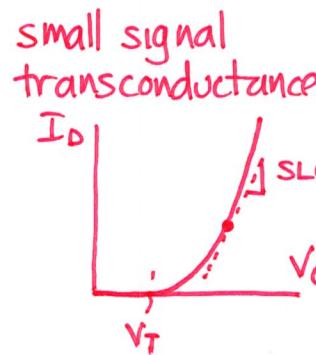
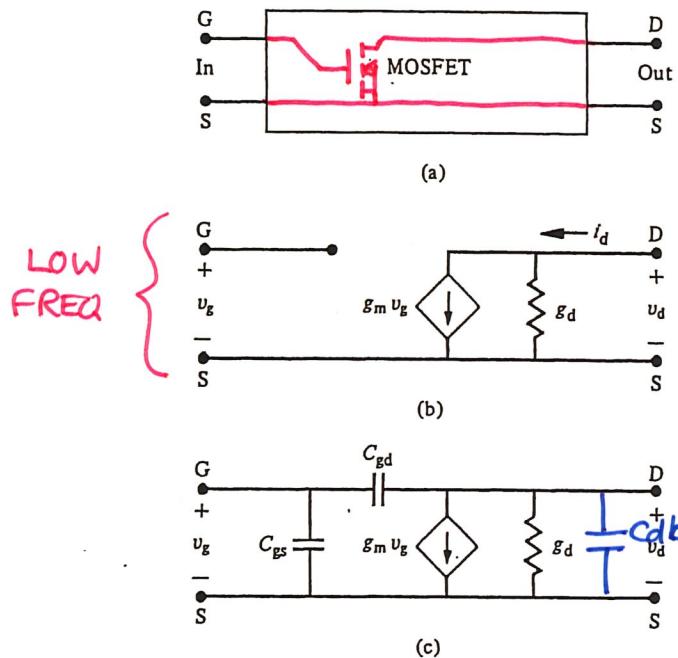
Figure 17.11 Subthreshold transfer characteristics of n -channel MOSFETs having the same parameters as the Fig. 17.10 device except $N_A = 10^{14}/\text{cm}^3$ or $N_A = 10^{15}/\text{cm}^3$ and $x_o = 0.013 \mu\text{m}$. The (*) are experimental data. Setting $V_D = 1 \text{ V}$, the solid- and dashed-line curves were computed respectively from the exact-charge and charge-sheet relationships found in Appendix D. The ideal-device curves were shifted along the voltage axis to enhance the comparison with the experimental data. (Reprinted from Pierret and Shields^[17], © 1983, with kind permission from Elsevier Science Ltd.)



Small Signal Model: Transconductance



MOSFETS—THE ESSENTIALS 631



HIGH FREQ: CAPACITANCES

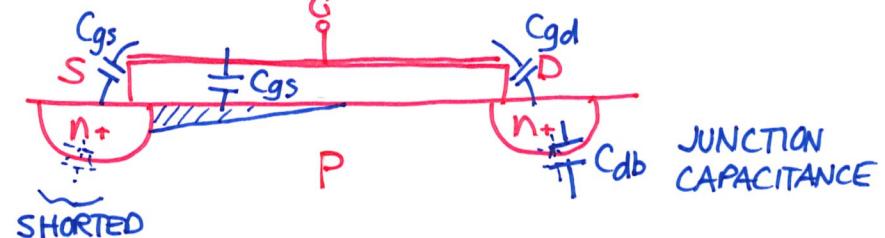


Figure 17.12 (a) The MOSFET viewed as a two-port network. (b) Low-frequency and (c) high-frequency small-signal equivalent circuits characterizing the a.c. response of the MOSFET.

Small Signal Model: pn Junction Capacitance

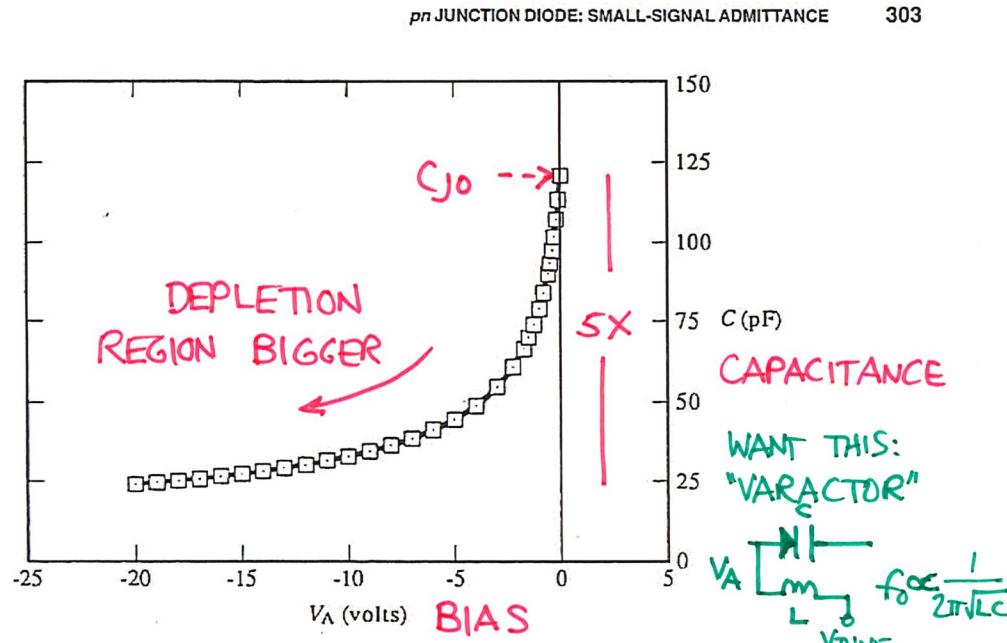
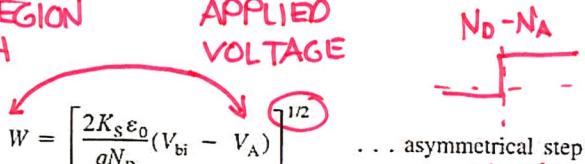


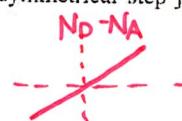
Figure 7.3 Monotonic decrease in the diode capacitance with increasing reverse bias. Sample C-V data derived from a IN5472A abrupt junction diode.

DEPL REGION WIDTH **APPLIED VOLTAGE**

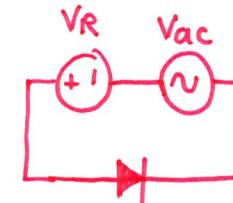
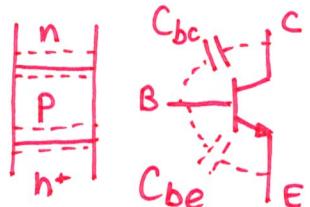
$$W = \left[\frac{2K_S \epsilon_0}{qN_B} (V_{bi} - V_A) \right]^{1/2} \quad \dots \text{asymmetrical step junction} \quad (7.3)$$



$$W = \left[\frac{12K_S \epsilon_0}{qa} (V_{bi} - V_A) \right]^{1/3} \quad \dots \text{linearly graded junction} \quad (7.4)$$

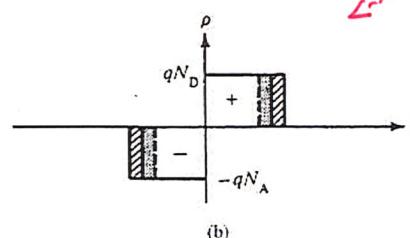
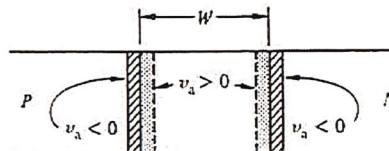


ALSO
FOR BJT

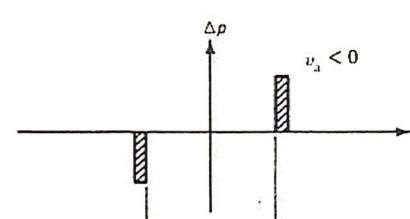
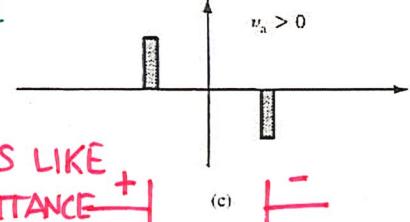


REV BIAS: $I_{DC} \approx 0$

$\Delta V_A \rightarrow \Delta W$



AMOUNT OF UNCOVERED CHARGE CHANGES



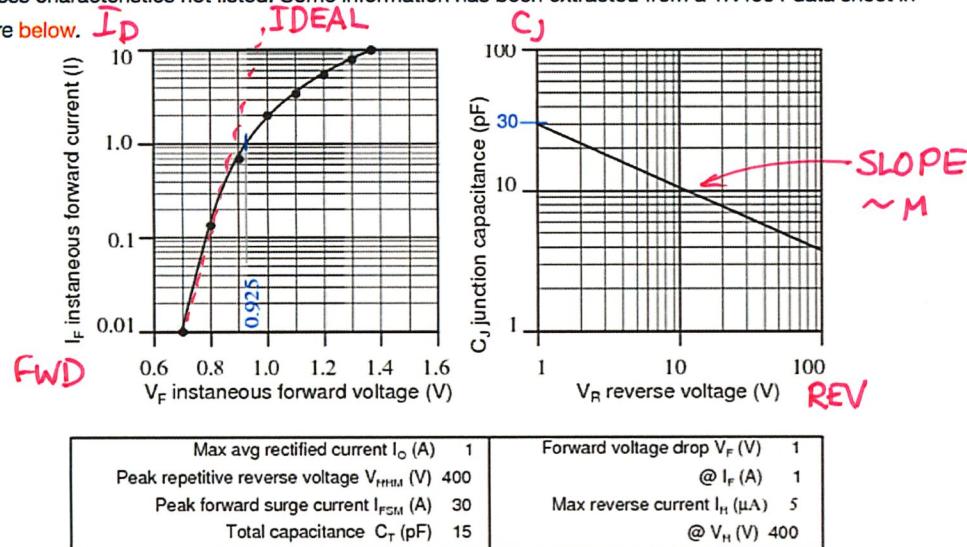
$$C_J = \frac{K_S \epsilon_0 A}{W}$$

C_J w d SEPARATION OF "PLATES"
JUNCTION CAPACITANCE

Figure 7.4 Depletion-layer charge considerations. (a) Depletion width and (b) total charge density oscillations in response to an applied a.c. signal. (c) $v_a > 0$ and (d) $v_a < 0$ a.c. charge densities.

Diode Modeling in SPICE

The SPICE circuit simulation program provides for modeling diodes in circuit simulations. The diode model is based on characterization of individual devices as described in a product data sheet and manufacturing process characteristics not listed. Some information has been extracted from a 1N4004 data sheet in Figure below.



Data sheet 1N4004 excerpt, after [D14].

The diode statement begins with a diode element name which must begin with "d" plus optional characters. Example diode element names include: d1, d2, dtest, da, db, d101. Two node numbers specify the connection of the anode and cathode, respectively, to other components. The node numbers are followed by a model name, referring to a subsequent ".model" statement.

The model statement line begins with ".model," followed by the model name matching one or more diode statements. Next, a "d" indicates a diode is being modeled. The remainder of the model statement is a list of optional diode parameters of the form ParameterName=ParameterValue. None are used in Example below. Example2 has some parameters defined. For a list of diode parameters, see Table below.

```

General form: d[name] [anode] [cathode] [modelname]
              .model ([modelname] d [parmtr1=x] [parmtr2=y] . . .)

Example:      d1 1 2 mod1
              .model mod1 d

Example2:     D2 1 2 Da1N4004
              .model Da1N4004 D (IS=18.8n RS=0 BV=400 IBV=5.00u CJ0=30 M=0.333 N=2)
  
```

REVERSE VOLTAGE: CAP

$$W = \sqrt{\frac{2K_s \epsilon_0 V_{bi}}{q N D}} \sqrt{1 - \frac{V_A}{V_{bi}}}$$

JUNCTION CAP

$$C_J = \frac{K_s \epsilon_0 A}{W}$$

$$C_J = \frac{K_s \epsilon_0 A}{\sqrt{\frac{2K_s \epsilon_0 V_{bi}}{q N B}}} \underbrace{\frac{1}{\sqrt{1 - \frac{V_A}{V_{bi}}}}}_{C_{j0}}$$

$$\frac{1}{\sqrt{1 - \frac{V_A}{V_{bi}}}} \underbrace{V_j}_{C_{j0}}$$

ZERO BIAS
CAPACITANCE

$$C_J = C_{j0} \underbrace{\frac{1}{(1 - \frac{V_A}{V_j})^M}}_{\text{ZERO BIAS}} \} \text{ JUNCTION GRADING}$$

V_j BUILT IN VOLTAGE

Diode Modeling in SPICE

The easiest approach to take for a SPICE model is the same as for a data sheet: consult the manufacturer's web site. Table below lists the model parameters for some selected diodes. A fallback strategy is to build a SPICE model from those parameters listed on the data sheet. A third strategy, not considered here, is to take measurements of an actual device. Then, calculate, compare and adjust the SPICE parameters to the measurements.

Diode SPICE parameters

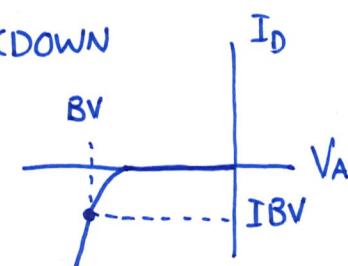
Symbol	Name	Parameter	Units	Default
I _s	IS	Saturation current (diode equation)	A	1E-14
R _s	RS	Parsitic resistance (series resistance)	Ω	0
n	N	Emission coefficient, 1 to 2	-	1
T _D	TT	Transit time	s	0
C _{D(0)}	CJO	Zero-bias junction capacitance	F	0
Φ ₀	VJ	Junction potential	V	1
m	M	Junction grading coefficient	-	0.5
-	-	0.33 for linearly graded junction	-	-
-	-	0.5 for abrupt junction	-	-
E _g	EG	Activation energy:	eV	1.11
-	-	Si: 1.11	-	-
-	-	Ge: 0.67	-	-
-	-	Schottky: 0.69	-	-
p _i	XTI	IS temperature exponent	-	3.0
-	-	pn junction: 3.0	-	-
-	-	Schottky: 2.0	-	-
k _f	KF	Flicker noise coefficient	-	0
a _f	AF	Flicker noise exponent	-	1
FC	FC	Forward bias depletion capacitance coefficient	-	0.5
BV	BV	Reverse breakdown voltage	V	∞
IBV	IBV	Reverse breakdown current	A	1E-3

$$I_D = I_s e^{q V_A / n kT}$$

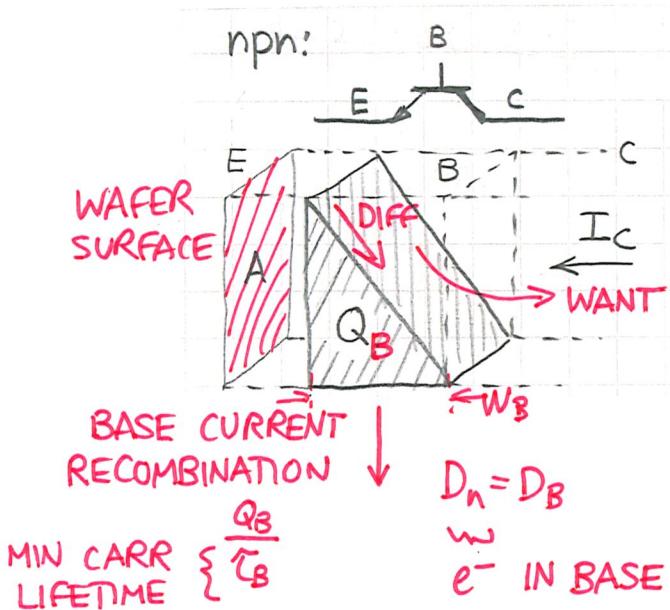
$$C_J = \frac{C_{JO}}{\left(1 - \frac{V_A}{V_J}\right)^m}$$

$$I_S = I_{SO} \left(1 + \frac{T}{300K}\right)^{XTI}$$

REVERSE BREAKDOWN



BJT Charge Control Model: Base Transit Time τ_T



$$= \frac{Q_B}{\tau_T} \quad \text{BASE TRANSIT TIME}$$

$$\tau_T = \frac{Q_B}{I_C} = \frac{\cancel{q} A W_B n_i^2 e^{(V_{BE}/V_T)}}{\cancel{(2)} N_A} \cancel{\frac{e^{(V_{BE}/V_T)} \times W_B N_A}{q A D_B n_i^2 e^{(V_{BE}/V_T)}}} = \frac{W_B^2}{D_B}$$

$$\frac{D}{\mu} = \frac{kT}{q} \Rightarrow D = \mu \frac{kT}{q}$$

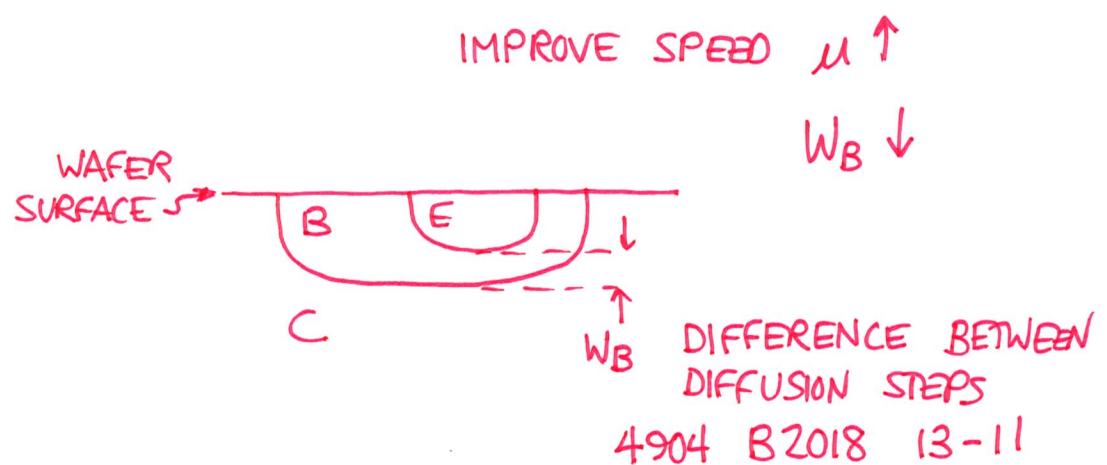
$$\tau_T = \frac{W_B^2}{2\mu(\frac{kT}{q})}$$

Charge in base:

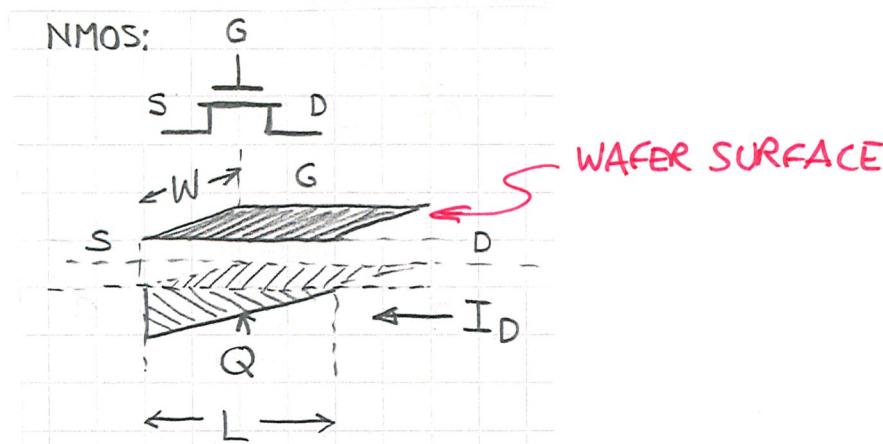
$$Q = \frac{q A W_B n_i^2}{2 N_A} e^{(V_{BE}/V_T)}$$

Current in collector terminal:

$$I_C = \underbrace{\cancel{q} A D_n n_i^2 e^{(V_{BE}/V_T)}}_{I_S} \cancel{W_B N_A}$$



MOSFET - BJT Comparison: Channel Transit Time τ_T



Charge in channel:

$$Q = \frac{C_{ox} WL}{2} (V_{GS} - V_t)$$

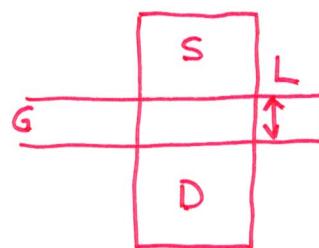
Current in drain terminal (active region):

$$I_D = \frac{\mu C_{ox}}{2} \frac{W}{L} (V_{GS} - V_t)^2$$

$$\frac{Q}{I} = \frac{C_{ox} WL (V_{GS} - V_t) L}{\mu C_{ox} W (V_{GS} - V_t)^2} = \frac{L^2}{\mu (V_{GS} - V_t)}$$

LENGTH IS CRITICAL DIMENSION

LOOK ONTO SURFACE OF WAFER



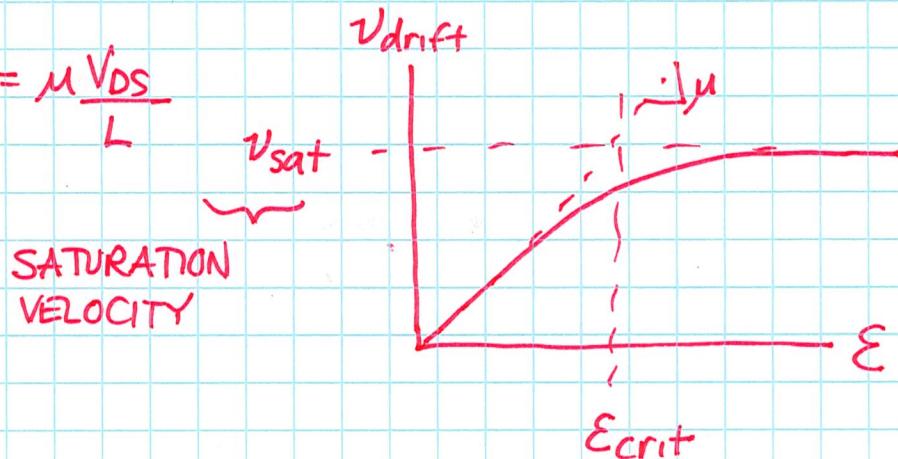
CONTROLLED BY
LITHOGRAPHY

MC14007 $L = 10\text{mm}$
today $L = 10\text{nm}$ 1000X
IMPROVEMENT

MOS BJT Comparison CORRECTED

<p>nph:</p>	<p>NMOS:</p>
<p>Current in collector terminal:</p> $I_C = \frac{qAD_n n_i^2}{2W_B N_A} e^{(V_{BE}/V_T)} \quad \cancel{I_S}$	<p>Current in drain terminal (active region):</p> $I_D = \frac{\mu C_{ox}}{2} \frac{W}{L} (V_{GS} - V_t)^2 \quad \checkmark$
<p>Representing current in form of $I = Q/\Delta T$</p>	
<p>Charge in base:</p> $Q = \frac{qAW_B n_i^2}{2N_A} e^{(V_{BE}/V_T)} \quad \checkmark$	<p>Charge in channel:</p> $Q = \frac{C_{ox}WL}{2} (V_{GS} - V_t) \quad \checkmark$
<p>Transit time through base:</p> $\Delta T = \frac{W_B^2}{2\mu V_T} \quad \checkmark$	<p>Transit time through channel:</p> $\Delta T = \frac{L^2}{2\mu(V_{GS} - V_t)} \quad \checkmark$
<p>Applied voltage:</p>	
V _{BE} : Applied across base-emitter junction	V _{GS} : Applied from gate to source
<p>Geometry under designer control, subject to process (mask lithography) minimum:</p>	
A: Base-emitter junction area	W: Width of channel under gate L: Length of channel under gate
<p>Process parameters:</p>	
W _B : Width of base region (determined by diffusion of dopant atoms for base, emitter regions)	C _{ox} : Gate oxide capacitance per unit area (determined by thickness, dielectric constant of gate oxide)
N _A : Dopant density of p-type atoms in base	V _t : Threshold voltage (determined by lots of things; see ECE3901)
<p>Physical parameters:</p>	
μ : Bulk mobility of electrons in base D _n ; Diffusion constant of electrons in base n _i : Intrinsic carrier concentration (strongly temperature dependent) q: Electron charge V _T : thermal voltage = kT/q ~ 26mV @ T=300K	μ : Surface mobility of electrons in channel

ALL OF THIS ASSUMED $v_d = \mu E = \mu \frac{V_{DS}}{L}$



"SHORT CHANNEL EFFECT"

$$Q = C_{ox} WL (V_{GS} - V_t)$$

$$v_{sat} = \frac{L}{\Delta t} \Rightarrow \Delta t = \frac{L}{v_{sat}} \quad \{ \text{was } \mu V_{DS} \}$$

$$I_D = \frac{Q}{\Delta t} = \frac{C_{ox} WL (V_{GS} - V_t) v_{sat}}{L}$$

$$I_D = C_{ox} W (V_{GS} - V_t) v_{sat}$$

NOT RESISTIVE!?

$$\text{FASTER: } I = C \frac{dV}{dt} \quad dt = \frac{CdV}{I} \Rightarrow \frac{C}{C_{ox} W L} \frac{dV}{V_{DD} v_{sat}} \Rightarrow \frac{L}{v_{sat}} \quad \{ \text{IMPROVES AS } L \downarrow \}$$