

# **ECE 4902 Analog Integrated Circuit Design – Project Report**

**Worcester Polytechnic Institute**

**B-Term 2022**

## **Project 2: Two-Stage Op-Amp 50n Short Channel Implementation**

Submitted by

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Drew Solomon

Jonathan Lopez

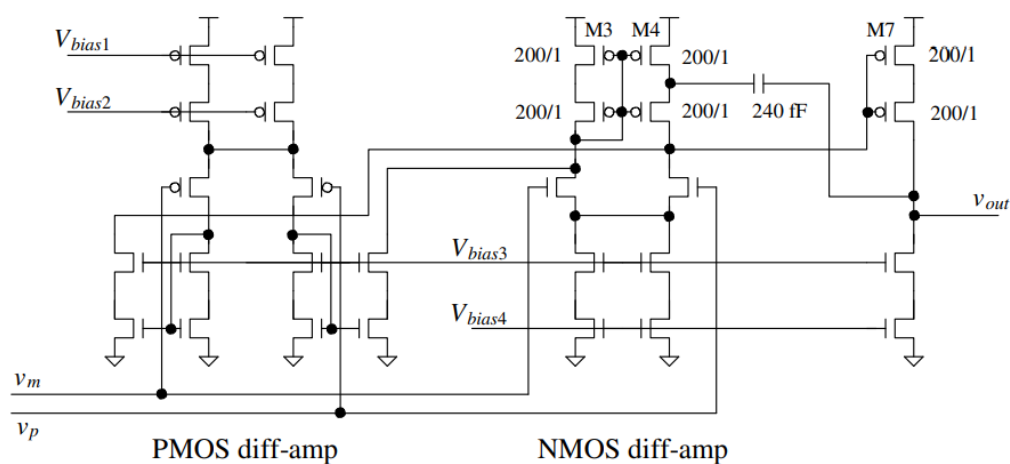
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Professor Guler

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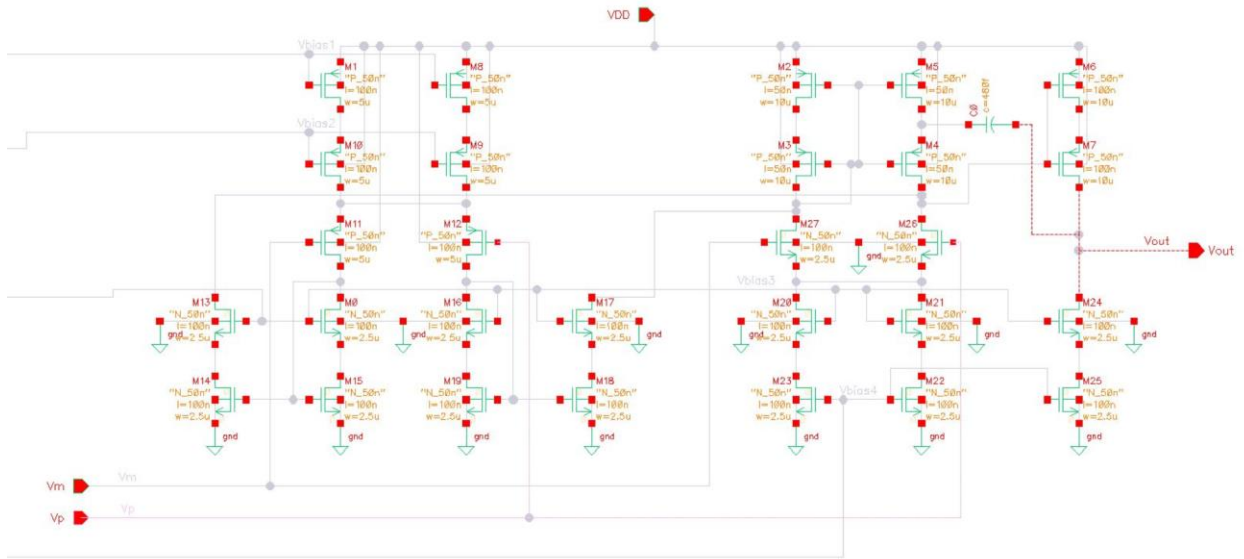
# Part 1: Op Amp Final Specs and Simulation Results

## Differential Amplifier Topology

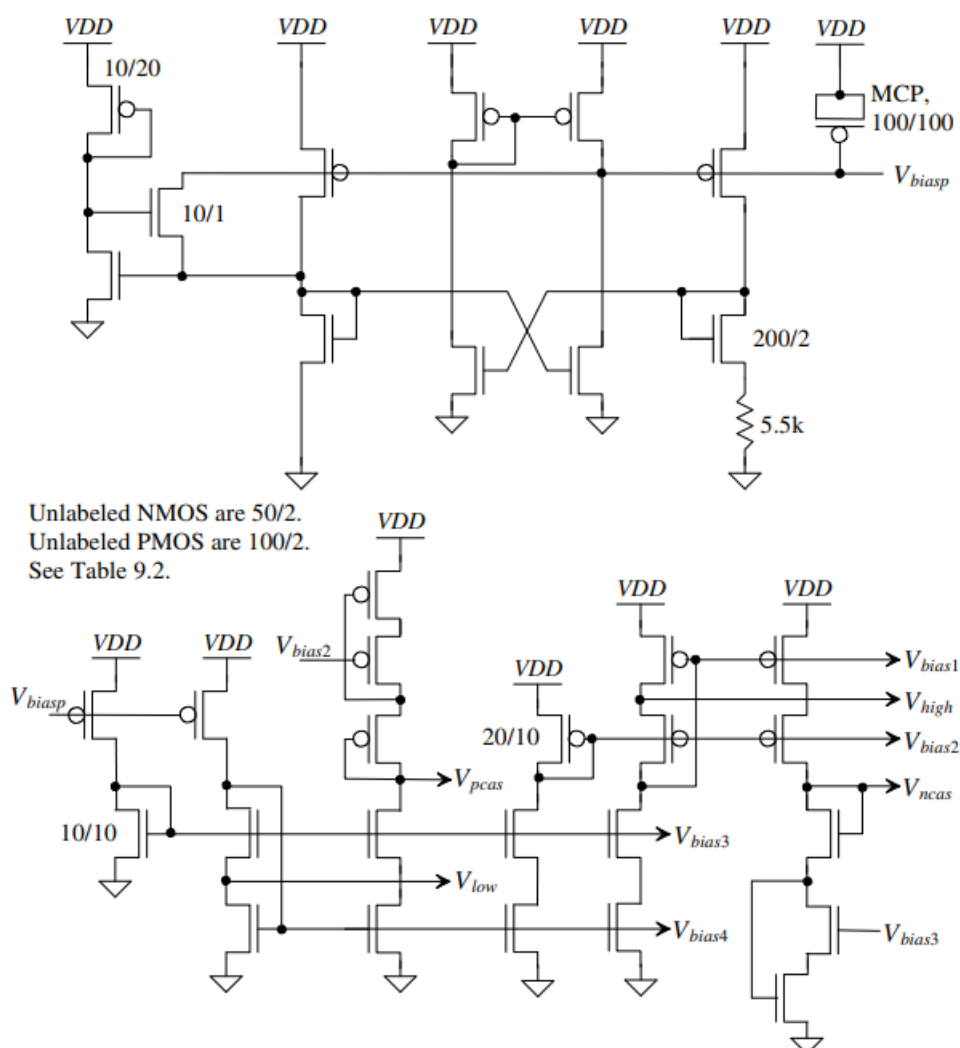


**Figure 24.28** Two-stage op-amp of Fig. 24.21 with rail-to-rail input range.

We used the above topology from R. Jacob Baker's Circuit Design, Layout, and Simulation textbook. [1]

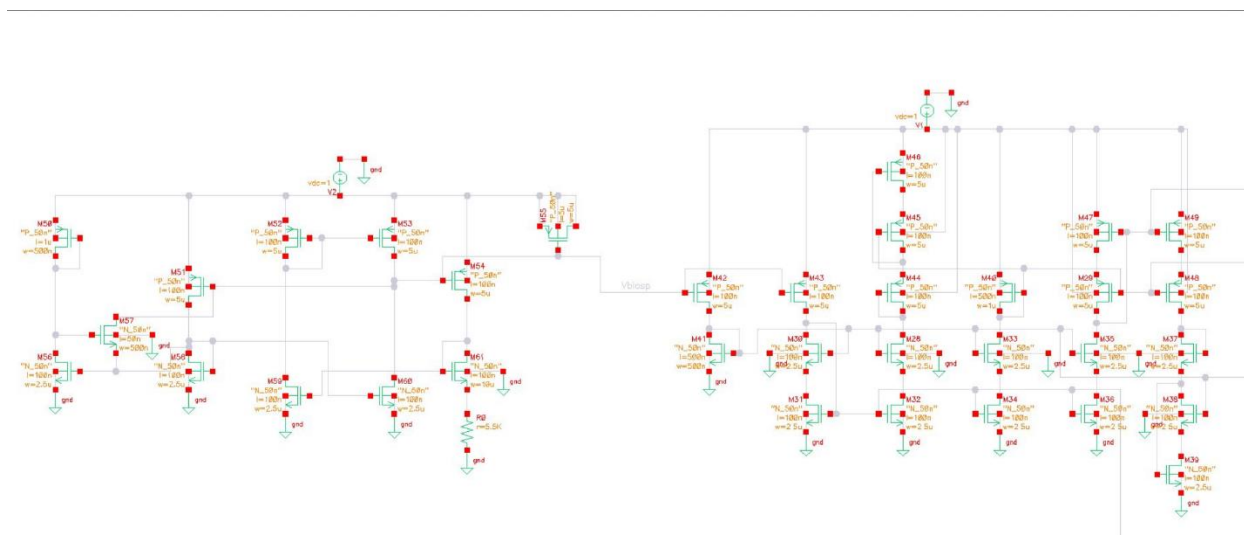


## Reference Topology

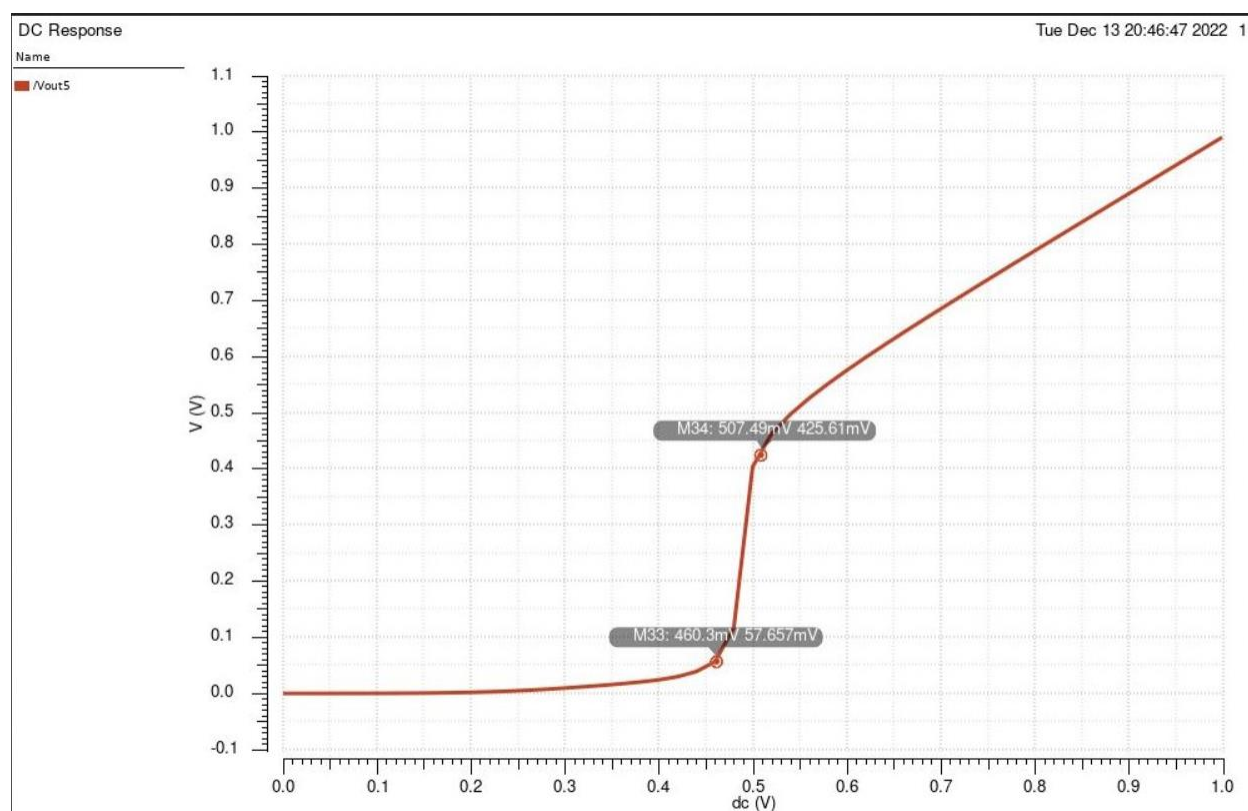


**Figure 20.47** General biasing circuit for short-channel design using the data in Table 9.2.

We also used the above bias circuit from R. Jacob Baker's Circuit Design, Layout, and Simulation textbook in making our op-amp. [1]

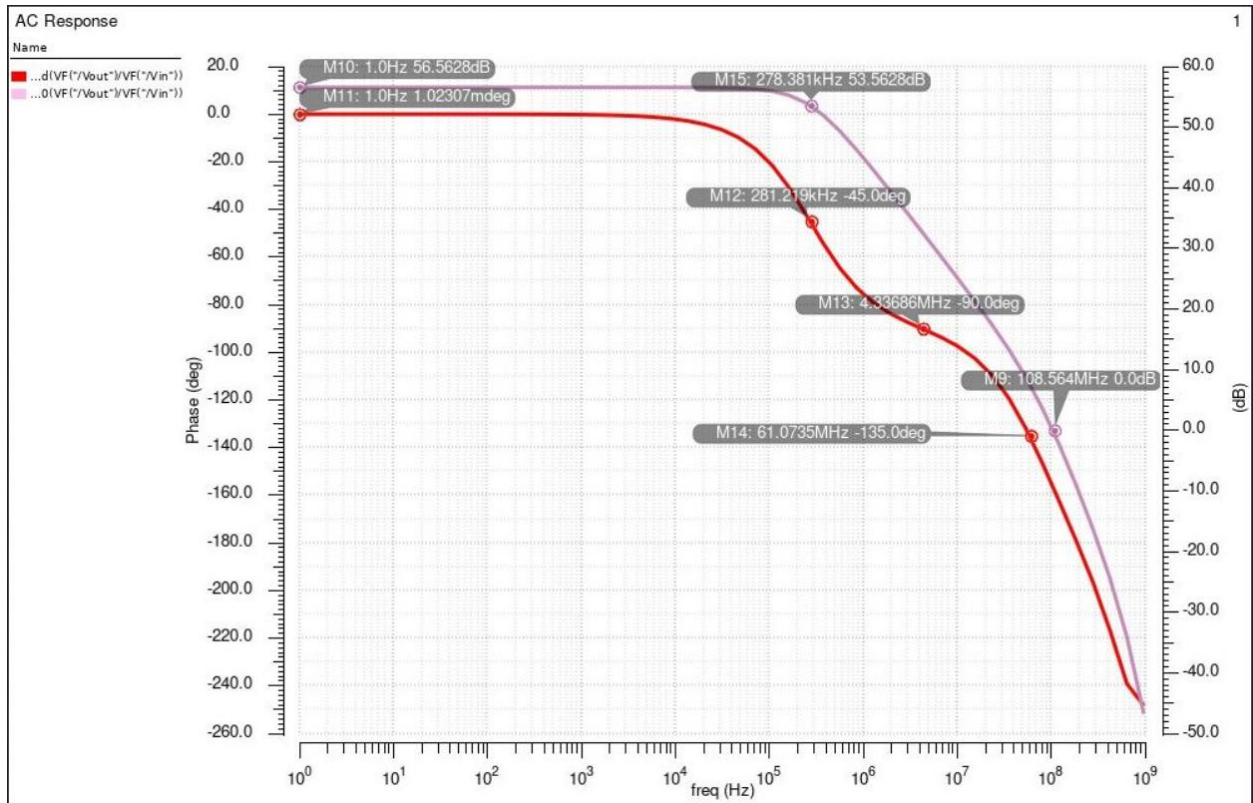


## Minimum Supply Voltage (V)



The minimum supply voltage needed for this amplifier to work was between 460mV-507mV.

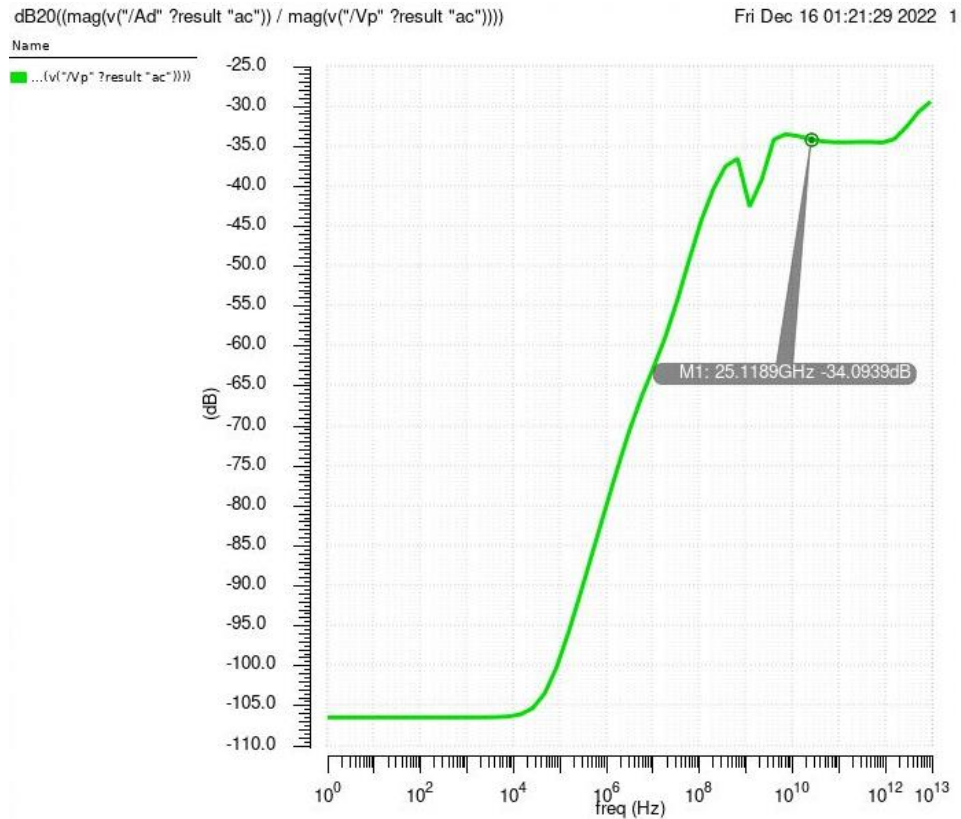
## Gain of Differential Amplifier (dB)



The differential gain of the operational amplifier was 56.5628 dB, as seen in the figure above.

## CMRR (dB) (Low Freq and Spectrum)

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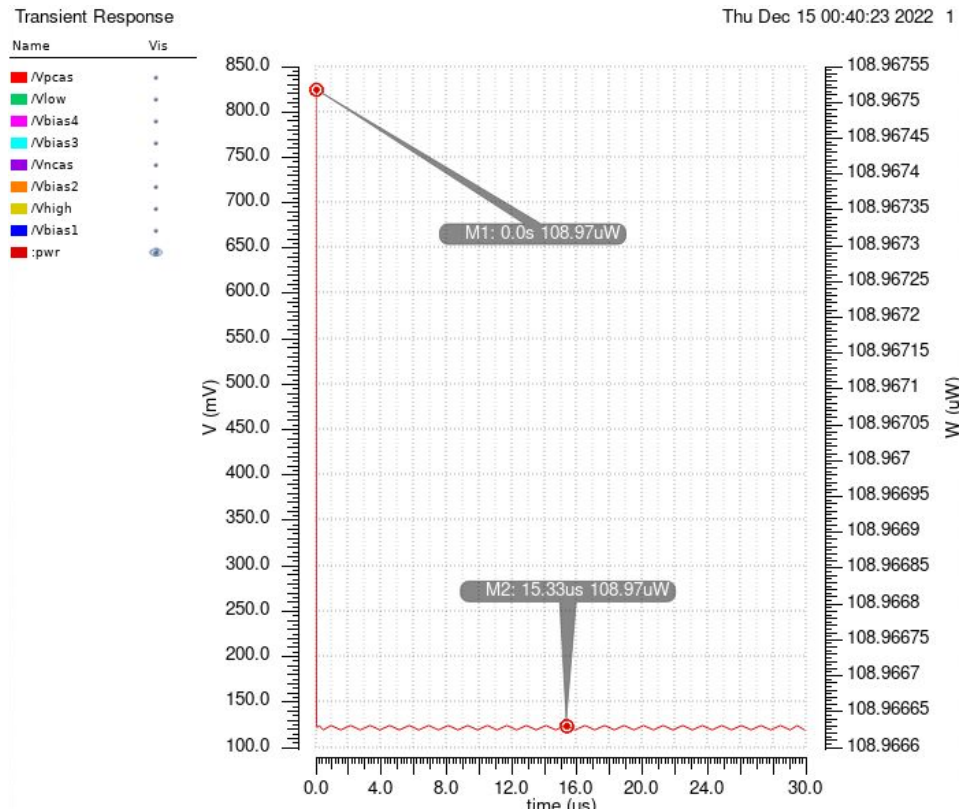


We found the Differential gain now for the Common Mode Gain Acm.

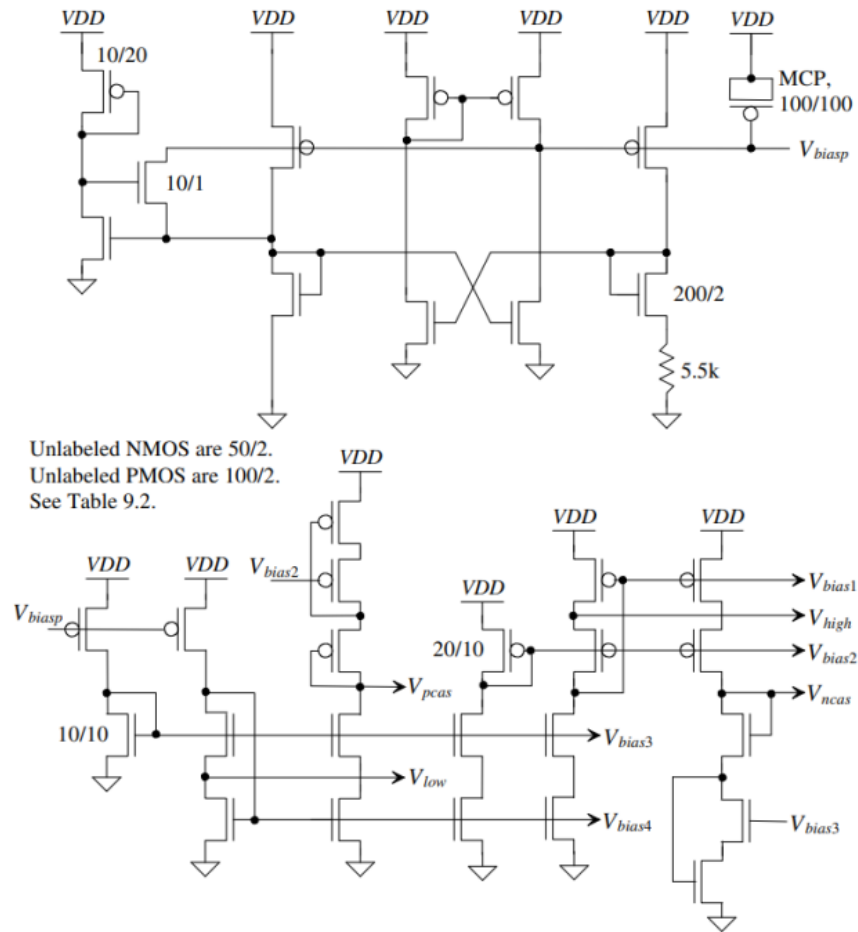
CMRR =  $20\log|(278.381\text{kHz}/25.1189\text{GHz})| = 99.107\text{dB}$  which is in range of the 110 +- 10%

## Reference Power Consumption (uW)

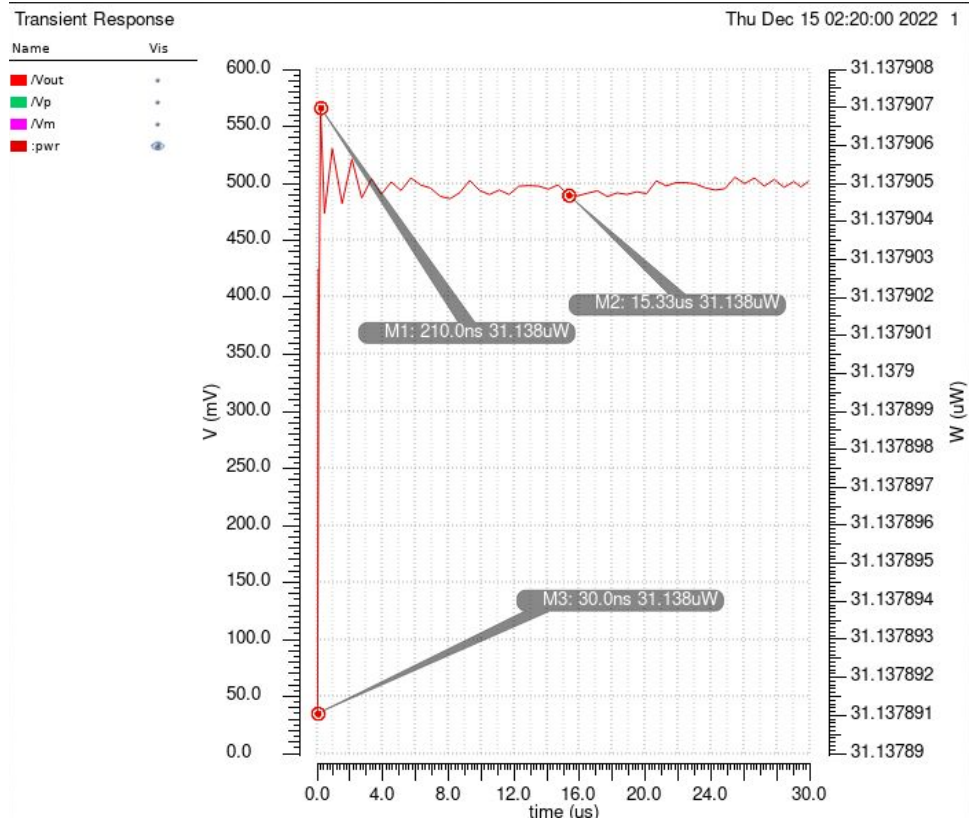




With no Ideal DC sources allowed beside VDD, the operational amplifier needed proper biasing. This is achieved via the via biasing circuit in R. Jacob Baker's Circuit Design, Layout, and Simulation. It used about 109 $\mu$ W

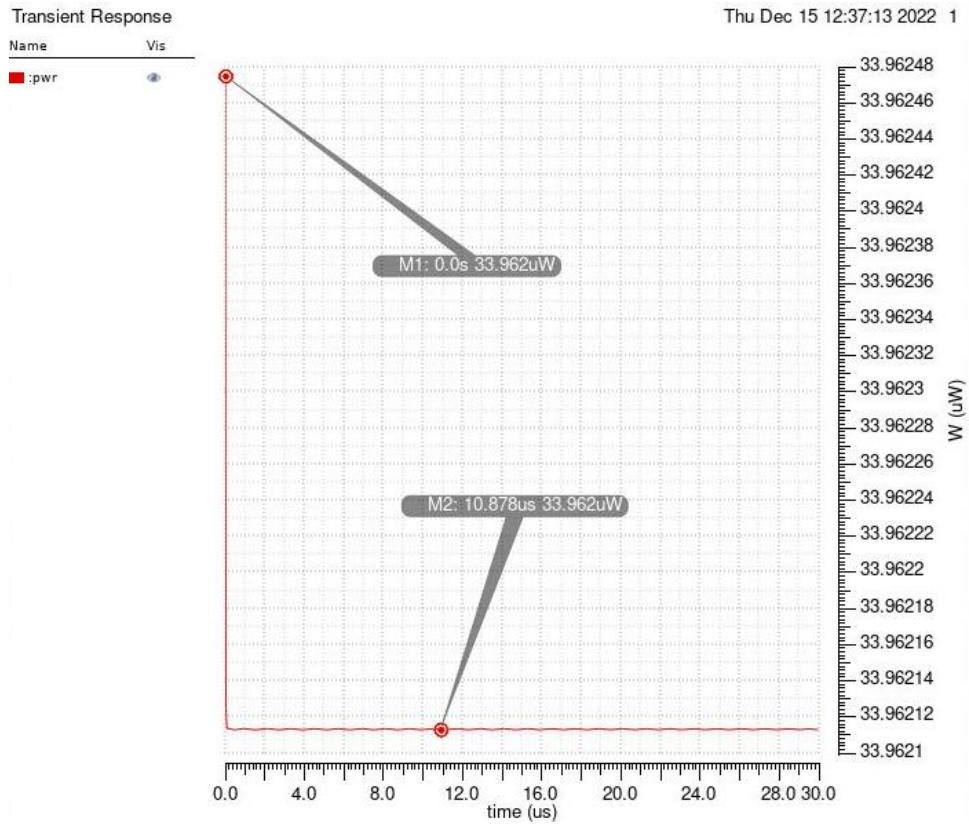


## Op Amp Power Consumption with Zero Input (uW)



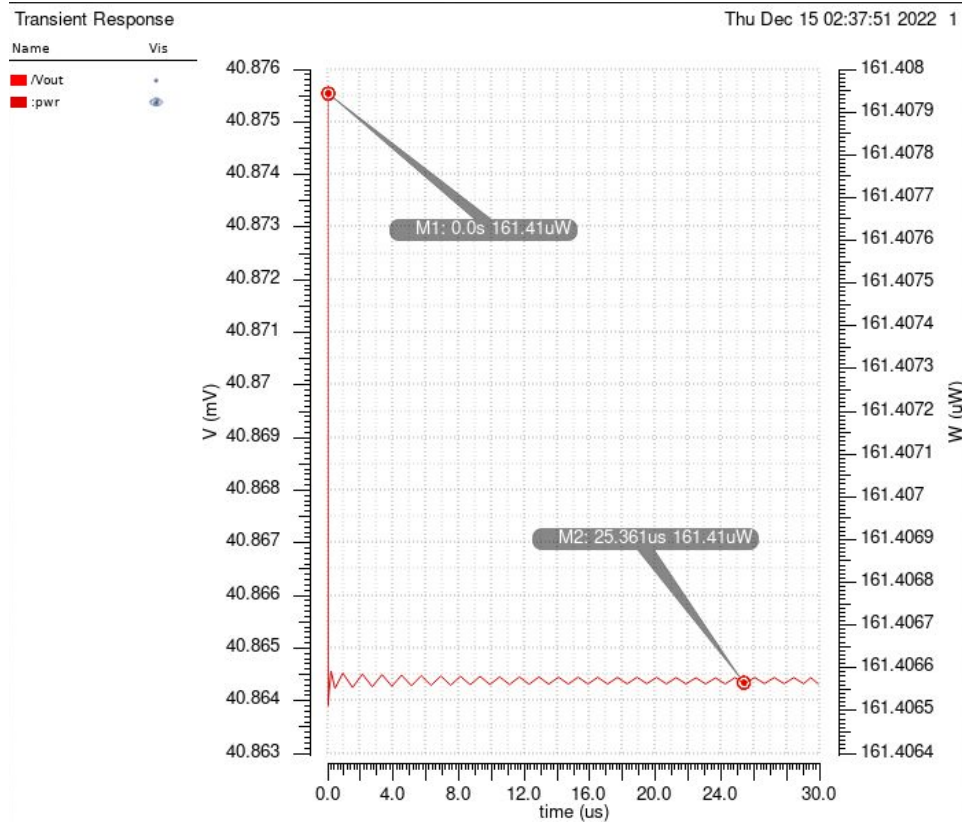
This is within spec as the maximum wattage is 40 $\mu$ W and we are pulling about 31 $\mu$ W

## Op Amp Power Consumption with No Load (uW)



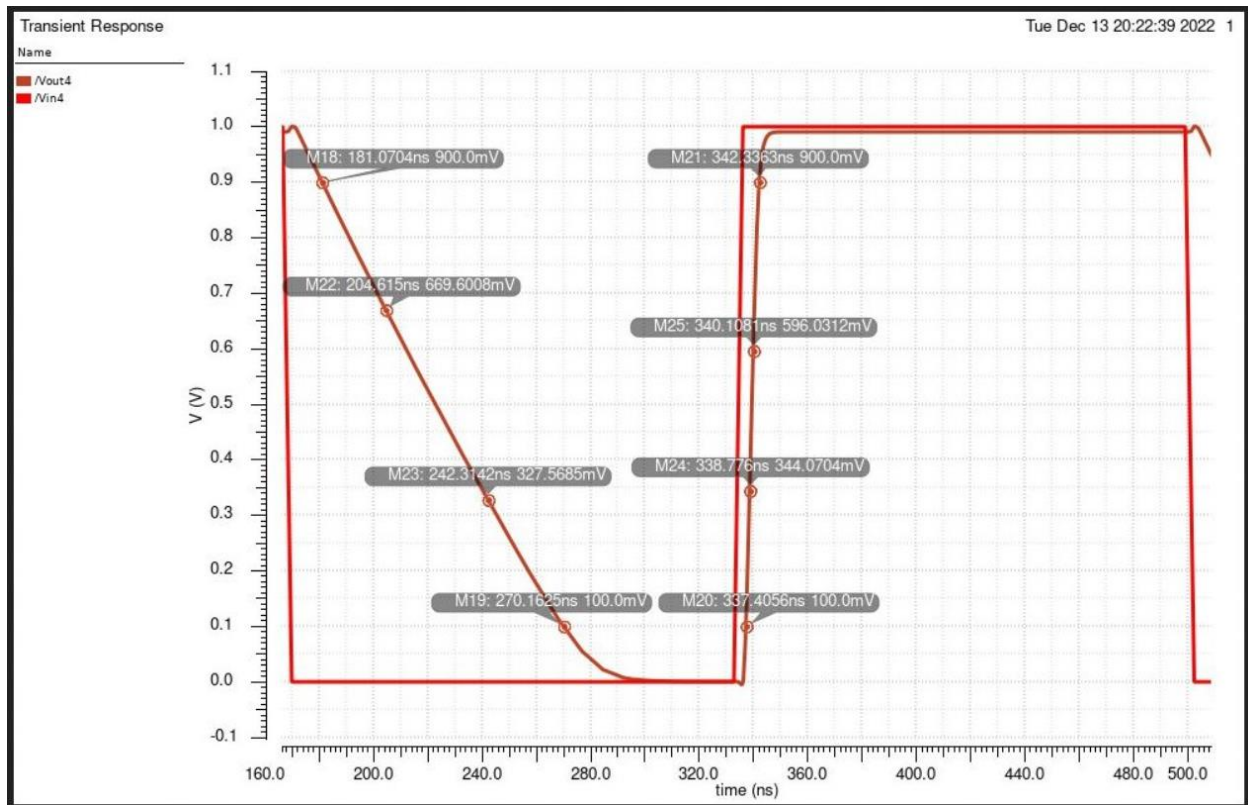
This is within spec as the maximum wattage is 40 $\mu$ W and we are pulling about 33 $\mu$ W

## Total Power Consumption (uW)



This is our total power consumption with the biasing circuit, the 2-stage amplifier, and the load. 161 $\mu$ W is our Maximum power consumption.

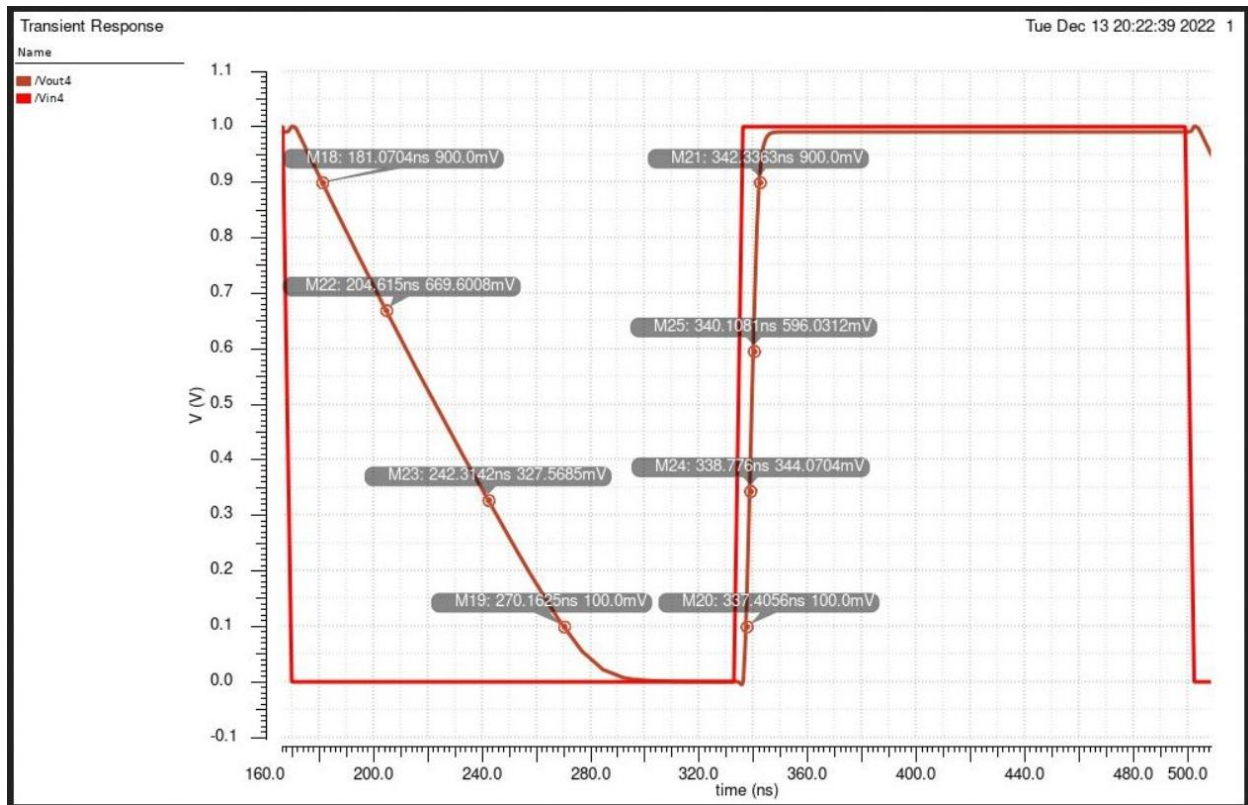
## Positive Slew Rate (V/us)



The positive slew rate was calculated using the above figure:

$$\text{Slew Rate} = (\Delta) \text{ Voltage} / (\Delta) \text{ Time} = (596\text{mV} - 344\text{mV}) / (340 \text{ ns} - 338.8 \text{ ns}) = 210\text{V}/\mu\text{s}$$

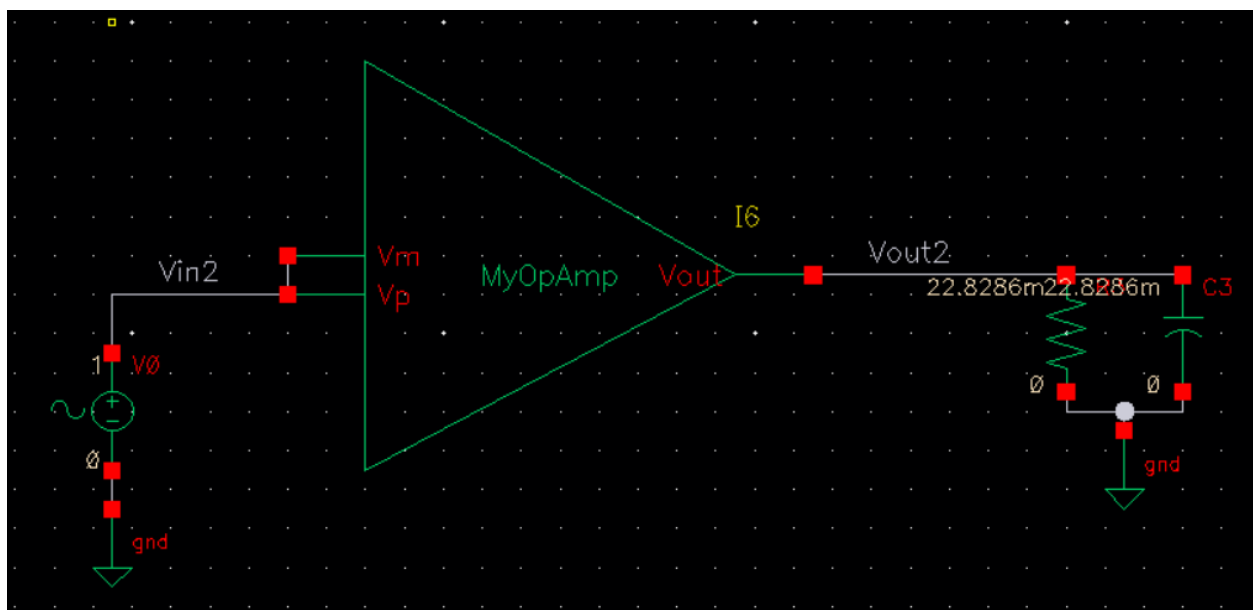
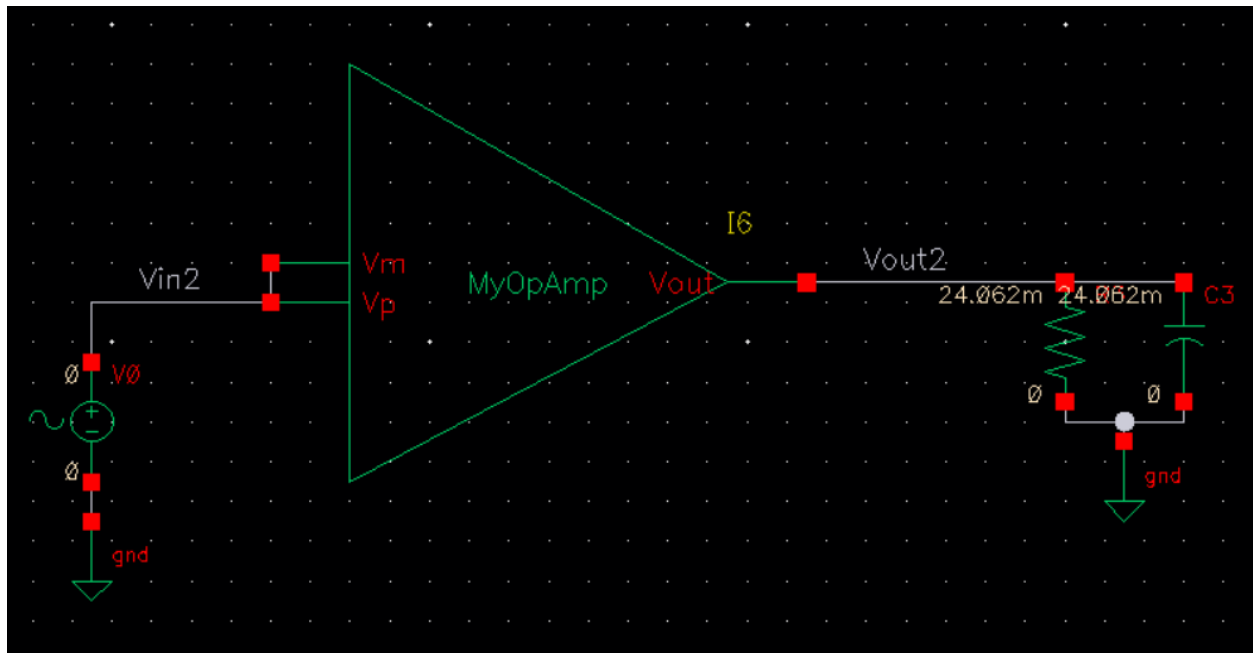
## Negative Slew Rate (V/us)



The negative slew rate was calculated using the above figure:

$$\text{Slew Rate} = (\Delta) \text{ Voltage} / (\Delta) \text{ Time} = (670\text{mV} - 327.5\text{mV}) / (242 \text{ ns} - 205 \text{ ns}) = 9.26\text{v/uS}$$

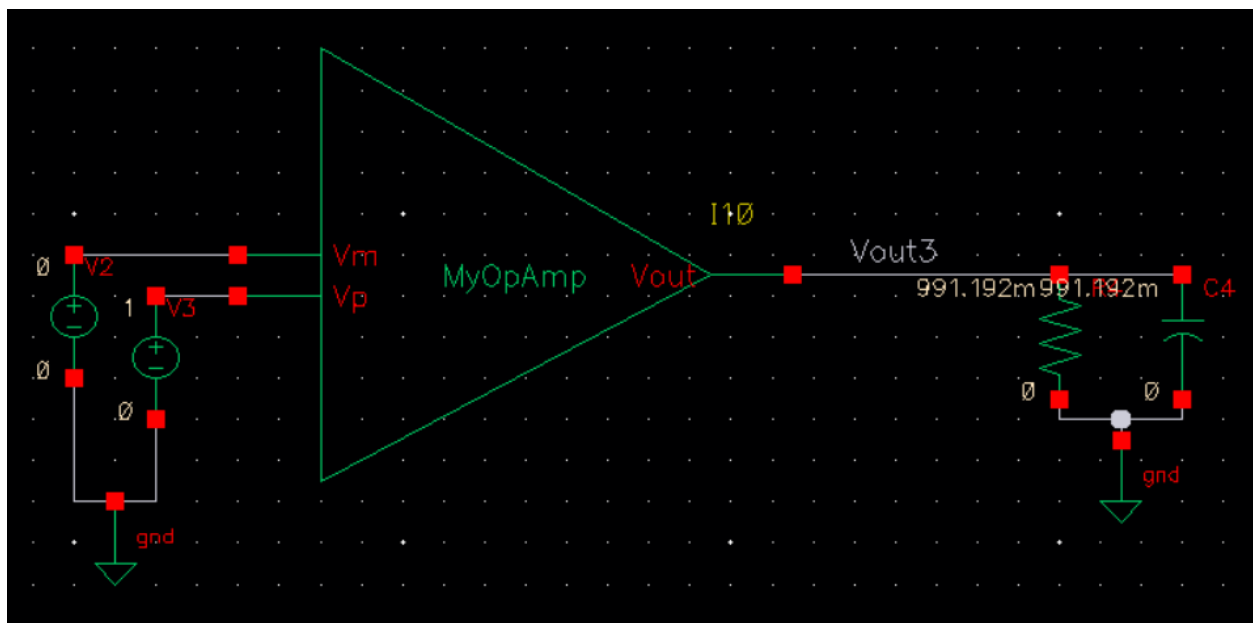
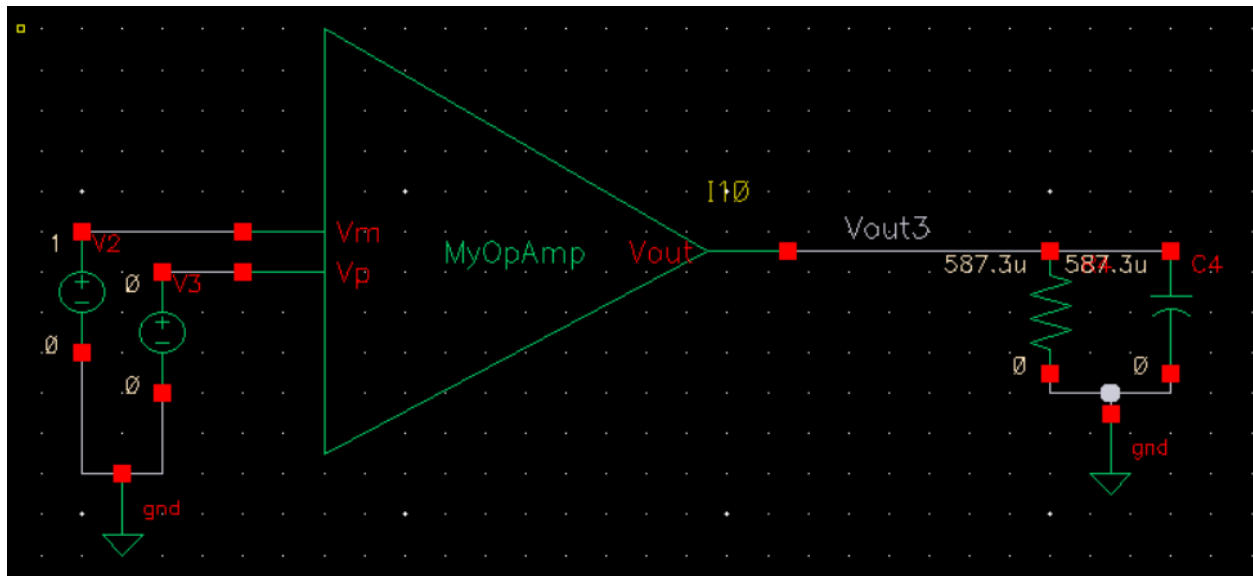
**ICMR ( $V_{\min} \sim V_{\max}$ )**



$$0V < ICMR < 1V$$

**Output Swing ( $V_{min} \sim V_{max}$ )**





Output Swing = 587.3uV – 991.192mV

## VDD PSRR (dB)

$$PSRR^+ = \frac{A_{OL}(f)}{v_{out}/v^+}$$

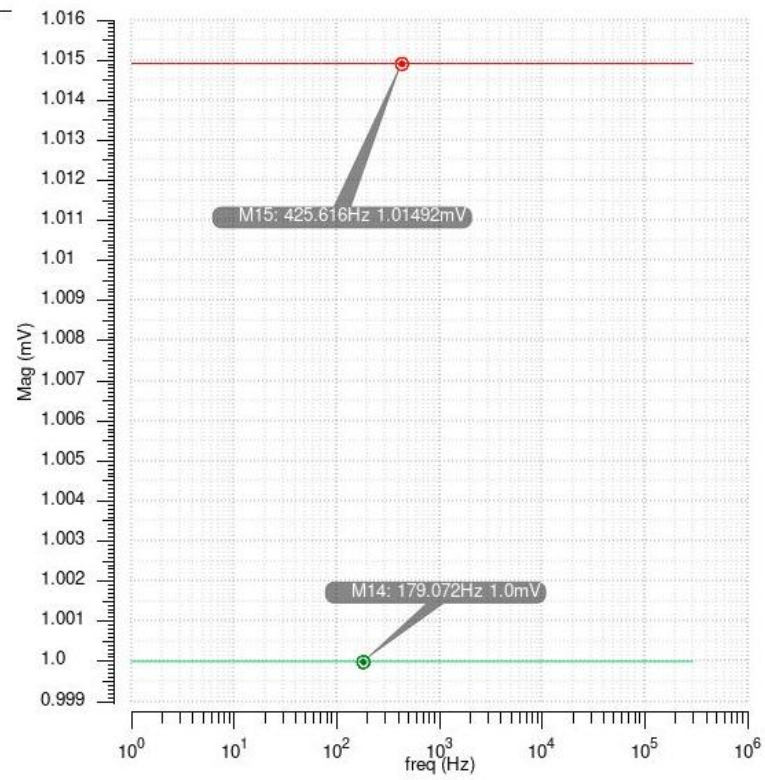
## AC Response

Thu Dec 15 04:20:44 2022 1

Name

■ /vout

■ /vdd!



$$PSRR^+ = \frac{A_{OL}(f)}{V_{out}/V^+}$$

Unloaded Frequency = 182.666kHz

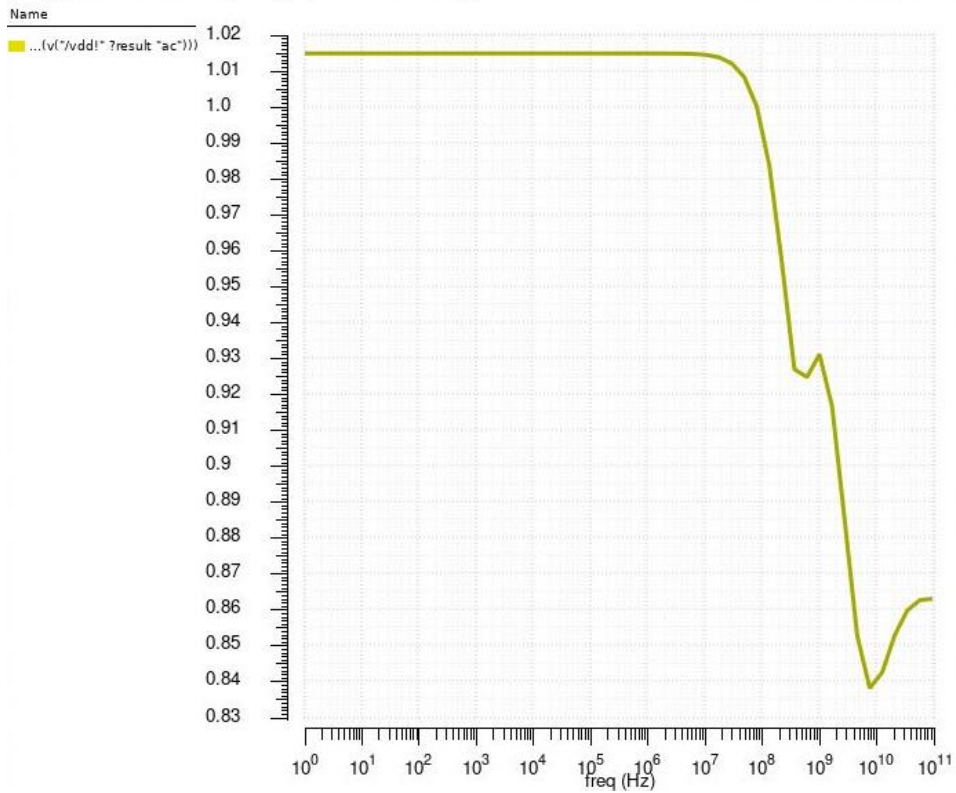
$V_{out}/V^+ = 1.01492/1 = 0.985299V/V$

$$\frac{182.666kHz}{0.985299 \frac{V}{V}} = 185.391kHz$$

105dB

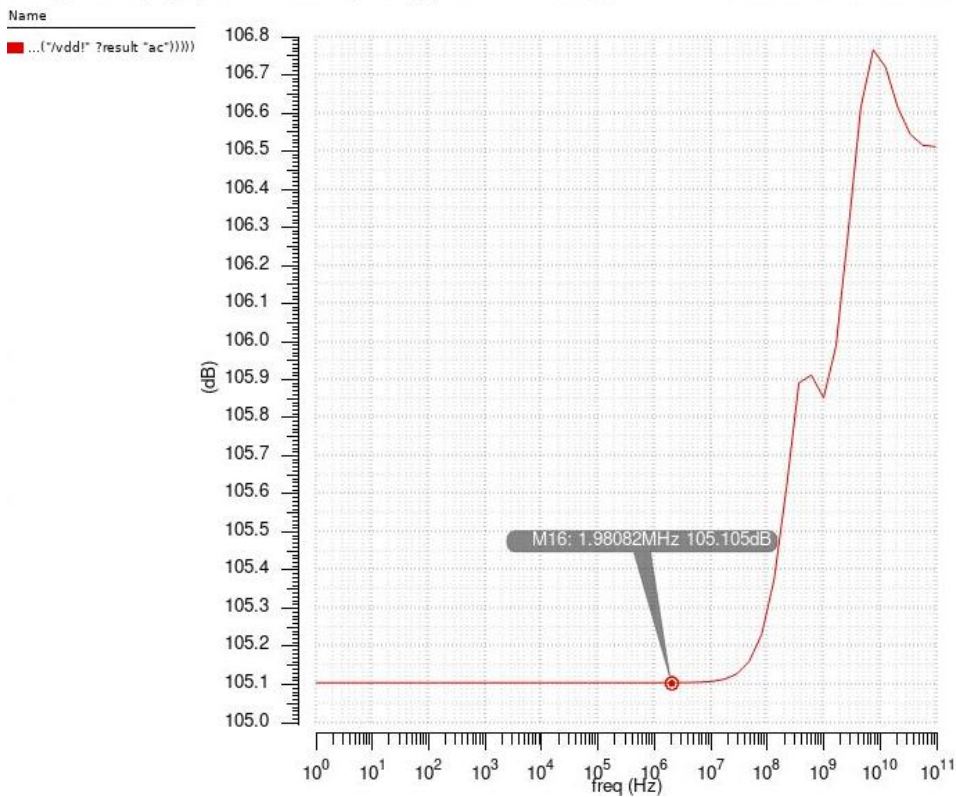
$$\frac{\text{mag}(v("/Vout" \text{ ?result "ac"}))}{\text{mag}(v("/vdd!" \text{ ?result "ac"}))}$$

Thu Dec 15 05:00:24 2022 1



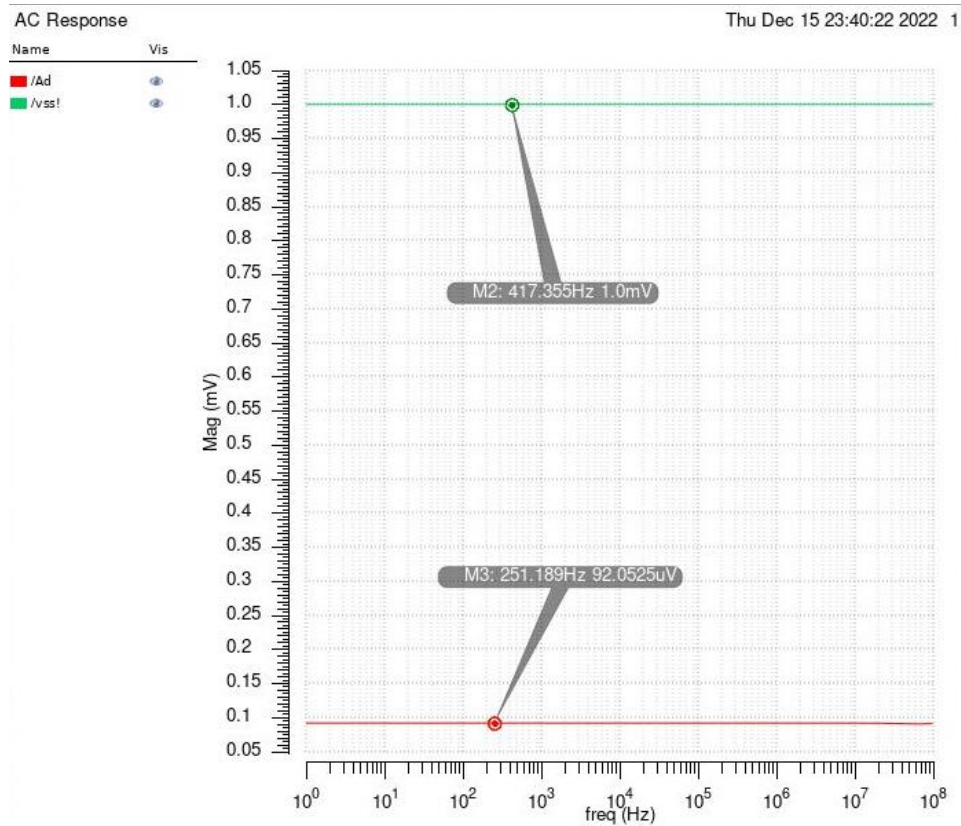
$$\text{dB20}((182666 / (\text{mag}(v("/Vout" \text{ ?result "ac"})) / \text{mag}(v("/vdd!" \text{ ?result "ac"}))))))$$

Thu Dec 15 04:58:03 2022 1



Hand calculation matched simulation.

## GND PSRR (dB)



$$PSRR^- = \frac{A_{OL}(f)}{v_{out}/v^-}$$

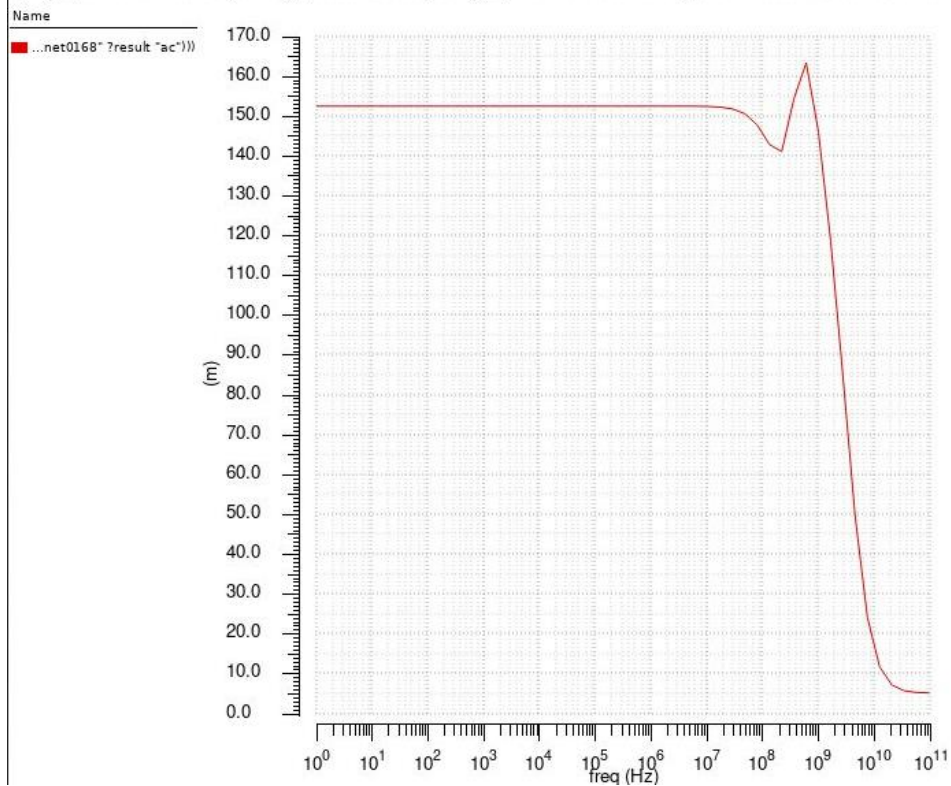
Unloaded Frequency = 182.666kHz

$V_{out}/V^- = 92.0525 \mu V/1mV = 0.0920525V/V$

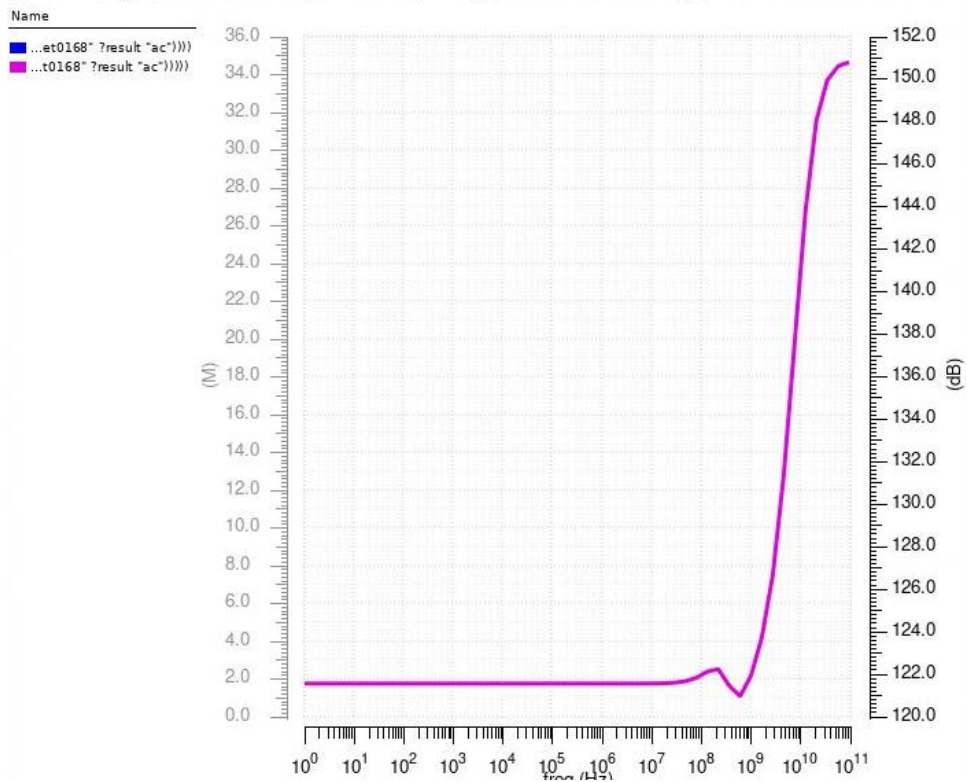
$$\frac{182.666kHz}{0.0920525} = 19,884,367Hz$$

125.9 dB

(mag(v("/Vout" ?result "ac")) / mag(v("/net0...lt "ac")) / mag(v("/net0168" ?result "ac")))) Thu Dec 15 04:47:36 2022 1



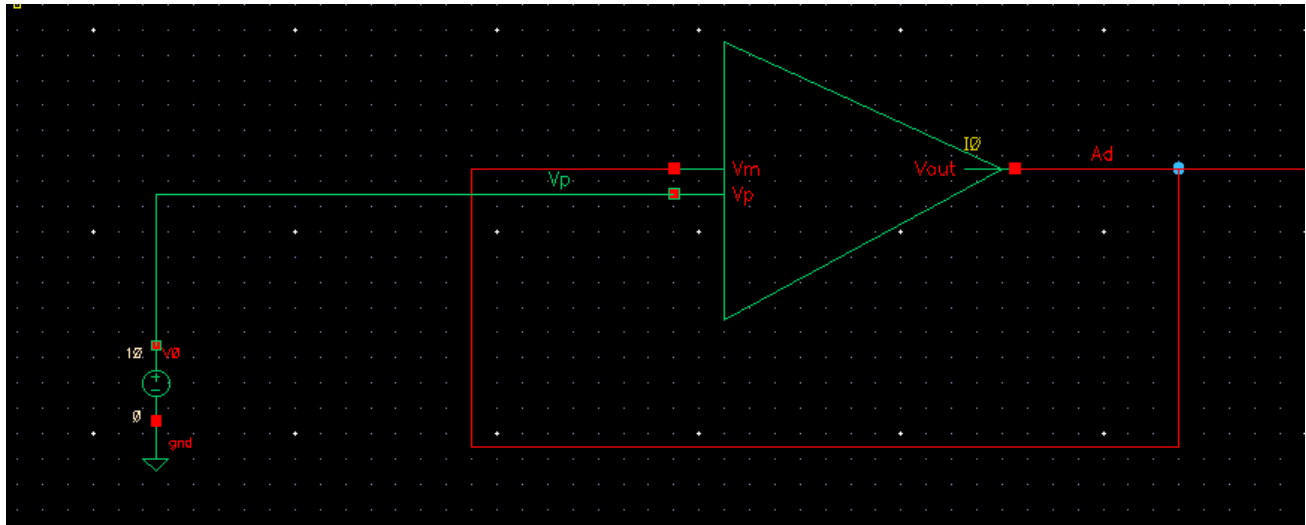
(182666 / (mag(v("/Vout" ?result "ac")) / ma... "ac")) / mag(v("/net0168" ?result "ac")))) Thu Dec 15 04:52:32 2022 1



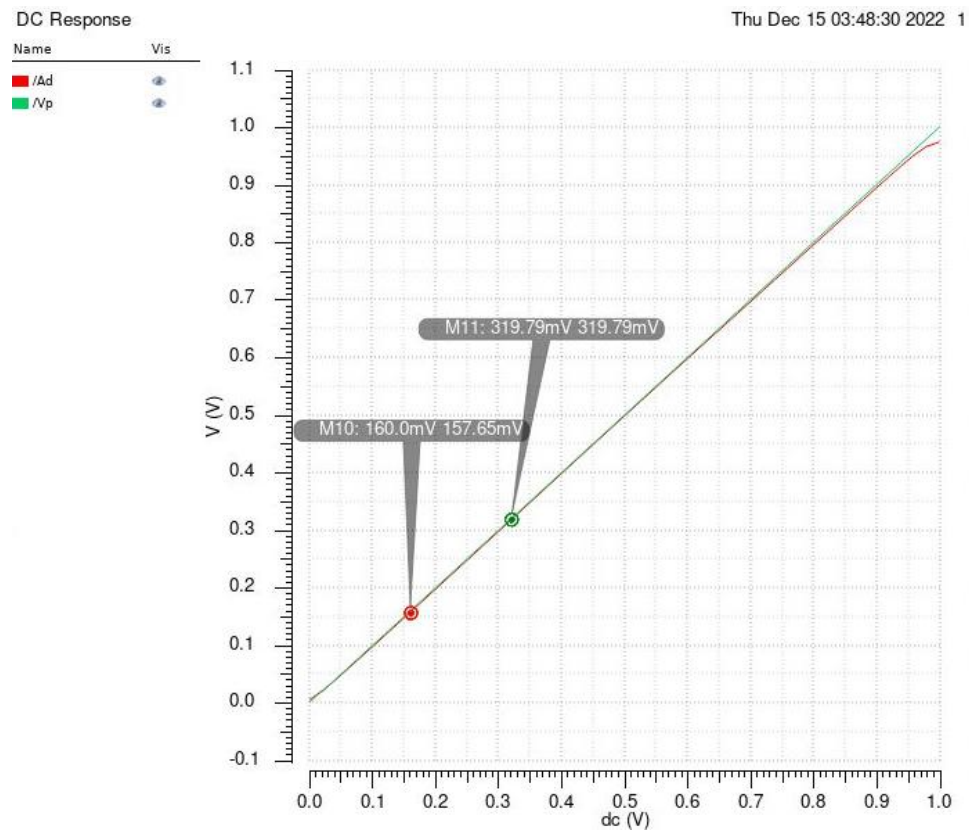
Hand calculation matched simulation.



## Nominal Output Voltage (V)



A Unity Gain Buffer or Voltage Follower Configuration is needed for this simulation



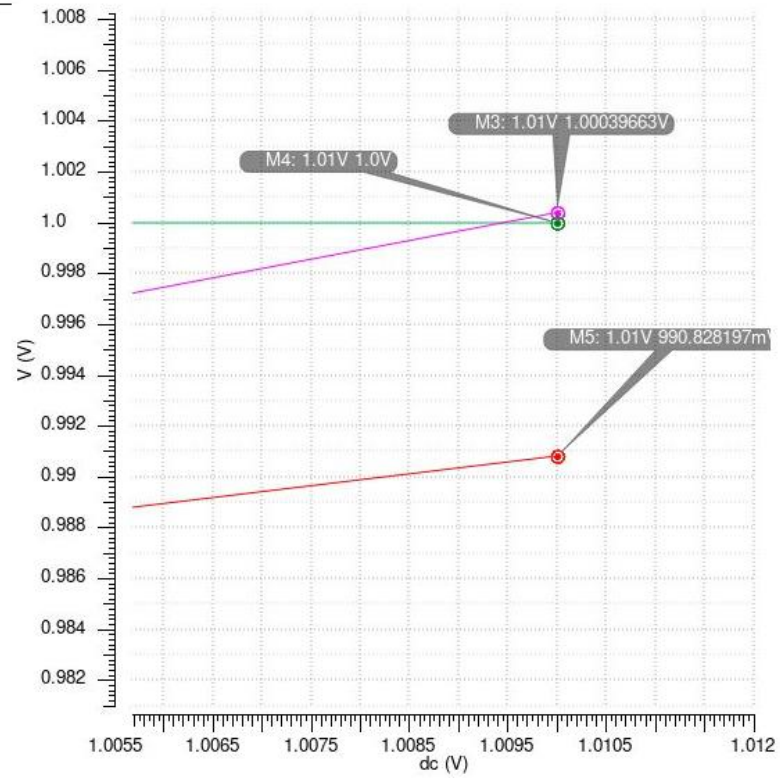
Both the Output and the Input lines follow each other when swept.

## Input Offset Voltage (Mv)

DC Response

Thu Dec 15 03:35:28 2022 1

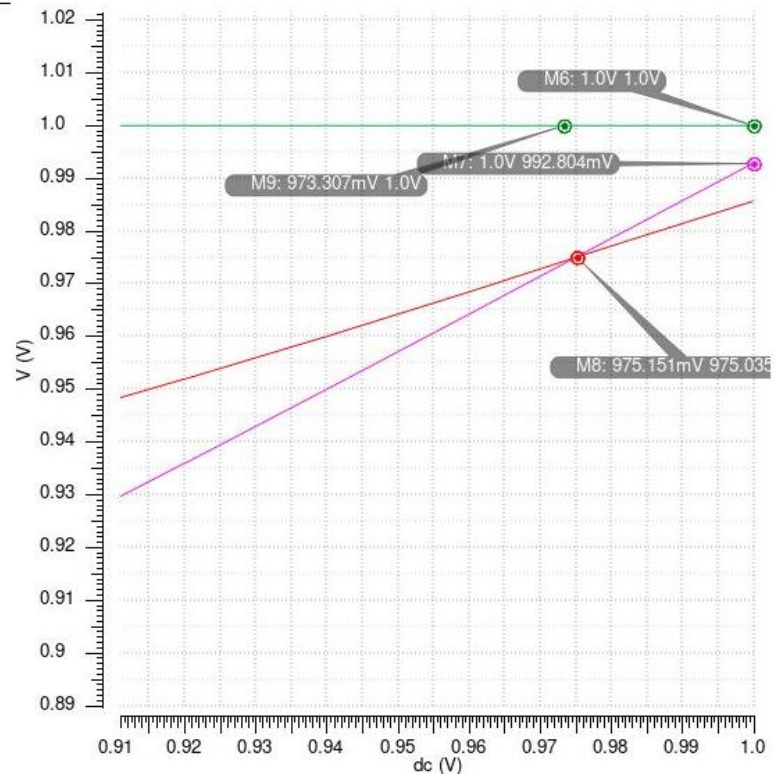
Name	Vis
<span style="color: red;">■</span> /Ad	<input checked="" type="checkbox"/>
<span style="color: green;">■</span> /Vp	<input checked="" type="checkbox"/>
<span style="color: magenta;">■</span> /Vm	<input checked="" type="checkbox"/>



DC Response

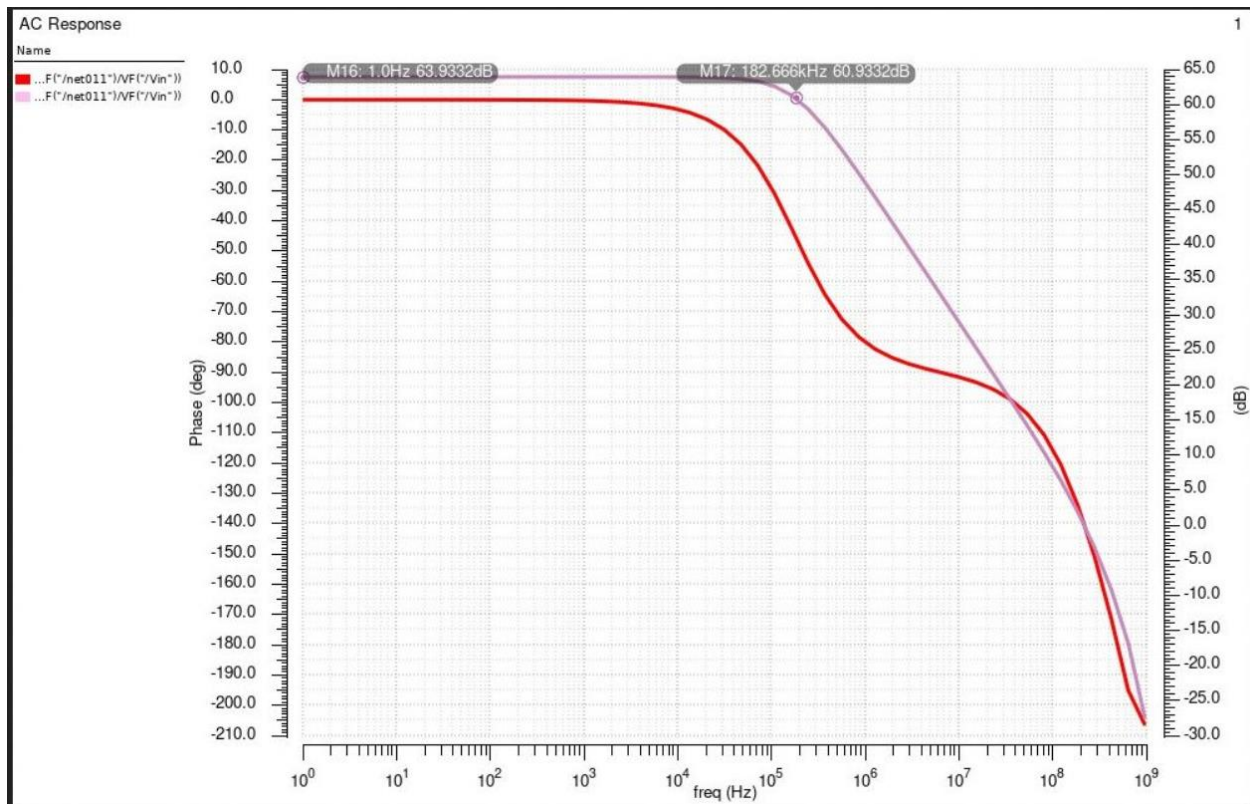
Thu Dec 15 03:38:37 2022 1

Name	Vis
<span style="color: red;">■</span> /Ad	<input checked="" type="checkbox"/>
<span style="color: green;">■</span> /Vp	<input checked="" type="checkbox"/>
<span style="color: magenta;">■</span> /Vm	<input checked="" type="checkbox"/>



An offset is applied to one of the terminal results in a small error in the output

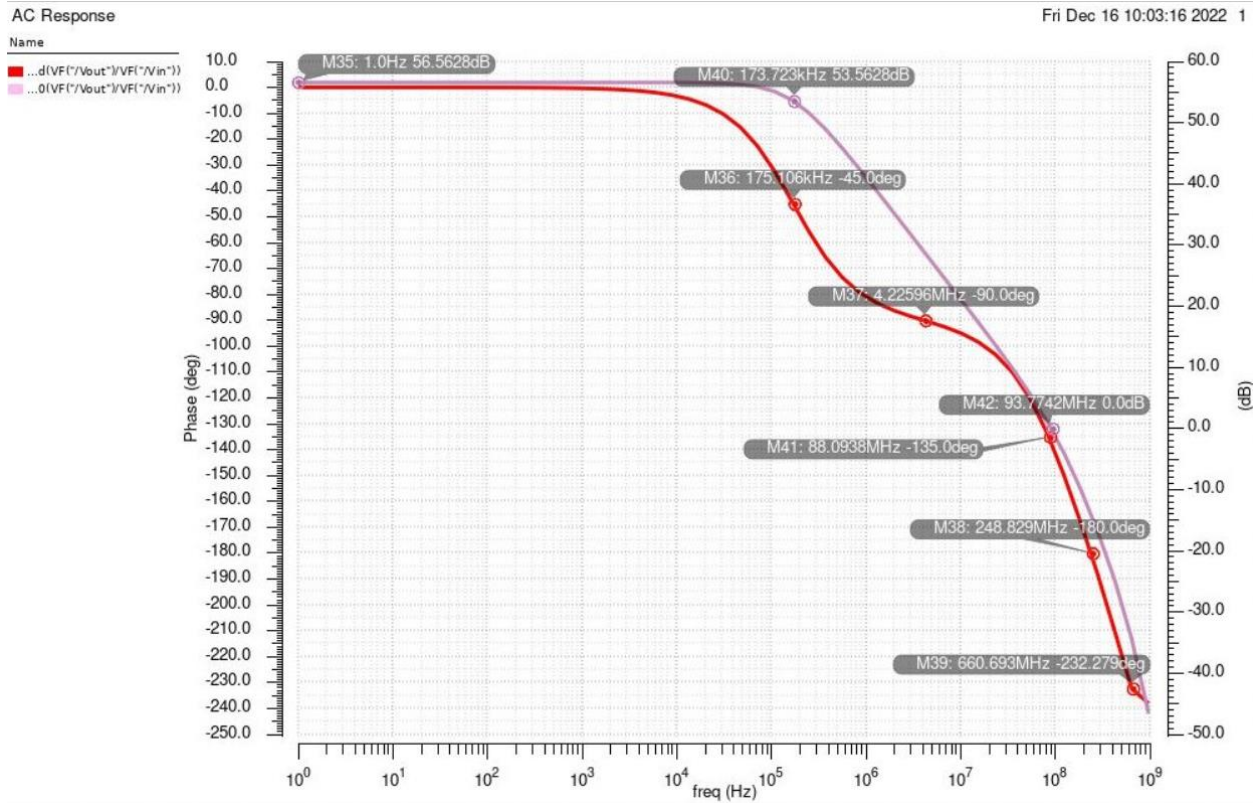
## Unloaded Bandwidth (kHz)



Unloaded Bandwidth = 182.666kHz

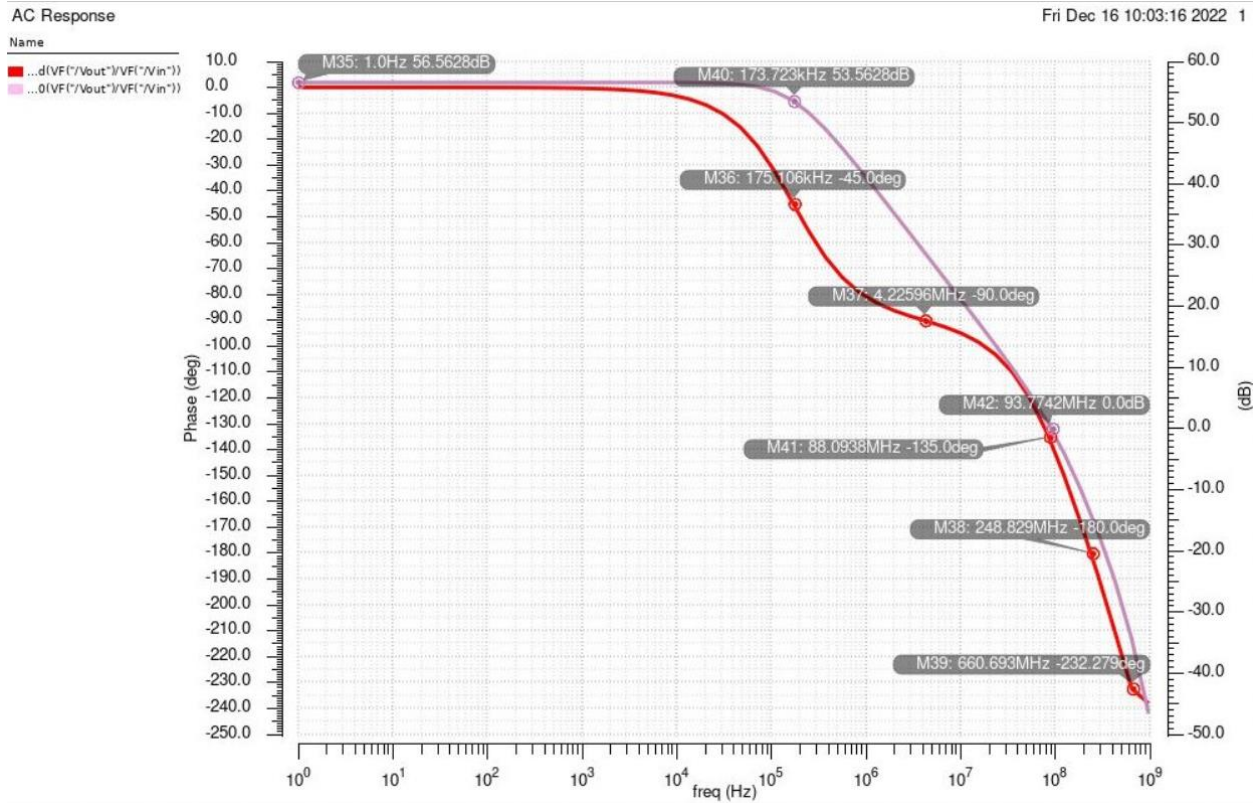
## Loaded Bandwidth (kHz)





Loaded Bandwidth = 178.723kHz

**Gain-Bandwidth Product (MHz)**

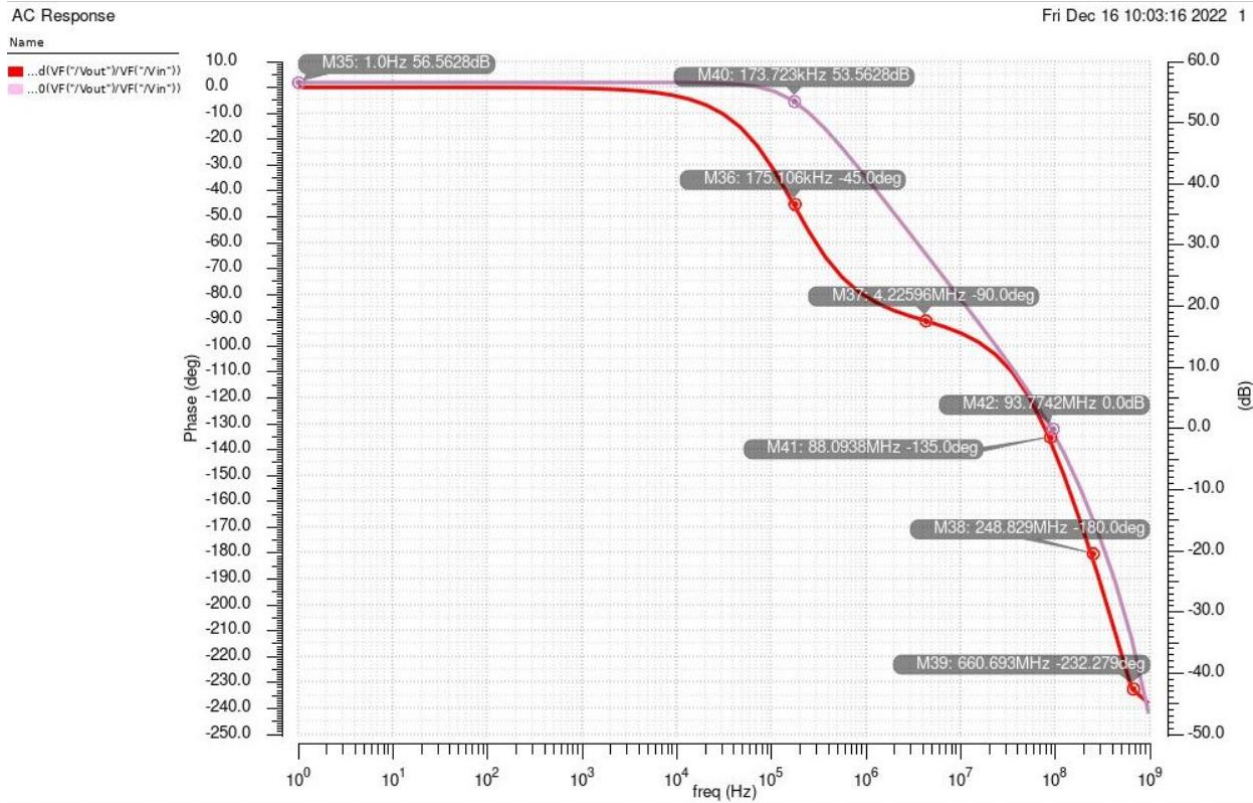


Gain-Bandwidth Product = 93.7742 MHz

## Compensation Capacitor (pF)

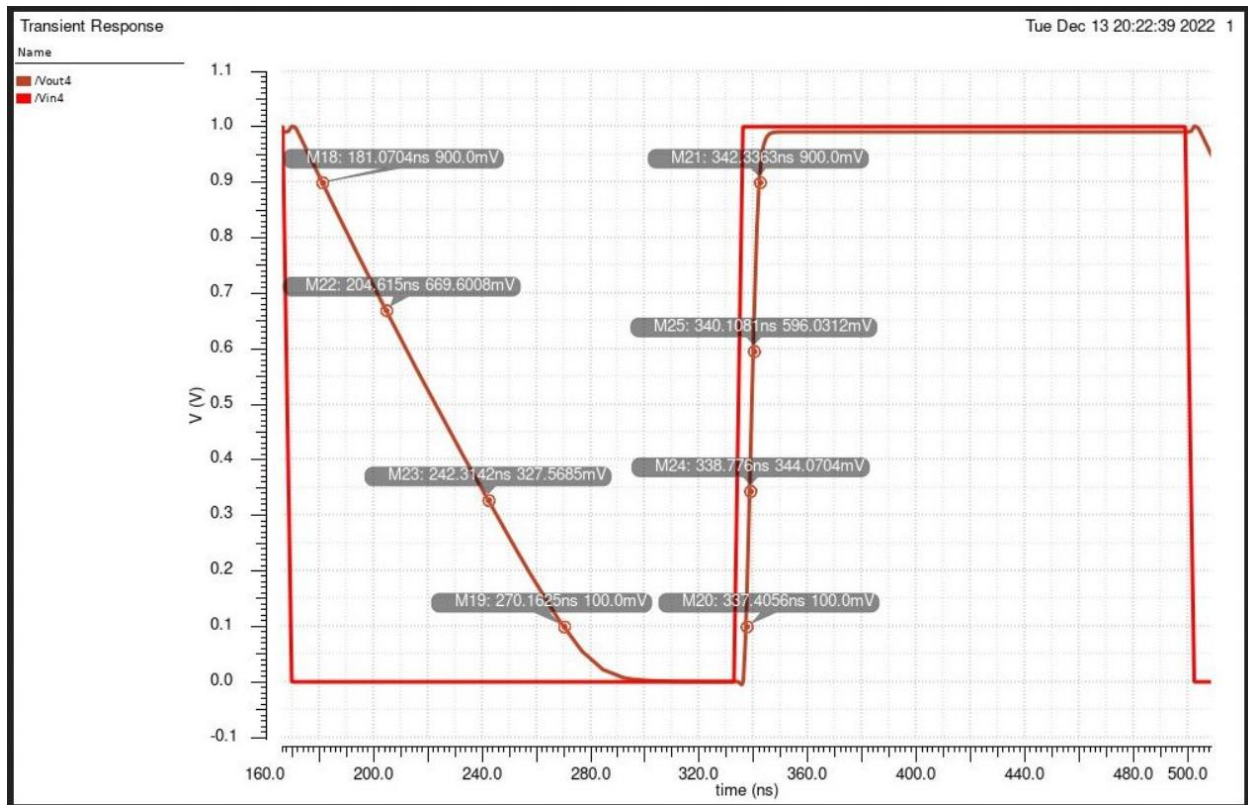
Compensation Cap = 480pF [1]

## Phase Margin (Degrees)



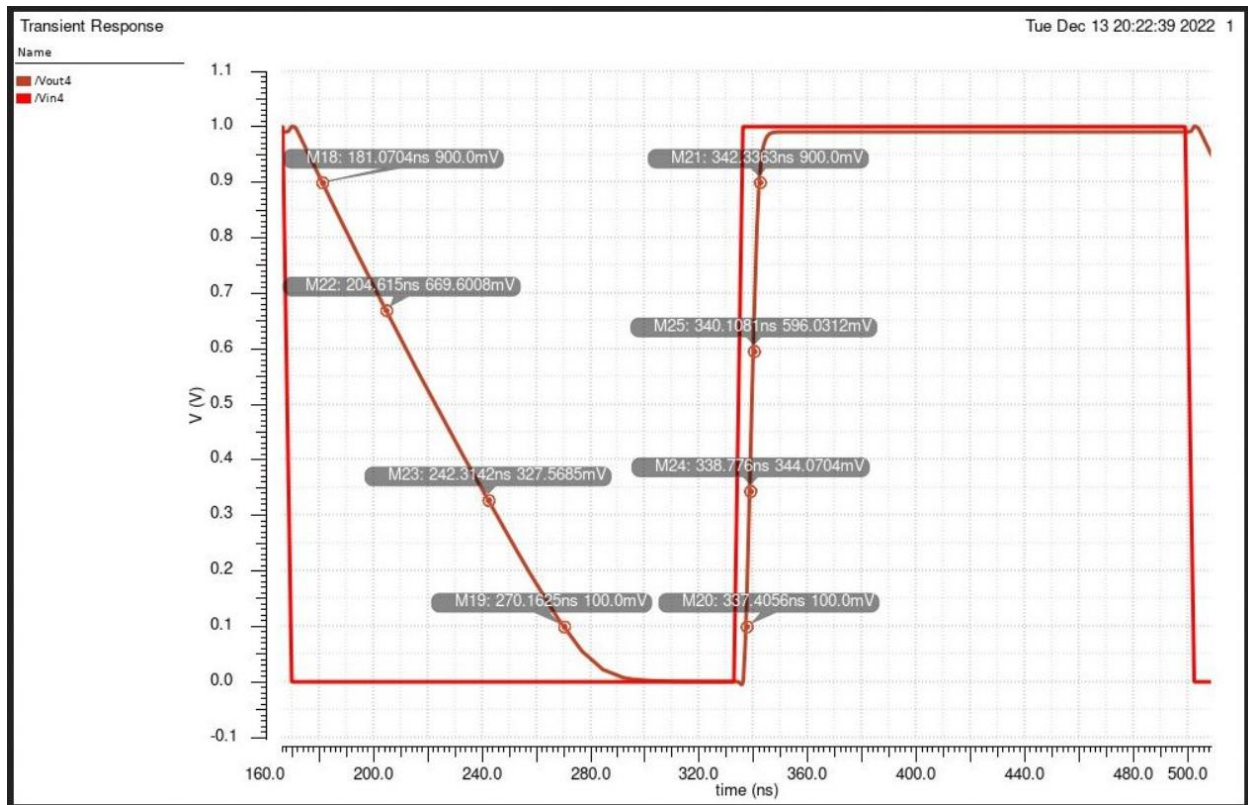
$$\text{Phase Margin} = | -232.279 + 180 | = 52.279 \text{ degrees}$$

## Rise Time (ns) (Step Response)



$$\text{Rise Time} = 342.3363\text{ns} - 337.4056\text{ns} = 4.93\text{ns}$$

**Fall Time (ns) (Step Response)**



$$\text{Fall Time} = 270.1625\text{ns} - 181.0704\text{ns} = 89\text{ns}$$

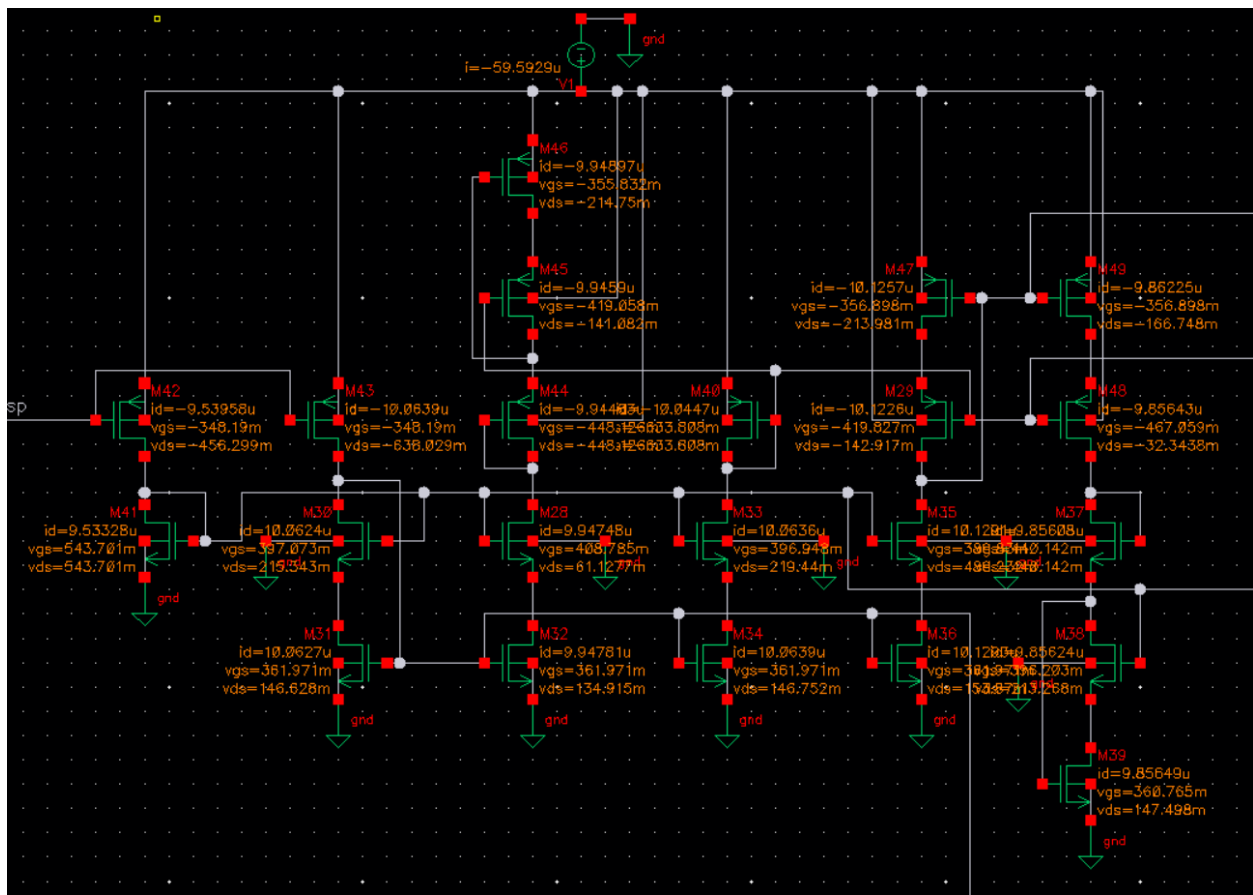
## Settling Time (ns) (Step Response)



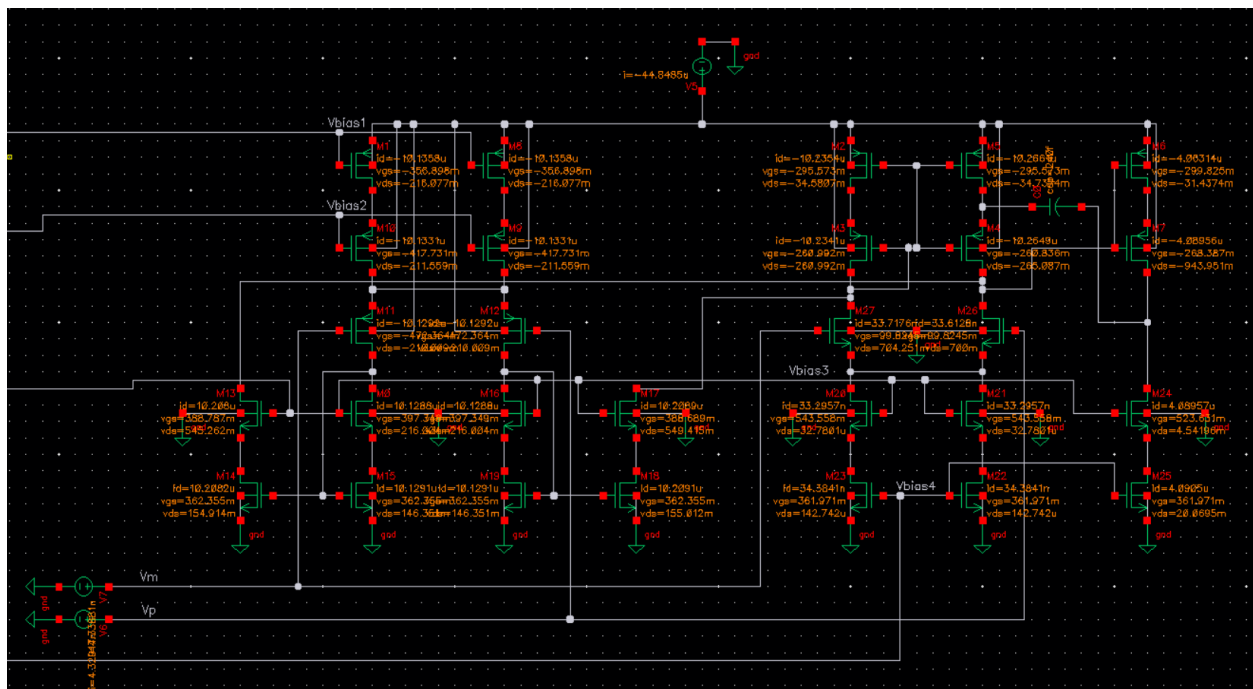
The schematic illustrates a 10-bit DAC using a 2-5T1 architecture. It consists of the following components and parameters:

- Transistors:**
  - M50-M59:** NMOS transistors.
    - M50:  $I_D = -5.3291\mu$ ,  $V_{GS} = -966.221m$ ,  $V_{DS} = -966.221m$
    - M51:  $I_D = -10.0863\mu$ ,  $V_{GS} = -348.19m$ ,  $V_{DS} = -646.02m$
    - M52:  $I_D = -11.9665\mu$ ,  $V_{GS} = -363.456m$ ,  $V_{DS} = -363.456m$
    - M53:  $I_D = -11.9034\mu$ ,  $V_{GS} = -363.456m$ ,  $V_{DS} = -348.19m$
    - M54:  $I_D = -10.0842\mu$ ,  $V_{GS} = -348.19m$ ,  $V_{DS} = -646.271m$
    - M55:  $I_D = 1.37314n$ ,  $V_{GS} = -348.19m$ ,  $V_{DS} = 0$
    - M56:  $I_D = 5.34198\mu$ ,  $V_{GS} = 353.98m$ ,  $V_{DS} = 33.7791m$
    - M57:  $I_D = 80.3814p$ ,  $V_{GS} = 320.201m$ ,  $V_{DS} = 297.83m$
    - M58:  $I_D = 10.0858\mu$ ,  $V_{GS} = 353.98m$ ,  $V_{DS} = 353.98m$
    - M59:  $I_D = 11.9681\mu$ ,  $V_{GS} = 354.728m$ ,  $V_{DS} = 636.544m$
    - M60:  $I_D = 11.9073\mu$ ,  $V_{GS} = 353.98m$ ,  $V_{DS} = 651.81m$
    - M61:  $I_D = 10.0838\mu$ ,  $V_{GS} = 299.266m$ ,  $V_{DS} = 299.288m$
  - Current Source:**
    - V2:** PMOS transistor acting as a current source,  $I = -49.3866\mu$ .
  - Resistor:**
    - R0:** Load resistor,  $R = 55.4624m\Omega$ ,  $V = 55.4624m$ ,  $I = 10.0841\mu$ ,  $PWR = 559.287n$ .

The circuit is powered by a ground reference (gnd) and includes various biasing and signal lines. The output is taken from the drain of M59, which is connected to a load resistor R0 and a ground.



Throughout the bias circuit the branch current is roughly 10uA as per Baker's standards.



$$@ V_m = V_p = 100\text{mV}$$

In the amplifier circuit, however, the current will max at 10uA but the current of a branch at any given time is dependent on the current operating conditions (+ and – terminal voltages, mainly)



## Part 2: Report Tables

**Table 1: Partner Contributions to Circuit Design and Report**

Contribution	Drew	Jonathan
Researching Topologies	X	X
Implementing Topology	X	X
Modifications to Reach Specified Gain	X	
CMRR		X
Timing Related Measurements	X	
ICMR	X	
Output Swing	X	
PSRR		X
Nominal + Offset Voltages		X
Frequency Response	X	
DC Currents in Branches	X	
All Power Related Measurements		X
Tables	X	

**Table 2: Specifications vs. Actual Results**

Criteria	Specified Value	Achieved
Max Power Consumption	40 $\mu$ W	33 $\mu$ W
Differential Gain	60dB	56.5628 dB
CMRR	110dB	99.107dB
ICMR	0-1V	0-1V
Output Swing	.1-.9V	587.3uV – 991.192mV
Bandwidth	10kHz	178.723kHz
Slew Rate (V/us)	4 V/ $\mu$ s	Worst: 9.26V/ $\mu$ s

# References

- [1] Baker, R. J. (2019). In CMOS: Circuit Design, Layout, and Simulation (4th ed., pp. 657–821). essay, Wiley.