ECE 4902 Analog Integrated Circuit Design – Project Report

Worcester Polytechnic Institute

B-Term 2022

Project 2: Two-Stage Op-Amp 50n Short Channel Implementation

Submitted by

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Professor Guler

Part 1: Op Amp Final Specs and Simulation Results

Differential Amplifier Topology

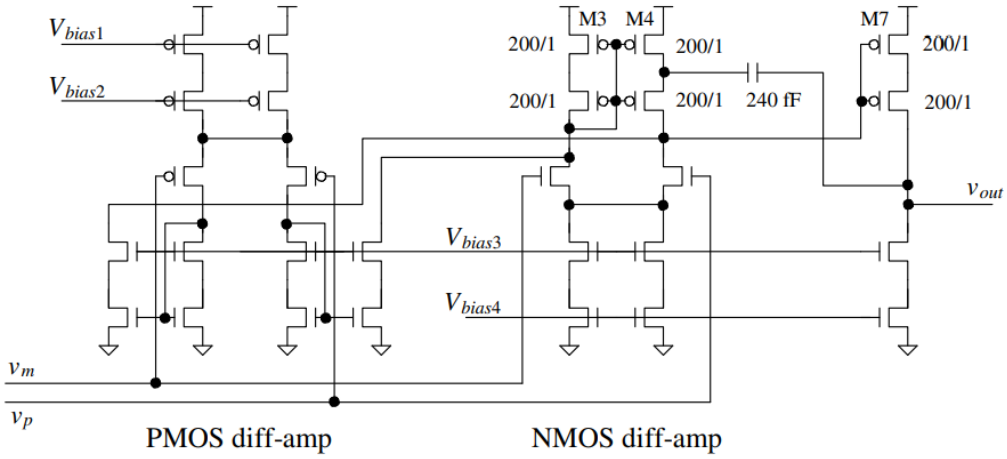
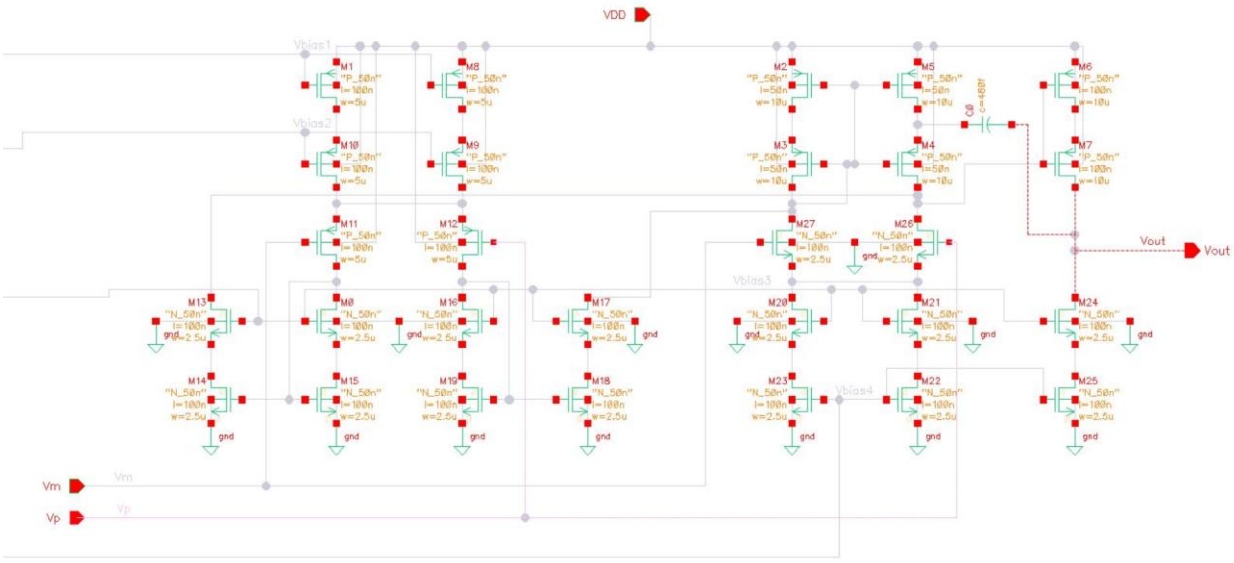


Figure 24.28 Two-stage op-amp of Fig. 24.21 with rail-to-rail input range.

We used the above topology from R. Jacob Baker's Circuit Design, Layout, and Simulation textbook. [1]



Reference Topology

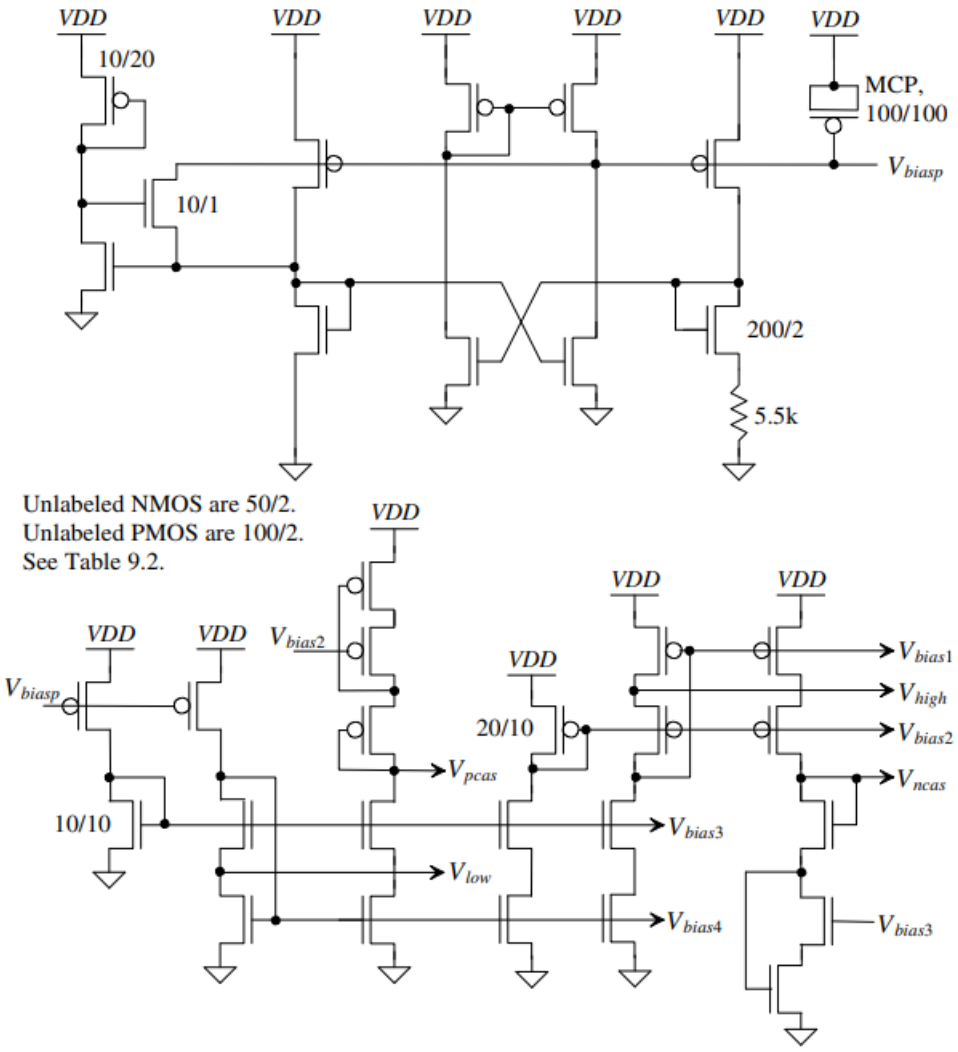
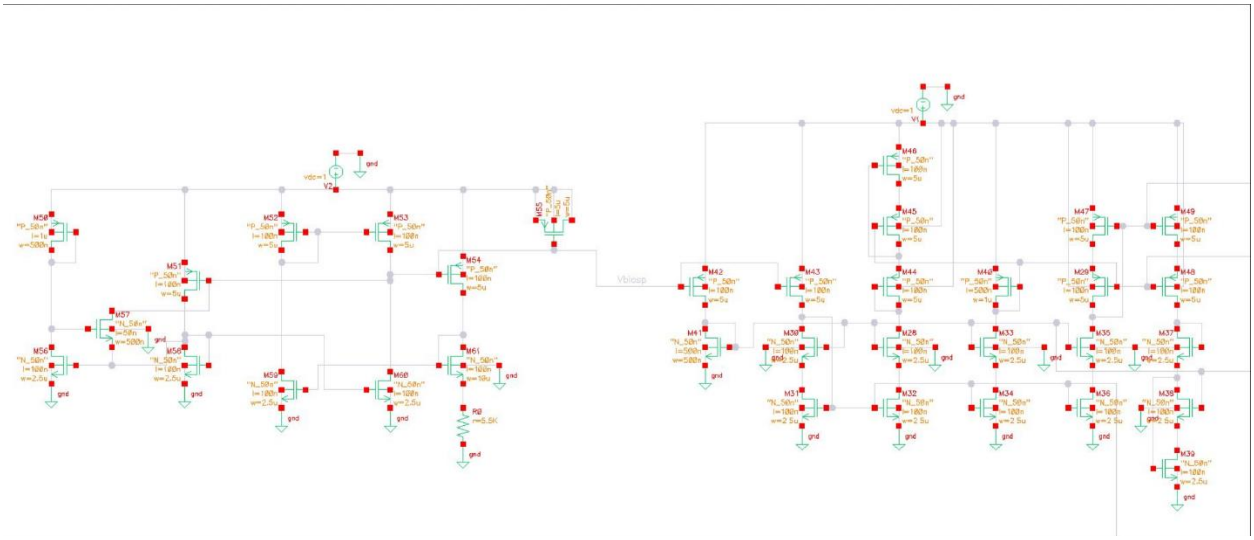
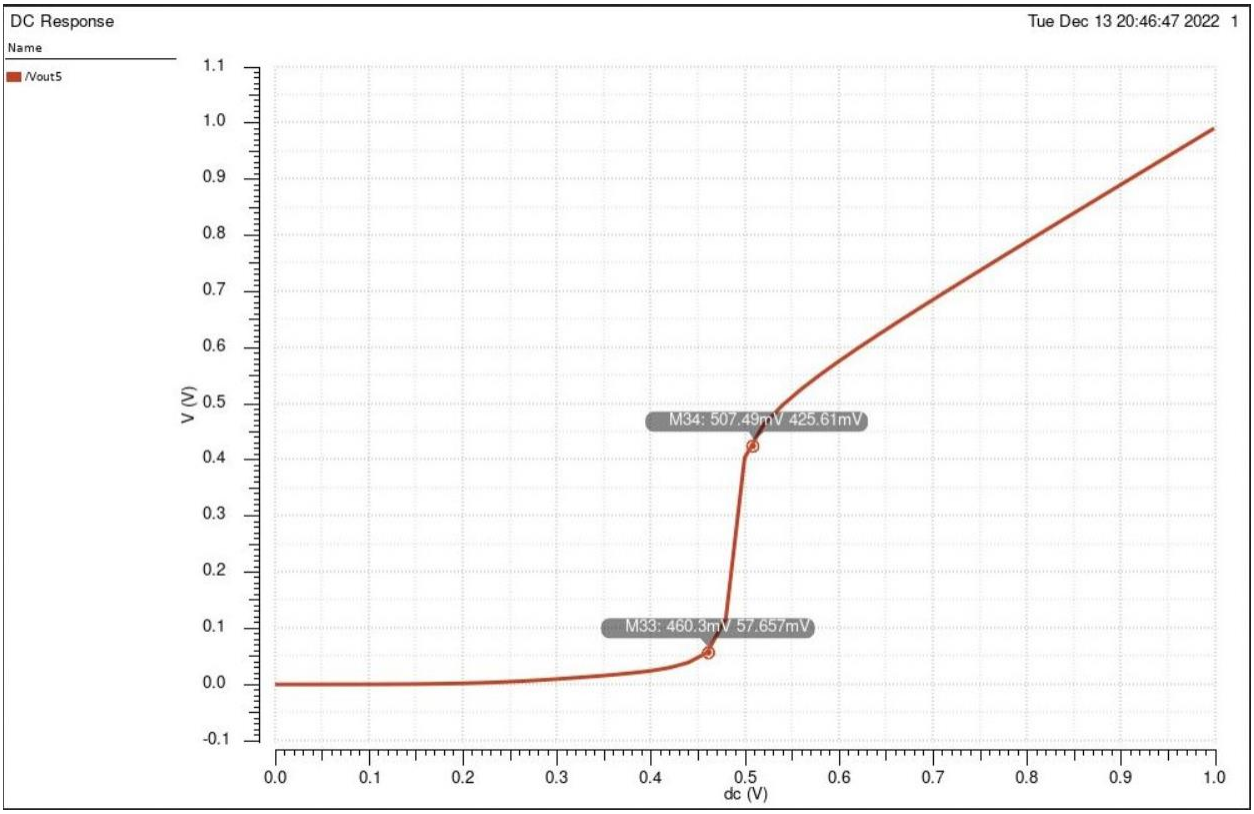


Figure 20.47 General biasing circuit for short-channel design using the data in Table 9.2.

We also used the above bias circuit from R. Jacob Baker's Circuit Design, Layout, and Simulation textbook in making our op-amp. [1]

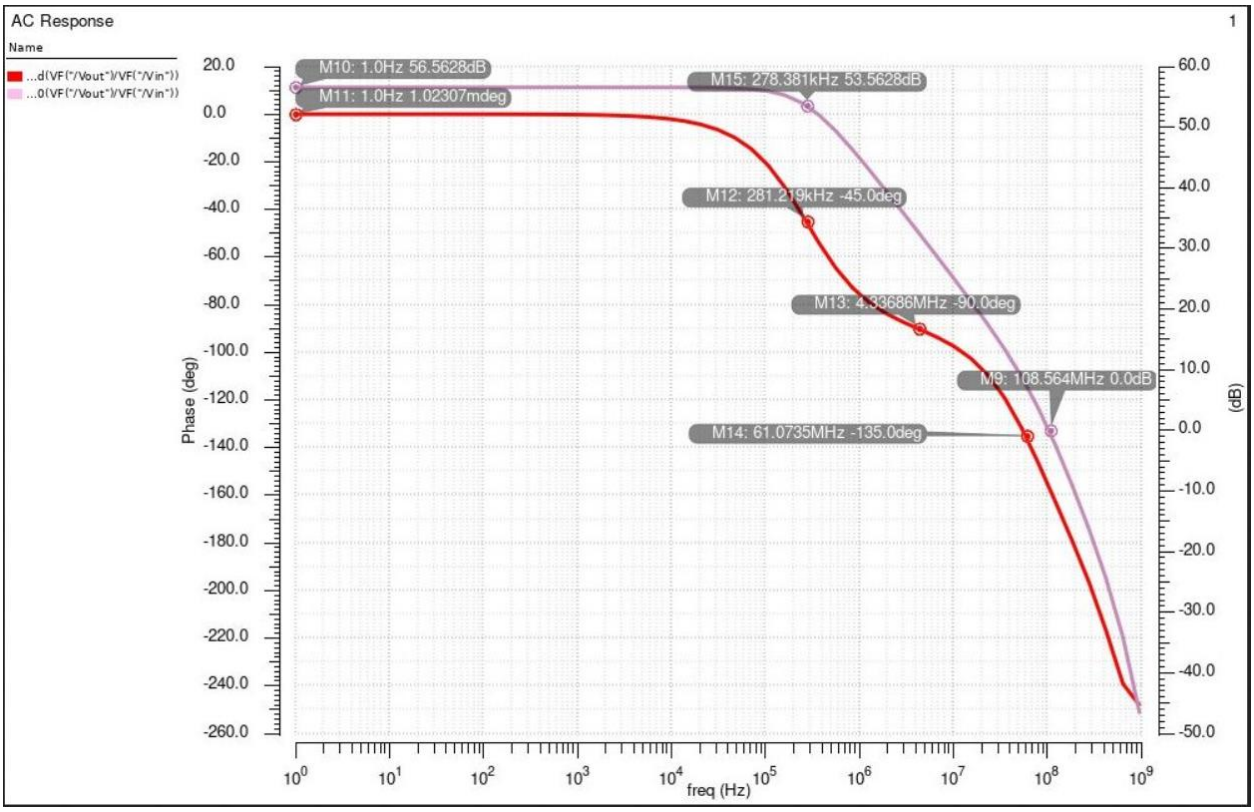


Minimum Supply Voltage (V)



The minimum supply voltage needed for this amplifier to work was between 460mV-507mV.

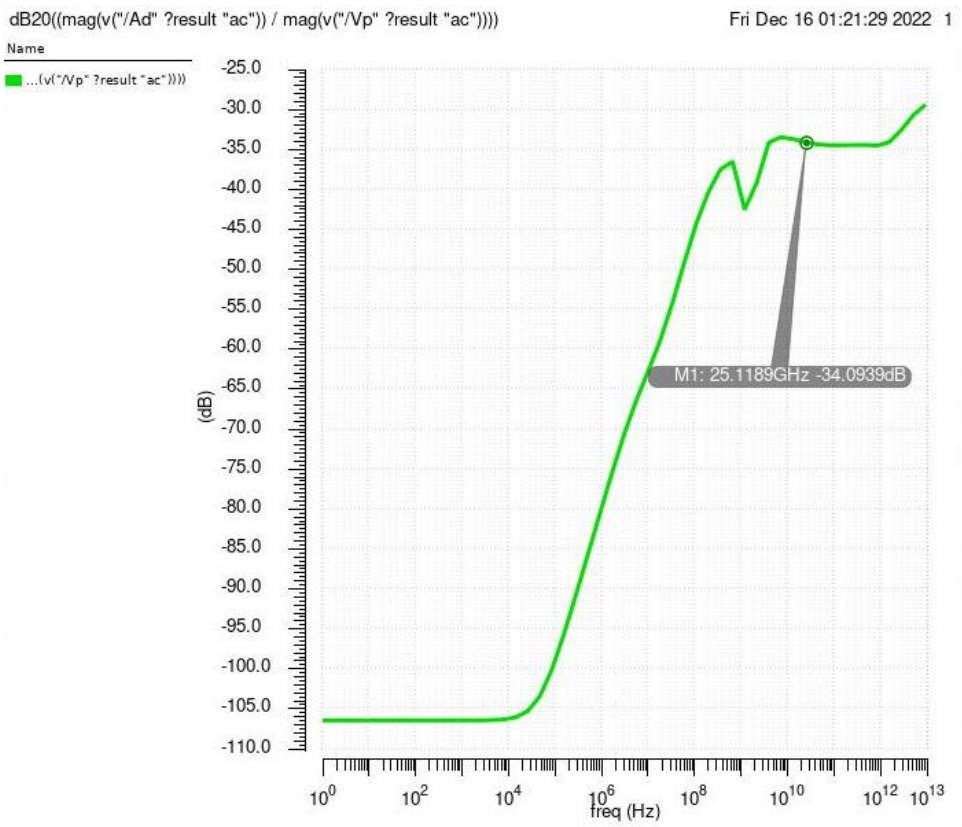
Gain of Differential Amplifier (dB)



The differential gain of the operational amplifier was 56.5628 dB, as seen in the figure above.

CMRR (dB) (Low Freq and Spectrum)

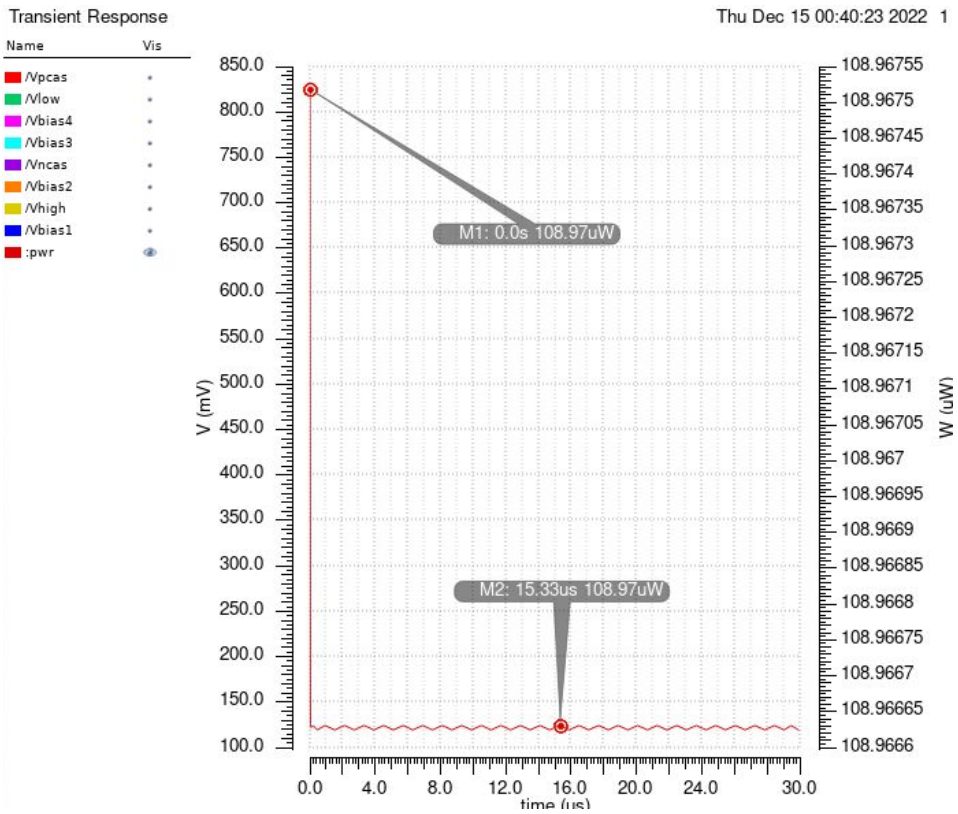
The picture can't be displayed.



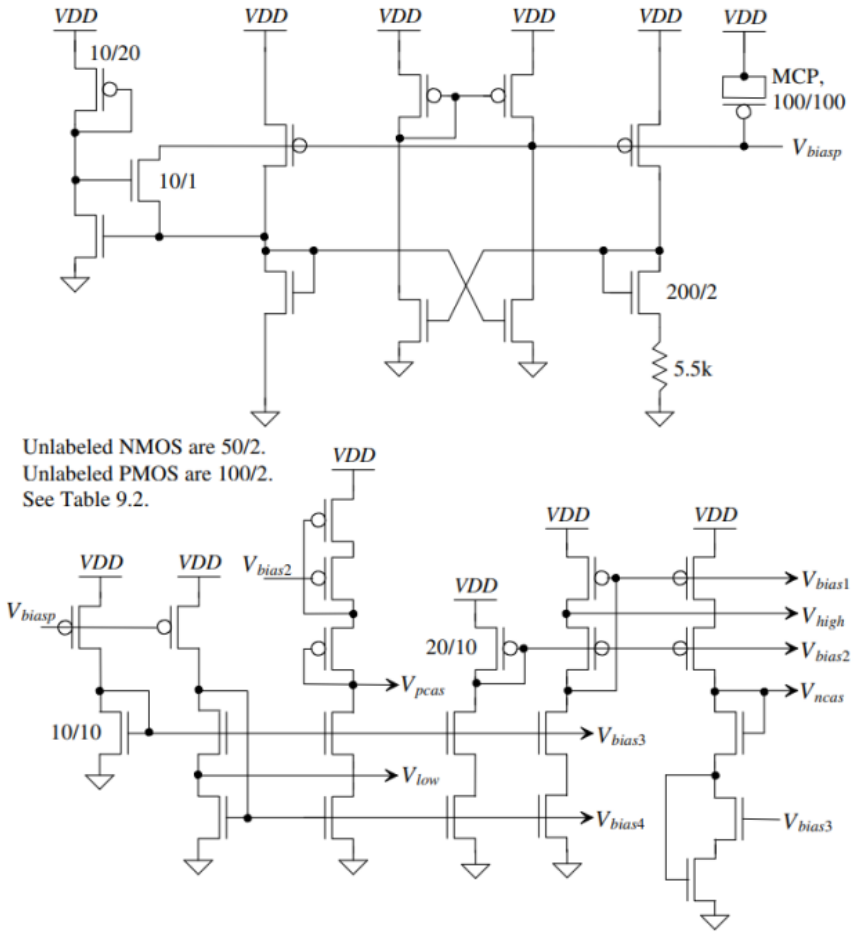
We found the Differential gain now for the Common Mode Gain Acm.

CMRR = 20log|(278.381kHz/25.1189GHz) | = 99.107dB which is in range of the 110 +- 10%

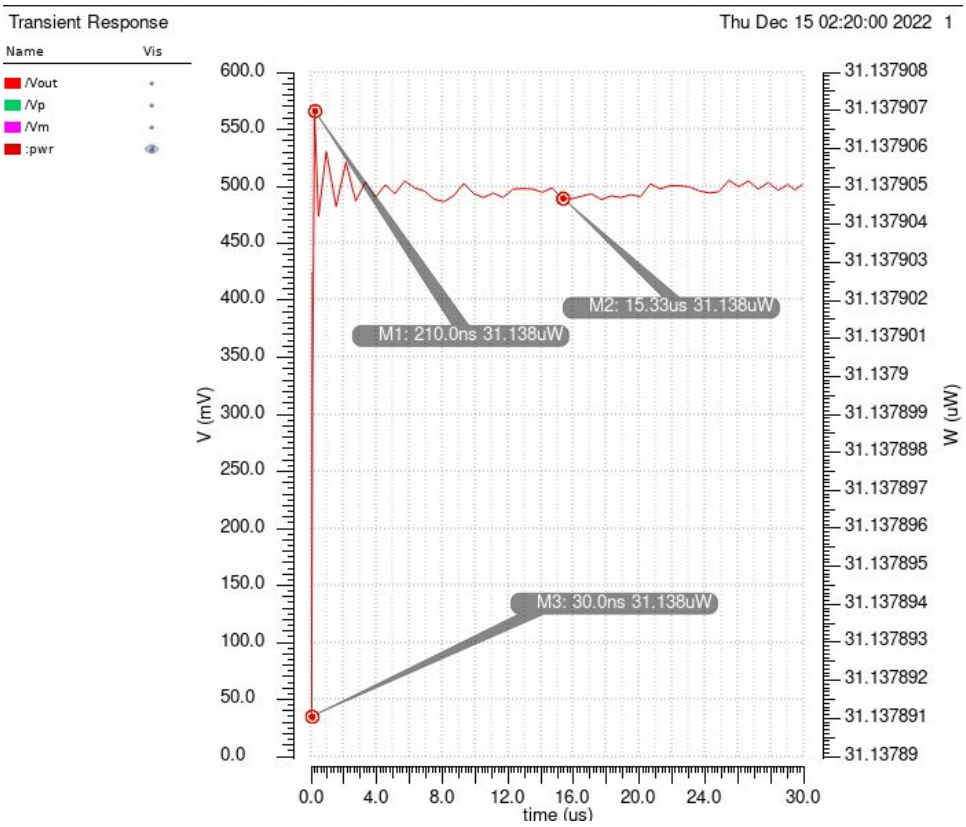
Reference Power Consumption (uW)



With no Ideal DC sources allowed beside VDD, the operational amplifier needed proper biasing. This is achieved via the via biasing circuit in R. Jacob Baker's Circuit Design, Layout, and Simulation. It used about 109µW

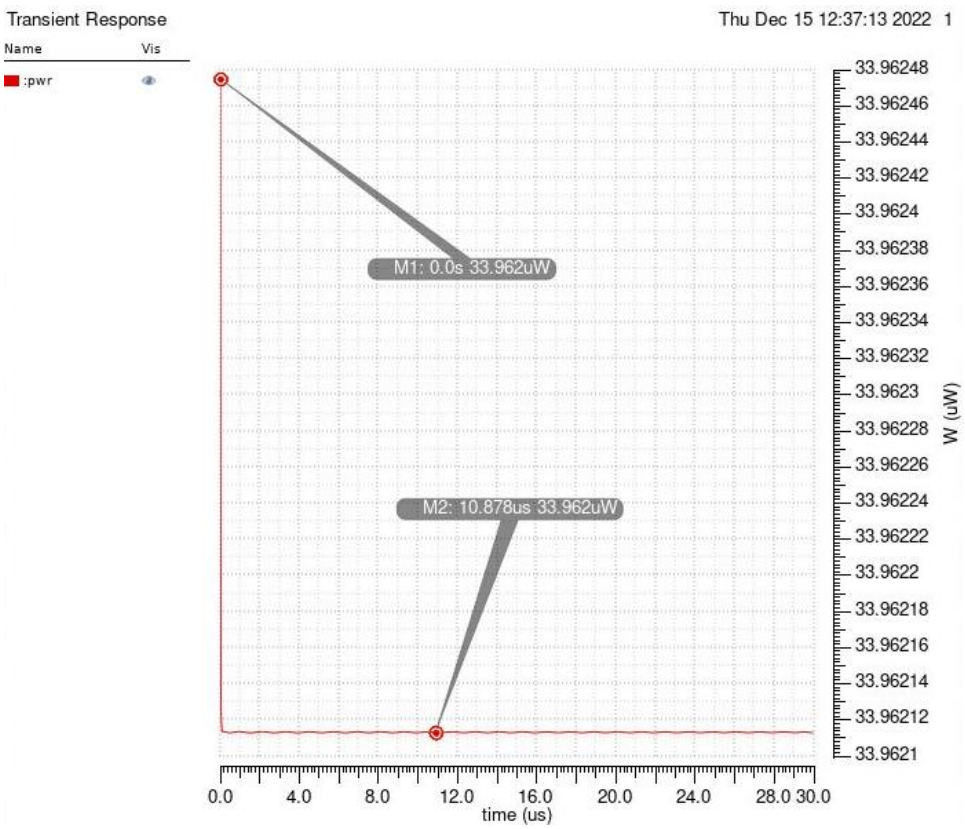


Op Amp Power Consumption with Zero Input (uW)



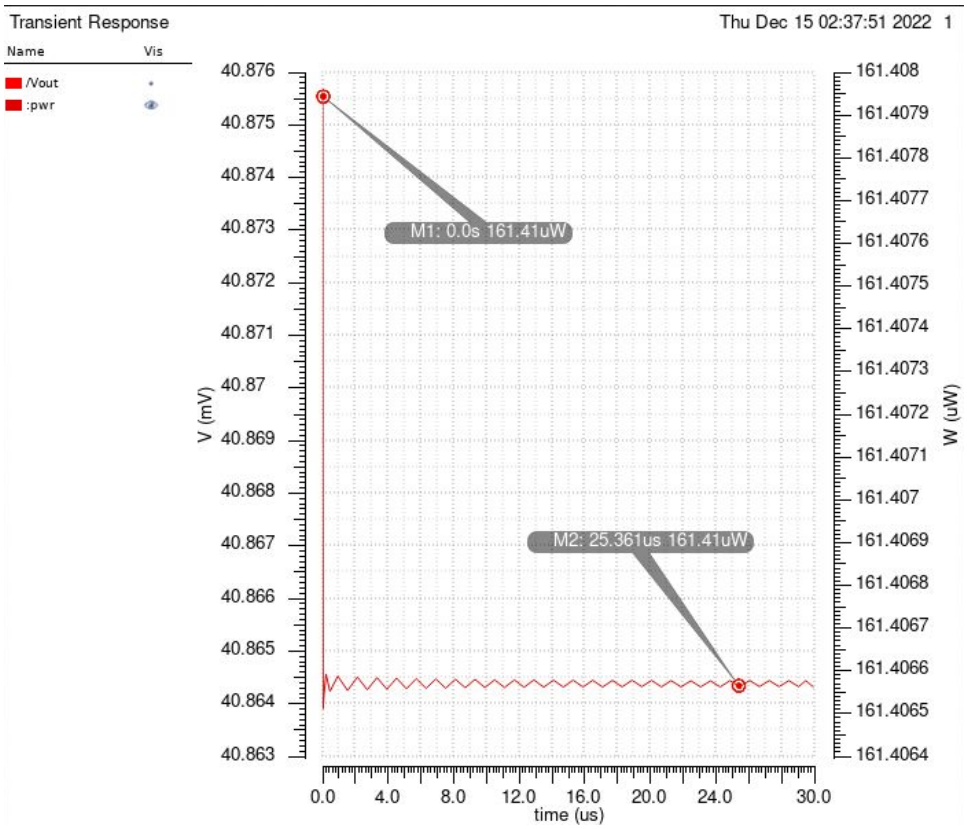
This is within spec as the maximum wattage is 40µW and we are pulling about 31µW

Op Amp Power Consumption with No Load (uW)



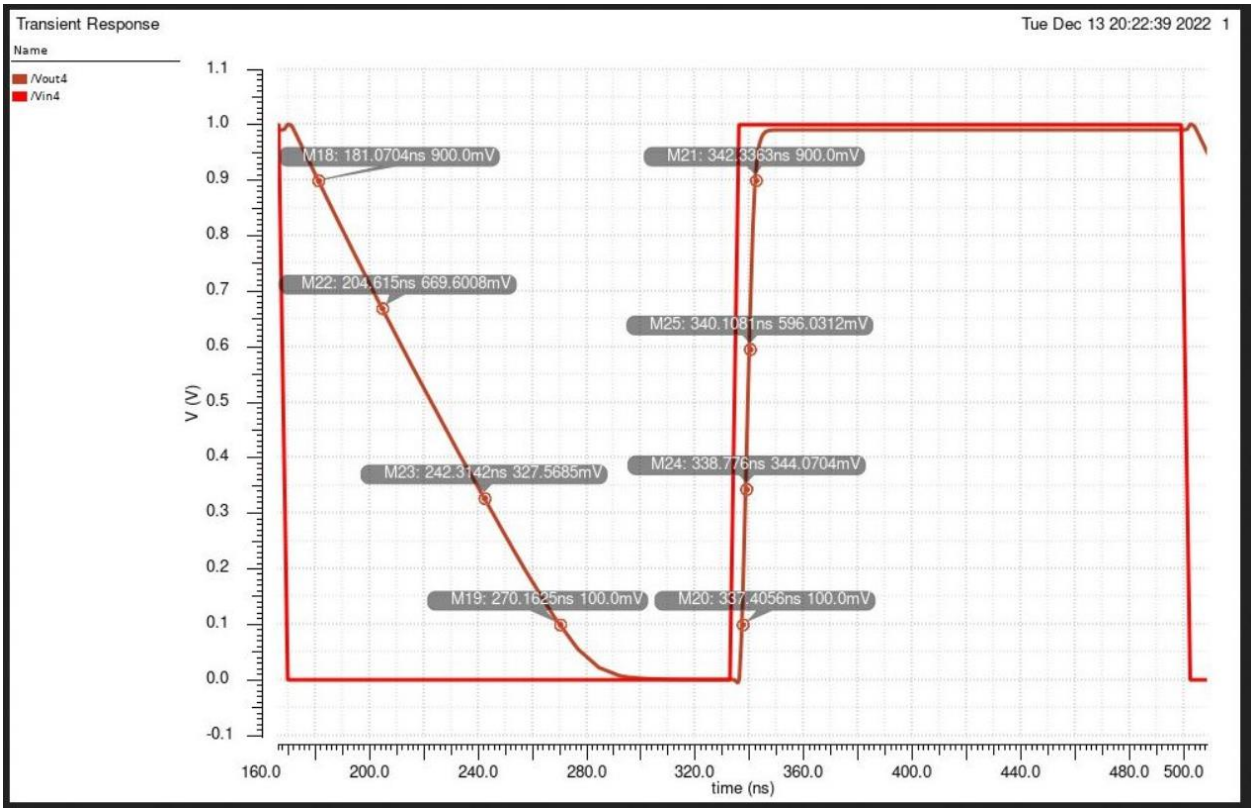
This is within spec as the maximum wattage is 40µW and we are pulling about 33µW

Total Power Consumption (uW)



This is our total power consumption with the biasing circuit, the 2-stage amplifier, and the load. 161µW is our Maximum power consumption.

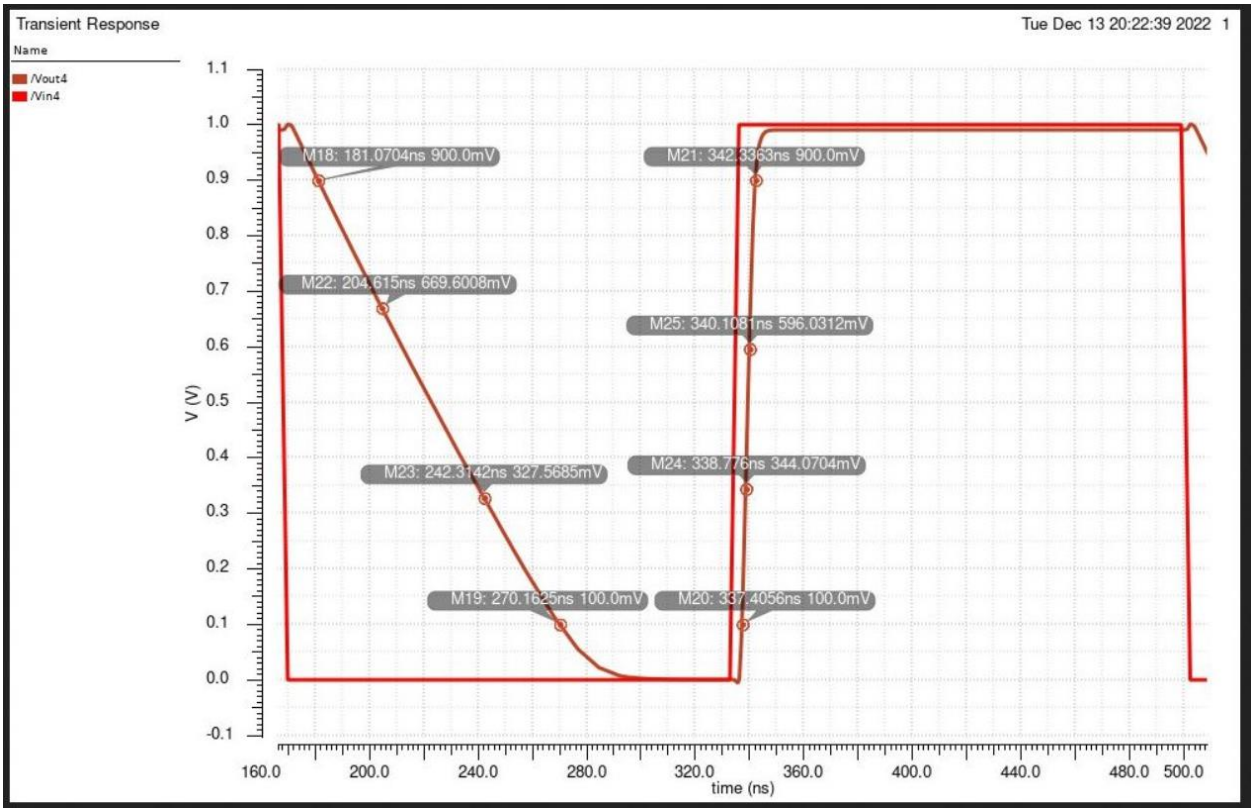
Positive Slew Rate (V/us)



The positive slew rate was calculated using the above figure:

Slew Rate = (Delta) Voltage / (Delta) Time = (596mV - 344mV) / (340 ns – 338.8 ns) = 210V/uS

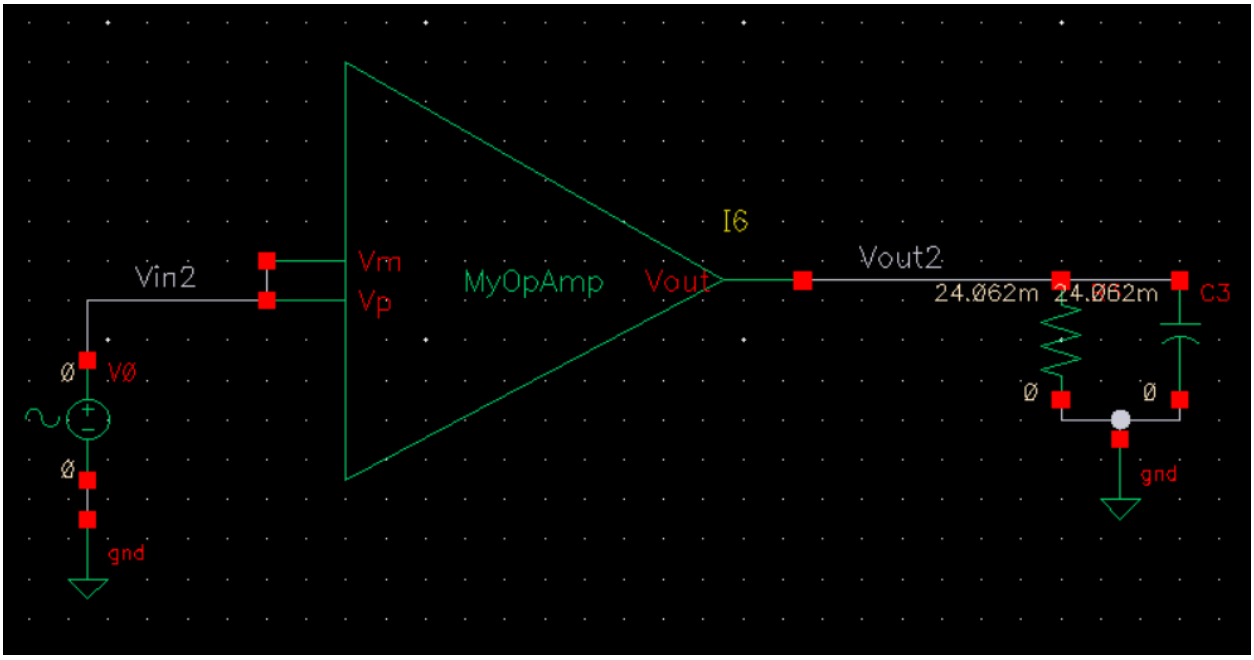
Negative Slew Rate (V/us)

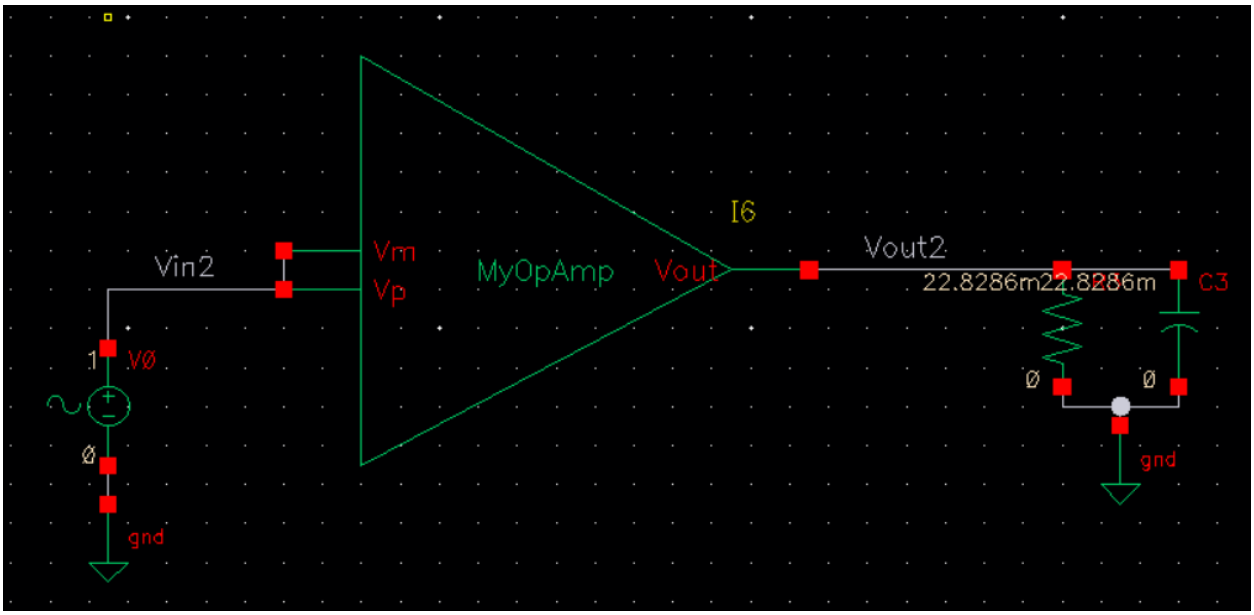


The negative slew rate was calculated using the above figure:

Slew Rate = (Delta) Voltage / (Delta) Time = (670mV - 327.5mV) / (242 ns - 205 ns) = 9.26v/uS

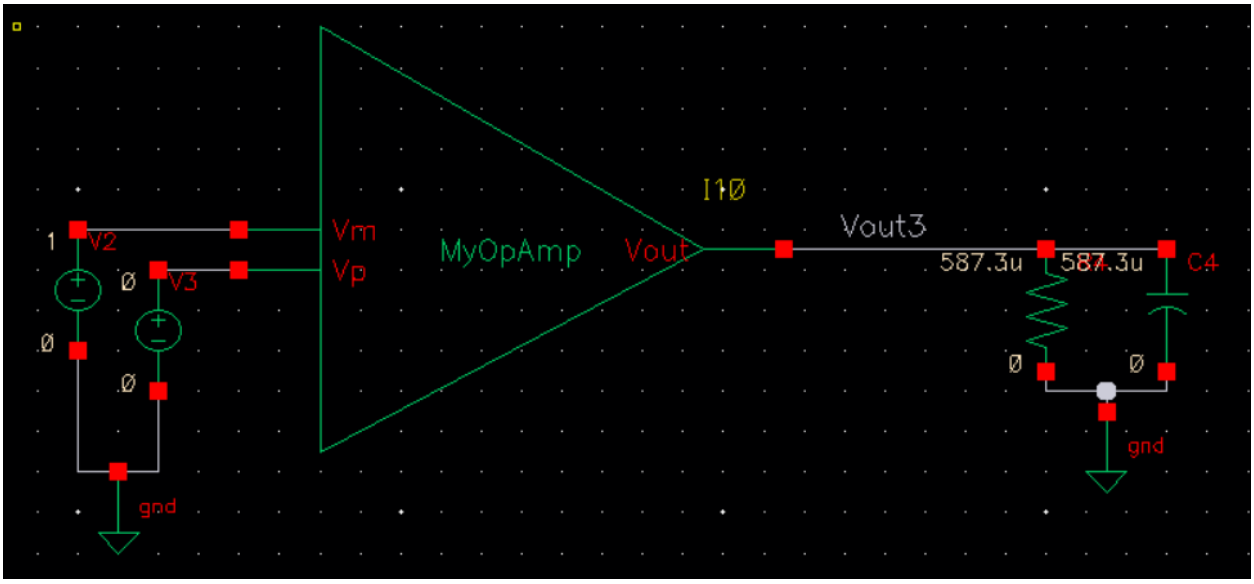
ICMR (Vmin ~ Vmax)

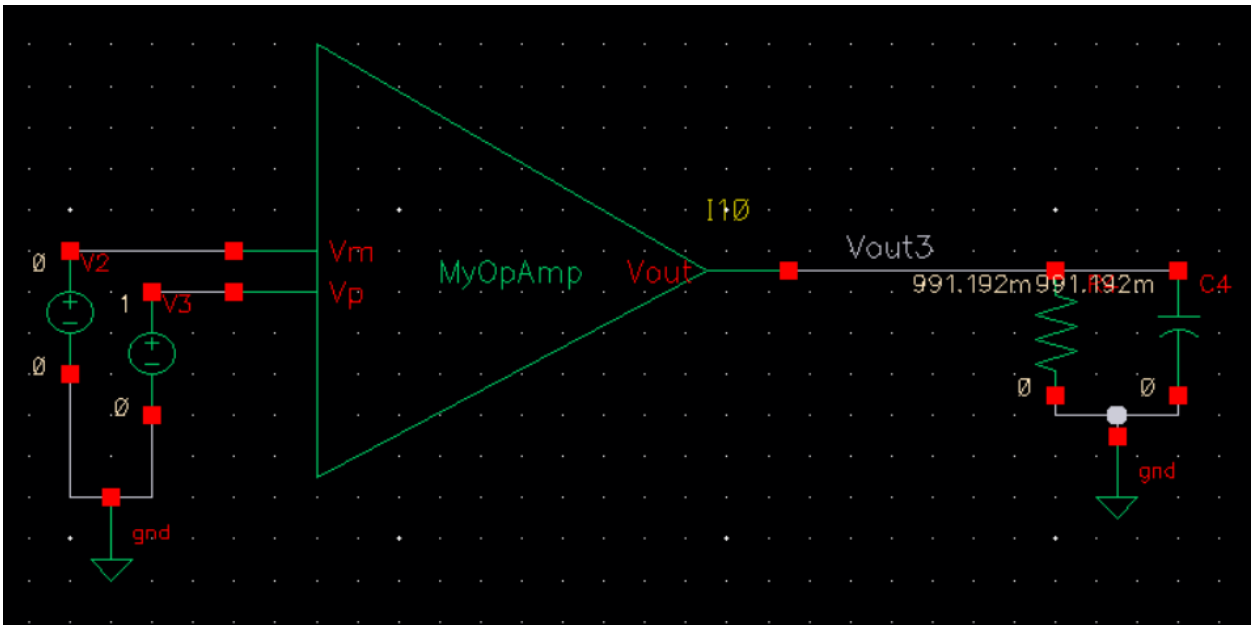




0V < ICMR < 1V

Output Swing (Vmin ~ Vmax)

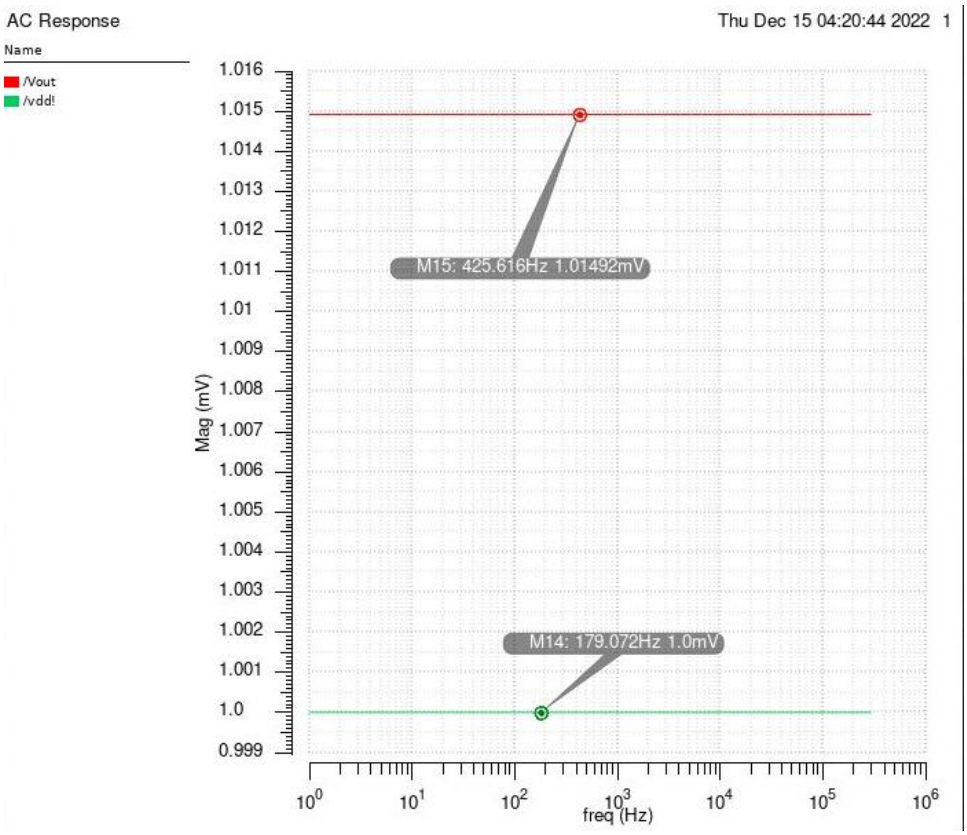




Output Swing = 587.3uV – 991.192mV

VDD PSRR (dB)

$$PSRR^{+} = \frac{A_{OL}(f)}{v_{out}/v^{+}}$$



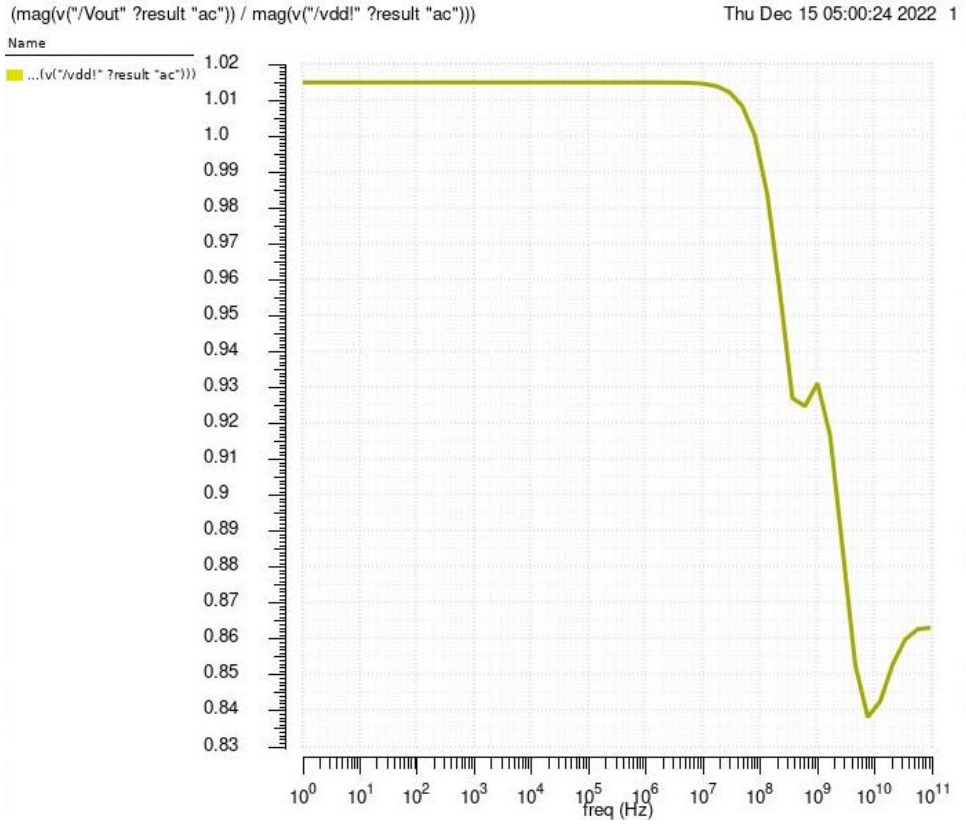
$$PSRR^{+} = \frac{A_{OL}(f)}{v_{out}/v^{+}}$$

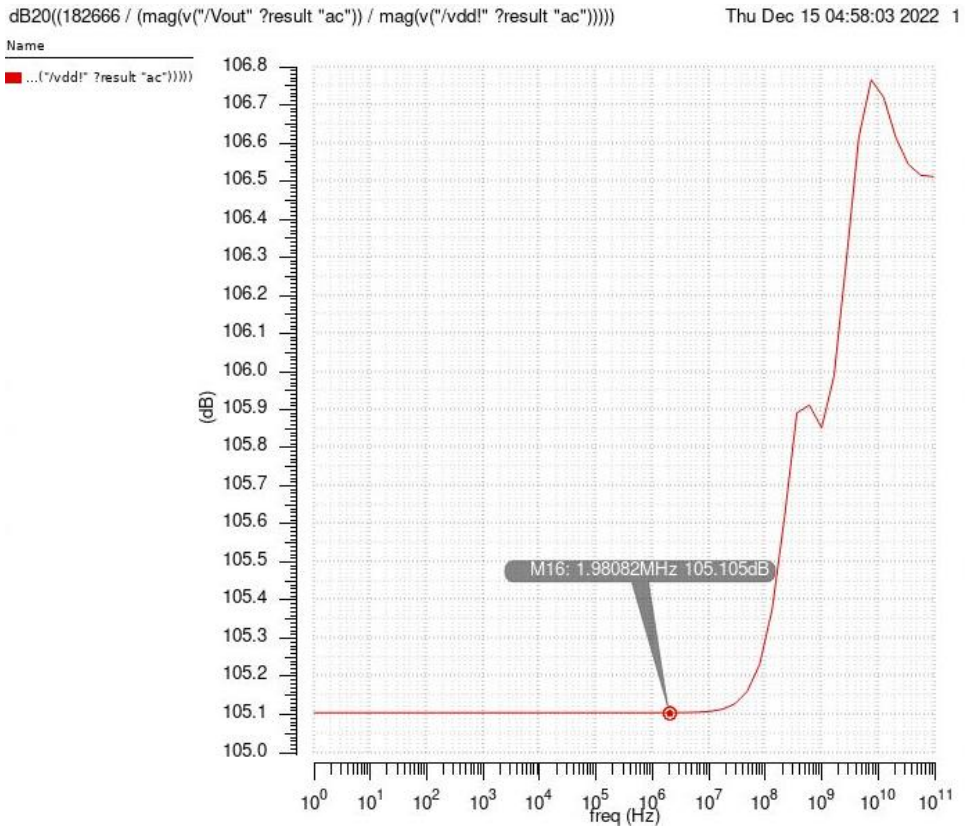
Unloaded Frequency = 182.666kHz

Vout/V+ = 1.01492/1 = 0.985299V/V

$$\frac{182.666kHz}{.985299\ \frac{V}{V}} = 185.391kHz$$

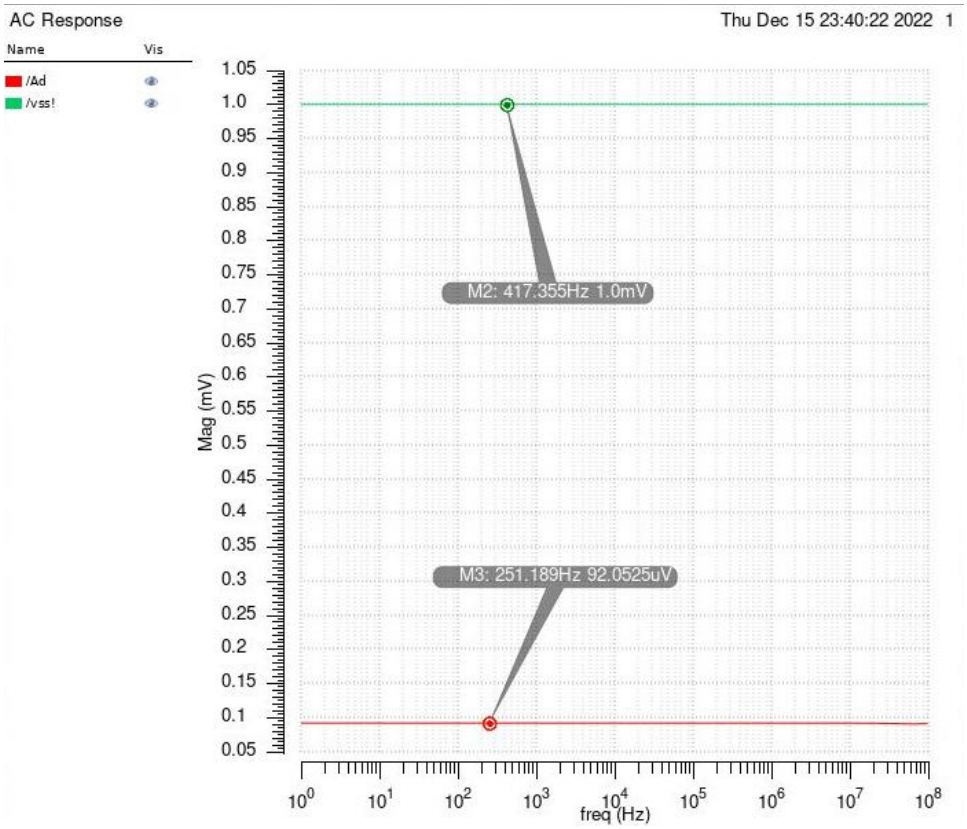
105dB





Hand calculation matched simulation.

GND PSRR (dB)



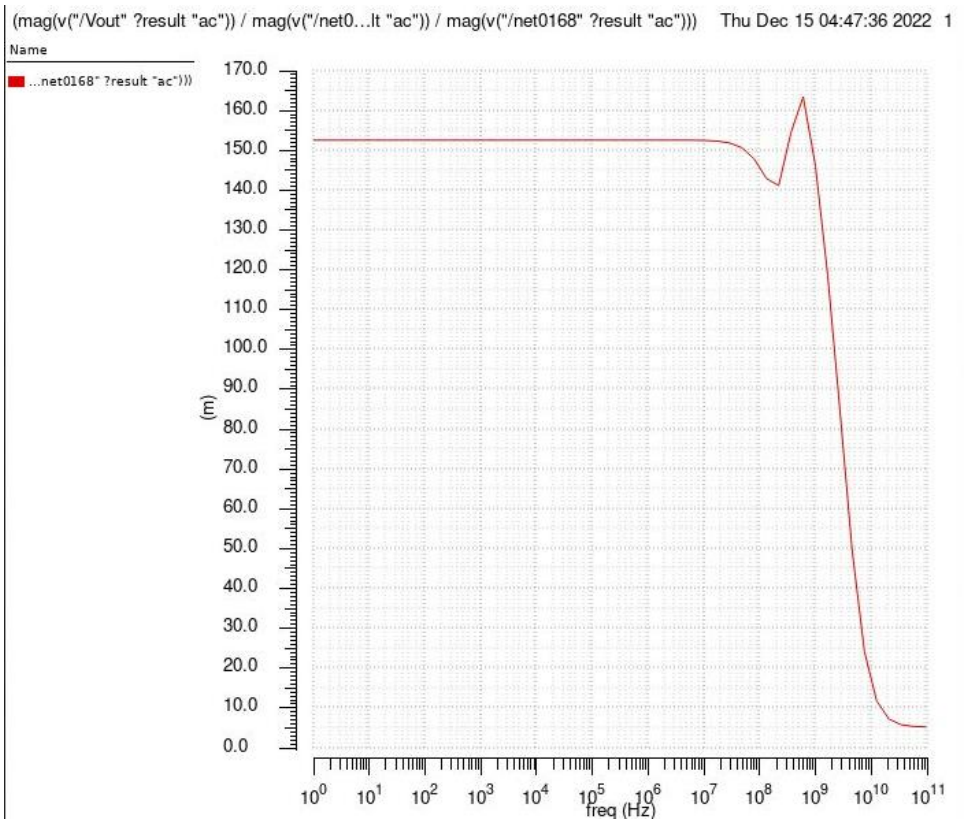
$$PSRR^{-} = \frac{A_{OL}(f)}{v_{out}/v^{-}}$$

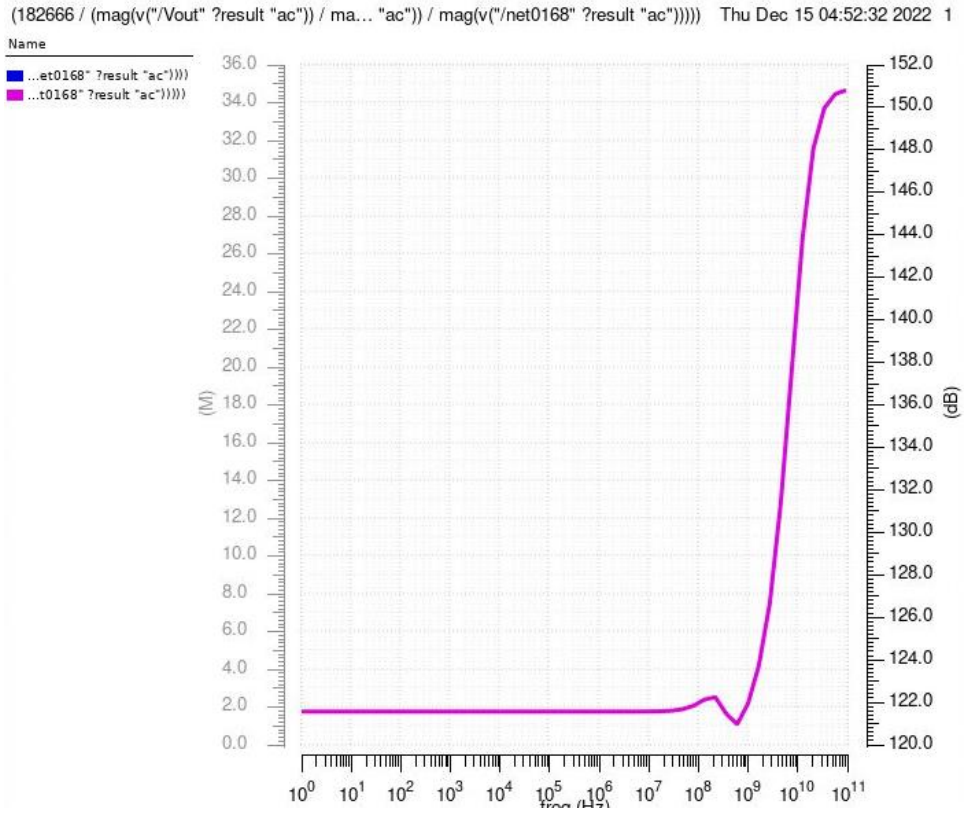
Unloaded Frequency = 182.666kHz

Vout/V- = 92.0525µ V/1mV = 0.0920525V/V

$$\frac{182.666kHz}{0.0920525\ \frac{V}{V}} = 19{,}884{,}367Hz$$

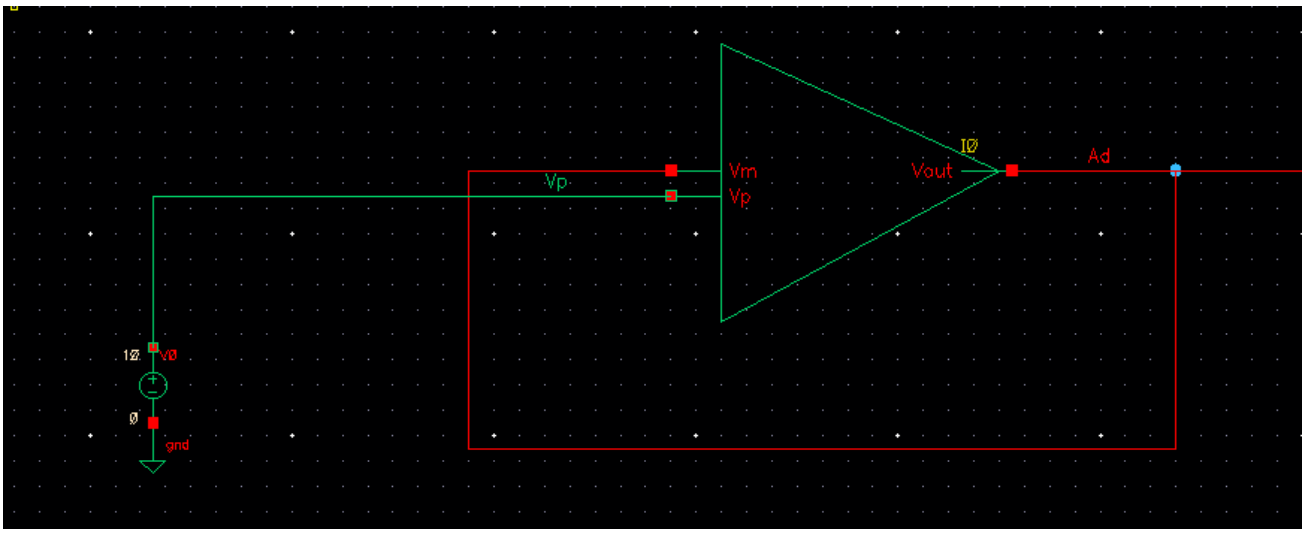
125.9 dB



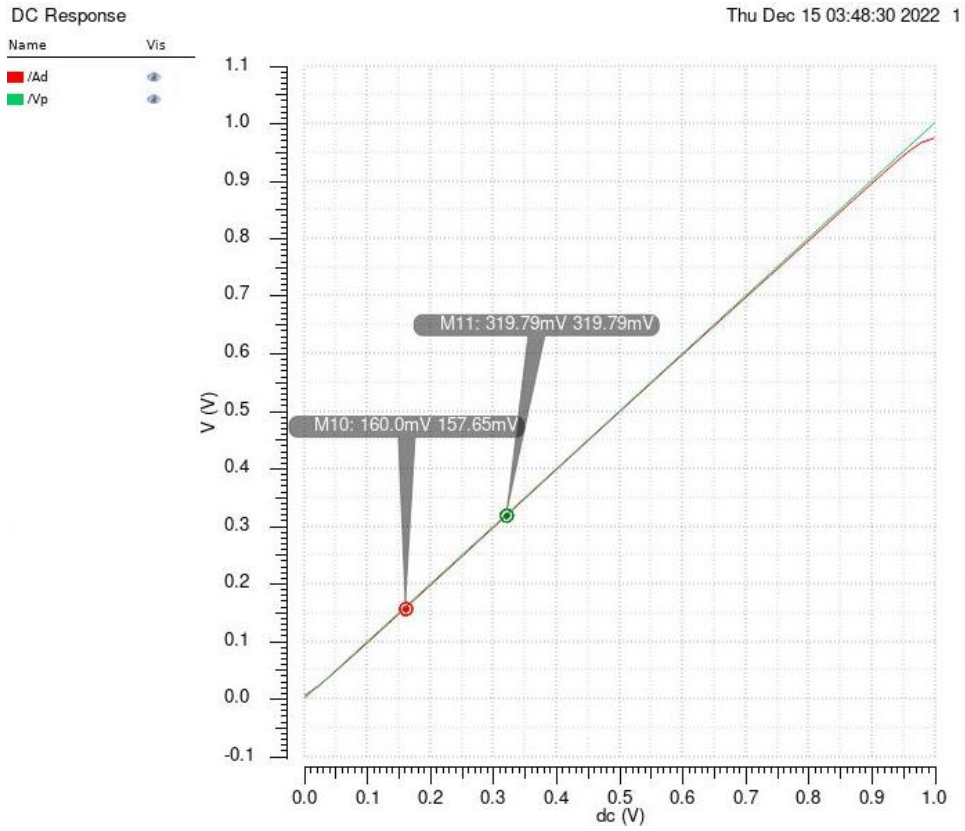


Hand calculation matched simulation.

Nominal Output Voltage (V)

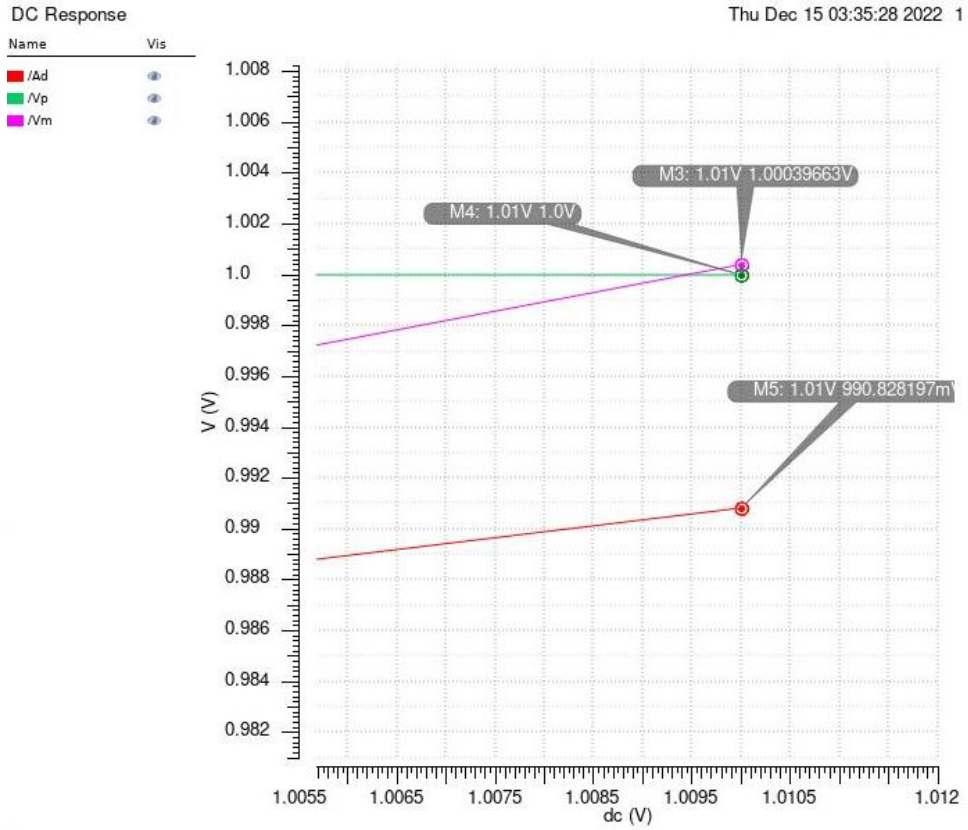


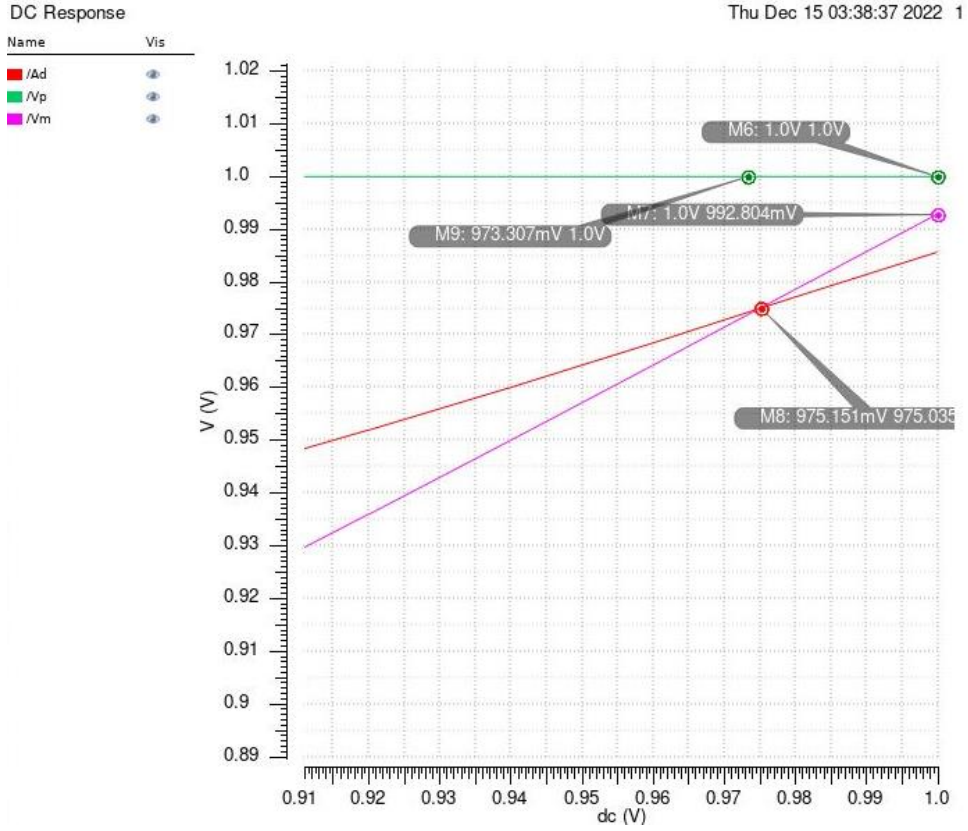
A Unity Gain Buffer or Voltage Follower Configuration is needed for this simulation



Both the Output and the Input lines follow each other when swept.

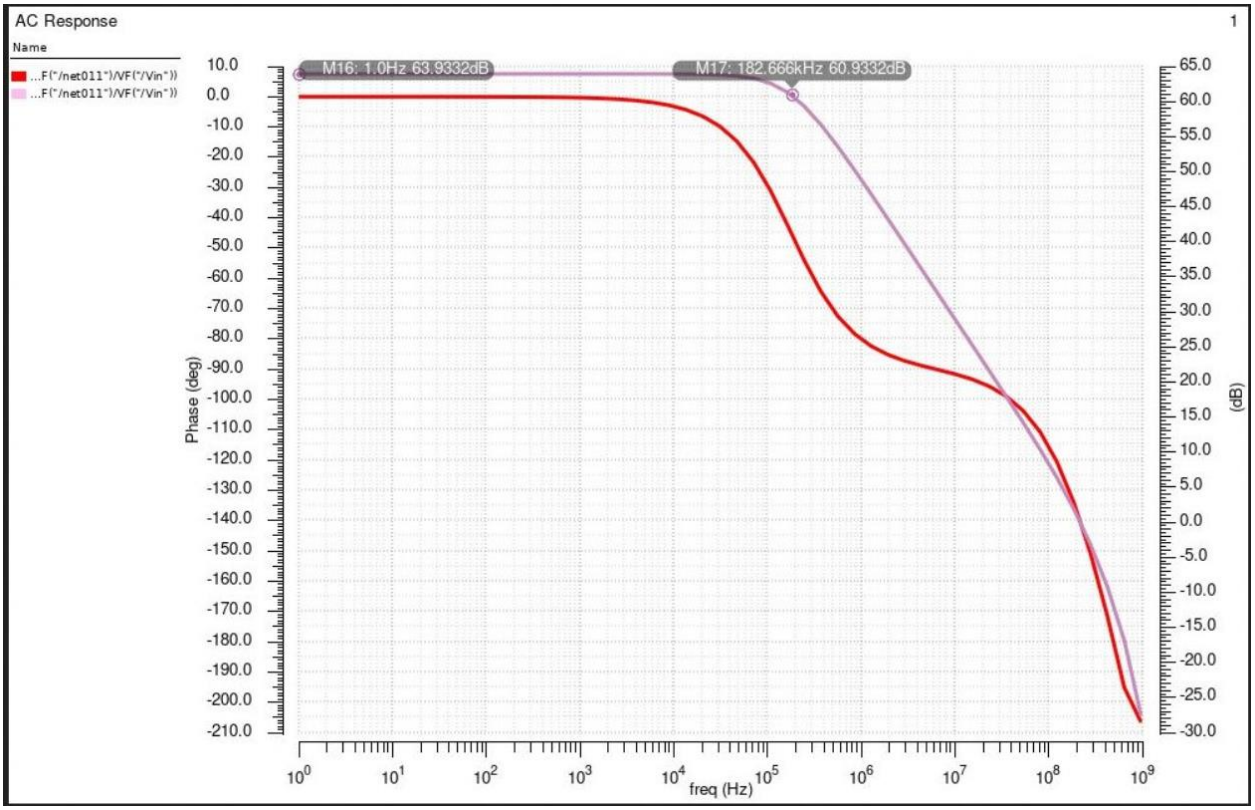
Input Offset Voltage (Mv)


DC Response
Thu Dec 15 03:35:28 2022 1
Name
Vis
/Ad
/Vp
/Vm
M3: 1.01V 1.00039663V
M4: 1.01V 1.0V
M5: 1.01V 990.828197m
V (V)
dc (V)


DC Response
Thu Dec 15 03:38:37 2022 1
Name
Vis
/Ad
/Vp
/Vm
M6: 1.0V 1.0V
M7: 1.0V 992.804mV
M9: 973.307mV 1.0V
M8: 975.151mV 975.035
V (V)
dc (V)

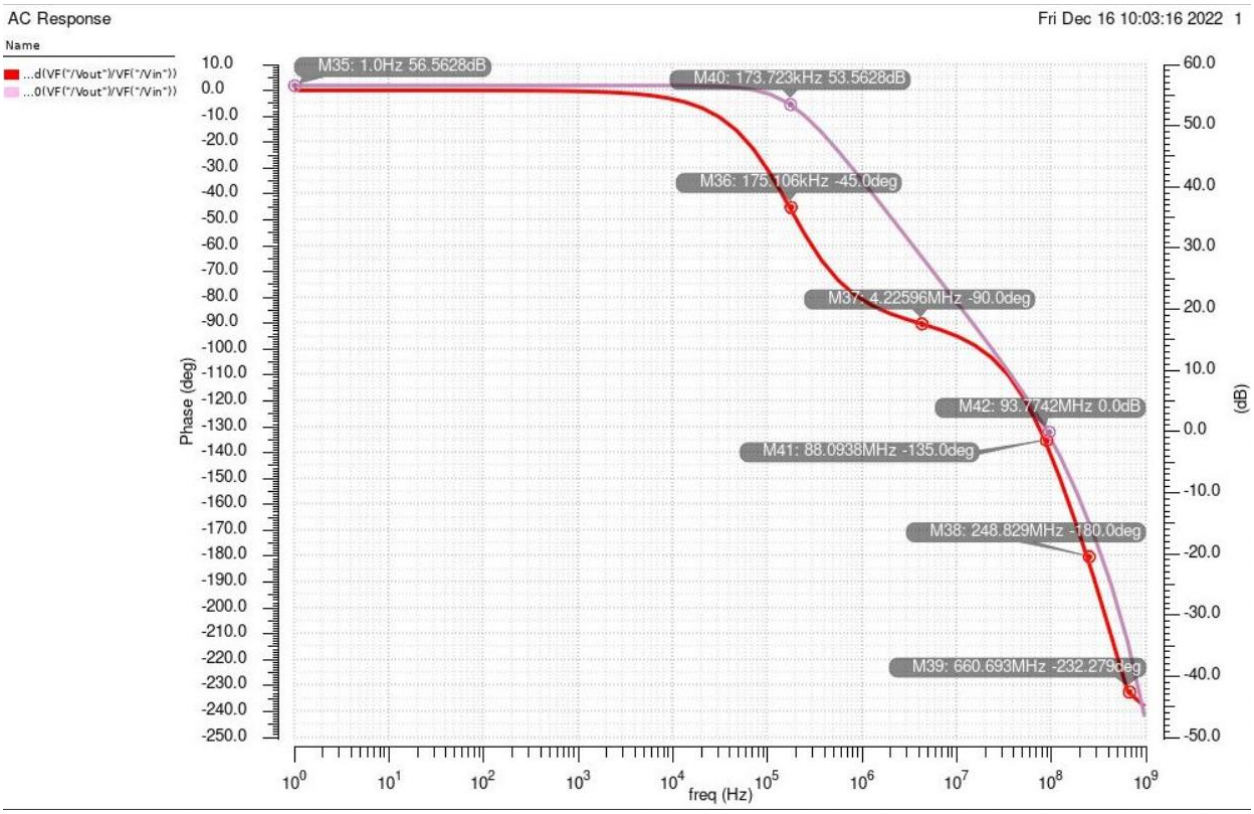
An offset is applied to one of the terminal results in a small error in the output

Unloaded Bandwidth (kHz)



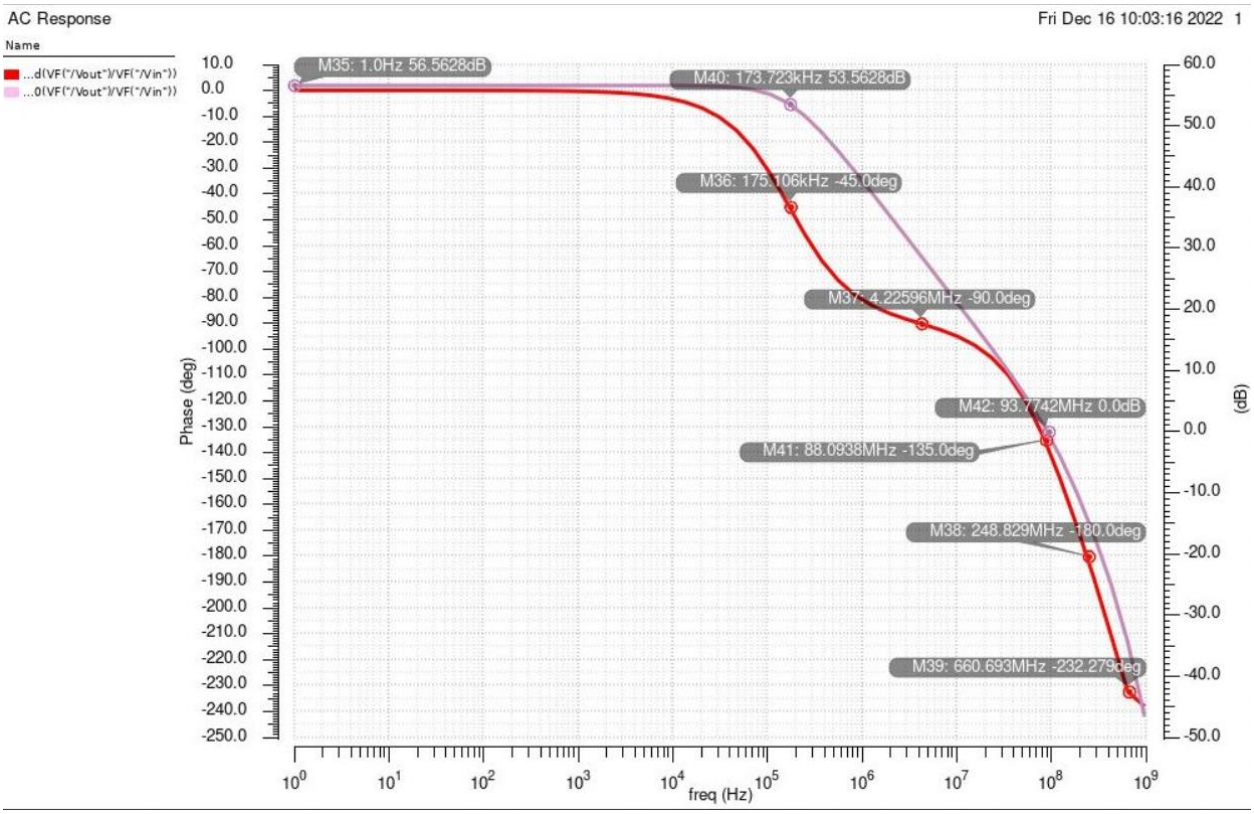
Unloaded Bandwidth = 182.666kHz

Loaded Bandwidth (kHz)



Loaded Bandwidth = 178.723kHz

Gain-Bandwidth Product (MHz)

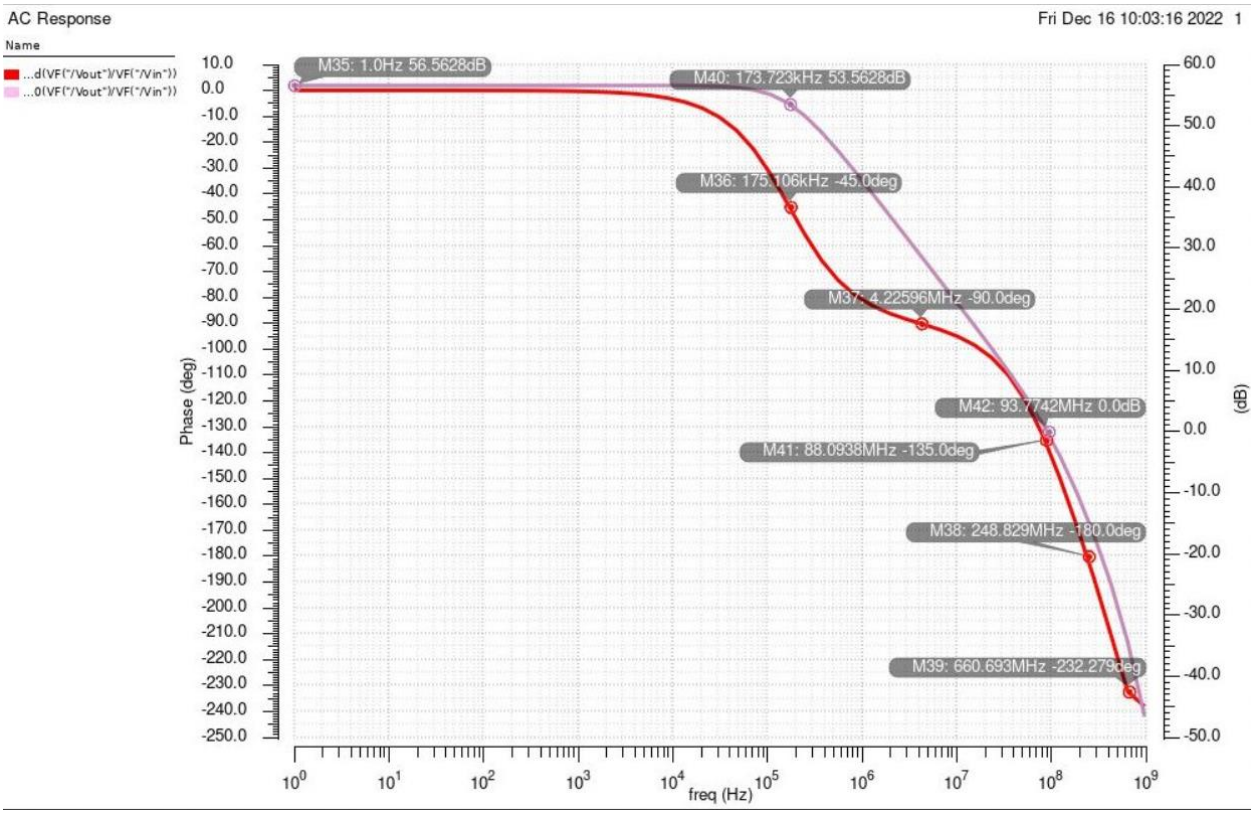


Gain-Bandwidth Product = 93.7742 MHz

Compensation Capacitor (pF)

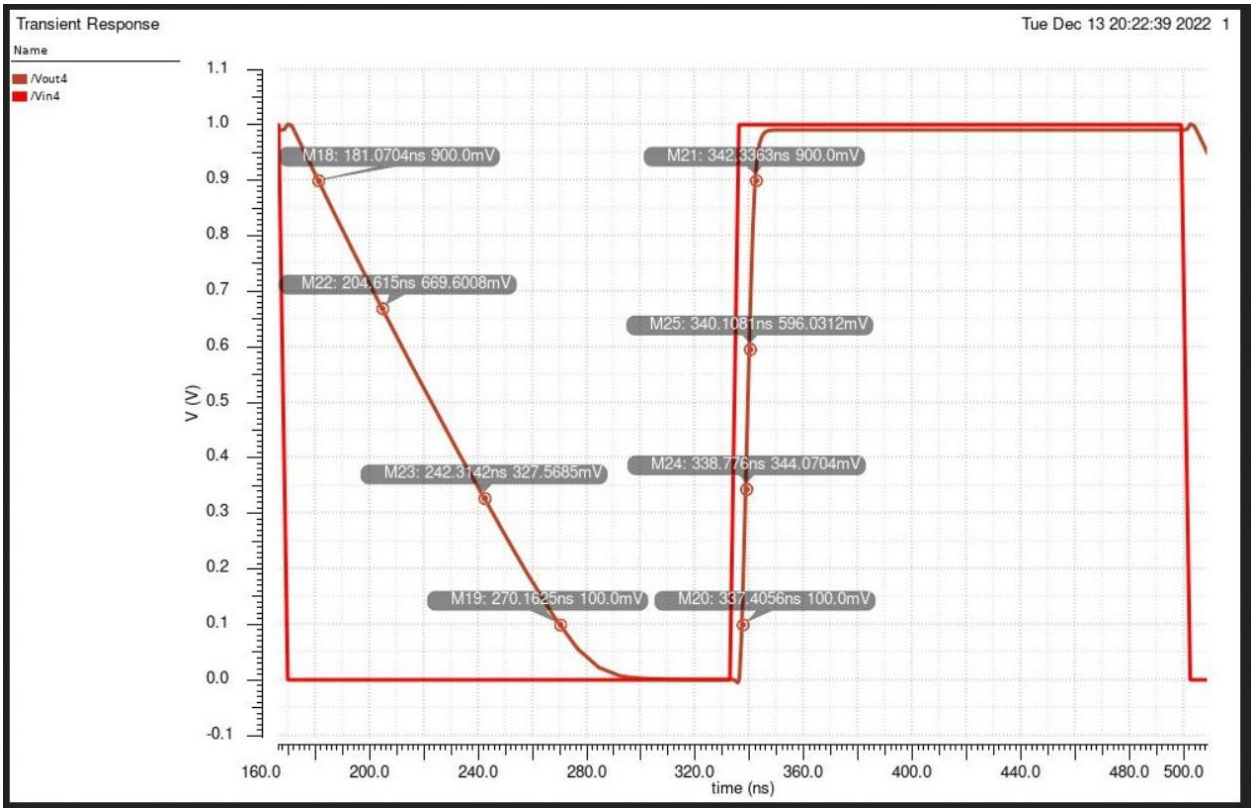
Compensation Cap = 480pF [1]

Phase Margin (Degrees)



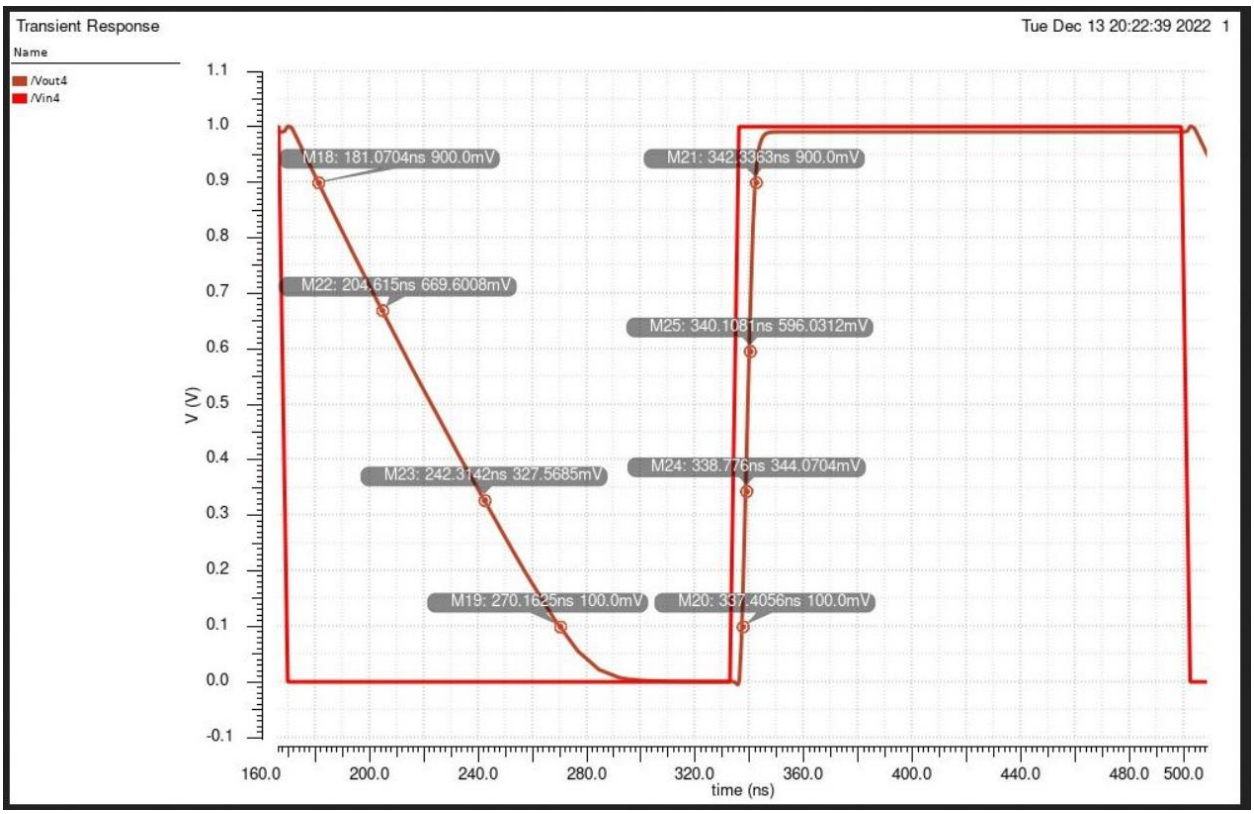
Phase Margin = | -232.279 + 180 | = 52.279 degrees

Rise Time (ns) (Step Response)



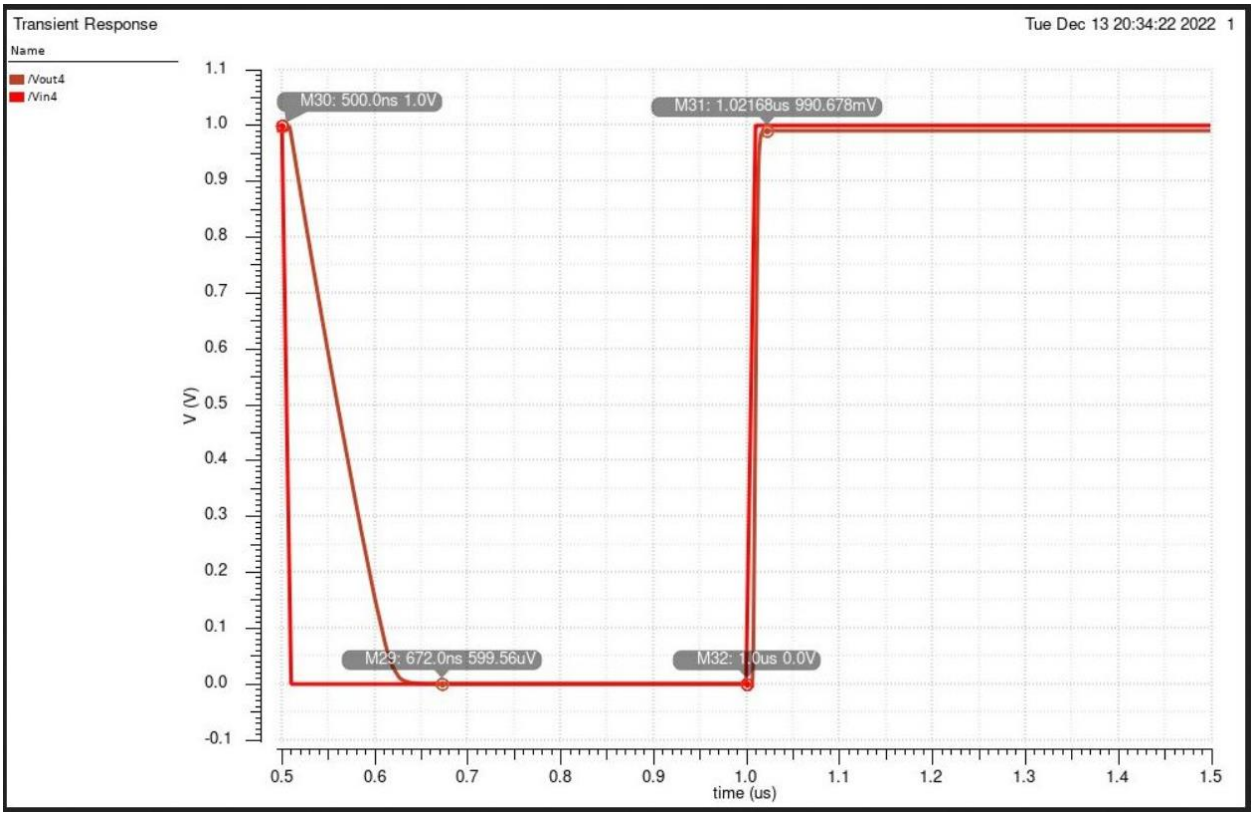
Rise Time = 342.3363ns – 337.4056ns = 4.93ns

Fall Time (ns) (Step Response)

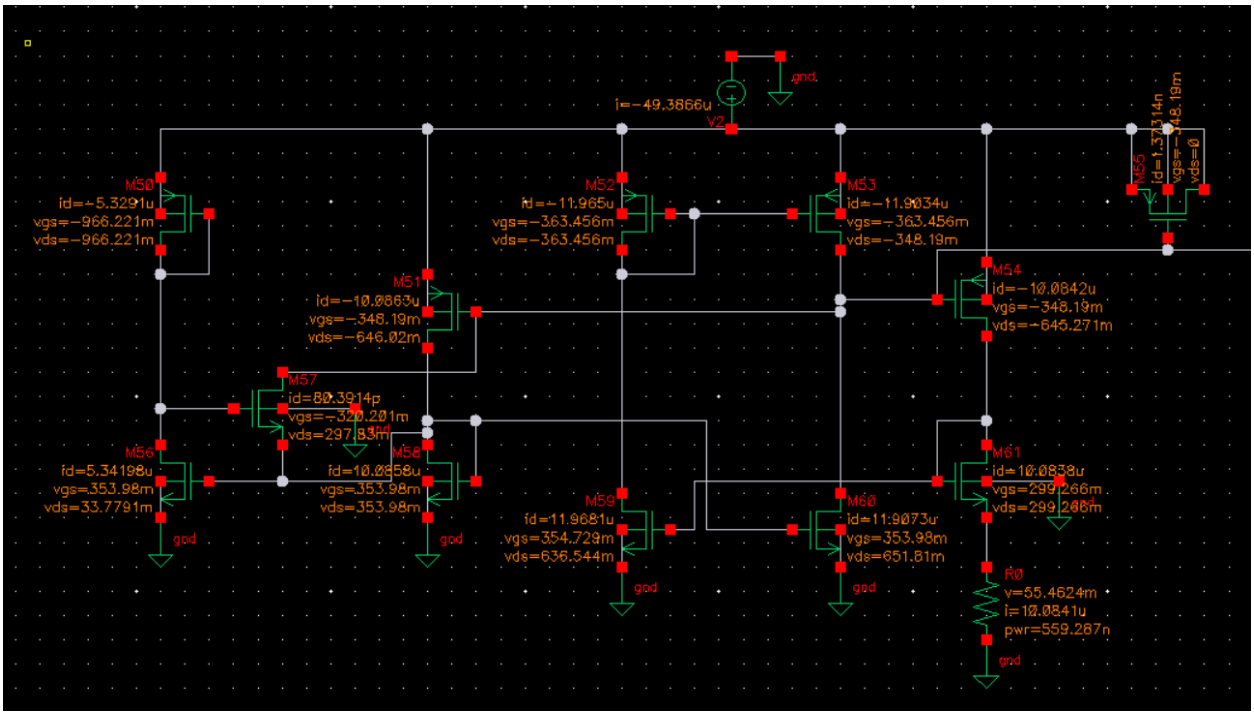


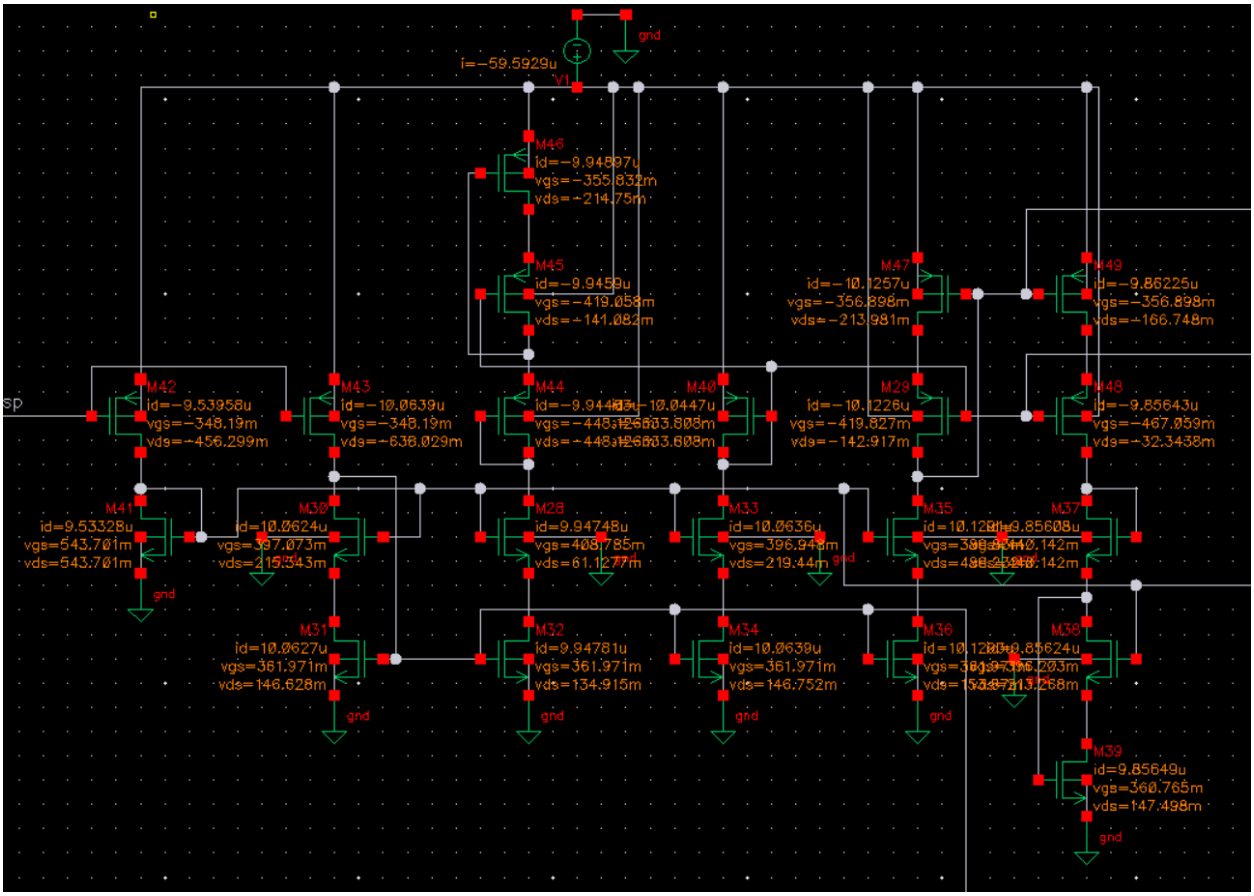
Fall Time = 270.1625ns – 181.0704ns = 89ns

Settling Time (ns) (Step Response)

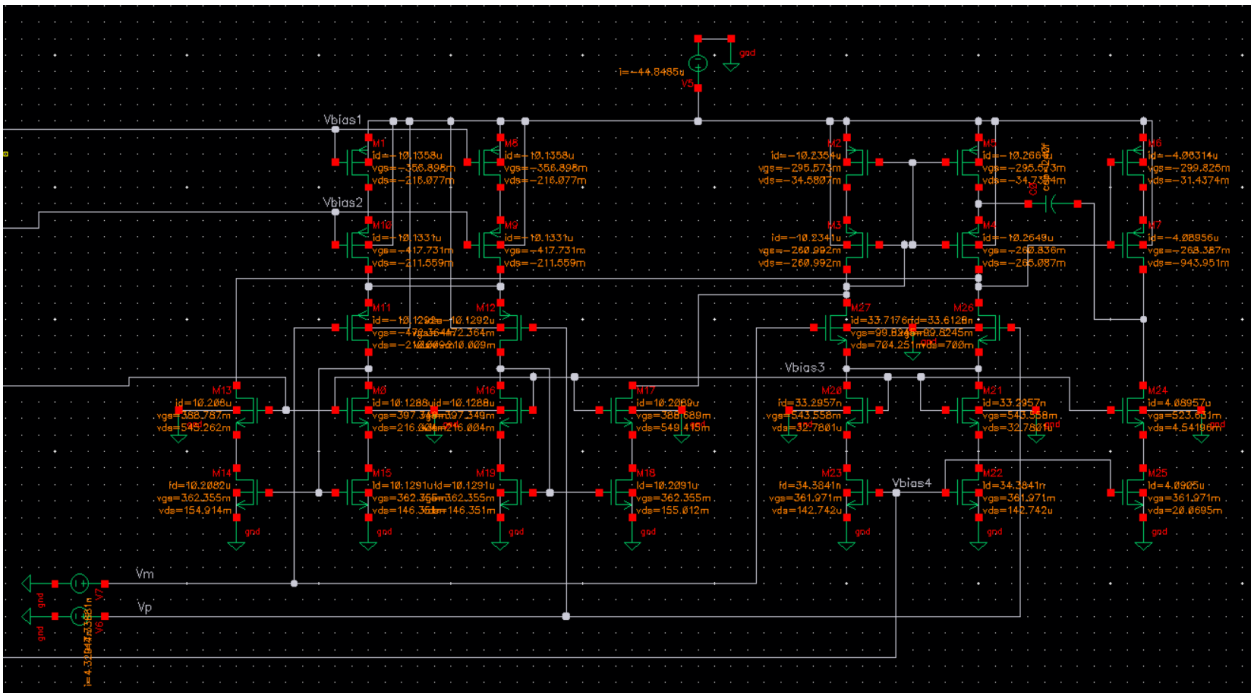


DC Currents in All Branches





Throughout the bias circuit the branch current is roughly 10uA as per Baker's standards.



@ Vm = Vp = 100mV

In the amplifier circuit, however, the current will max at 10uA but the current of a branch at any given time is dependent on the current operating conditions (+ and – terminal voltages, mainly)

Part 2: Report Tables

Table 1: Partner Contributions to Circuit Design and Report

Contribution	Drew	Jonathan
Researching Topologies	X	X
Implementing Topology	X	X
Modifications to Reach Specified Gain	X	
CMRR		X
Timing Related Measurements	X	
ICMR	X	
Output Swing	X	
PSRR		X
Nominal + Offset Voltages		X
Frequency Response	X	
DC Currents in Branches	X	
All Power Related Measurements		X
Tables	X	

Table 2: Specifications vs. Actual Results

Criteria	Specified Value	Achieved
Max Power Consumption	40µW	33µW
Differential Gain	60dB	56.5628 dB
CMRR	110dB	99.107dB
ICMR	0-1V	0-1V
Output Swing	.1-.9V	587.3uV – 991.192mV
Bandwidth	10kHz	178.723kHz
Slew Rate (V/us)	4 V/µs	Worst: 9.26V/µs

References

[1] Baker, R. J. (2019). In CMOS: Circuit Design, Layout, and Simulation (4th ed., pp. 657–821). essay, Wiley.