

ECE 4902 Analog Integrated Circuit Design – Project Report

Worcester Polytechnic Institute

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Project 1: BGR 50n Short Channel Implementation

Submitted by

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Part 1: Designing BGR Core

CMOS Process: 50nm

Supply (V): 1V

Topology: Short Channel

Vref (V): 0.5V

BGR Core Schematic with Startup Circuit

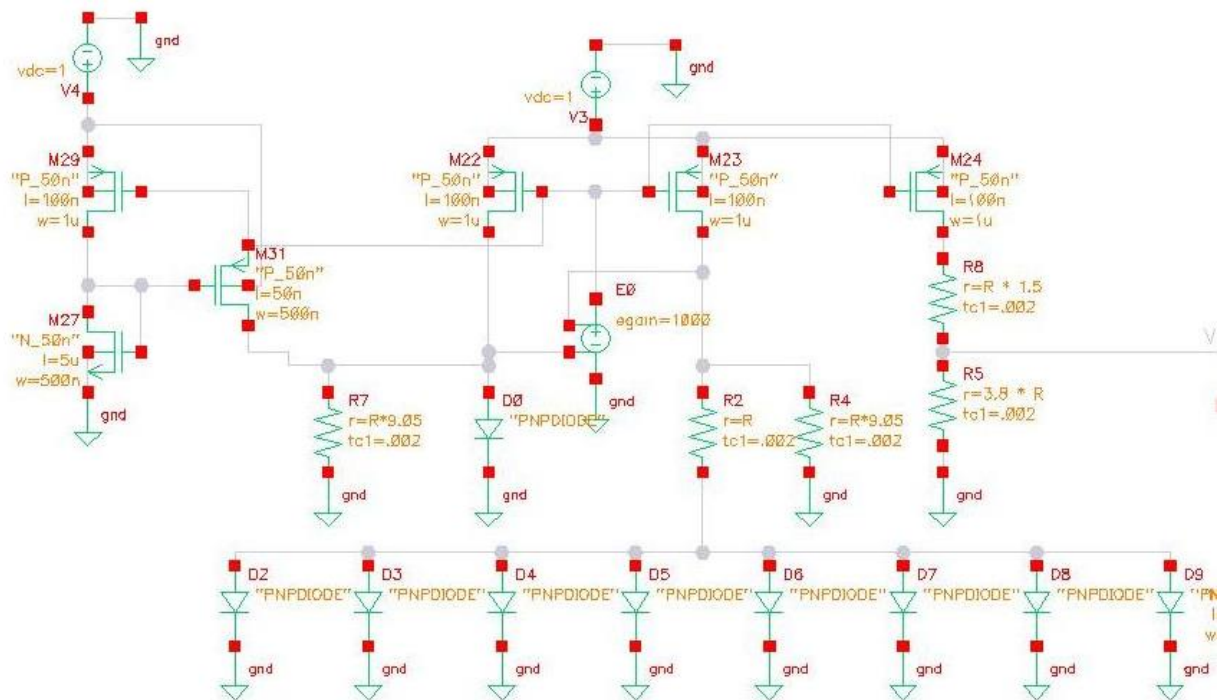


Figure 1: BGR Core Schematic with Startup Circuit

Iref (μA): 1μA

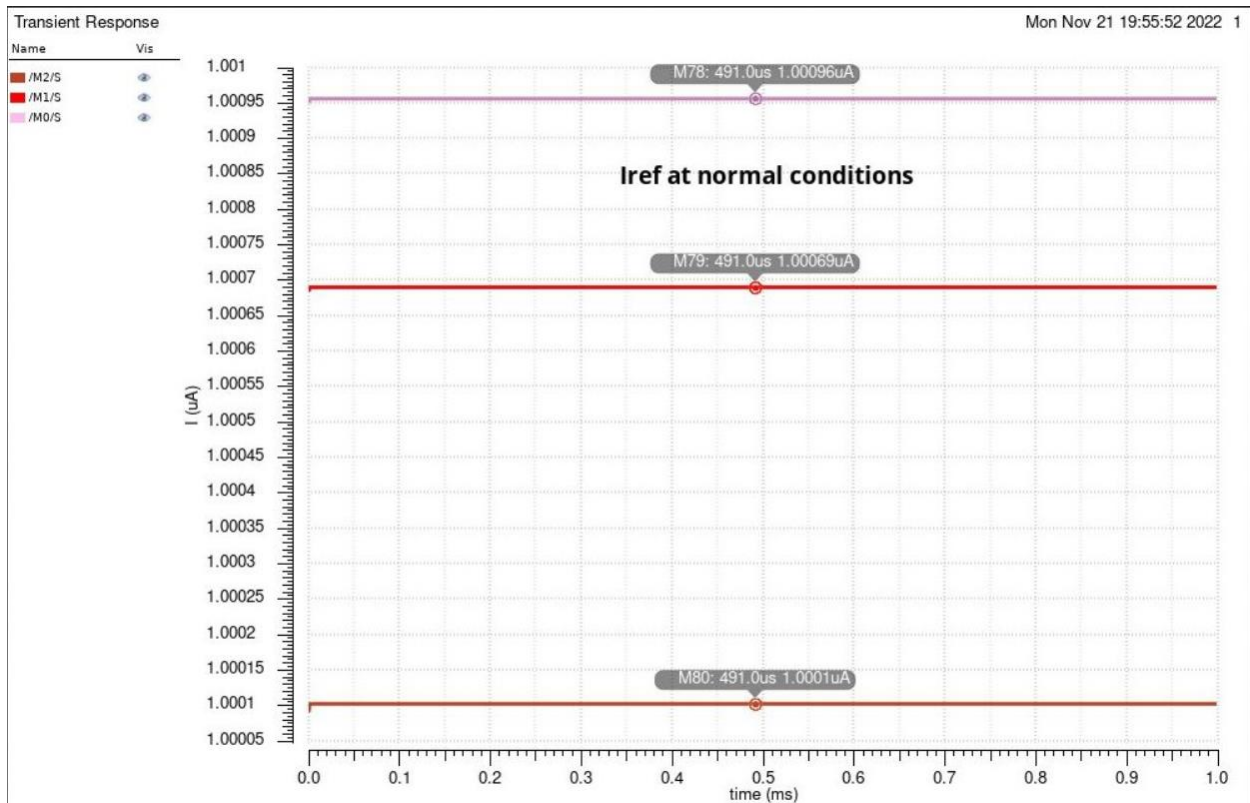


Figure 2: Iref under Normal Conditions

Vref (V): 500mV

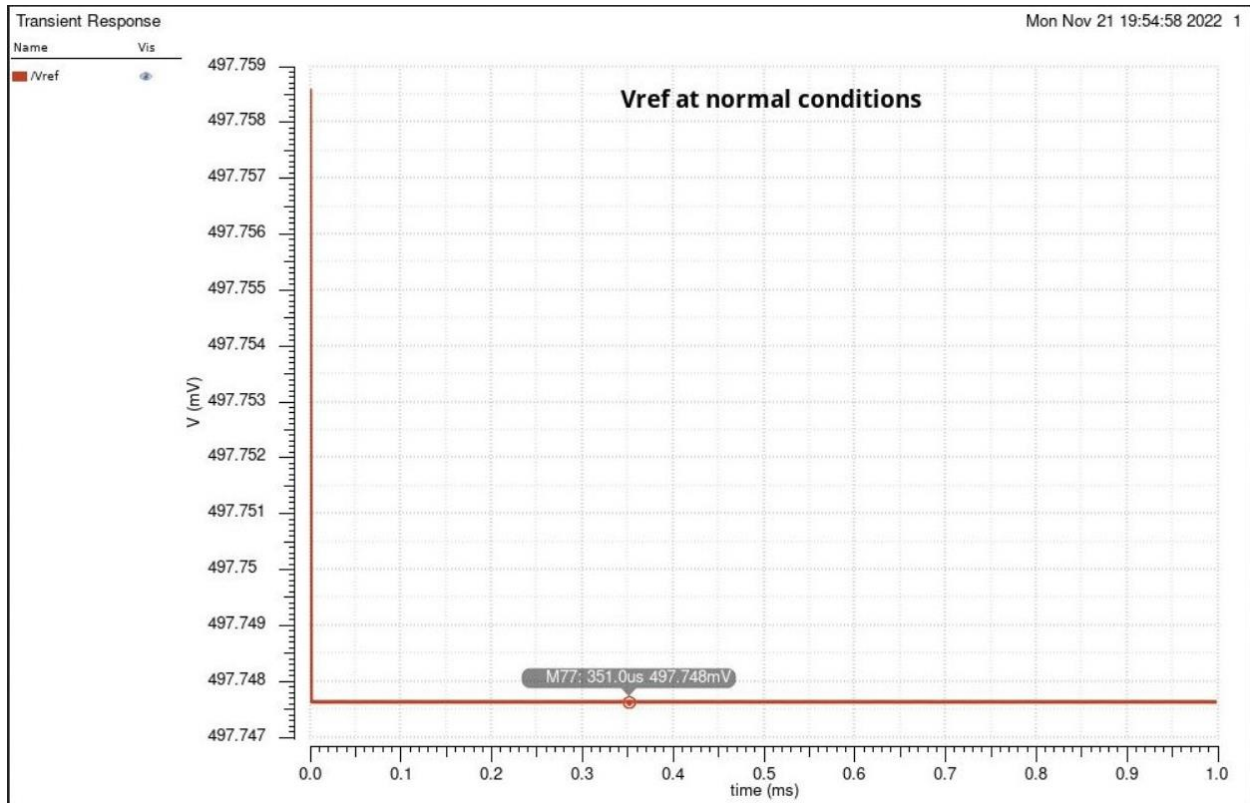


Figure 3: Vref under Normal Conditions

Max. Supply Sensitivity (ppm): 1500ppm

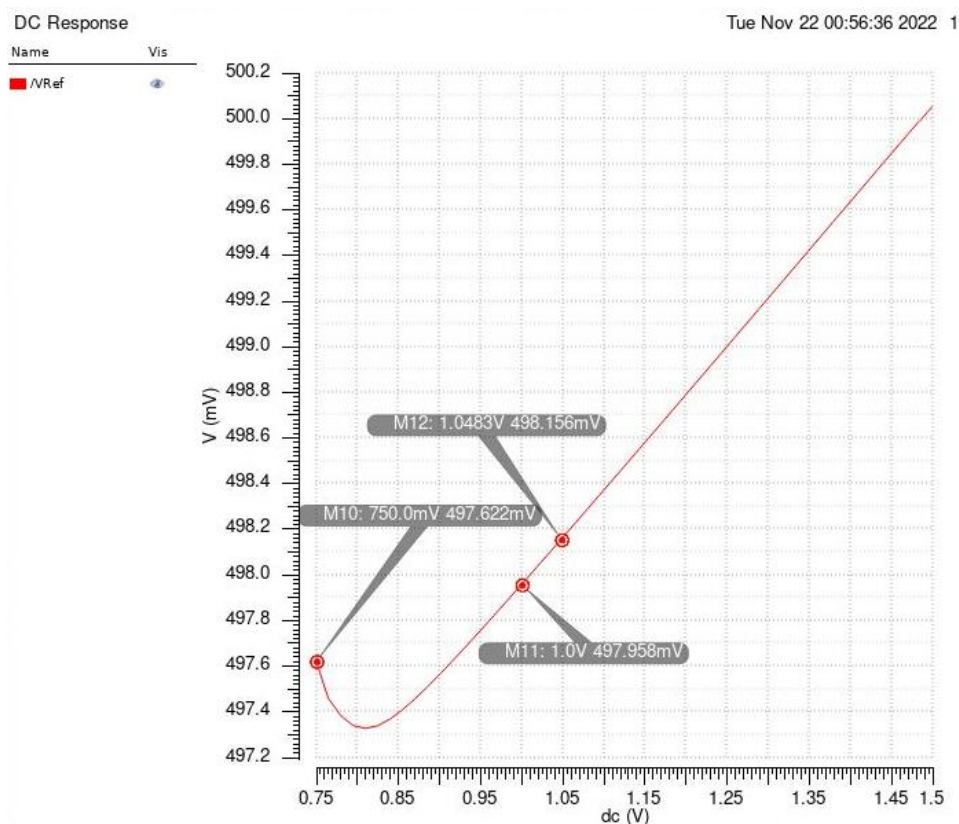


Figure 4: VREF from Vomin to 1.5VDD

Used Vomin to 1.1*VDD

$$\text{Max Supply Sensitivity} = \frac{\Delta V_{REF}}{V_{REFnom}} \cdot 1 \cdot 10^6$$

$$\frac{0.4981555 - 0.49732754}{0.4979576} \cdot 1 \cdot 10^6 = 1071.59 \text{ ppm}$$

This is within spec as the max allowable is 1500ppm

Max. Temp Sensitivity (ppm @ C): 100ppm @ 37°C

$$\text{Max Temp. Stability} = \frac{\Delta V_{REF}}{V_{REFnom}} \cdot 1 \cdot 10^6 \cdot \frac{1}{37^\circ\text{C} - 27^\circ\text{C}}$$

$$\frac{4.28239V - 4.27846V}{4.28239V} \cdot 1 \cdot 10^6 \cdot \frac{1}{37^\circ\text{C} - 27^\circ\text{C}} = 91.7712 \frac{\text{ppm}}{^\circ\text{C}} @ 37^\circ\text{C}$$

This is within spec as the max allowable is 100 @37°C

Max. Power Consumption (μW): 10 μW

From the Total Power Consumption Graph in Figure X, below, the Max Power Consumption is 3.0011 μW

ΔI_{ref} with $\Delta R = \pm 10\%$ around Nominal Value

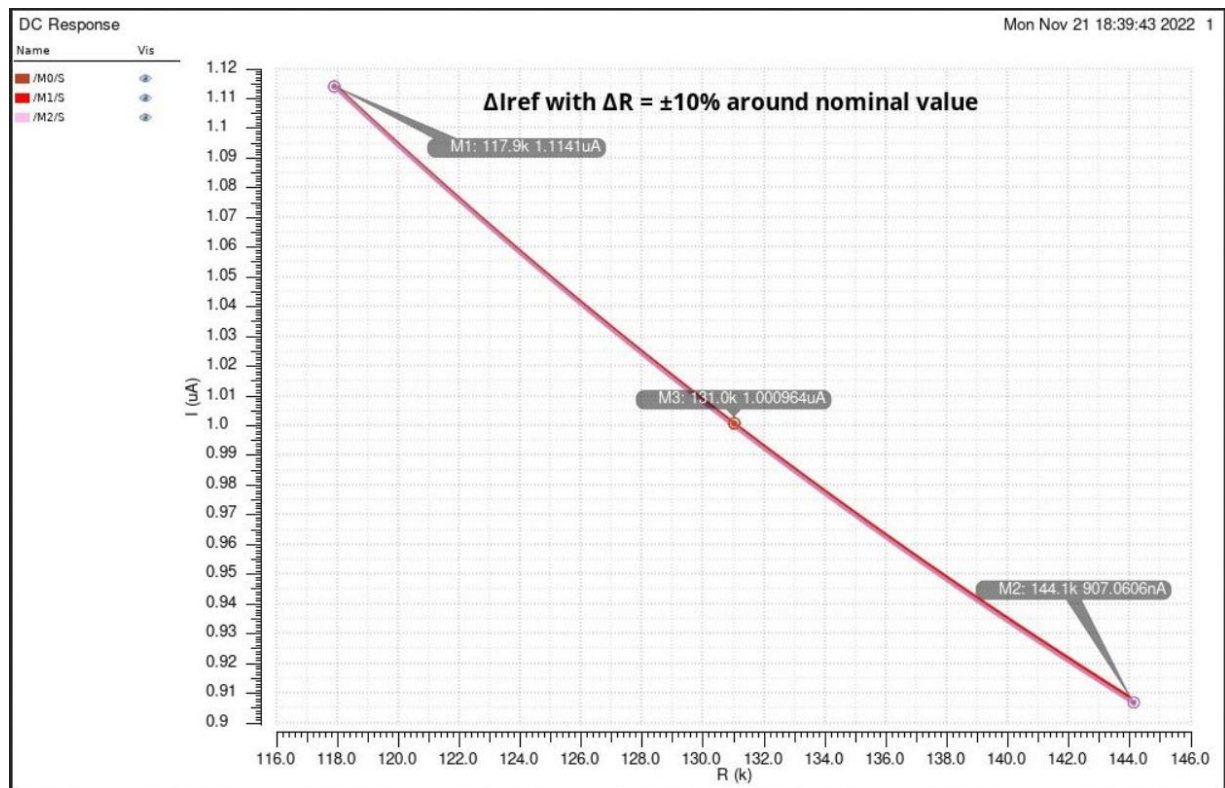


Figure 5: ΔI_{ref} with $\Delta R = \pm 10\%$ around Nominal Value

ΔI_{ref} with $\Delta V_{\text{DD}} = \pm 10\%$ Nominal Value

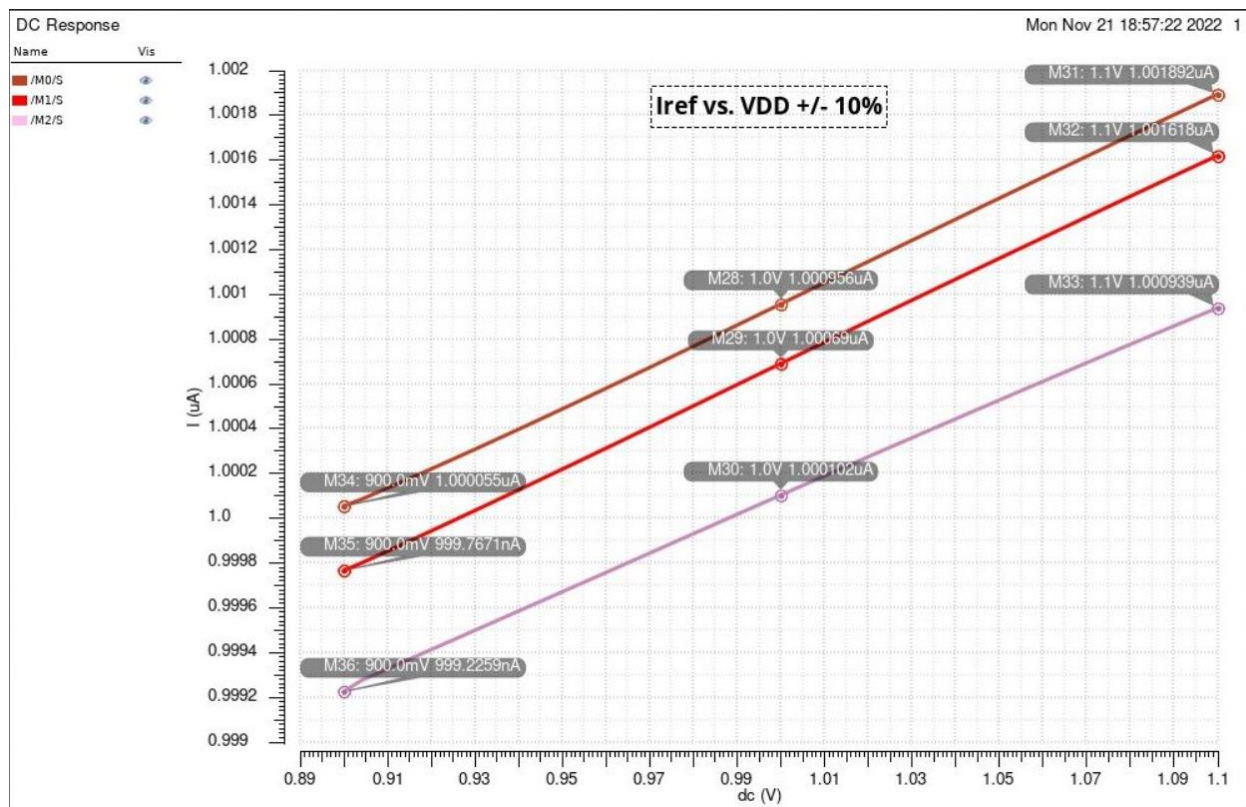


Figure 6: Iref vs. VDD

Iref with $\Delta V_{THn} = \pm 10\%$ and $\Delta V_{THp} = \pm 10\%$ Nominal Value

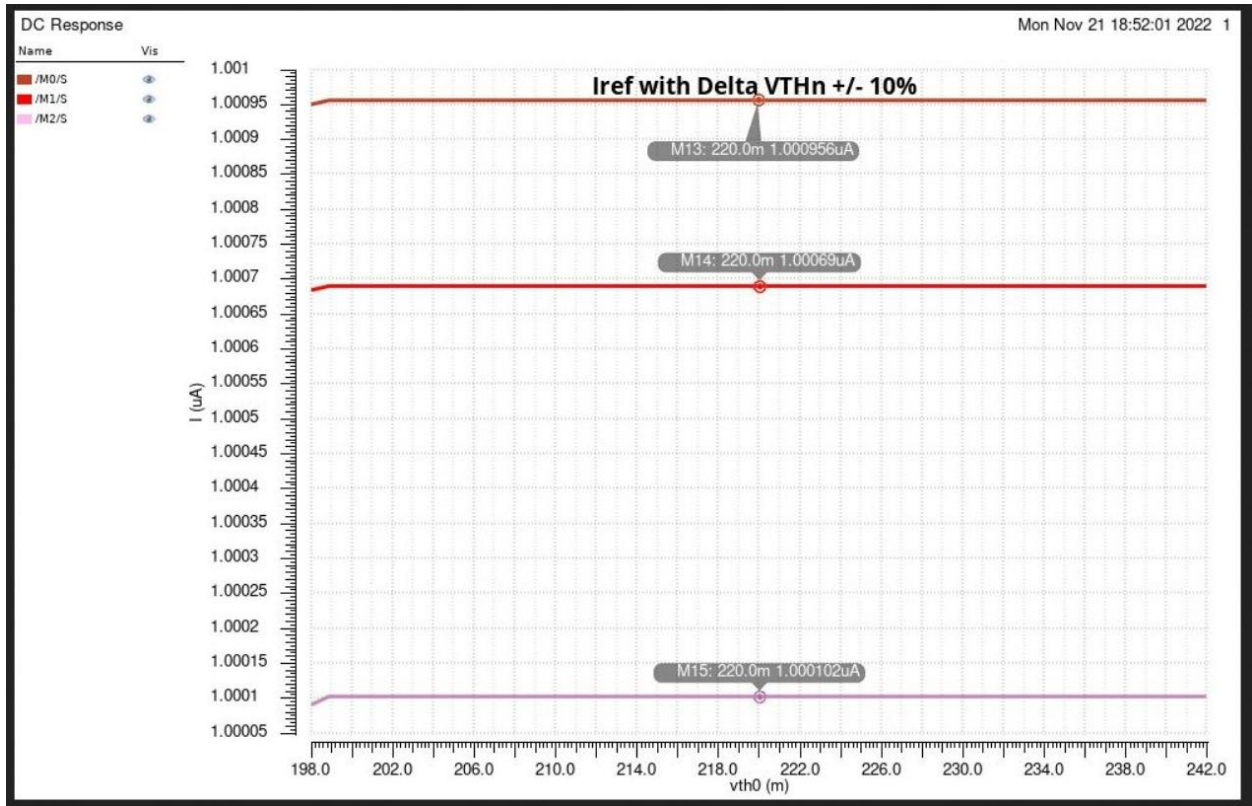


Figure 7: Iref vs. VTHn

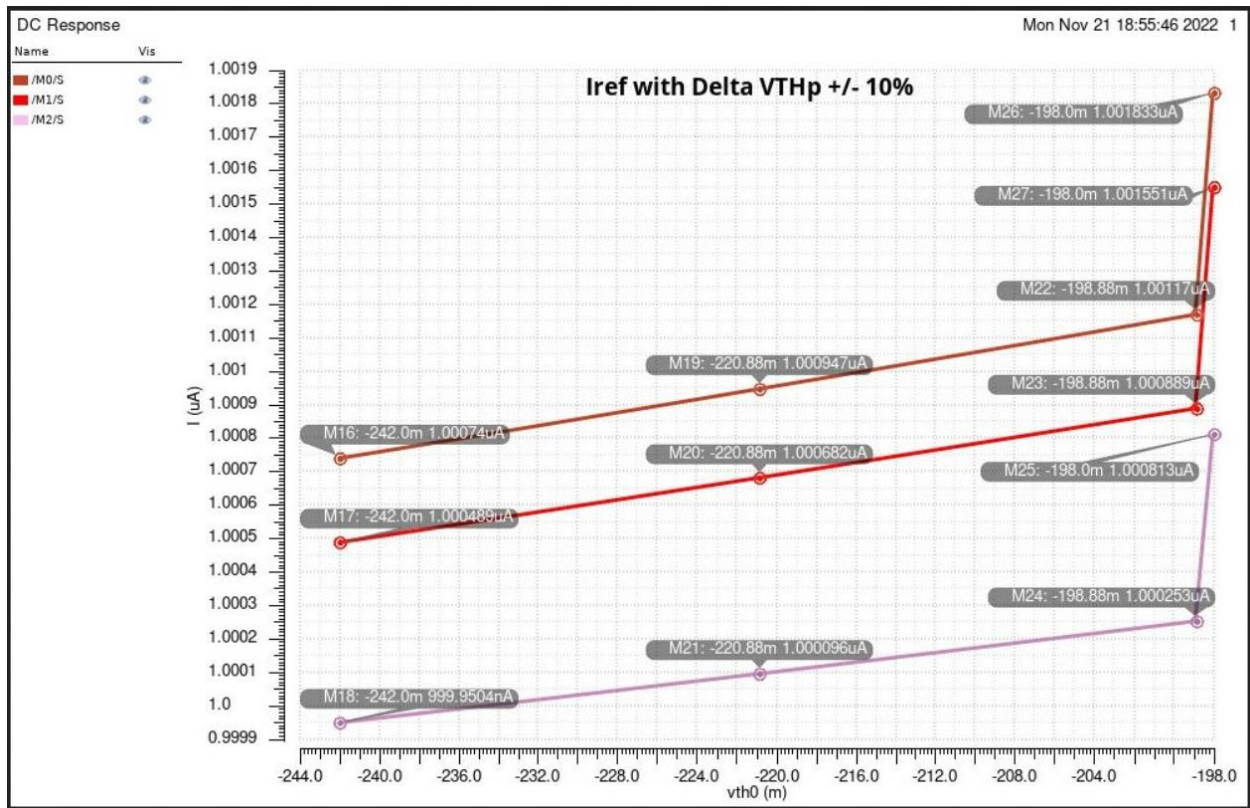


Figure 8: Iref vs. VTHp

ΔV_{ref} with $\Delta R = \pm 10\%$ Nominal Value

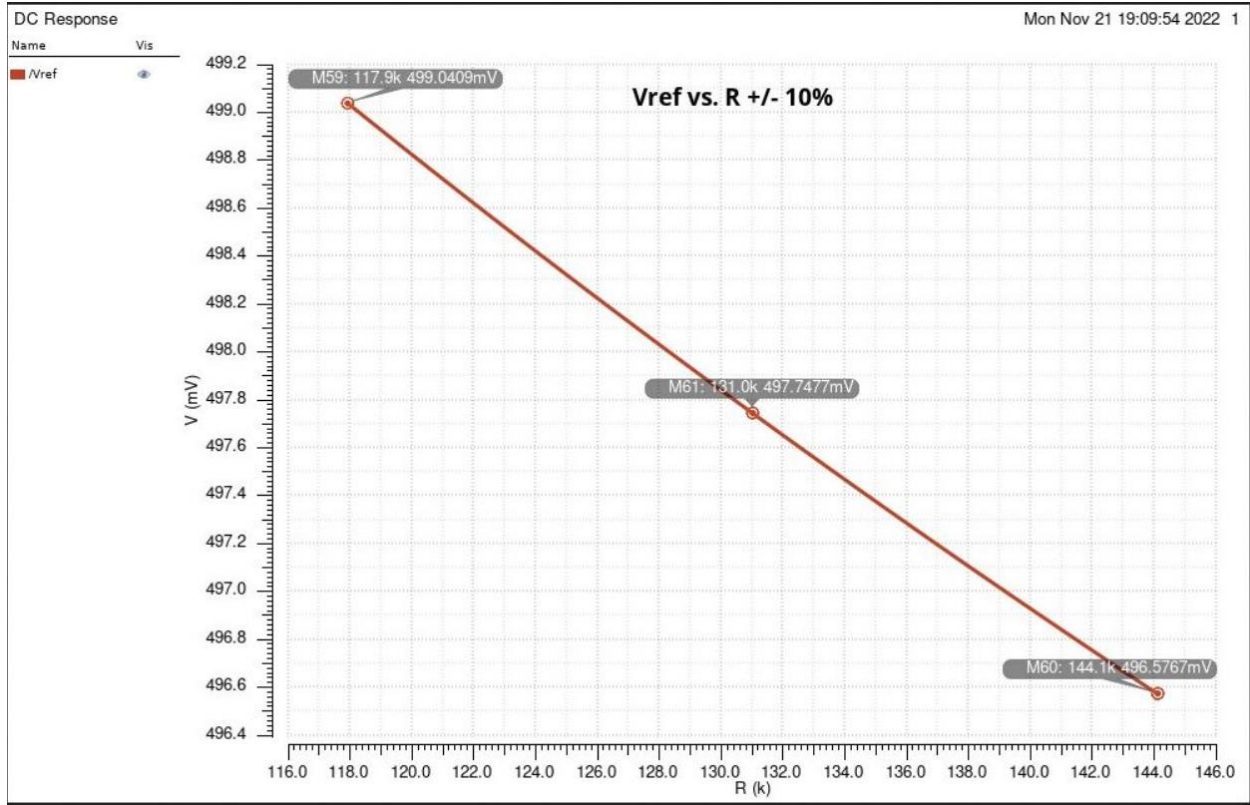


Figure 9: Iref vs. R

ΔV_{ref} with $\Delta V_{DD} = \pm 10\%$ Nominal Value

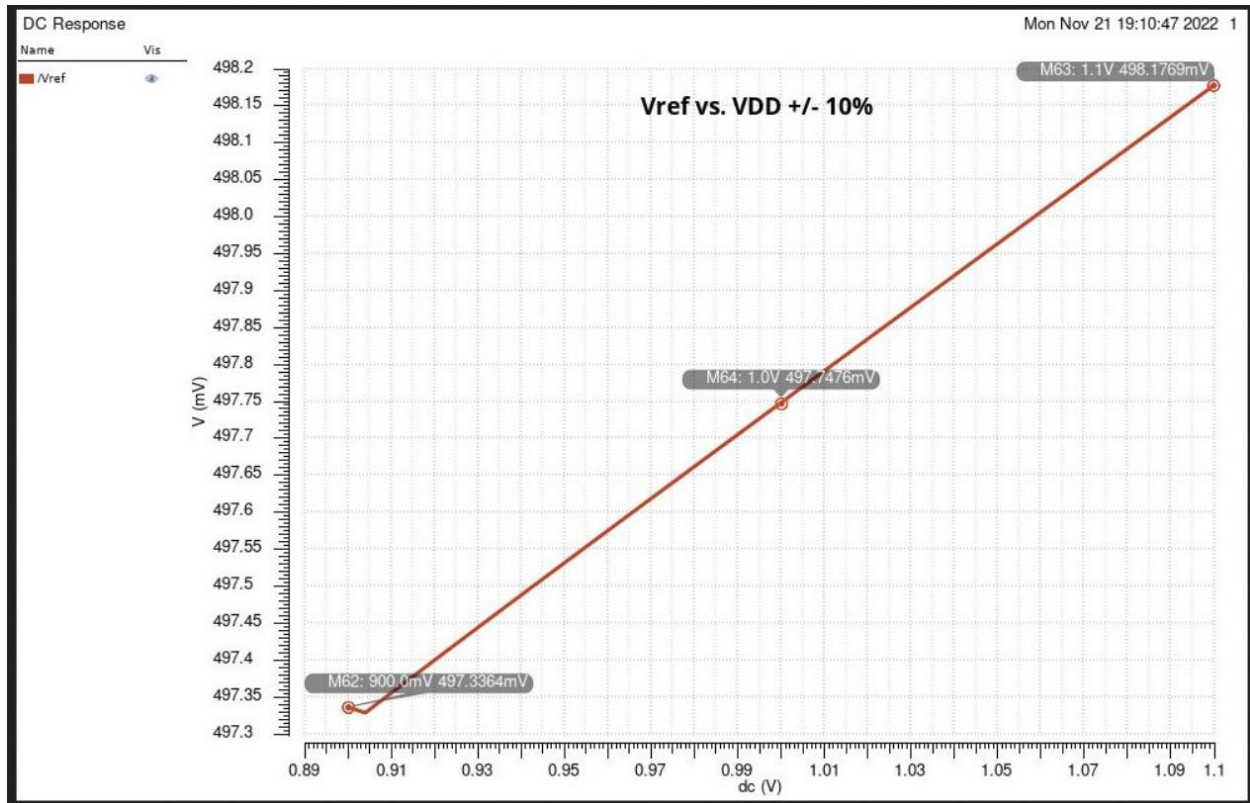


Figure 10: Vref vs. VDD

ΔV_{ref} with $\Delta V_{THn} = \pm 10\%$ and $\Delta V_{THp} = \pm 10\%$ Nominal Value

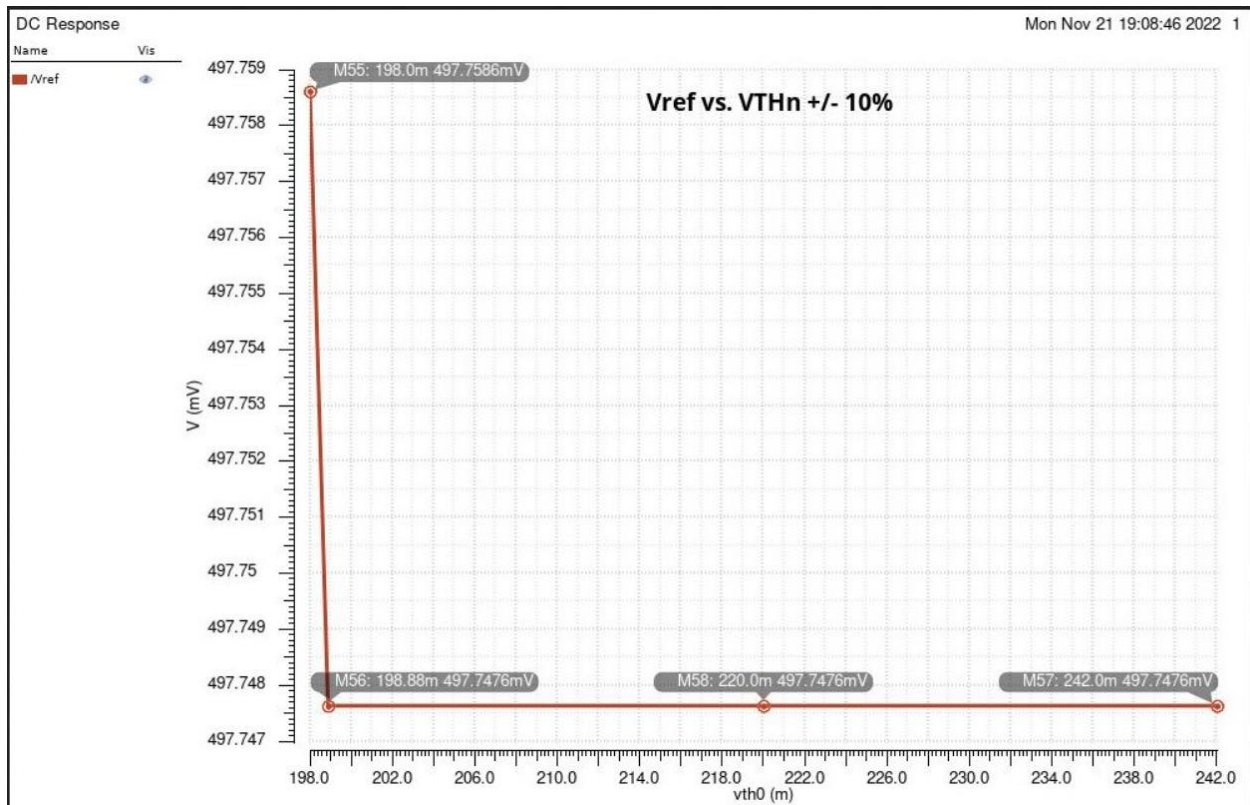


Figure 11: Vref vs. VTHn

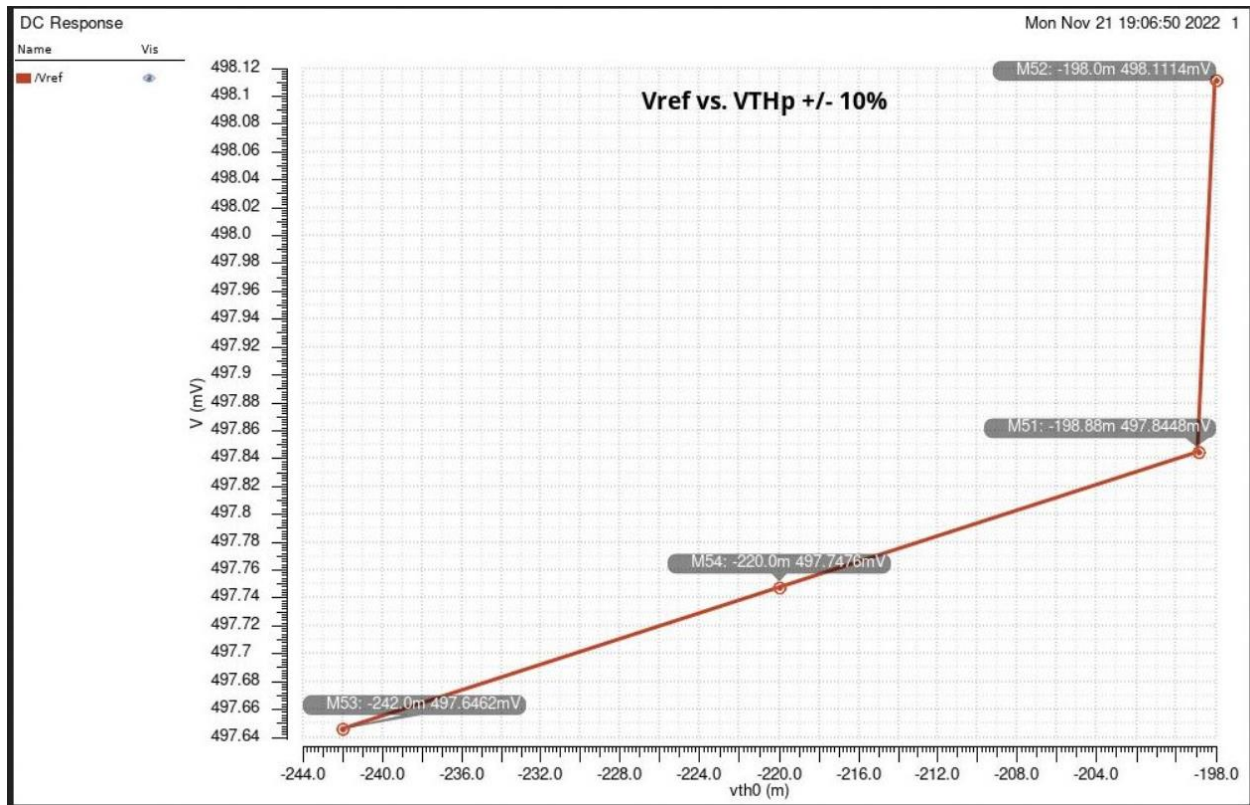


Figure 12: Vref vs. VTHp

Minimum/Maximum Supply Voltage such that the Circuit is Still Working

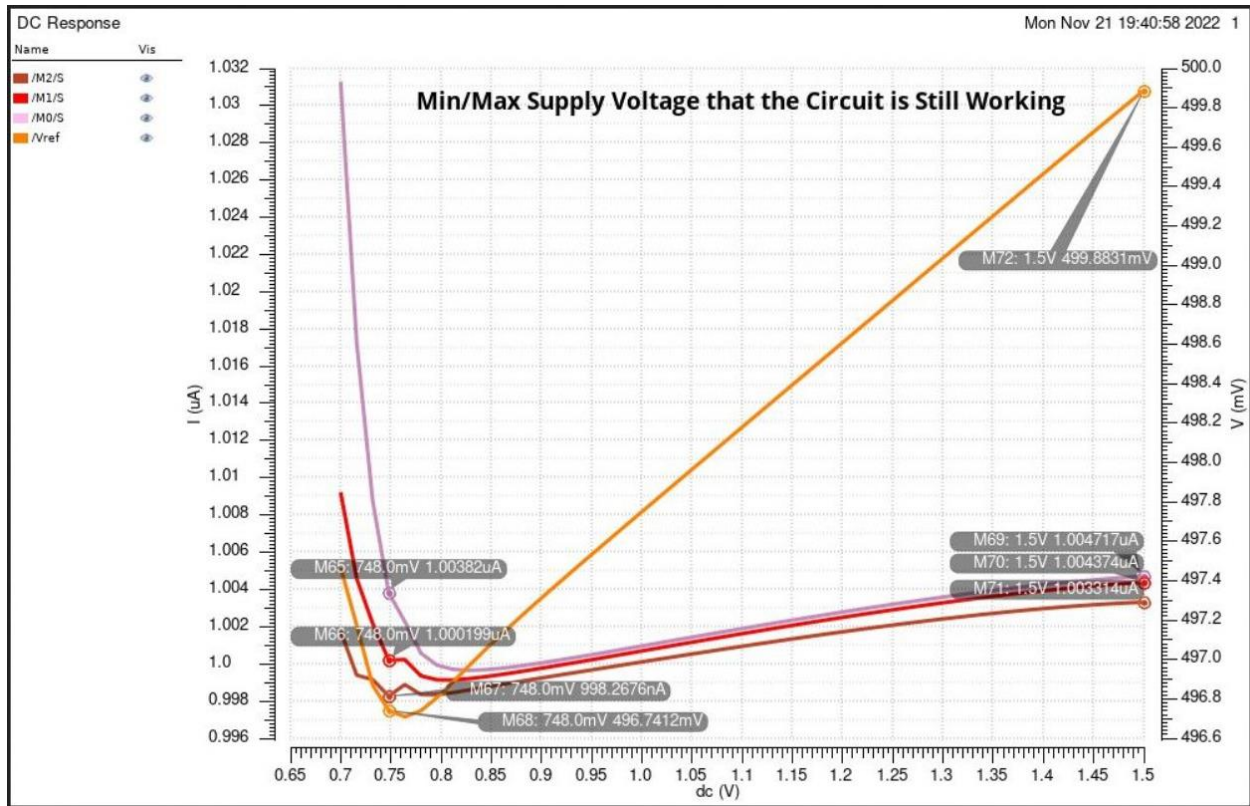


Figure 13: Minimum/Maximum Supply Voltage such that the Circuit is Still Working

Total Power Consumption

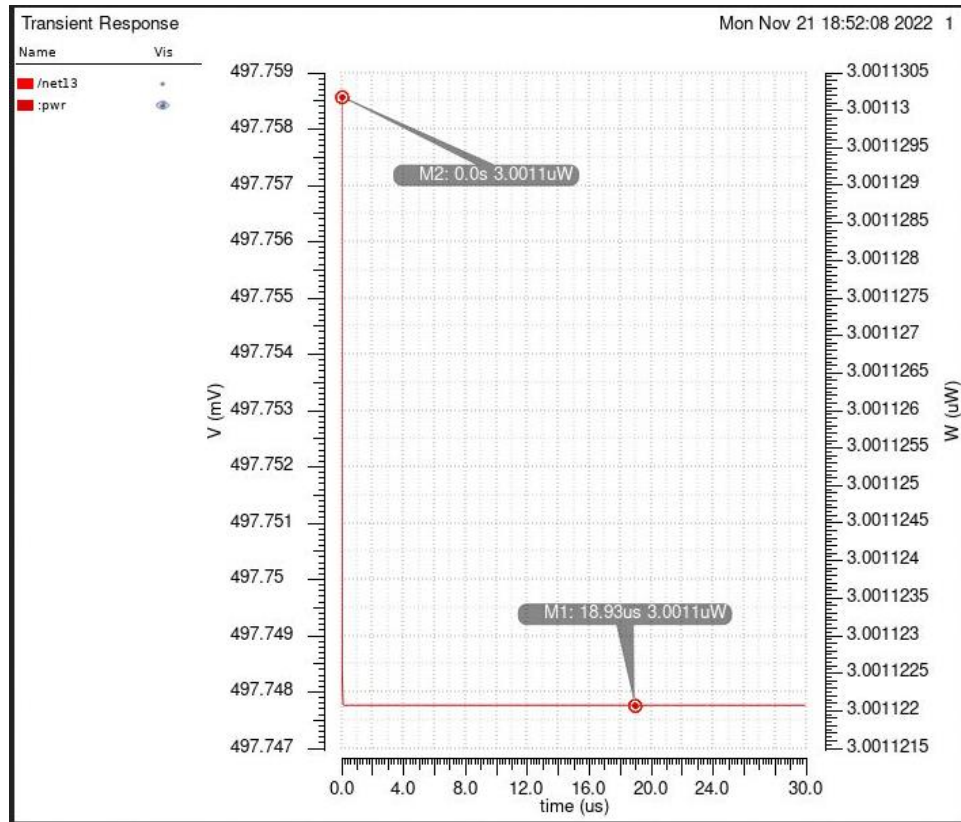


Figure 14: Total Power Consumption of the BGR Core

Vref and Iref within Temp Sweep (-20 to 100 C)

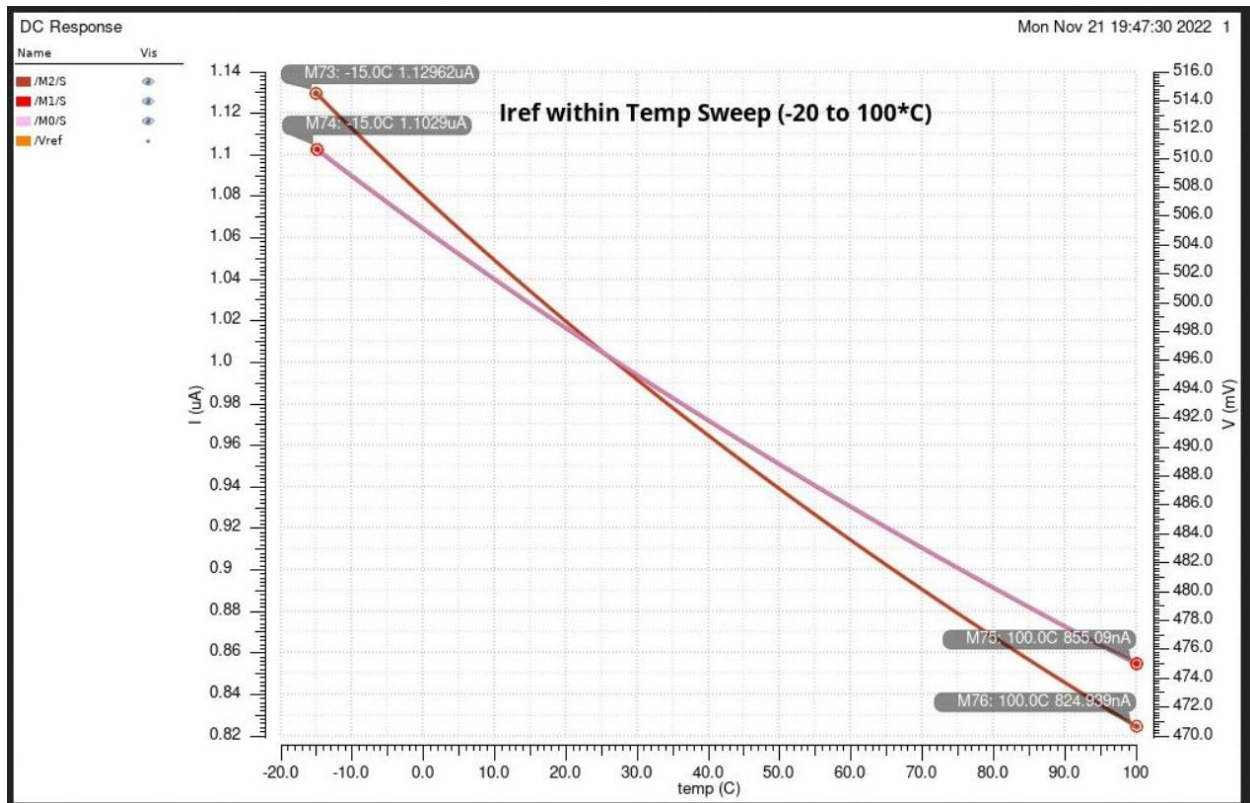


Figure 15: Iref vs. Temp Sweep

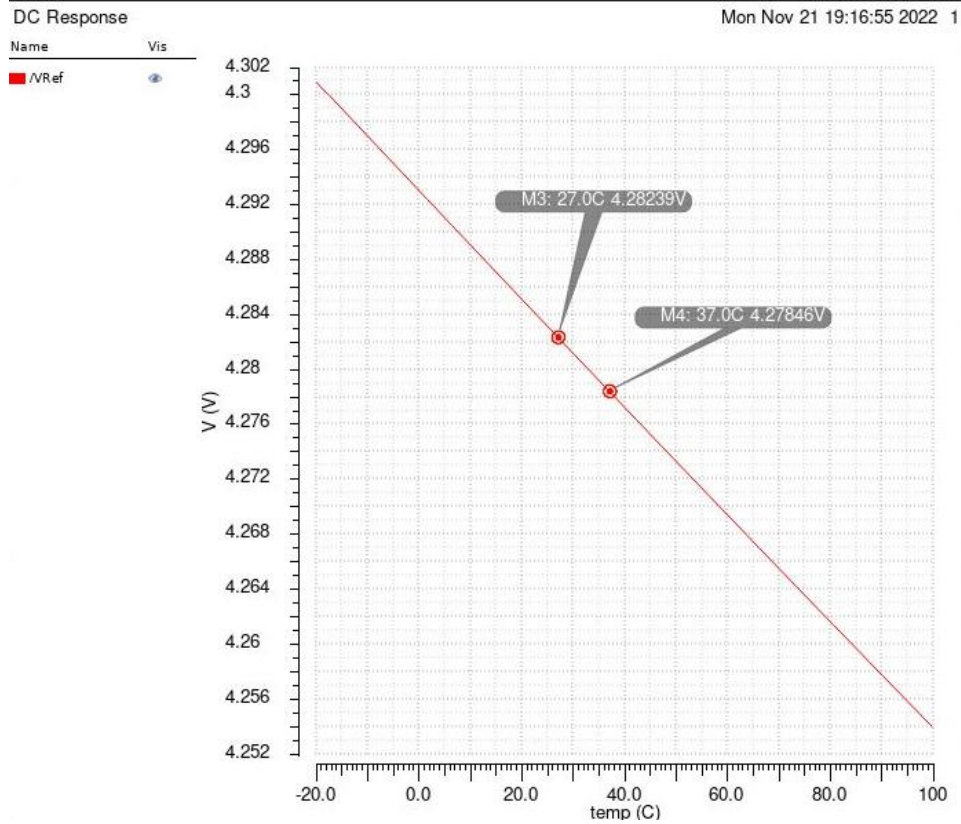


Figure 16: VDD with Temperature Sweep with 27°C and 37°C points

In Figure X, the 27°C and 37°C points are labeled for the Max Temp Analysis

Vref and Iref within Supply Sweep (10% to 150%)

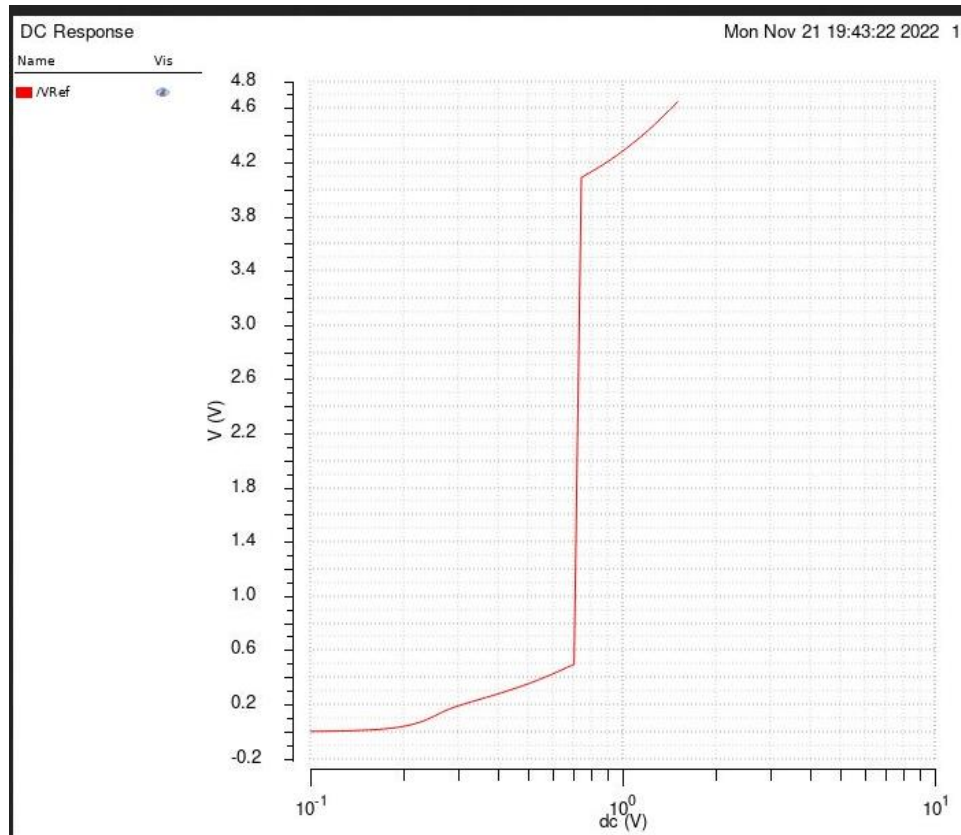


Figure 17: VREF Supply Sweep

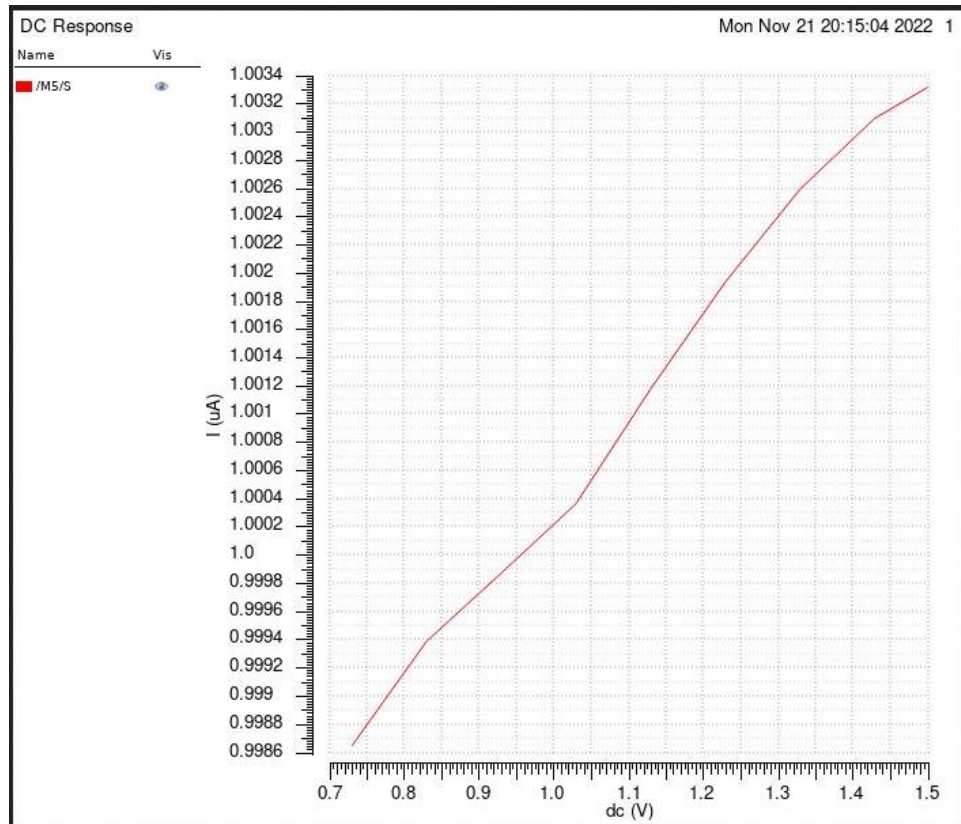


Figure 18: IREF Supply Sweep

TCIref (ppm) and TCVref (ppm)

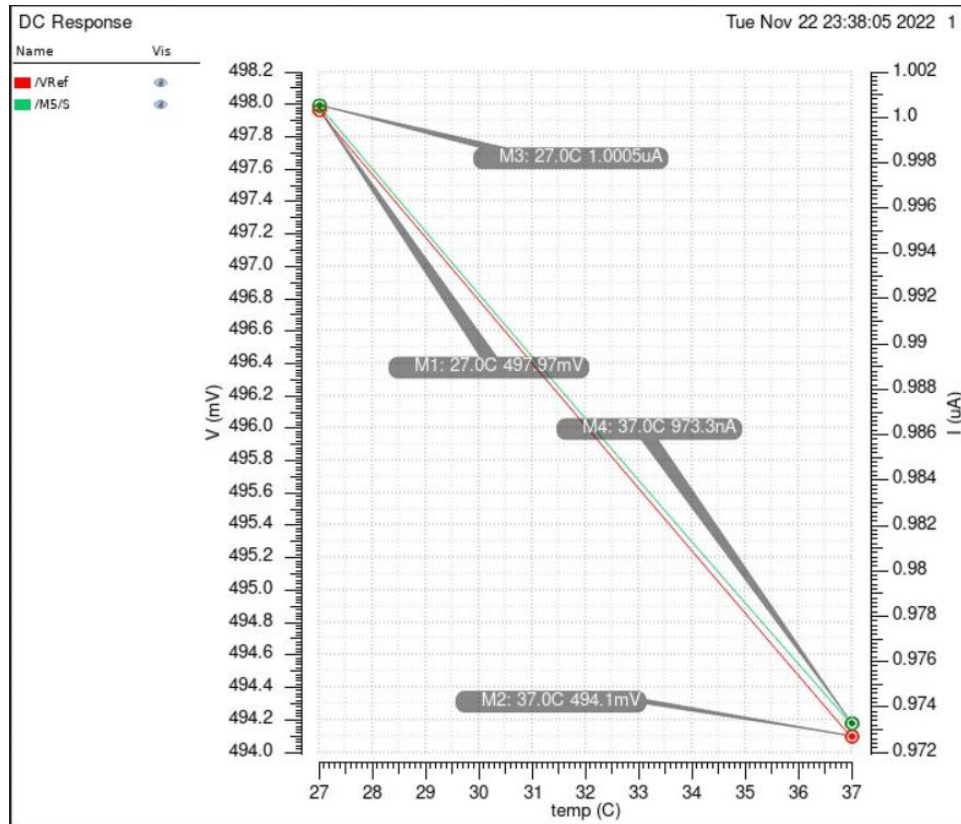


Figure 19: TCIREF and TCVREF

Figure X: VREF and IREF over the 27°C to 37°C

The slope of this graph would be the Temperature Coefficient

VREF

$$\frac{497.97\text{mV} - 494.1\text{mV}}{10^{\circ}\text{C}} = \frac{0.387\text{mV}}{^{\circ}\text{C}}$$

IREF

$$\frac{1000.5\text{nA} - 973.3\text{nA}}{10^{\circ}\text{C}} = \frac{2.72\text{nA}}{^{\circ}\text{C}}$$

Resistor Value (Ohm) and TCR1

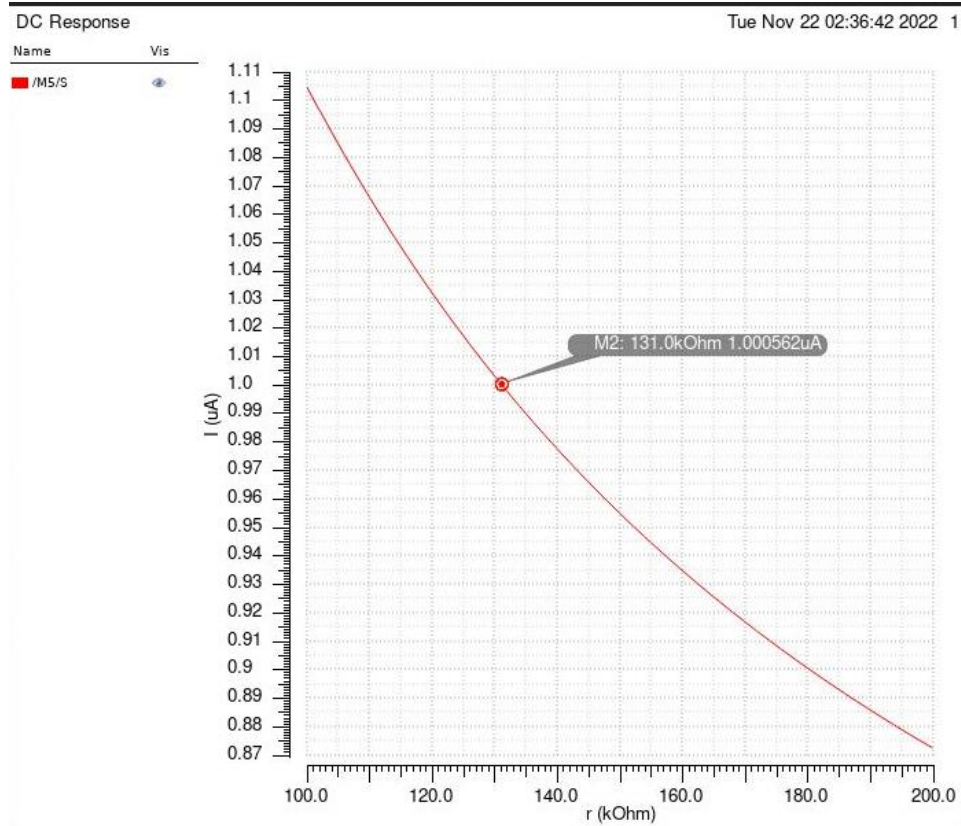


Figure 20: Resistor Value chose for 1uA IREF

For the simulations we used 0.002 for TCR1 (Temperature Coefficient for the Resistor) as per the project clarifications.

Startup Delay

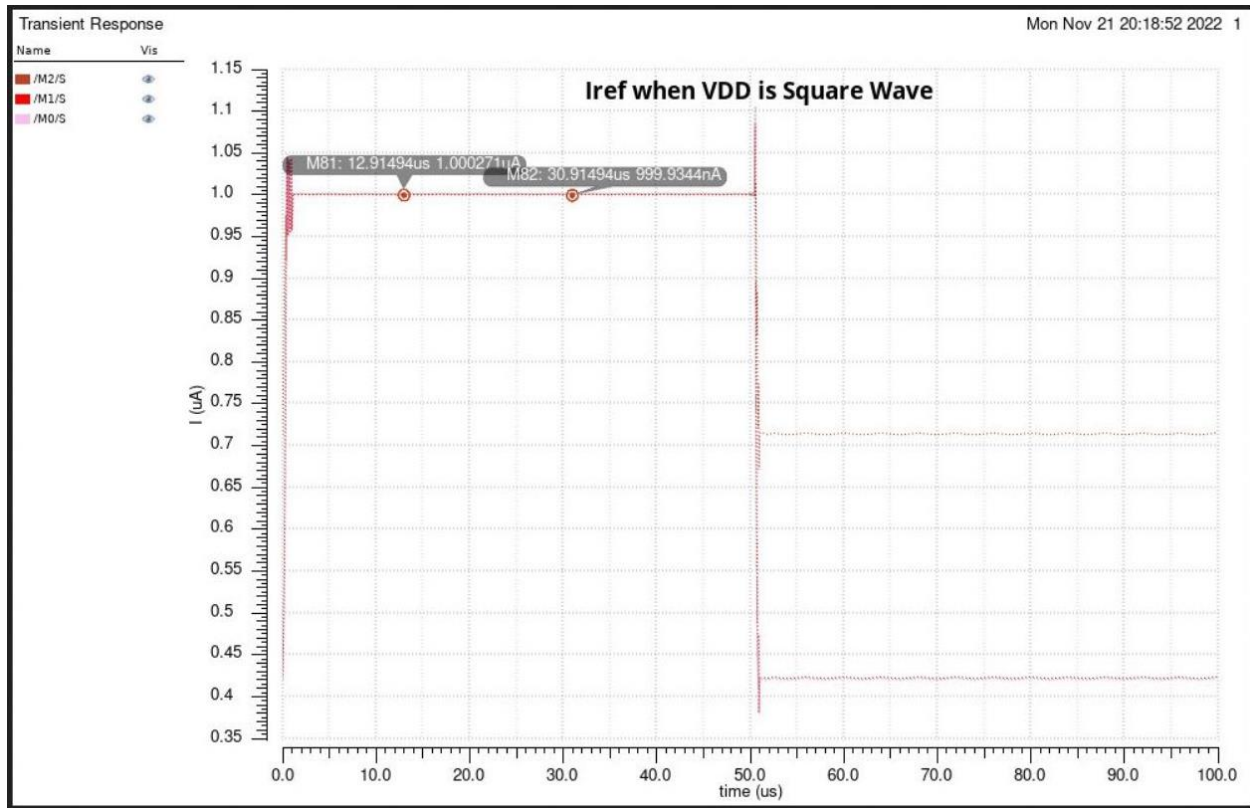


Figure 21: Iref under Square Wave

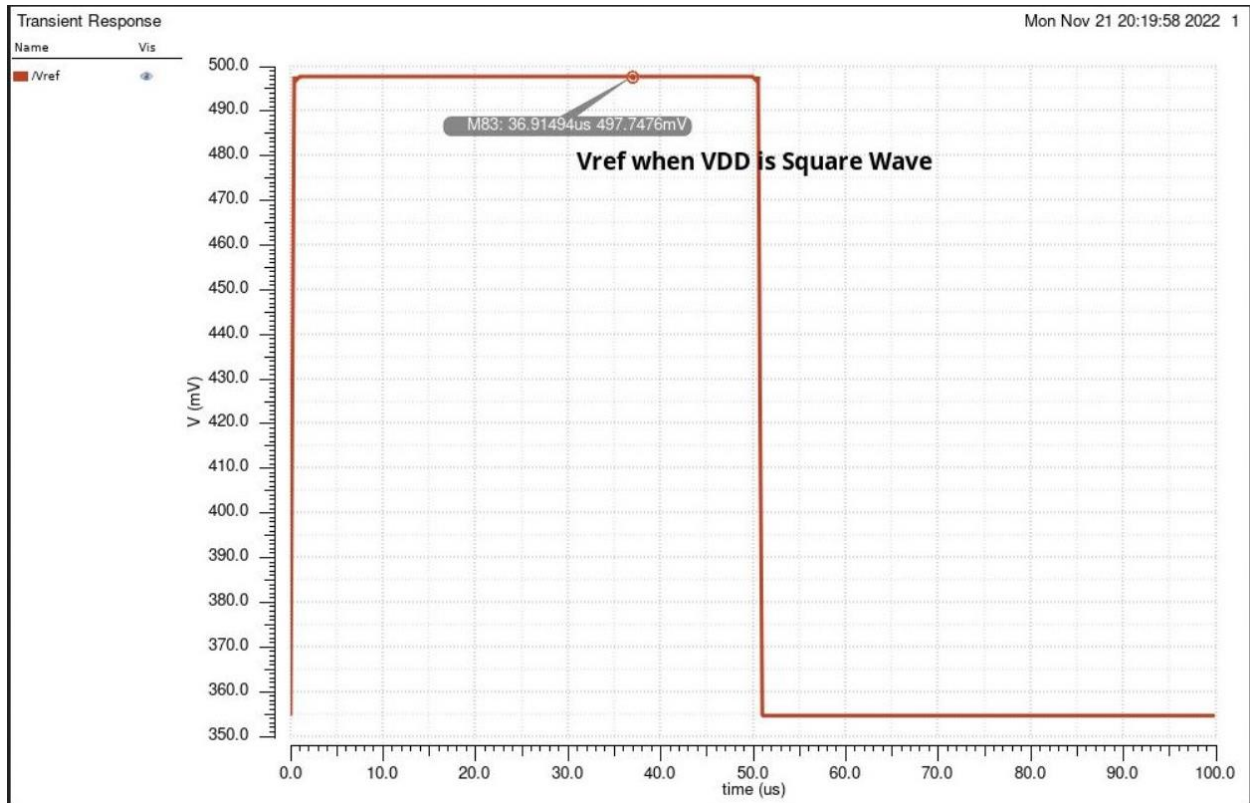


Figure 22: Vref under Square Wave

Comments

Particular Challenges?

- Becoming familiar with BGR technology
- Refreshing on BJT knowledge
- Startup circuit in project doc did not work, needed to find alternate circuit from work
- Getting reference circuit to output correct V_{ref} and I_{ref}
- Making schematic for bias circuit
- Sweeps for model parameters, global variables, and other new Cadence tricks

Other Possible Improvements?

- Voltage dividers in the BGR core for lower-voltage amplifiers

Part 2: Designing Bias Circuit

Biasing Circuit Schematic

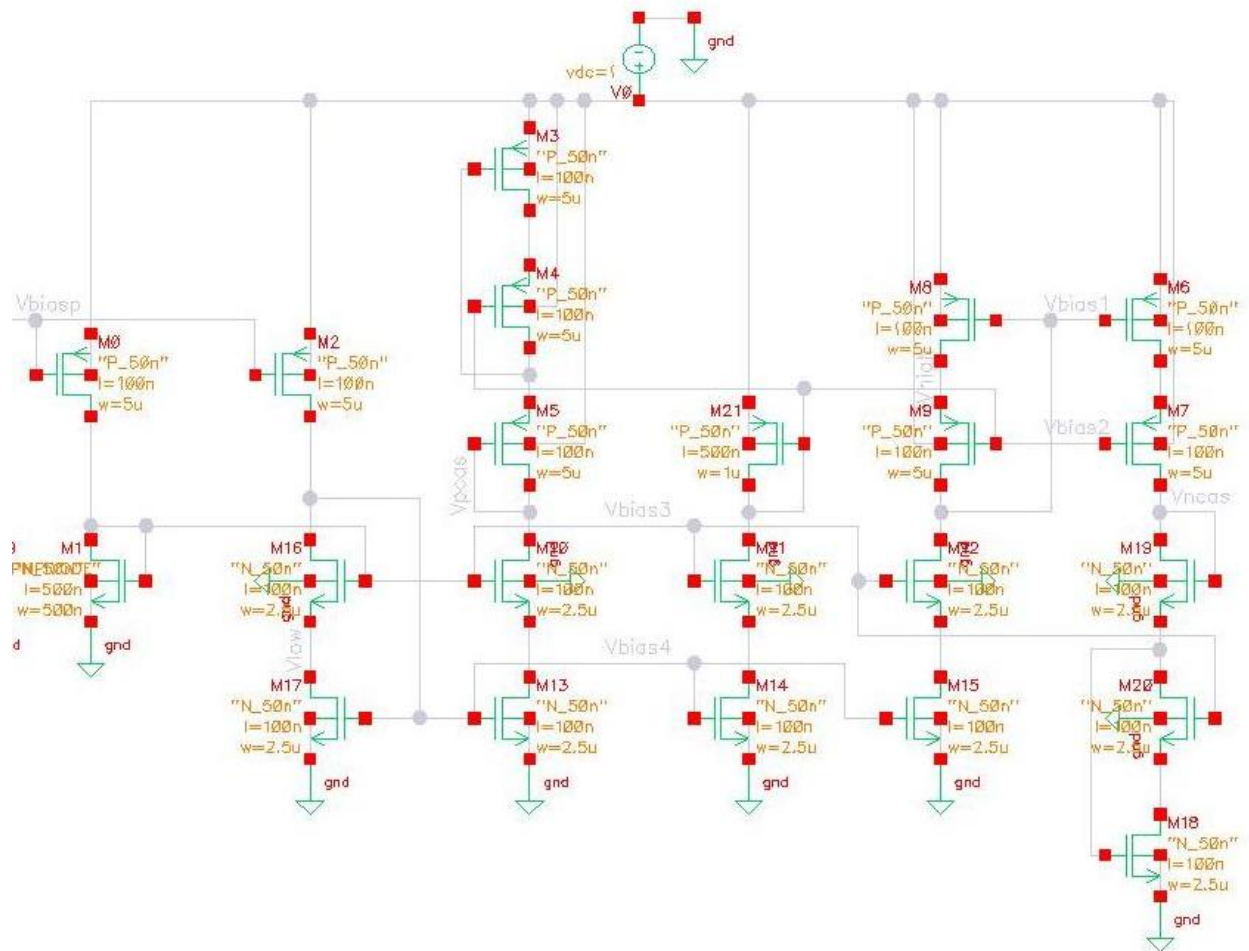


Figure 23: Biasing Circuit Schematic

BGR with Biasing Circuit Schematic

Hand Analysis in Finding Expected Values

Hand Analysis in Finding Expected Values

	$I_D = W \cdot V_{sat} \cdot L \cdot \alpha^1 (V_{gs} - V_{th} - V_{DSsat})$
	$\frac{I_D}{W \cdot V_{sat} \cdot L \cdot \alpha^1} = V_{gs} - V_{th} - V_{DSsat}$
NMOS	$V_{gs} = \frac{I_D}{W \cdot V_{sat} \cdot L \cdot \alpha^1} + V_{th} + V_{DSsat} = \frac{1 \mu A \cdot E^{-12}}{W \cdot 110E3 \cdot 25E-15 / E^{-12}} + 330 \text{ mV}$
	$= \frac{1E-9}{W \cdot 2.75} + 330 \text{ mV}$
PMOS	$V_{gs} = \frac{1E-9}{W \cdot 90E3 \cdot 25E-15} + 330 \text{ mV} = \frac{1E-9}{W \cdot 2.25} + 330 \text{ mV}$
$V_{gs}^{10/10}$	$V_{gs} = \frac{1E-9}{500E-15 \cdot 2.75} + 330 \text{ mV} = 330.73 \text{ mV}$
$V_{gs}^{20/10}$	$V_{gs} = \frac{1E-9}{1E-15 \cdot 2.25} + 330 \text{ mV} = 330.44 \text{ mV}$
$\frac{50}{2}$ Normal NMOS	$V_{gs} = \frac{1E-9}{2.5E-15 \cdot 2.75} + 330 \text{ mV} = 330.15 \text{ mV}$
$\frac{100}{2}$ Normal PMOS	$V_{gs} = \frac{1E-9}{5E-15 \cdot 2.25} + 330 \text{ mV} = 330.09 \text{ mV}$
V_{gs}	
$\sqrt{498 \text{ mV}}$	$V_{bias1} = V_{DD} - V_{gs} = 1V - 330 \text{ mV} = 670 \text{ mV}$
$\sqrt{41 \text{ mV}}$	$V_{bias2} = V_{DD} - V_{gs} - V_{DSsat} = 1V - 330 \text{ mV} - 50 \text{ mV} = 620 \text{ mV}$
$\sqrt{951 \text{ mV}}$	$V_{bias3} = V_{gs} + V_{DSsat} = 330 \text{ mV} + 50 \text{ mV} = 480 \text{ mV}$
$\sqrt{492 \text{ mV}}$	$V_{bias4} = V_{gs} = 330 \text{ mV}$
$\times 667 \text{ mV}$	$V_{high} = V_{DD} - V_{DSsat} = 1V - 50 \text{ mV} = 950 \text{ mV}$
$\sqrt{344 \text{ mV}}$	$V_{low} = V_{DSsat} = 50 \text{ mV}$
$\times 931 \text{ mV}$	$V_{bias5} = 2V_{gs} = 660 \text{ mV}$
$\times 52.7 \text{ mV}$	$V_{bias6} = V_{DD} - V_{gs} - V_{gs} = 1V - 660 \text{ mV} = 340 \text{ mV}$

Figure 25: Hand Calculations of BGR Bias Circuit

Values in Simulation for All Biasing Voltages

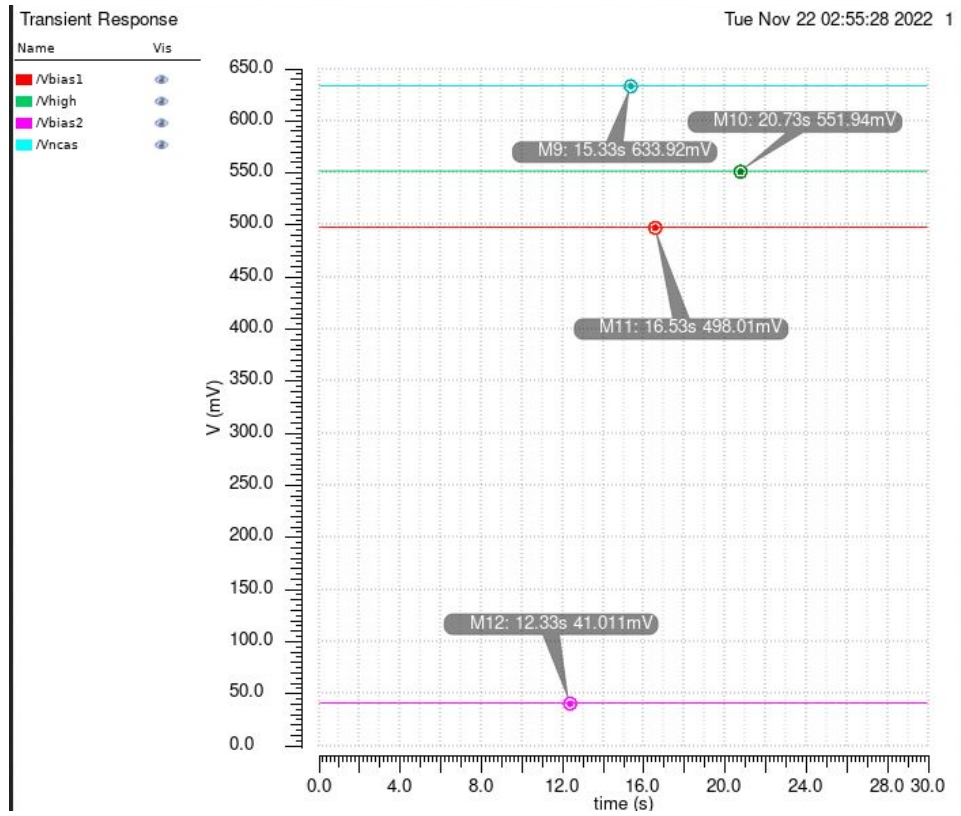


Figure 26: VBias1, VBias2, Vhigh, and Vncas

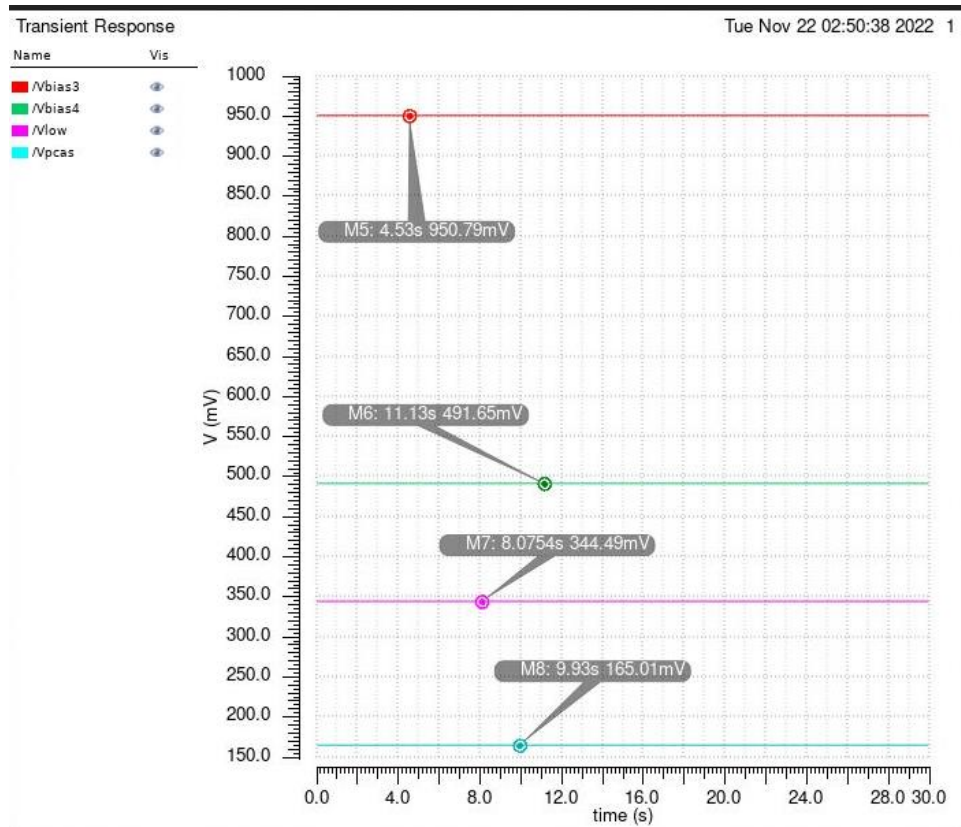


Figure 27: VBias3 VBias4, Vlow, and Vpcas

Supply Voltage Sweep for All Biasing Voltages

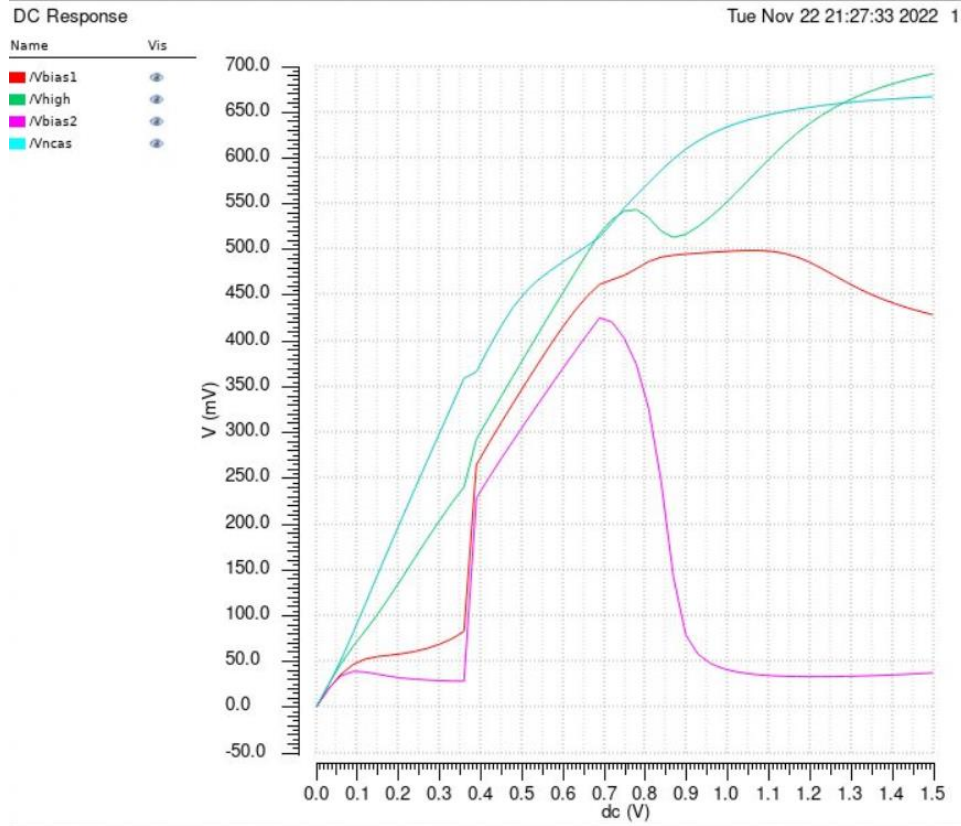
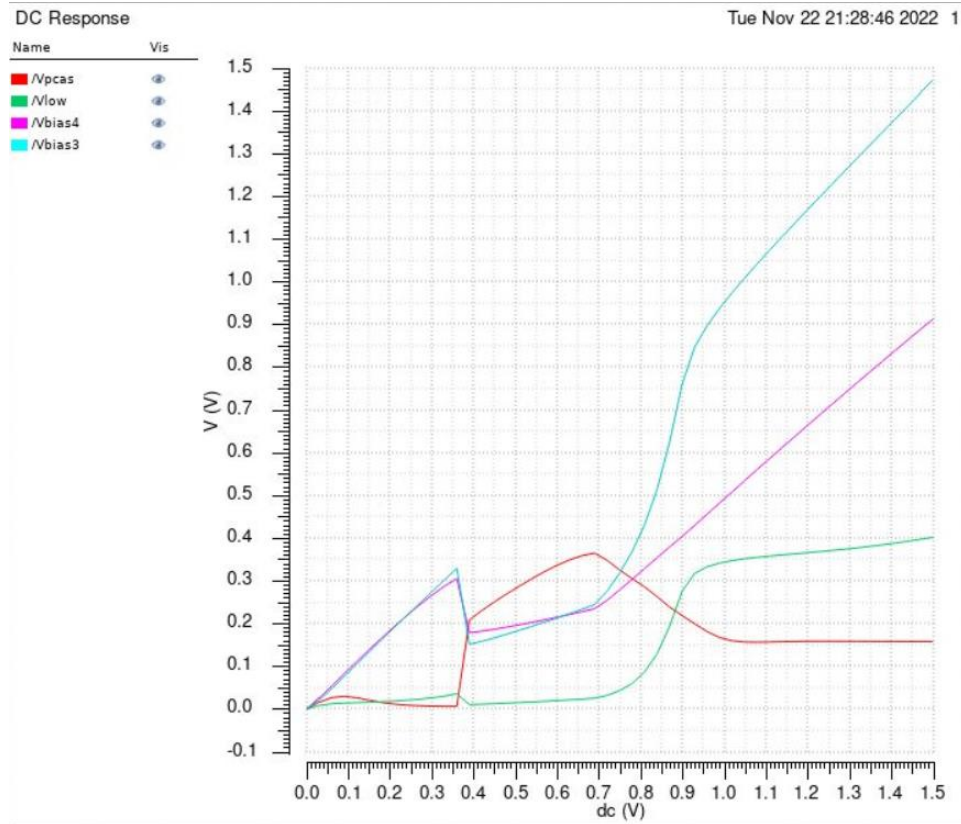


Figure 28: VBias1, VBias2, Vhigh, and Vncas with respect to VDD



Temperature Sweep from 0°C to 80°C for All Biasing Voltages

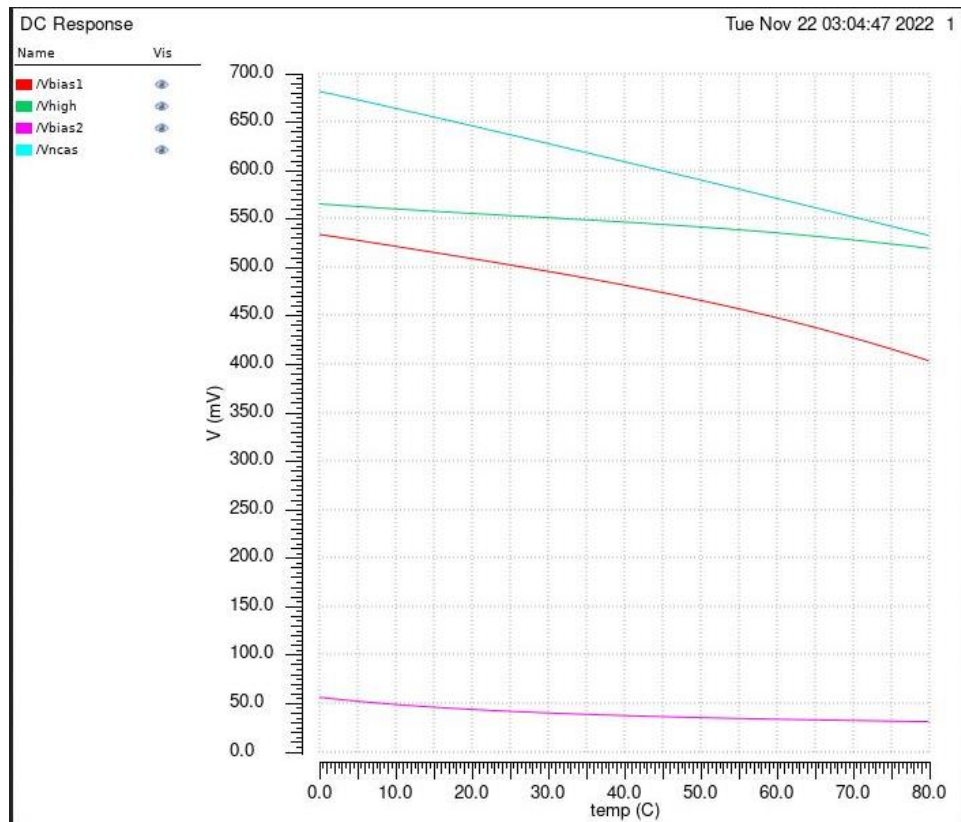


Figure 30: VBias1, VBias2, Vhigh, and Vncas with Respect to Temperature

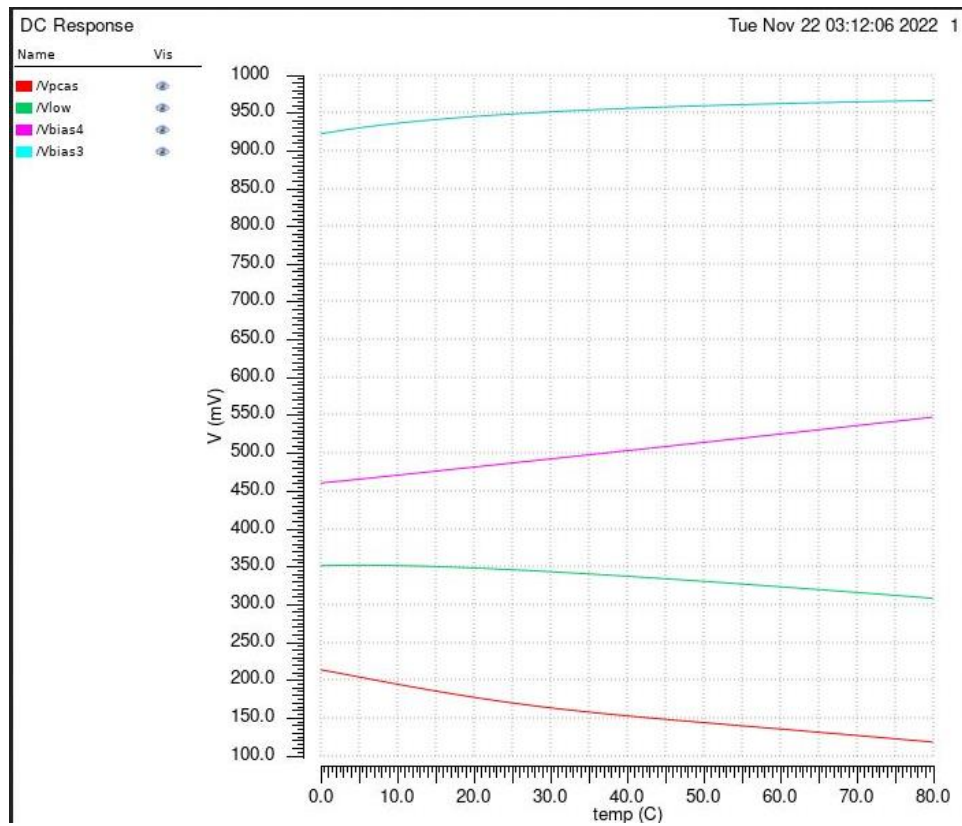


Figure 31: VBias3, VBias4, Vlow, and Vpcas with Respect to Temperature