ECE 4902 Analog Integrated Circuit Design – Project Report

Worcester Polytechnic Institute

B-Term 2022

Project 1: BGR 50n Short Channel Implementation

Submitted by

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Part 1: Designing BGR Core

CMOS Process: 50nm

Supply (V): 1V

Topology: Short Channel

Vref (V): 0.5V

BGR Core Schematic with Startup Circuit

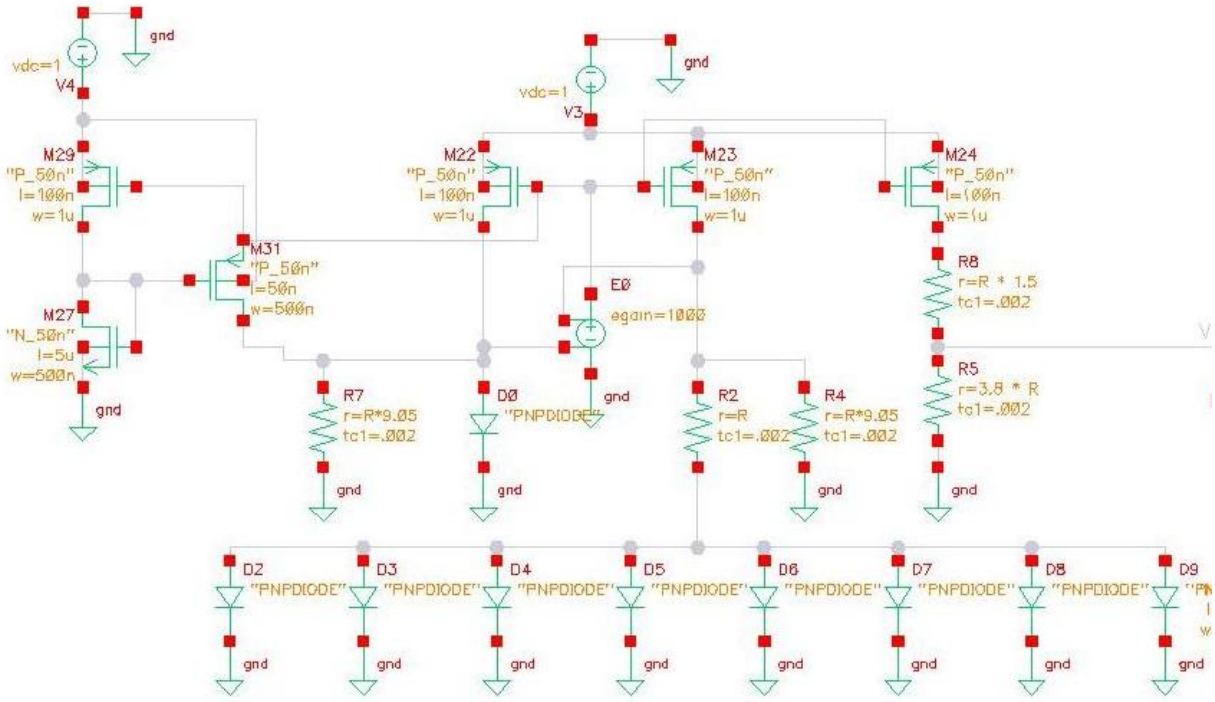

Figure 1: BGR Core Schematic with Startup Circuit

Iref (µA): 1µA

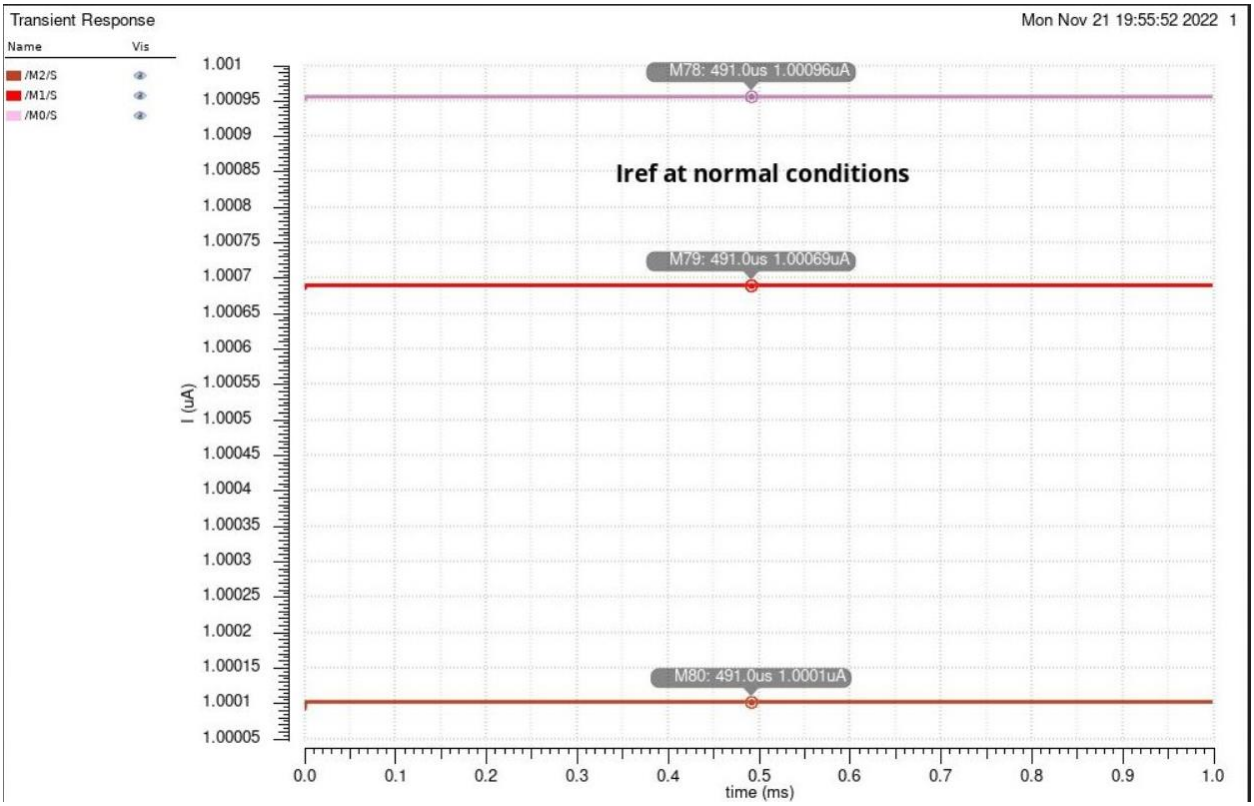

Figure 2: Iref under Normal Conditions

Vref (V): 500mV

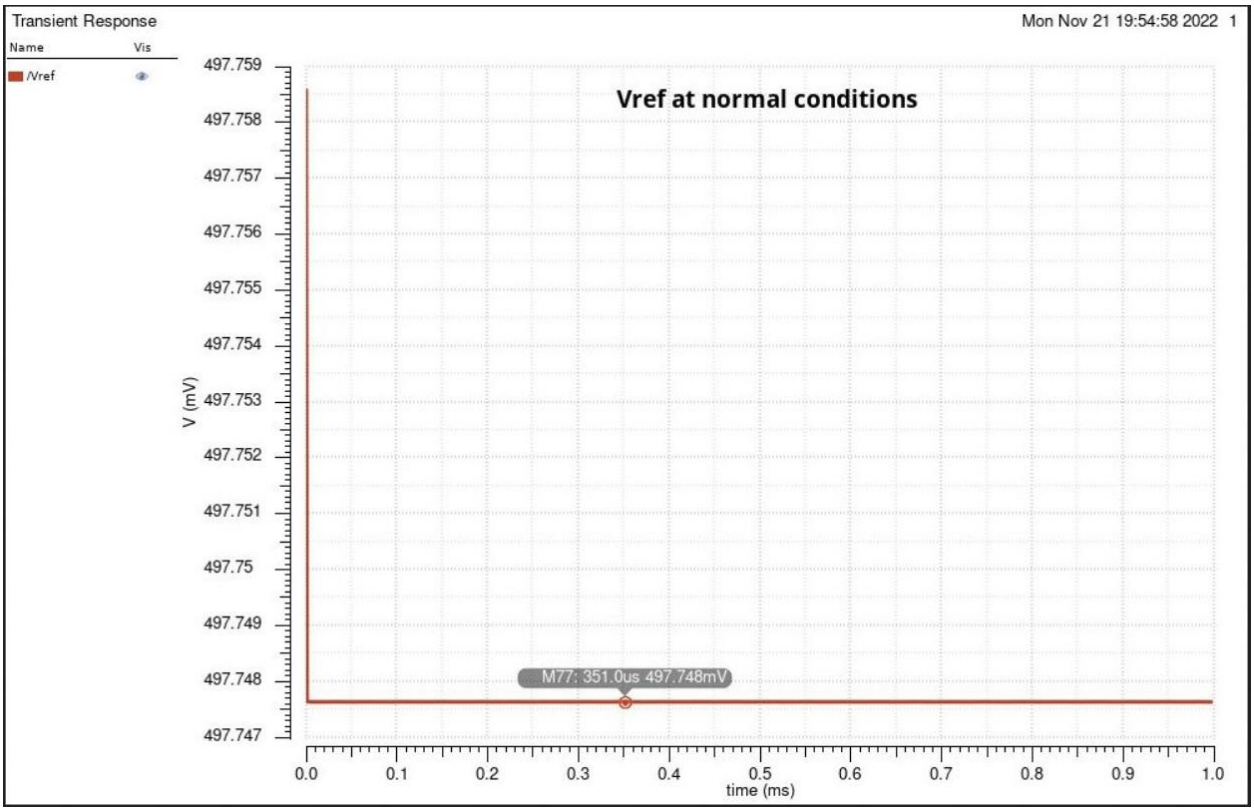

Figure 3: Vref under Normal Conditions

Max. Supply Sensitivity (ppm): 1500ppm

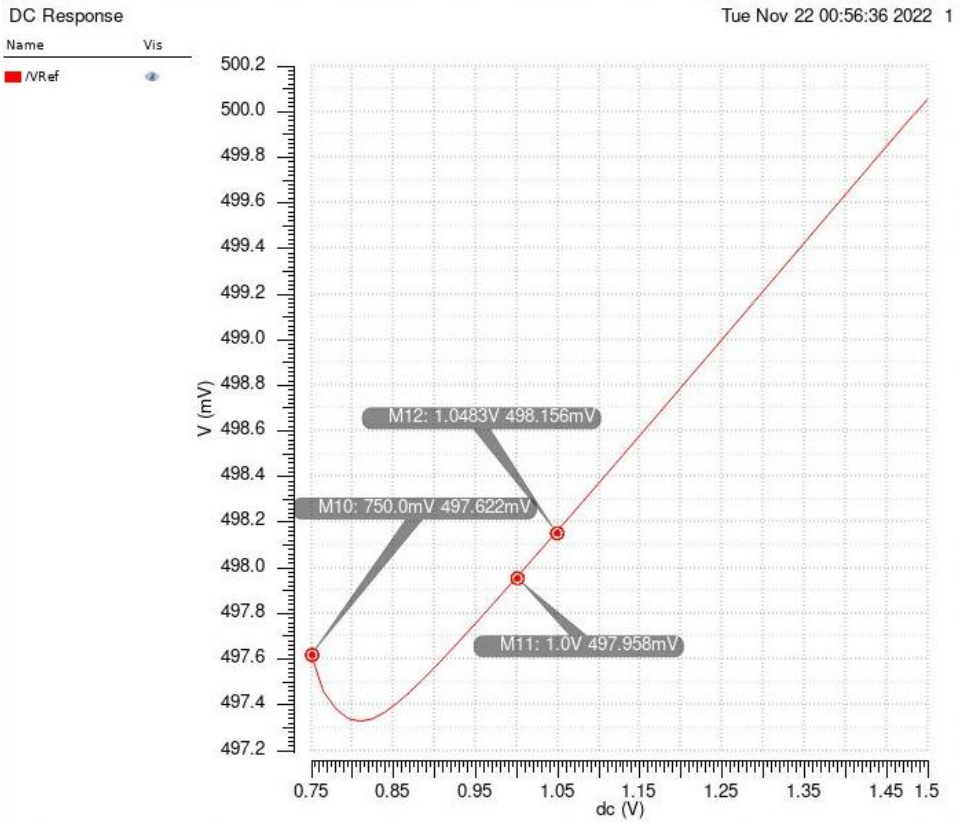

Figure 4: VREF from Vomin to 1.5VDD

Used Vomin to 1.1*VDD

Max Supply Sensitivity = $\frac{\Delta VREF}{VREFnom} \cdot 1 \cdot 10^6$

$\frac{0.4981555-0.49732754}{0.4979576} \cdot 1 \cdot 10^6$ = 1071.59 ppm

This is within spec as the max allowable is 1500ppm

Max. Temp Sensitivity (ppm @ C): 100ppm @ 37°C

Max Temp. Stability = $\frac{\Delta VREF}{VREFnom} \cdot 1 \cdot 10^6 \cdot \frac{1}{37^\circ C - 27^\circ C}$

$$\frac{4.28239V - 4.27846V}{4.28239V} \cdot 1 \cdot 10^6 \cdot \frac{1}{37^\circ C - 27^\circ C} = 91.7712 \ \frac{ppm}{^\circ C} \ @ \ 37^\circ C$$

This is within spec as the max allowable is 100 @37°C

Max. Power Consumption (µW): 10µW

From the Total Power Consumption Graph in Figure X, below, the Max Power Consumption is 3.0011µW

∆Iref with ∆R = ±10% around Nominal Value

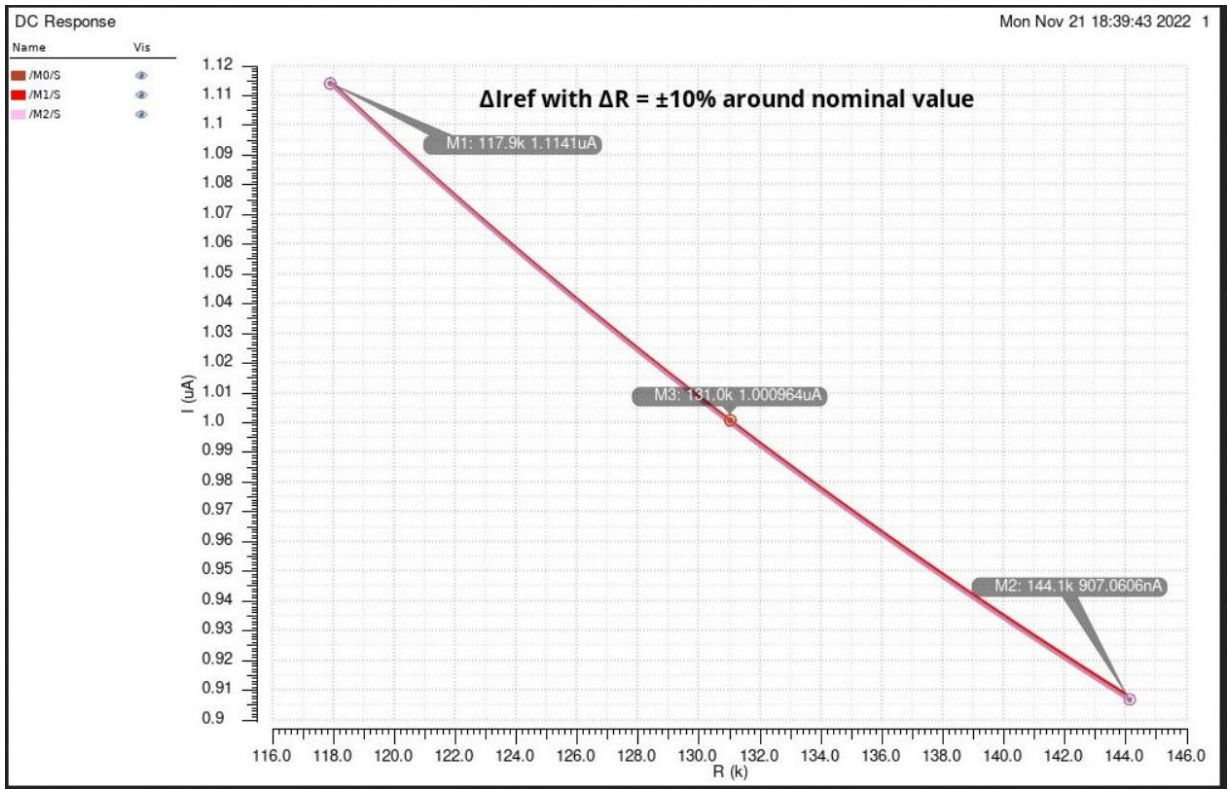

Figure 5: ∆Iref with ∆R = ±10% around Nominal Value

∆Iref with ∆VDD = ±10% Nominal Value

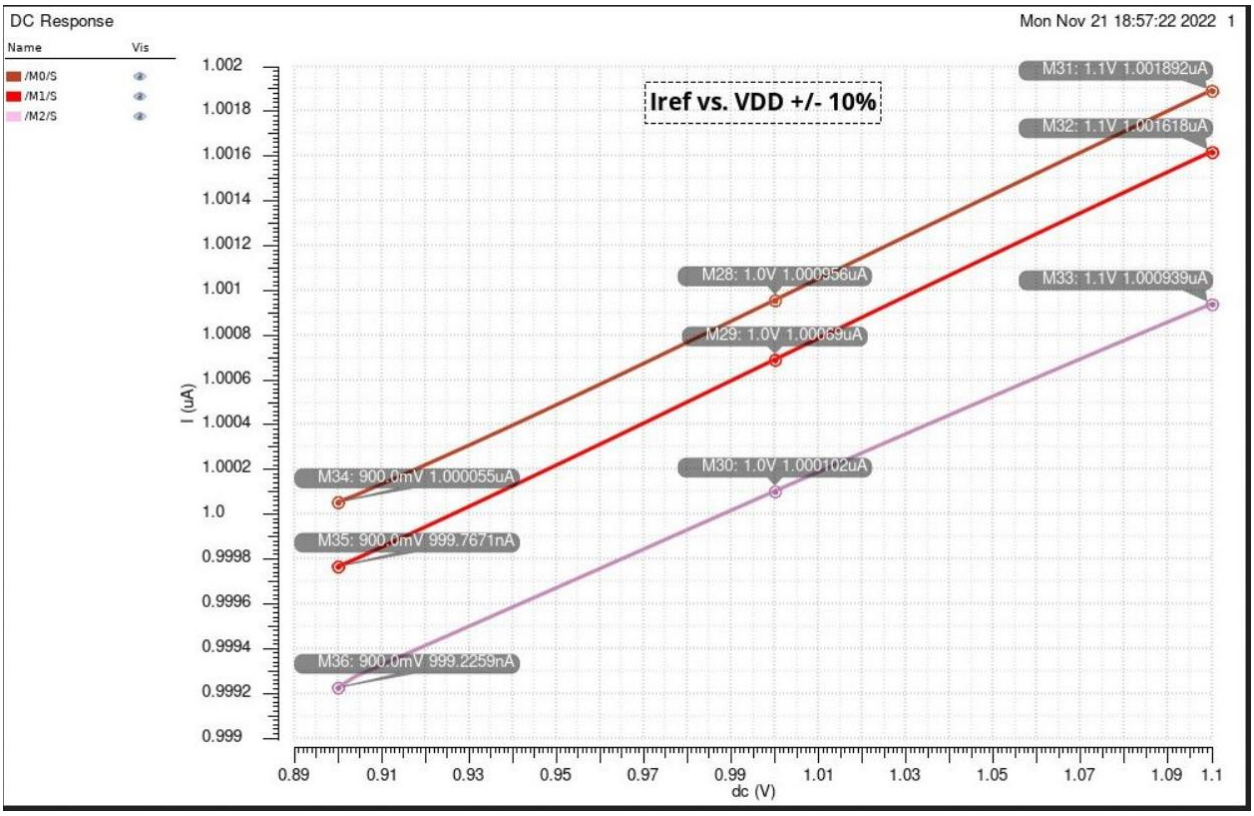

Figure 6: Iref vs. VDD

Iref with ΔVTHn = ±10% and ΔVTHp = ±10% Nominal Value

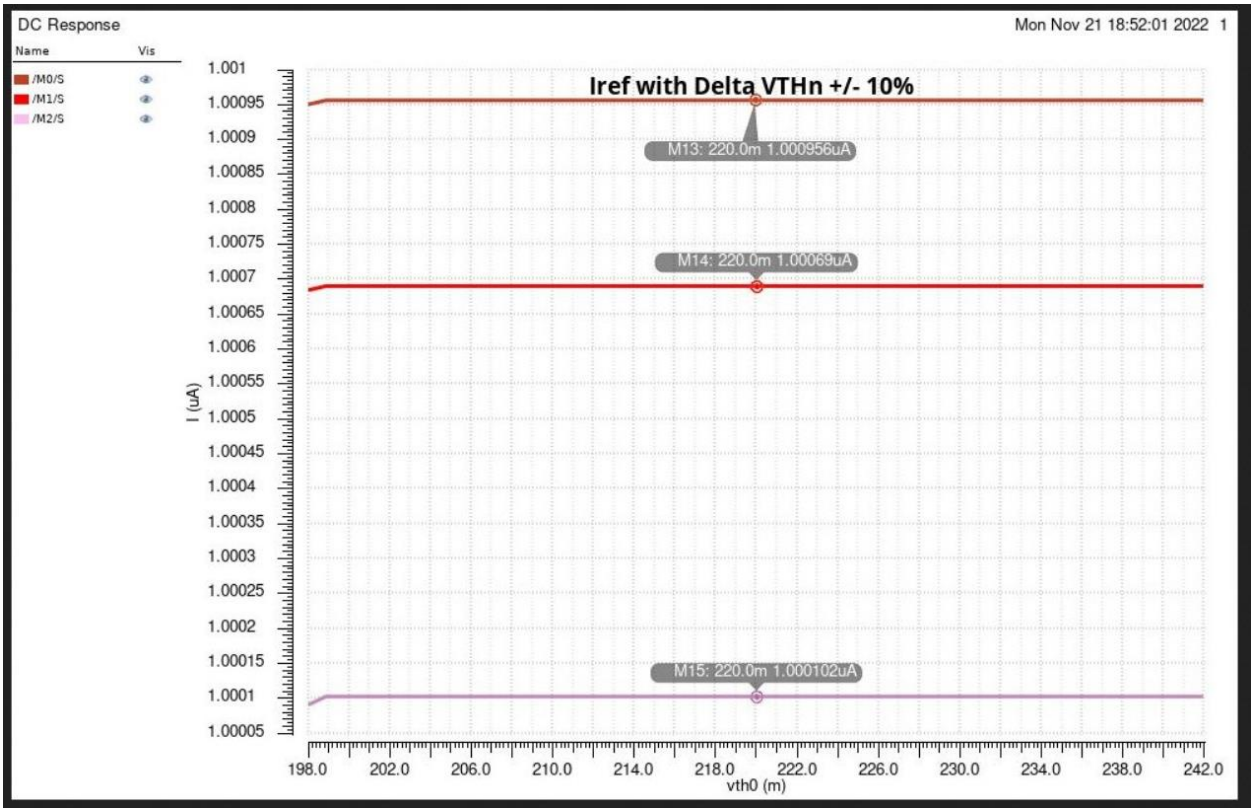

Figure 7: Iref vs. VTHn

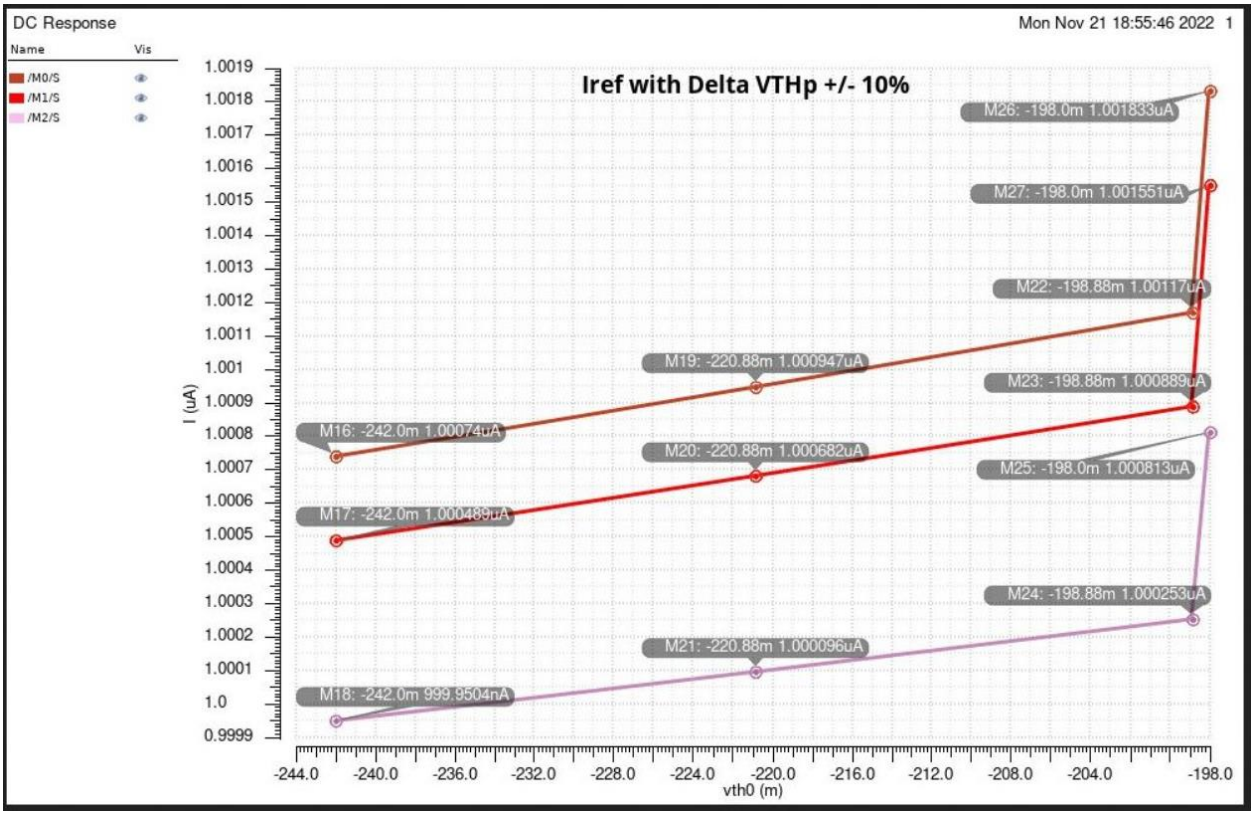

Figure 8: Iref vs. VTHp

∆Vref with ∆R = ±10% Nominal Value

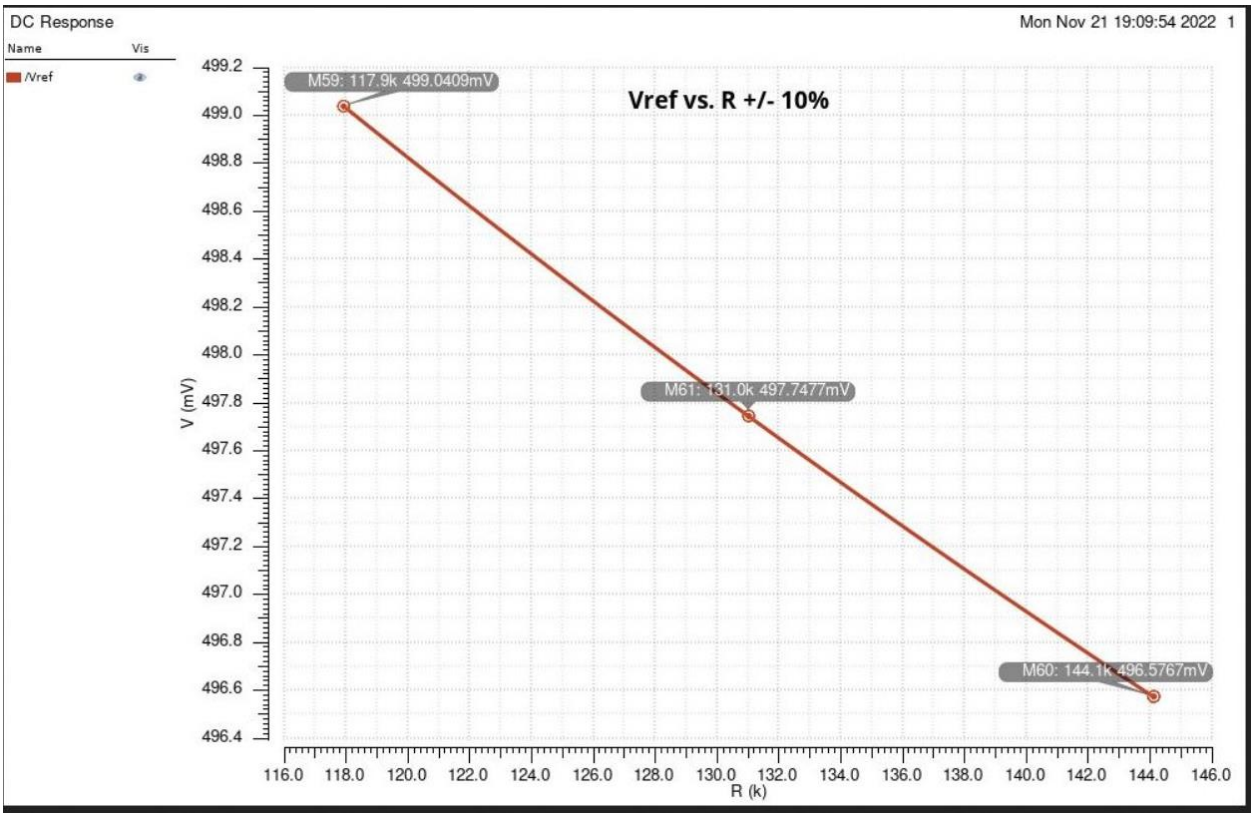

Figure 9: Iref vs. R

∆Vref with ∆VDD = ±10% Nominal Value

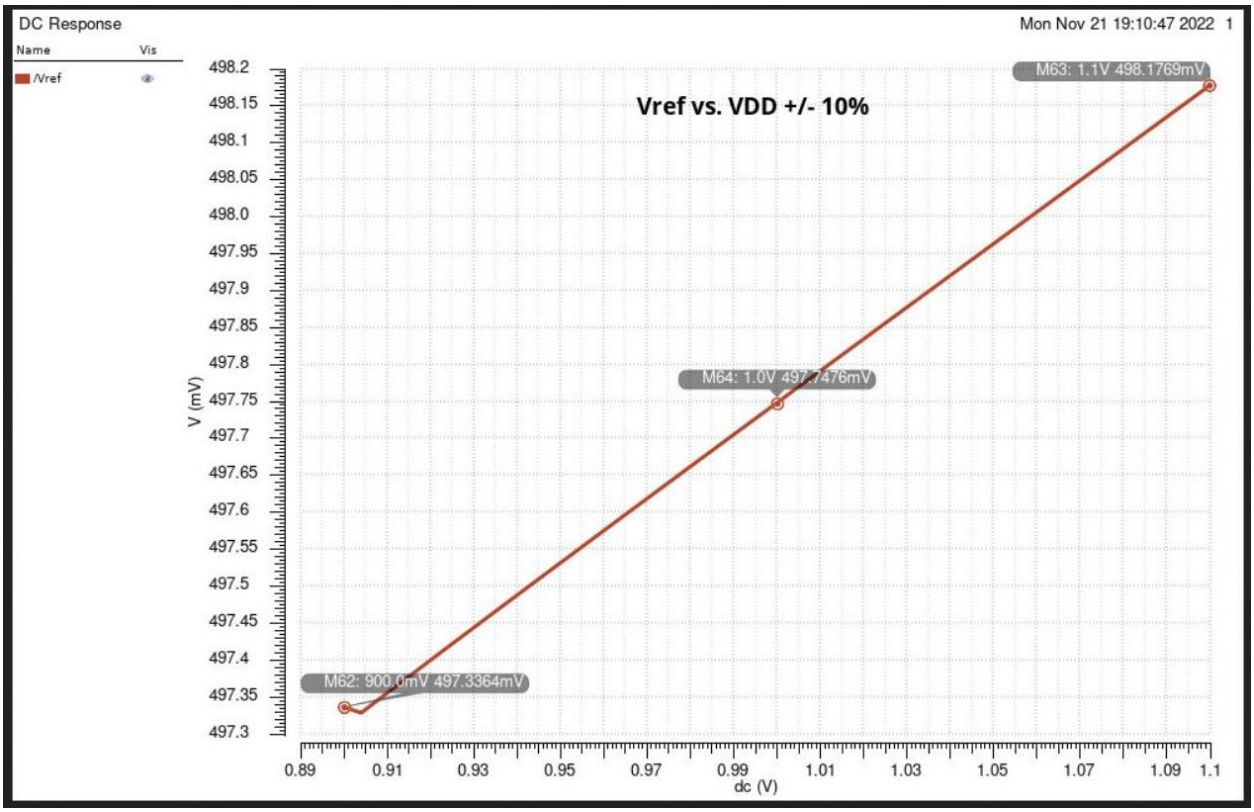

Figure 10: Vref vs. VDD

ΔVref with ΔVTHn = ±10% and ΔVTHp = ±10% Nominal Value

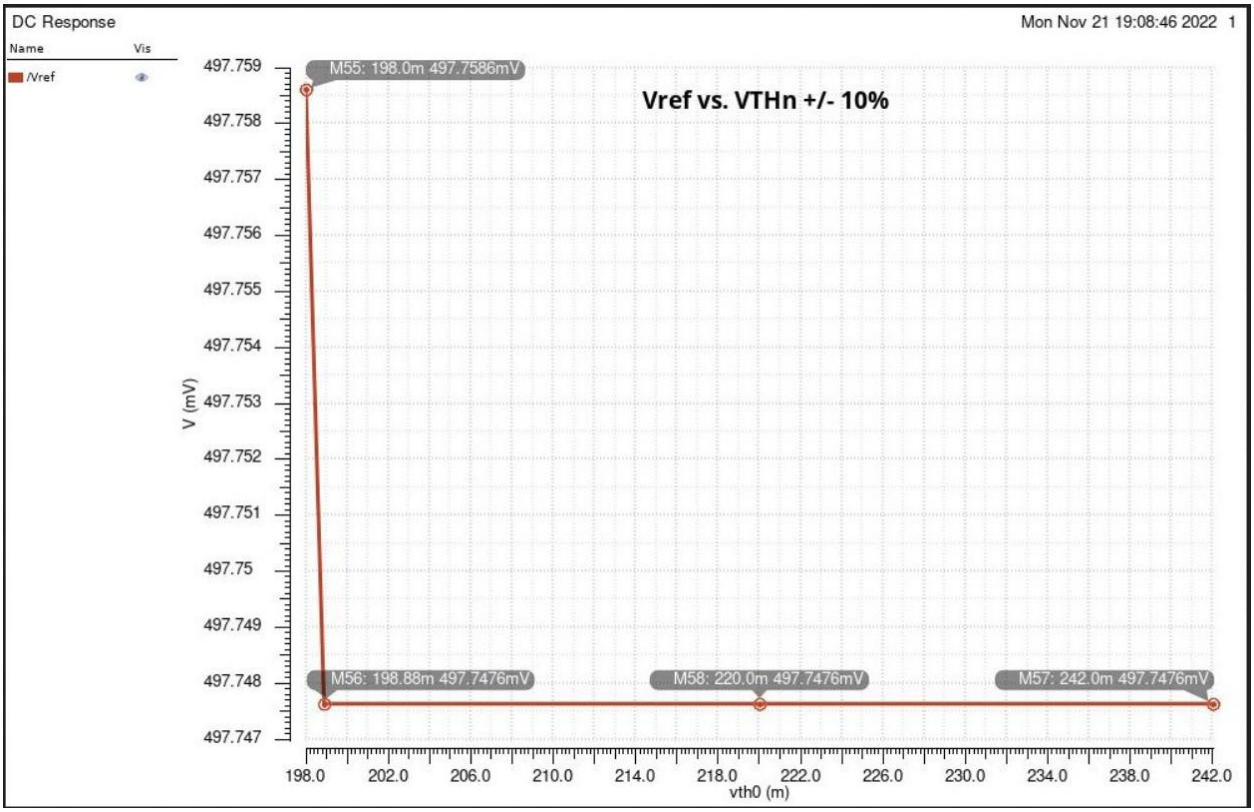

Figure 11: Vref vs. VTHn

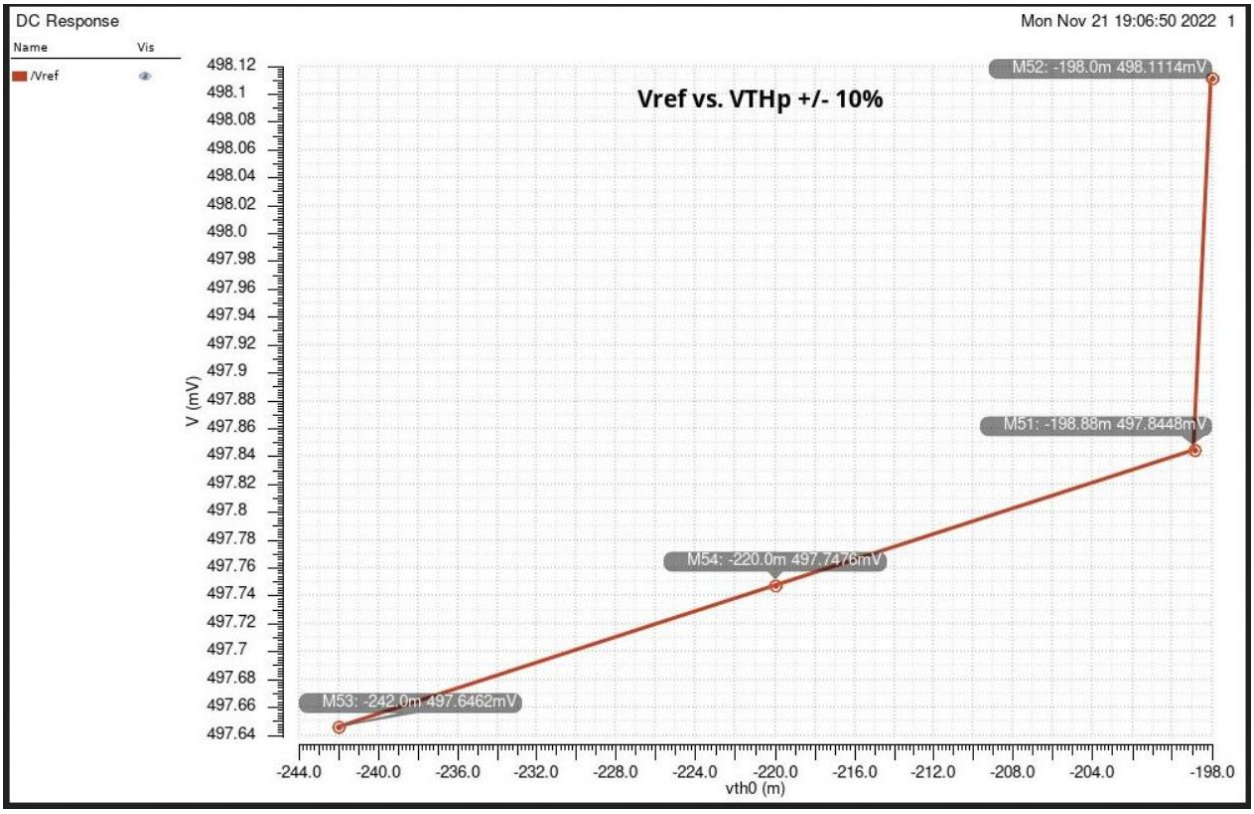

Figure 12: Vref vs. VTHp

Minimum/Maximum Supply Voltage such that the Circuit is Still Working

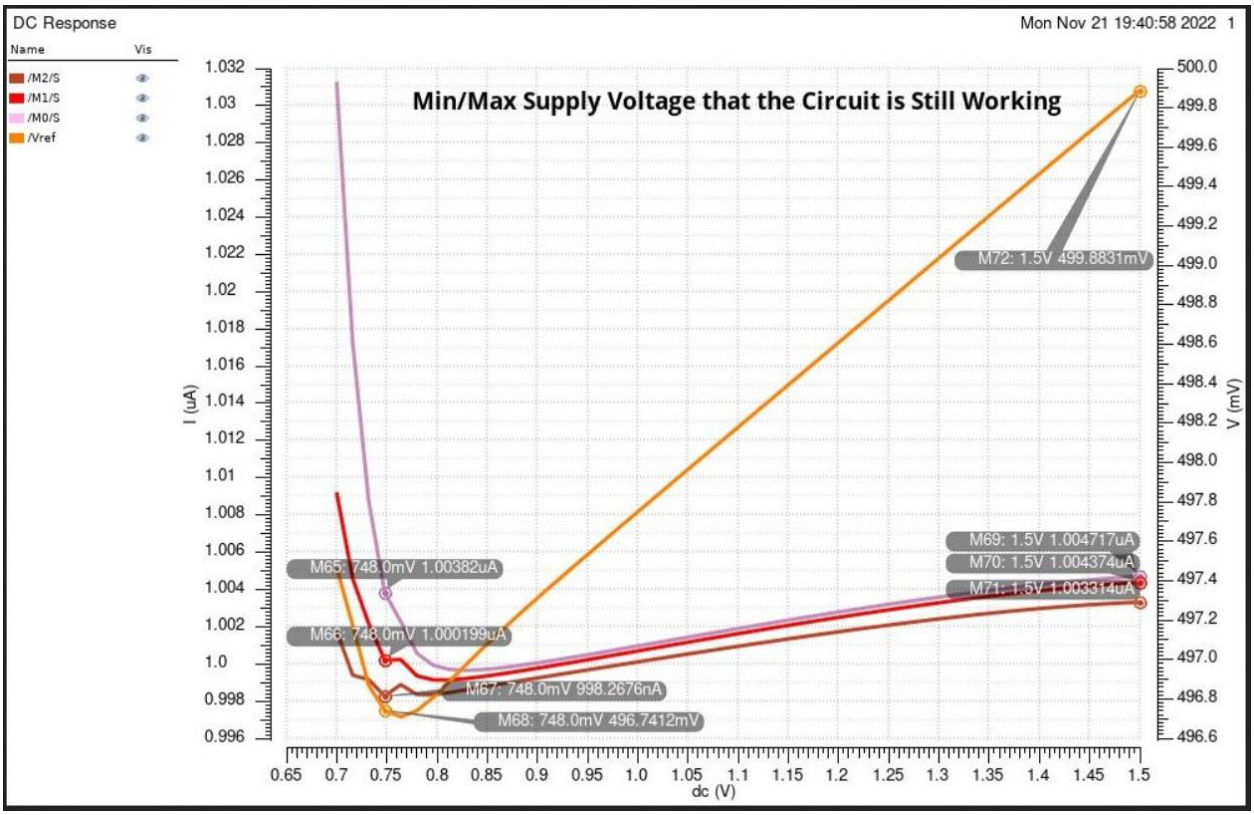

Figure 13: Minimum/Maximum Supply Voltage such that the Circuit is Still Working

Total Power Consumption

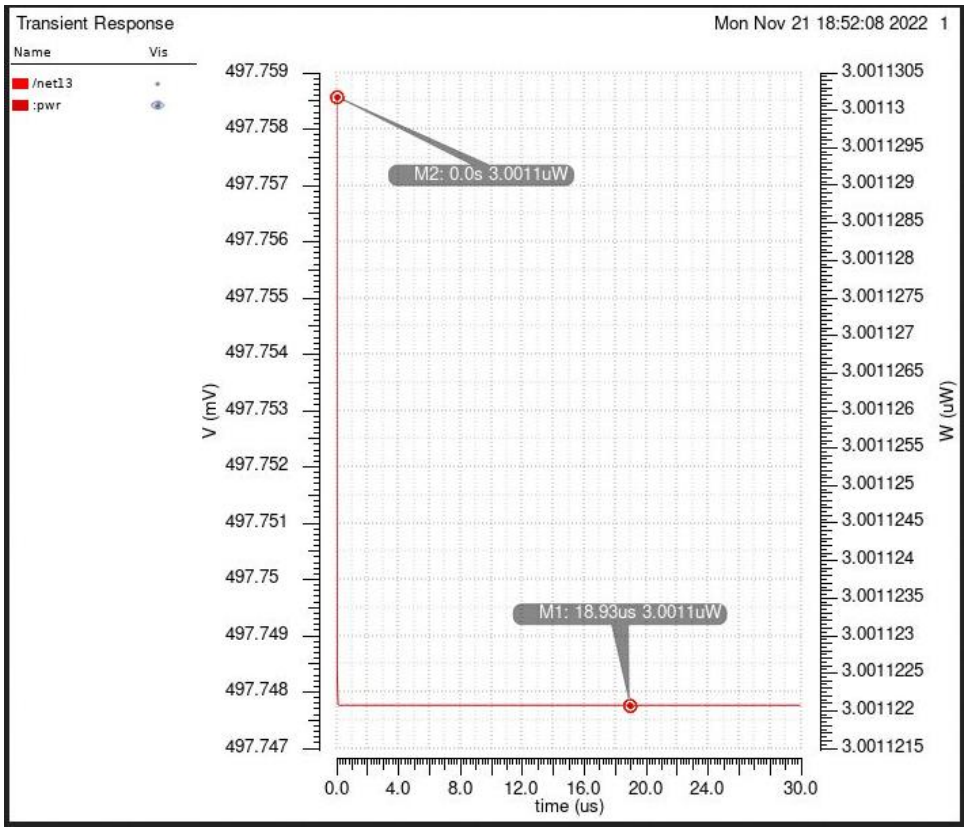

Figure 14: Total Power Consumption of the BGR Core

Vref and Iref within Temp Sweep (-20 to 100 C)

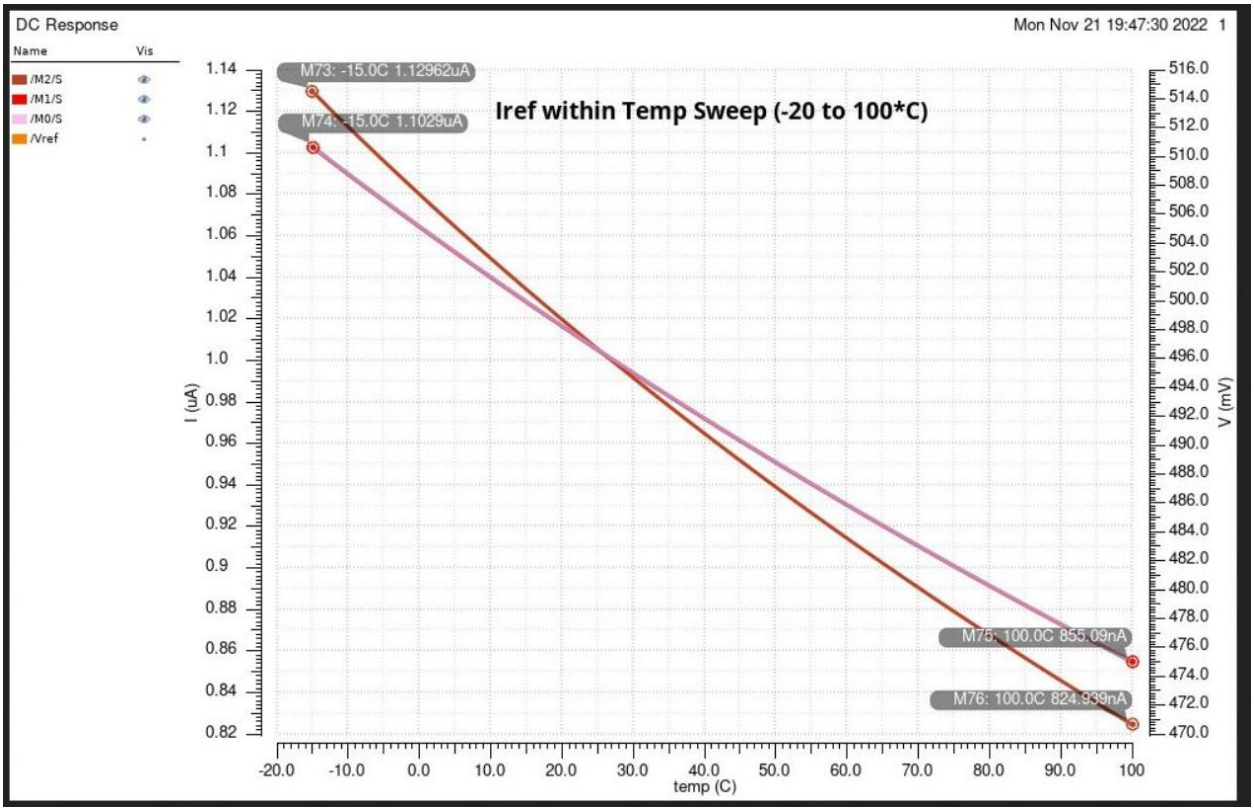

Figure 15: Iref vs. Temp Sweep

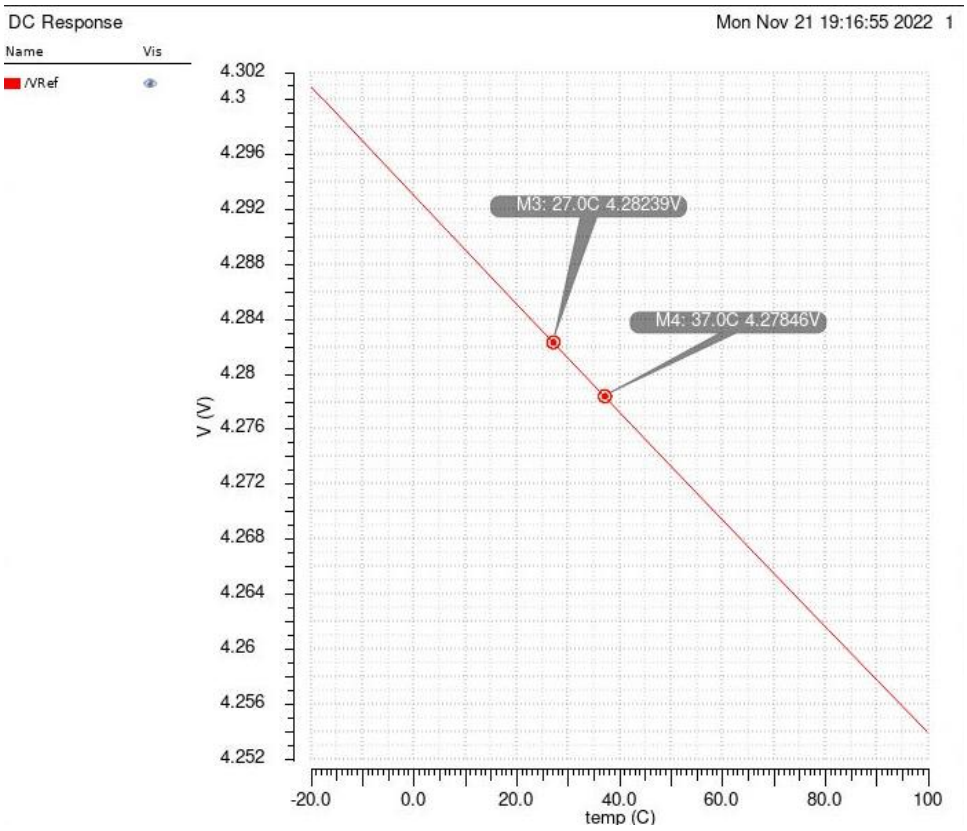

Figure 16: VDD with Temperature Sweep with 27°C and 37°C points

In Figure X, the 27°C and 37°C points are labeled for the Max Temp Analysis

Vref and Iref within Supply Sweep (10% to 150%)

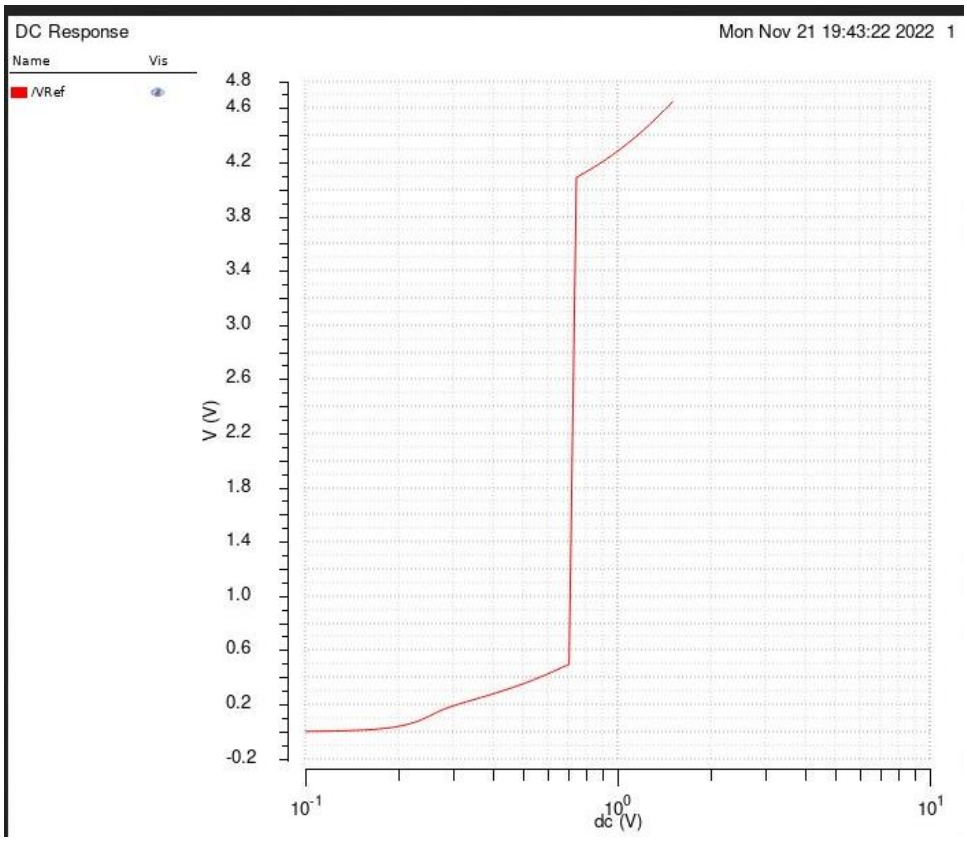

Figure 17: VREF Supply Sweep

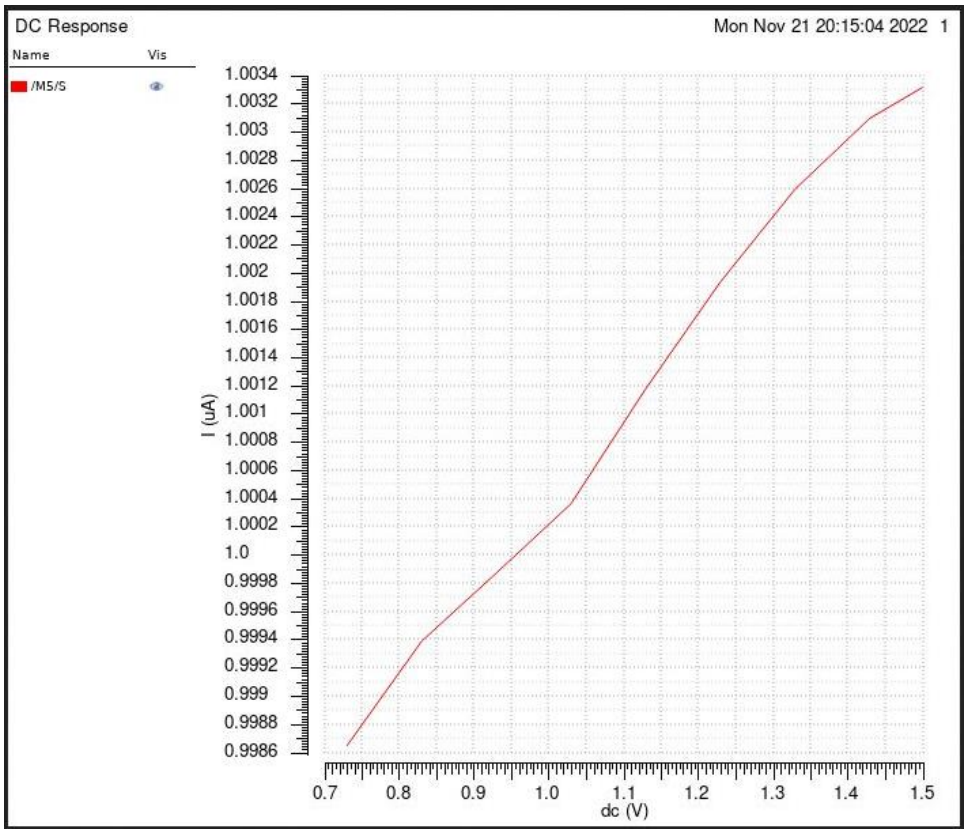

Figure 18: IREF Supply Sweep

TCIref (ppm) and TCVref (ppm)

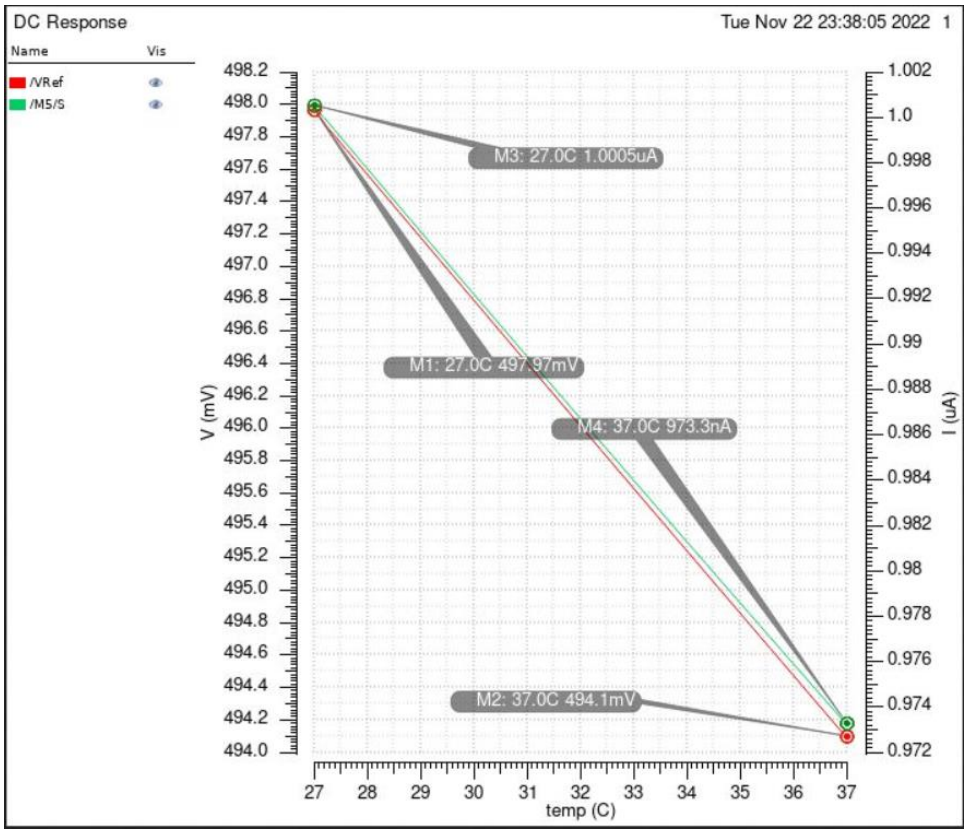

Figure 19: TCIREF and TCVREF

Figure X: VREF and IREF over the 27°C to 37°C

The slope of this graph would be the Temperature Coefficient

VREF

$$\frac{\mathbf{497.97mV - 494.1mV}}{\mathbf{10}℃} = \frac{\mathbf{0.387mV}}{℃}$$

IREF

$$\frac{\mathbf{1000.5nA - 973.3nA}}{\mathbf{10}℃} = \frac{\mathbf{2.72nA}}{℃}$$

Resistor Value (Ohm) and TCR1

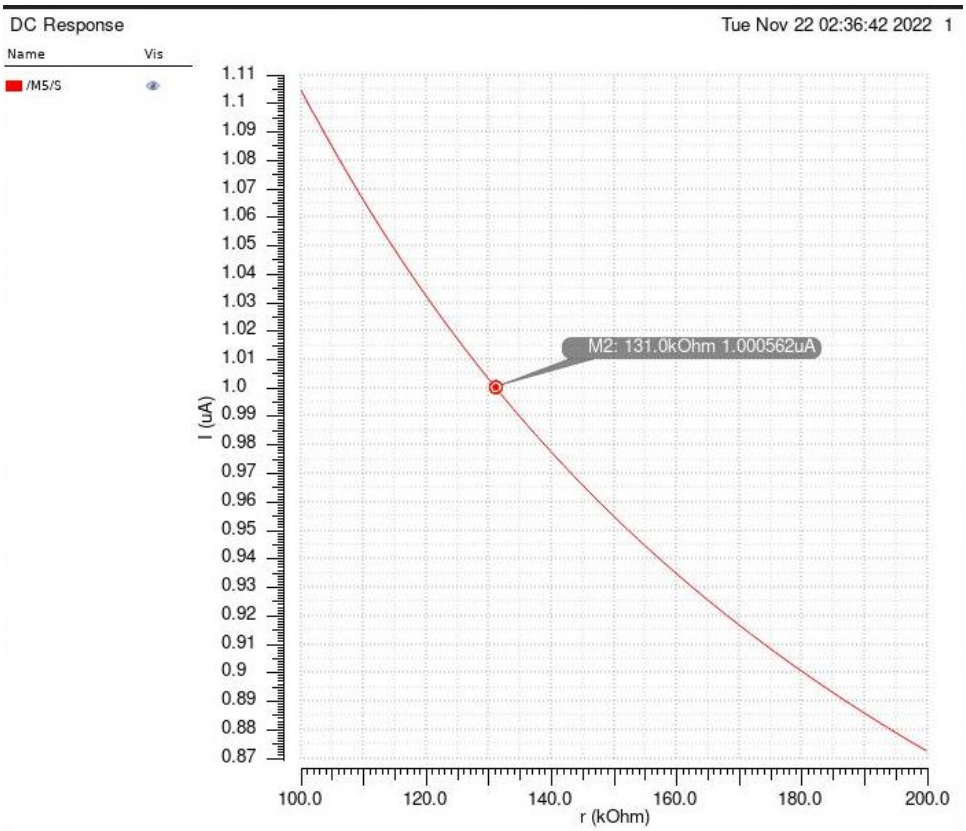

Figure 20: Resistor Value chose for 1uA IREF

For the simulations we used 0.002 for TCR1 (Temperature Coefficient for the Resistor) as per the project clarifications.

Startup Delay

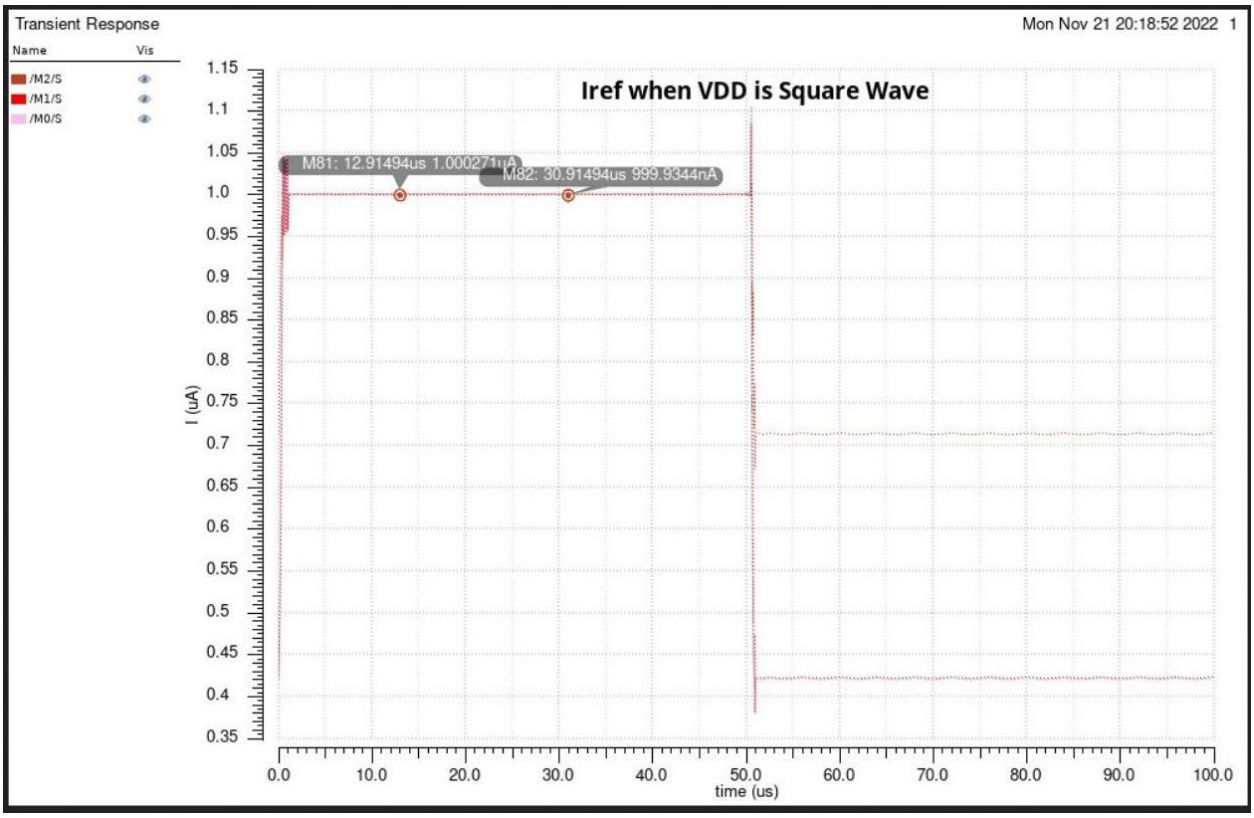

Figure 21: Iref under Square Wave

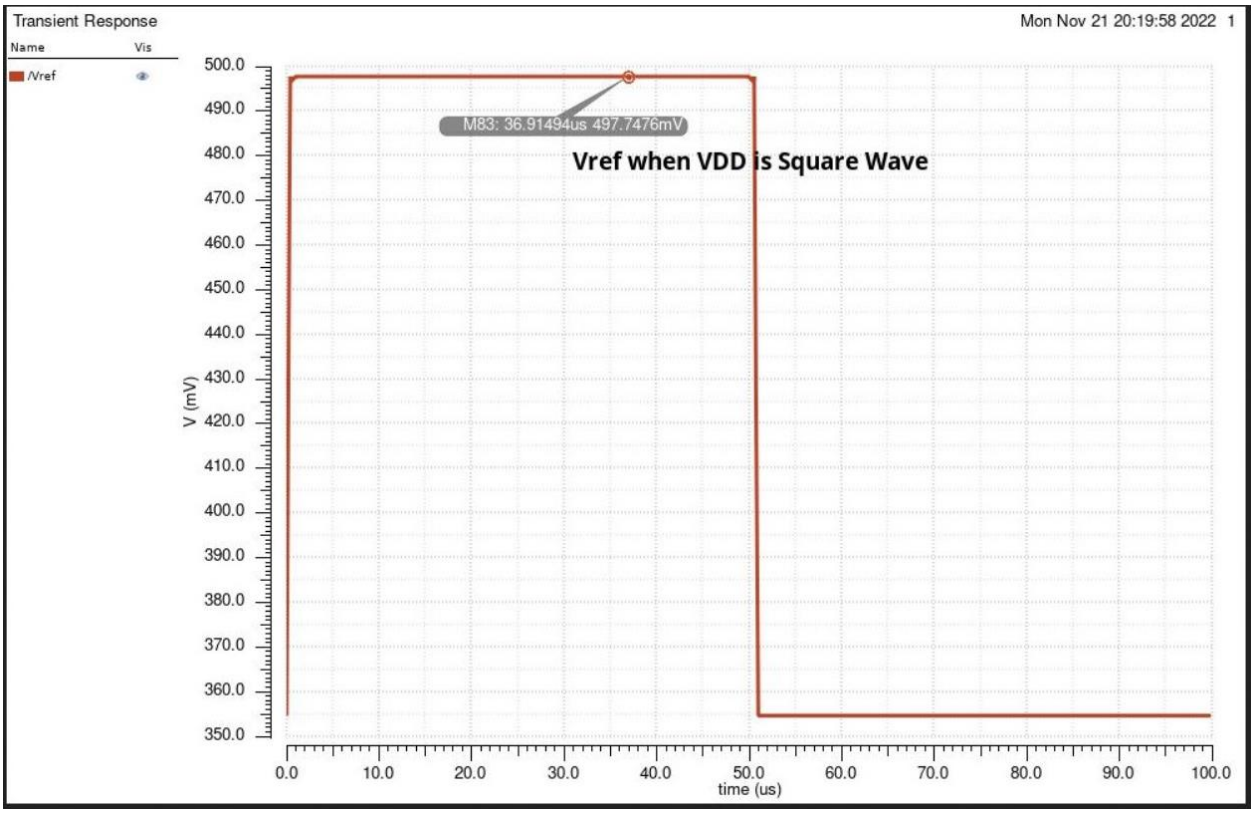

Figure 22: Vref under Square Wave

Comments

Particular Challenges?

- Becoming familiar with BGR technology
- Refreshing on BJT knowledge
- Startup circuit in project doc did not work, needed to find alternate circuit from work
- Getting reference circuit to output correct Vref and Iref
- Making schematic for bias circuit
- Sweeps for model parameters, global variables, and other new Cadence tricks

Other Possible Improvements?

- Voltage dividers in the BGR core for lower-voltage amplifiers

Part 2: Designing Bias Circuit

Biasing Circuit Schematic

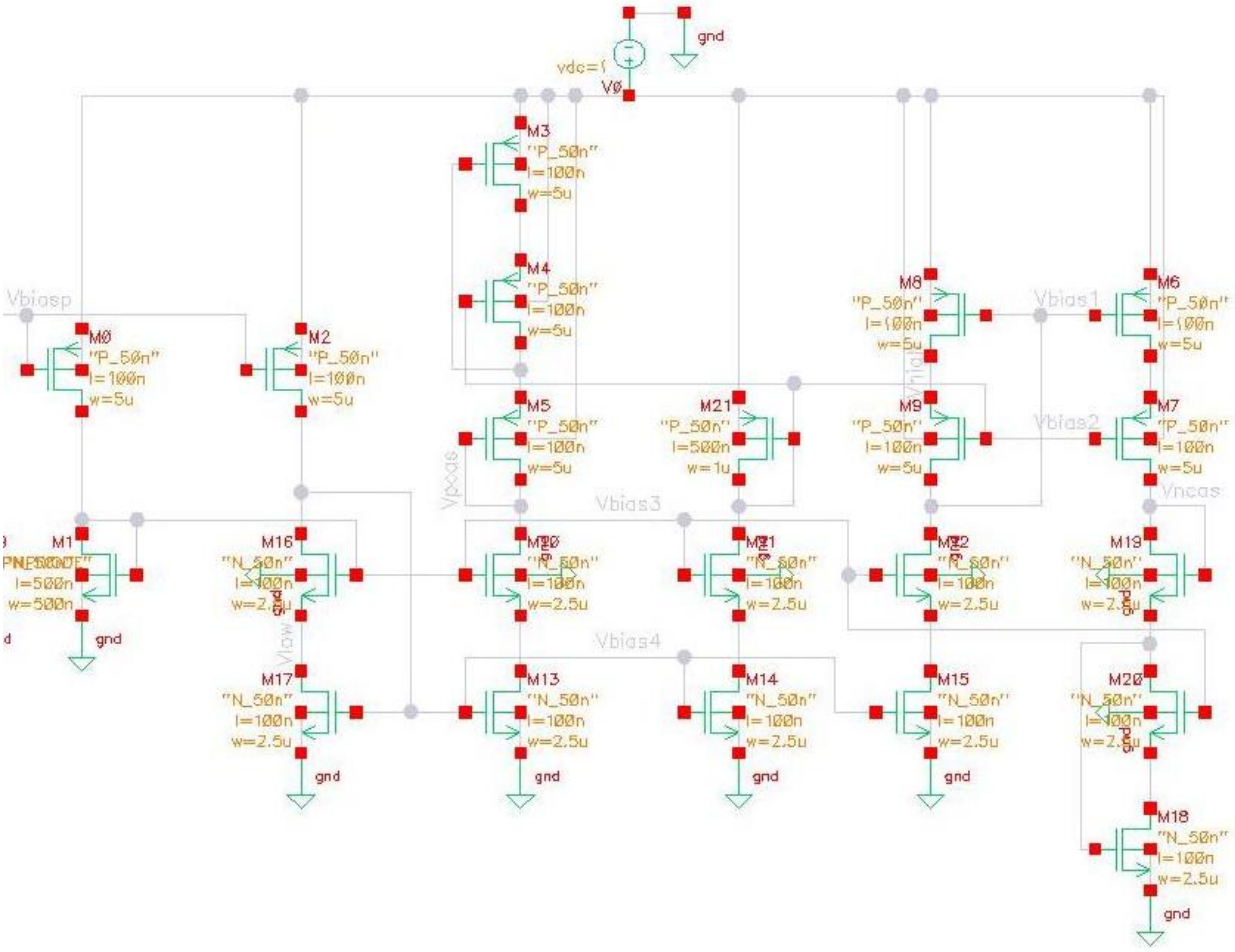

Figure 23: Biasing Circuit Schematic

BGR with Biasing Circuit Schematic

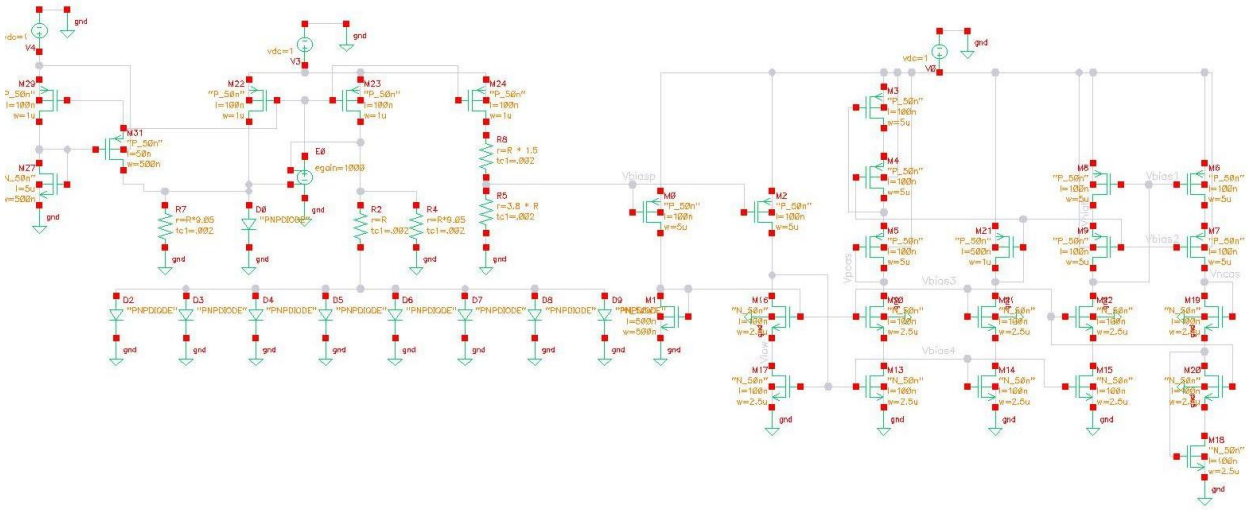

Figure 24: BGR with Biasing Circuit Schematic

Hand Analysis in Finding Expected Values

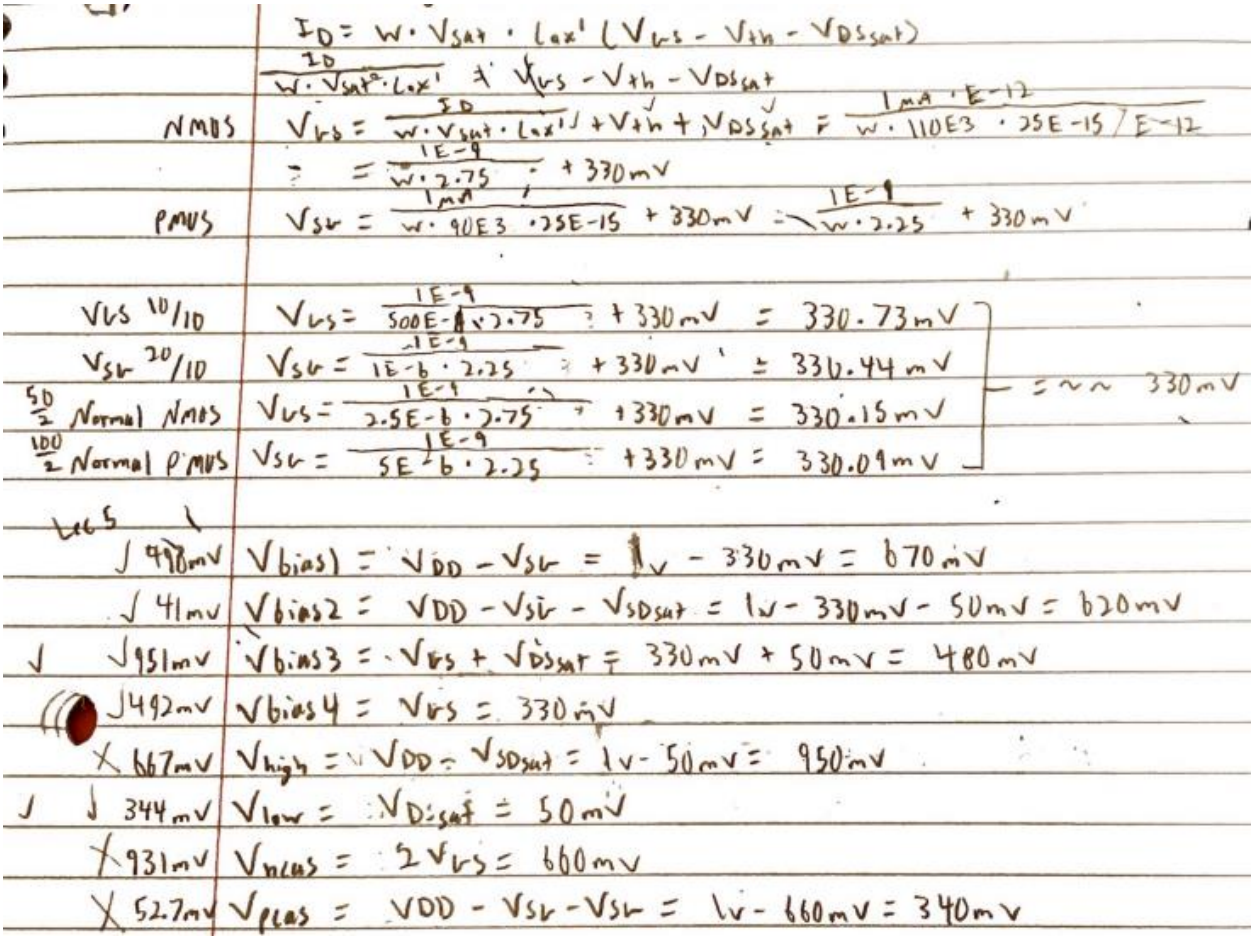

Figure 25: Hand Calculations of BGR Bias Circuit

Values in Simulation for All Biasing Voltages

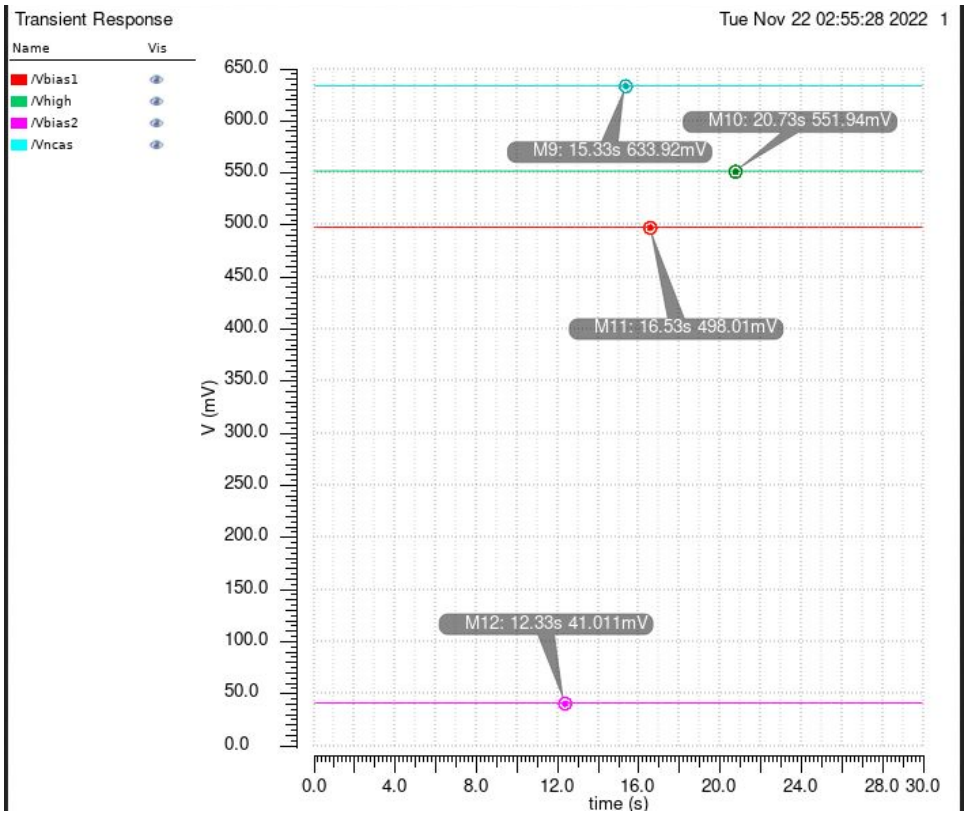

Figure 26: VBias1, VBias2, Vhigh, and Vncas

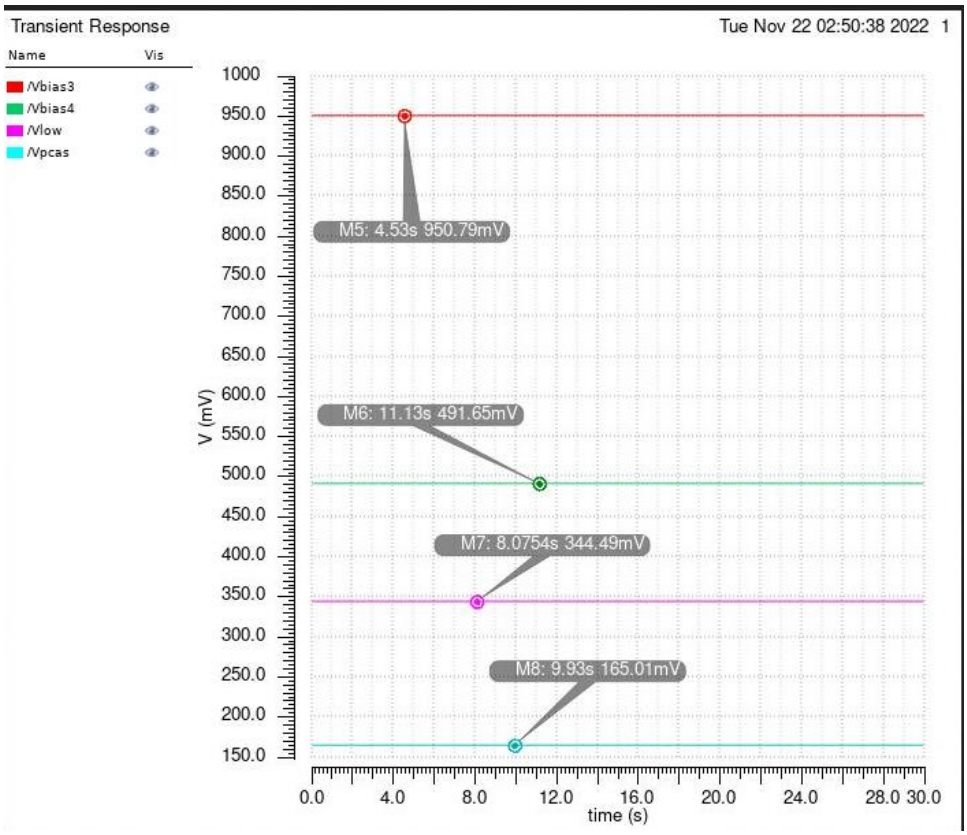

Figure 27: VBias3 VBias4, Vlow, and Vpcas

Supply Voltage Sweep for All Biasing Voltages

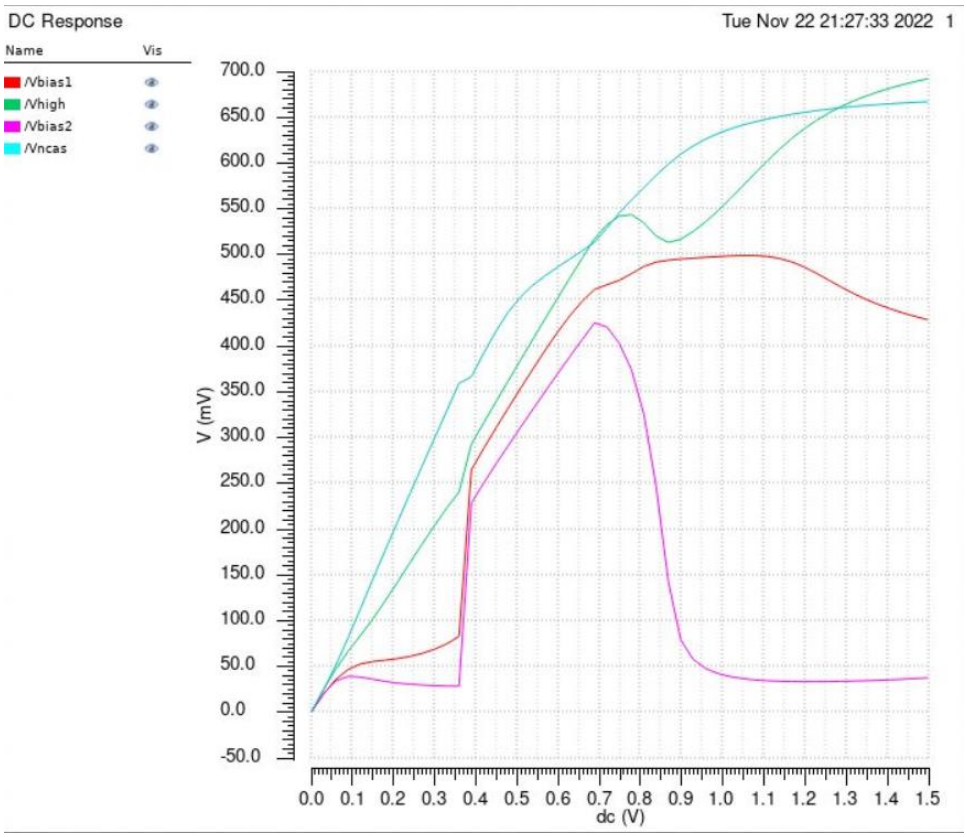

Figure 28: VBias1, VBias2, Vhigh, and Vncas with respect to VDD

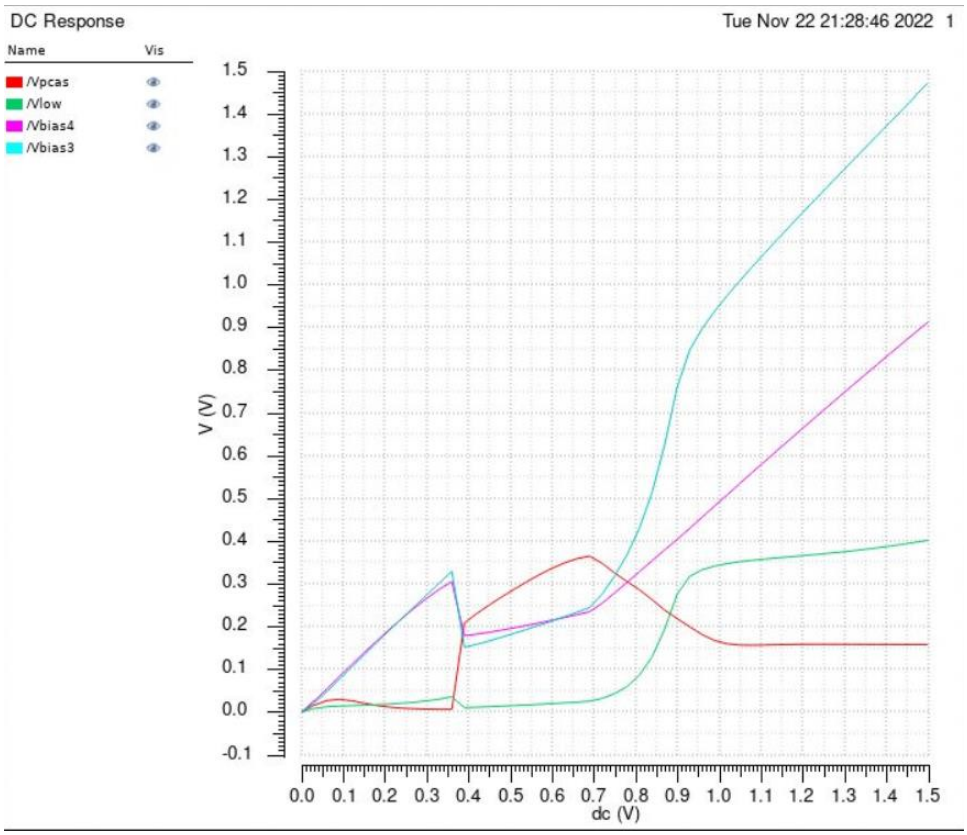

Figure 29: VBias3, VBias4, Vlow, and Vpcas with respect to VDD

Temperature Sweep from 0*C to 80*C for All Biasing Voltages

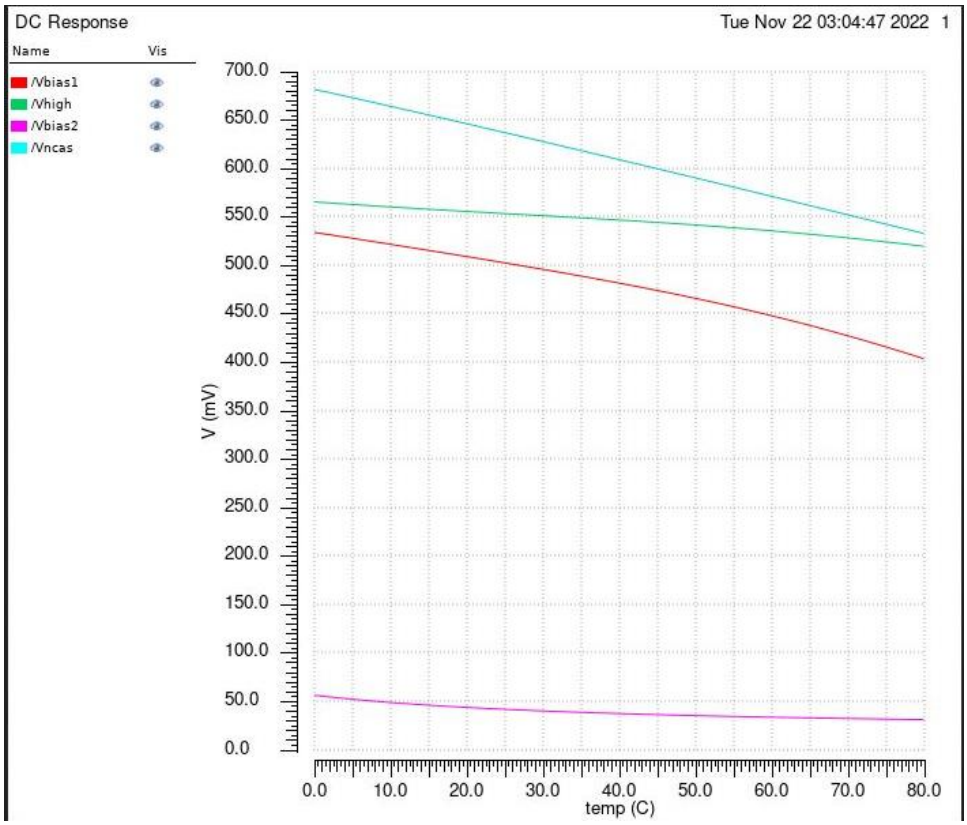

Figure 30: VBias1, VBias2, Vhigh, and Vncas with Respect to Temperature

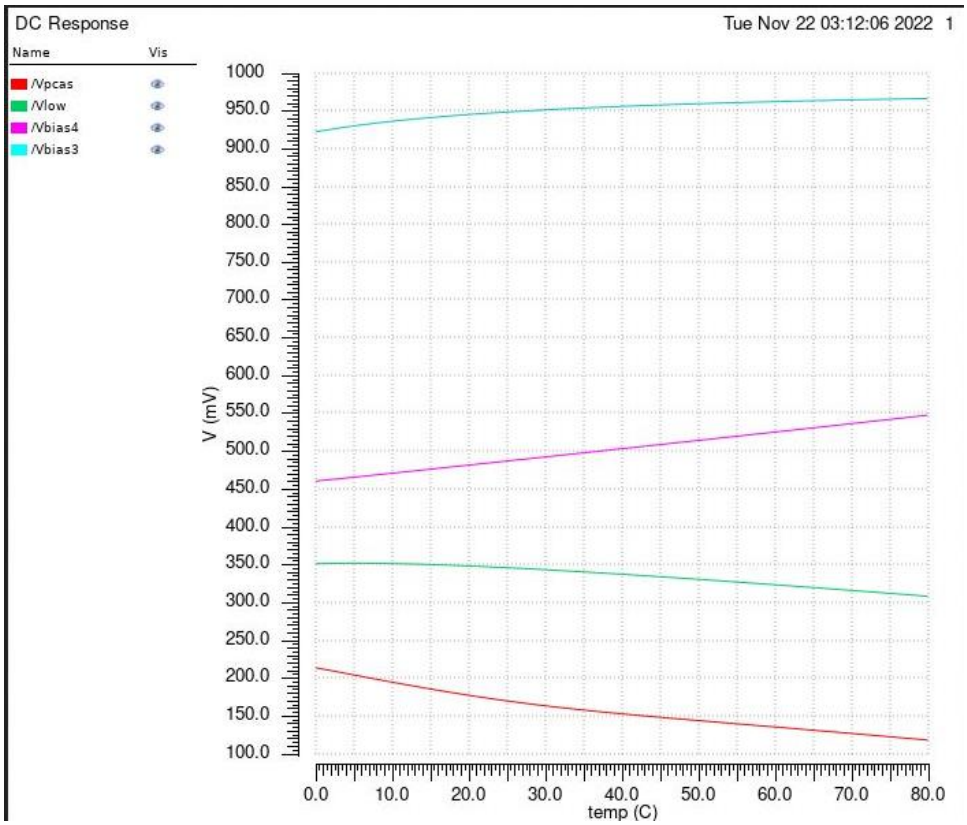

Figure 31: VBias3, VBias4, Vlow, and Vpcas with Respect to Temperature