

ECE 490X CMOS Fundamentals – Project Report

Worcester Polytechnic Institute

A-Term 2022

Ring Oscillator and Tapered Output Buffer

Submitted by

Drew Solomon &

Jonathan Lopez

Professor Guler

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Part 1: Ring Oscillator

Single Inverter

$$\begin{aligned} T &= t_{PLH} + t_{PHL} \quad \frac{1}{f} = \frac{1}{75\text{MHz}} = 13.33\text{ns} \\ &\quad /2 = 6.665\text{E-9} \\ &\quad 13.33\text{ns} \pm 10\% = 11.997 - 14.663\text{ns} \\ &\quad \text{each} \\ &\quad 83.33\text{MHz} - 68.21\text{MHz} \end{aligned}$$

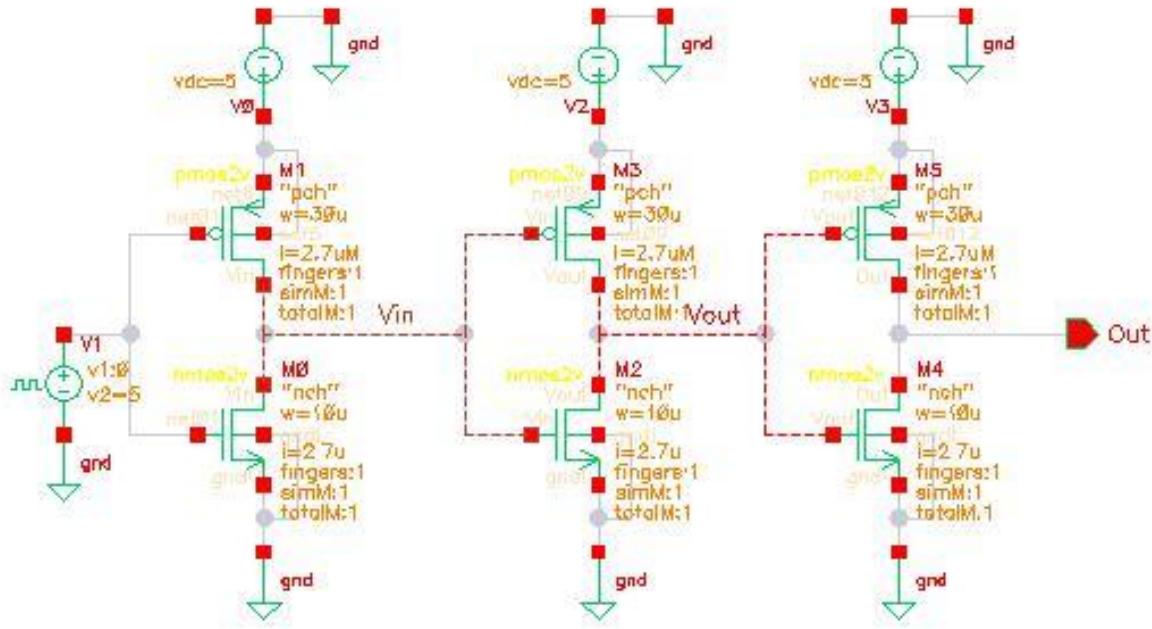
The first calculation made in creating the ring oscillator was to find the period which corresponds to the target frequency of 75MHz. This period was found to be 13.33ns. The margin of error of +/- 10% gave an acceptable range of 11.997ns - 14.663ns for our actual outcome.

$$\begin{aligned} \text{NMOS} & \quad t_{PHL} = 1.75 \cdot (15K \frac{L_n}{W_n}) \cdot (1.75 \text{fF}/\mu\text{m}^2 (W_n L_n + W_p L_p)) = 183.75\text{ps} \\ \text{PMOS} & \quad t_{PLH} = 1.75 \cdot (45K \frac{L_p}{W_p}) \cdot (1.75 \text{fF}/\mu\text{m}^2 (W_n L_n + W_p L_p)) = 183.75\text{ps} \quad] + = 367.5\text{E-11s} \\ \text{N} & \quad t_{PUL} = 73.5\text{ps} \\ \text{P} & \quad t_{PLH} = 73.5\text{ps} \quad] 1.47\text{ns} \\ \text{NMOS} & \quad t_{PLH} = 1.34\text{ns} \quad n = 13.33\text{ns}/2.68\text{ns} = 5 \text{ stages} \\ \text{PMOS} & \quad t_{PUL} = 1.34\text{ns} \quad] 2.68\text{ns} \end{aligned}$$

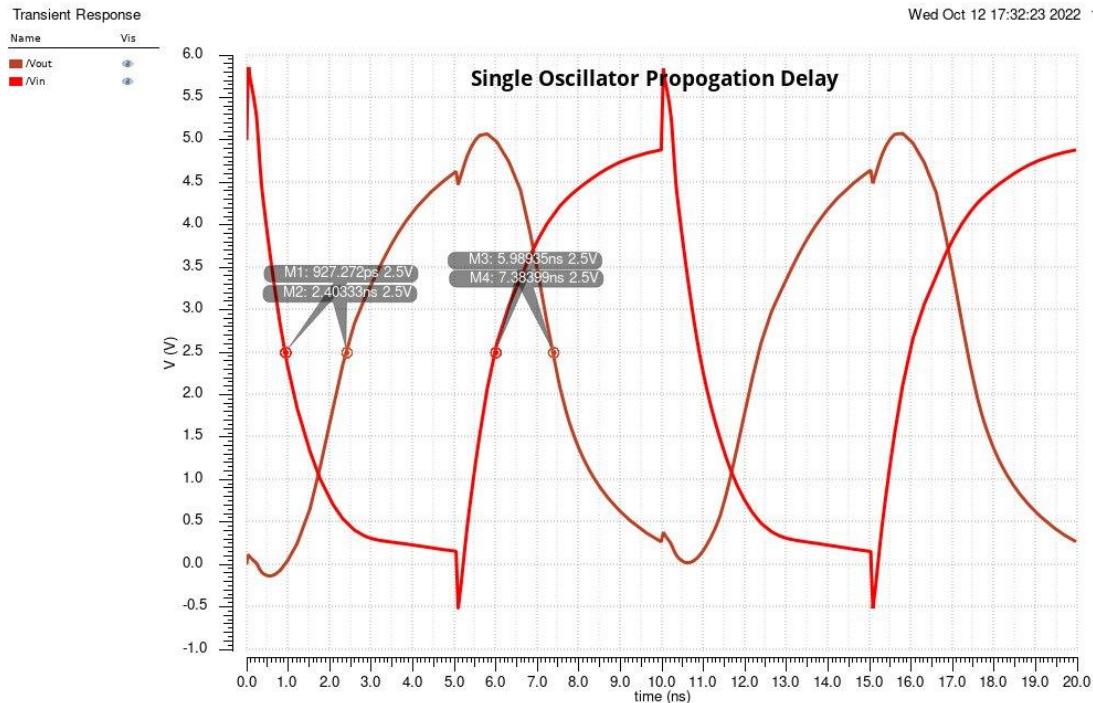
After experimenting with some different length values for the PMOS and NMOS used in each inverter stage (while keeping width constant), it was determined that using a length of 2.7μ would be suitable since it only required 5 stages to be used. The delay for PMOS or NMOS separately was 1.34ns and combined, 2.68ns.

$$n = \frac{1}{\sum (t_{PUL} + t_{PLH})}$$

The calculation for the number of stages needed used the above equation.



To test the propagation delay of a single inverter stage, 3 were connected together with the one being measured in the middle. This was necessary since the calculation used to obtain the propagation delay of a stage included capacitance values which encompass the output of the previous stage and the input of the subsequent stage. A voltage of 5v was used since the MOSFETs were made on a 1um scale.



The graph above shows the response of the output of a single stage (brown) compared to the input of that stage (red). The delays are as follows:

$$t_{PHL} = 7.38399\text{ns} - 5.98935\text{ns} = 1.39464\text{ns}$$

$$t_{PLH} = 2.40333\text{ns} - 927.272\text{ps} = 1.476058\text{ns}$$

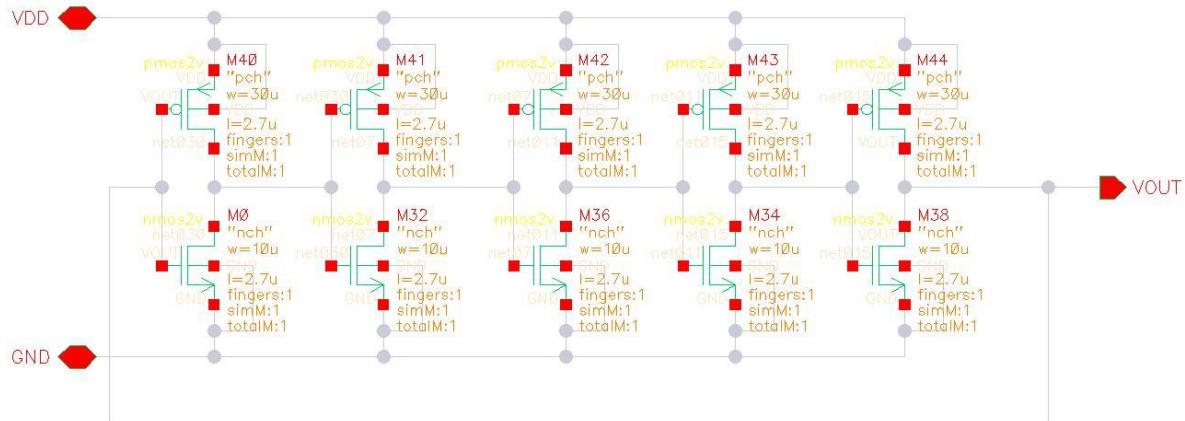
$$t_{PHL} + t_{PLH} = 2.8706089\text{ns}$$

These results are slightly higher than calculated but still within spec. If this inverter were to be used in a 5 stage ring oscillator, the results would be as follows:

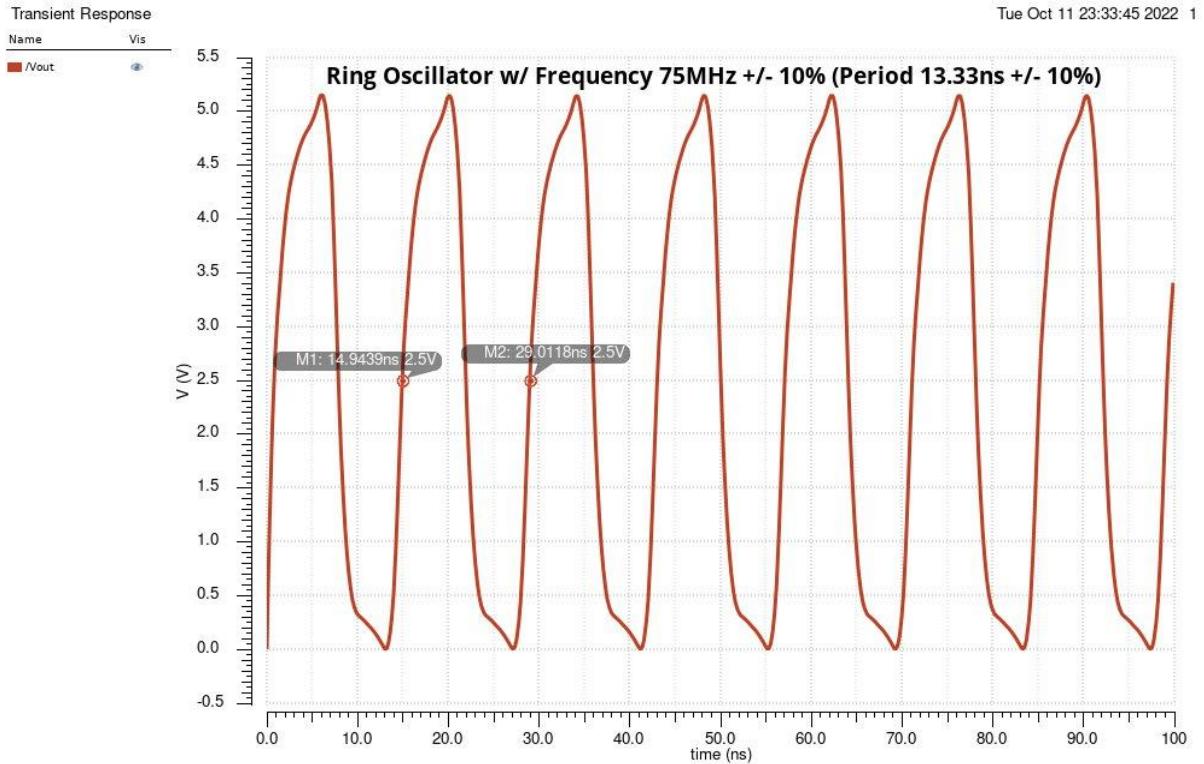
$$T_{osc} = 5 * (t_{PHL} + t_{PLH}) = 5 * 2.8706089\text{ns} = 14.35349\text{ns}$$

$$F_{osc} = 1/T_{osc} = 69.66946715\text{MHz}$$

Oscillator



A ring oscillator was then made using 5 of the inverter stages made in the previous step. VDD, GND, and VOUT pins were added in preparation for conversion to layout at this time.



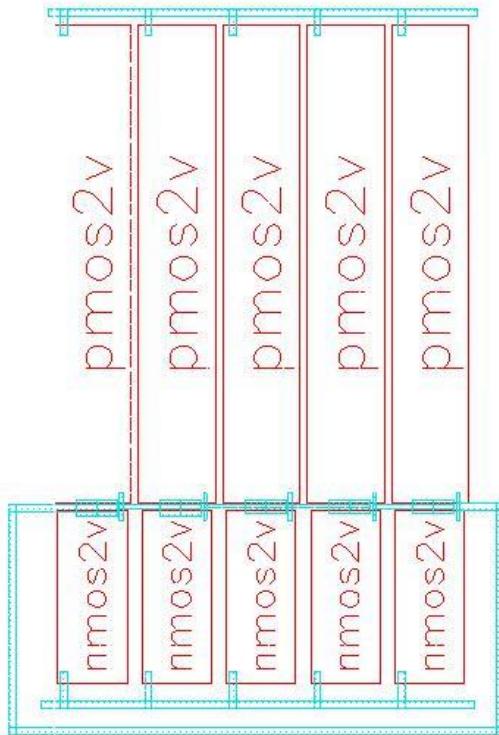
The graph above shows a transient simulation run on the oscillator, with the output of the oscillator displayed. The period of the oscillator is as follows:

$$T_{osc} = 29.0118\text{ns} - 14.9439\text{ns} = 14.0679\text{ns}$$

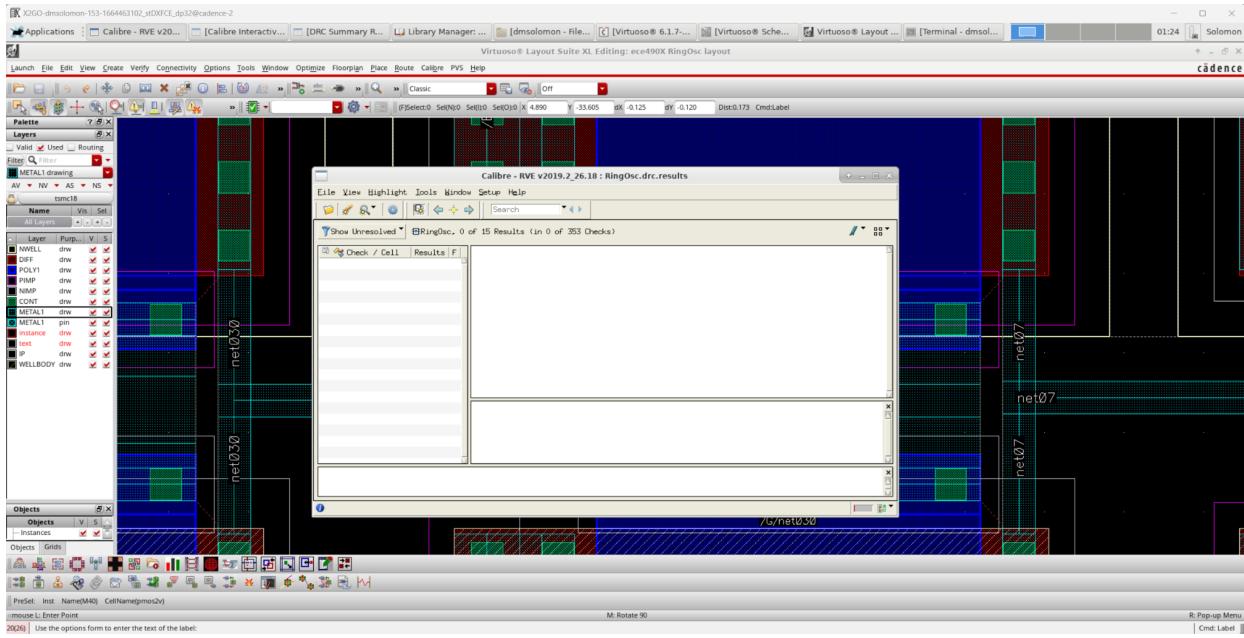
$$F_{osc} = 1/T_{osc} = 71.08381493\text{MHz}$$

This performance is closer to the target of 75MHz than the single inverter stage suggested, only off by 5.3%.

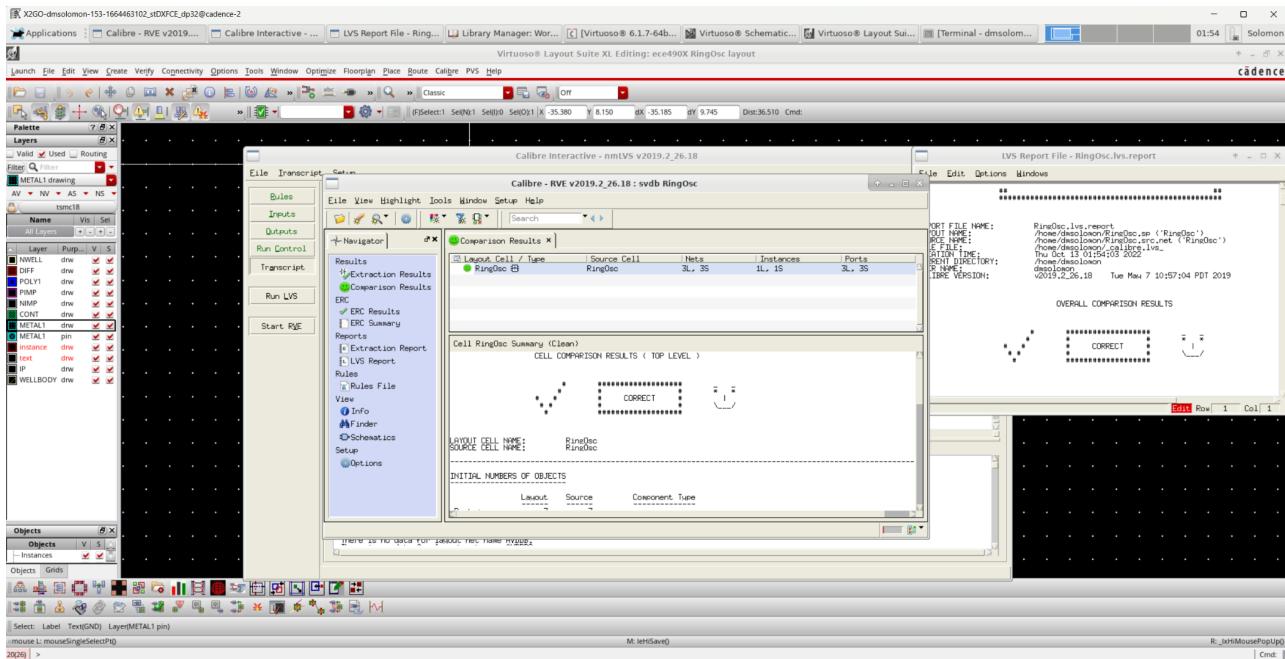
Layout



After generating the components used in layout form and connecting the terminals correctly using metal1 drawings, the above figure was achieved. For PMOS, the bulk was connected to VDD, and for the NMOS, the bulk was connected to ground. Although the labels are not visible, VDD is the top bus and GND the bottom, with the first and last stage connected by the long metal1 connecting from the right back to the left.



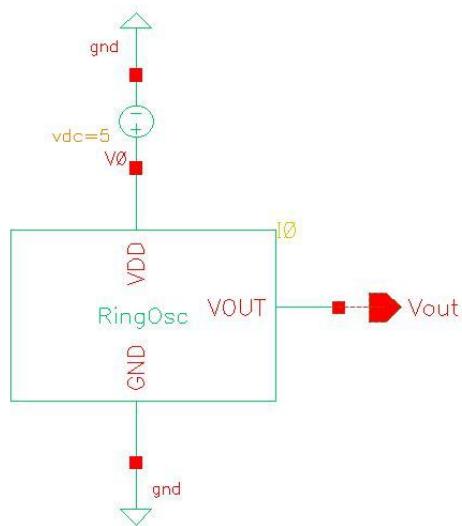
The layout passed DRC as seen in the screenshot above.



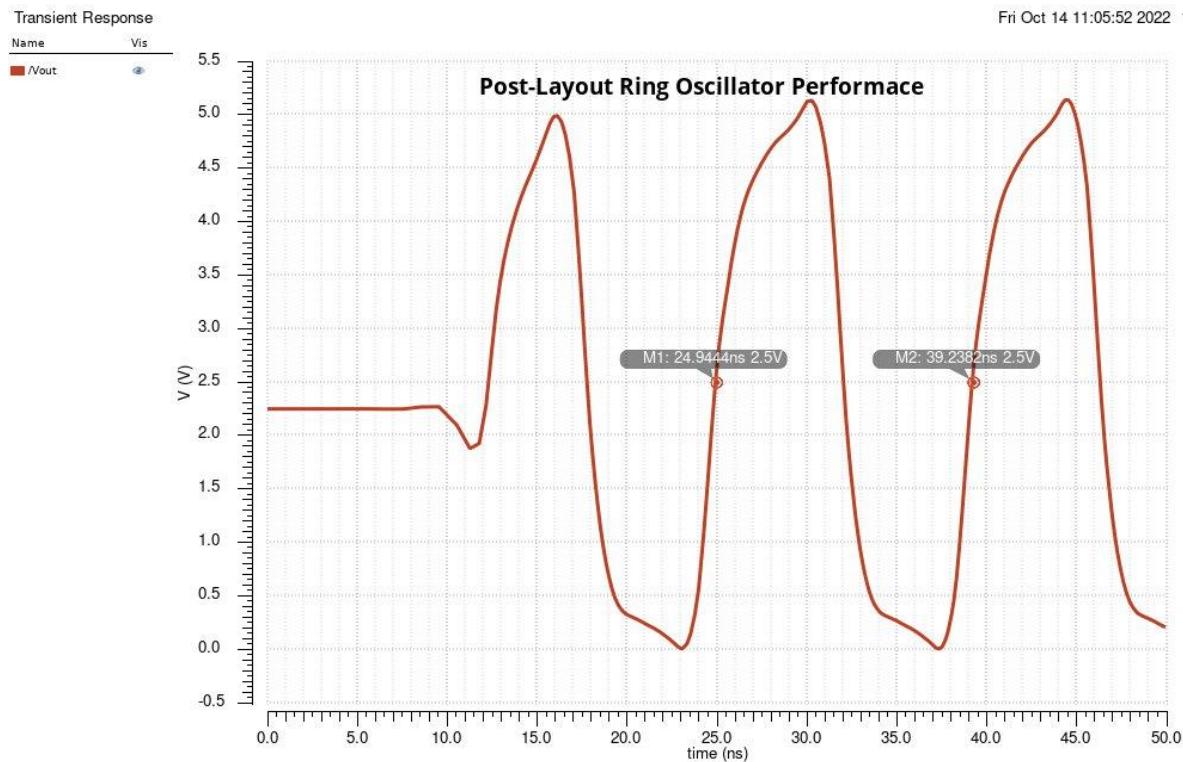
The layout passed LVS as seen in the screenshot above.

Post-Layout Performance

Since the layout passed DRC and LVS, it was deemed ready for parasitic extraction. A calibre file was generated for the oscillator, and this file would then be used to run a post-layout simulation.



Before running the post-layout simulation, a symbol for the oscillator was generated from the schematic. The full circuit used in the post-layout simulation is shown above.



The graph above shows the post-layout performance of the ring oscillator, with V_{out} being displayed. The performance is as follows:

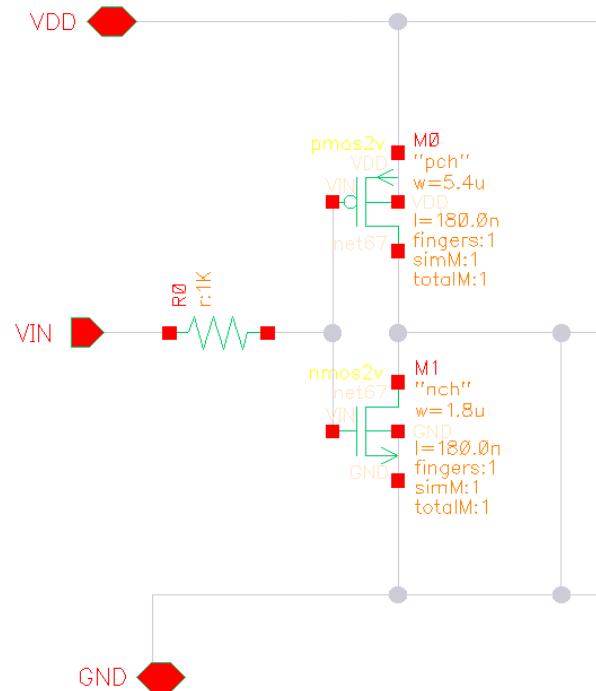
$$T_{osc} = 39.2382\text{ns} - 24.9444\text{ns} = 14.2938\text{ns}$$

$$F_{osc} = 1/T_{osc} = 69.96040241\text{MHz}$$

This result is 6.8% off of the target value, which is within the 10% acceptance range.

Part 2: Tapered Buffer

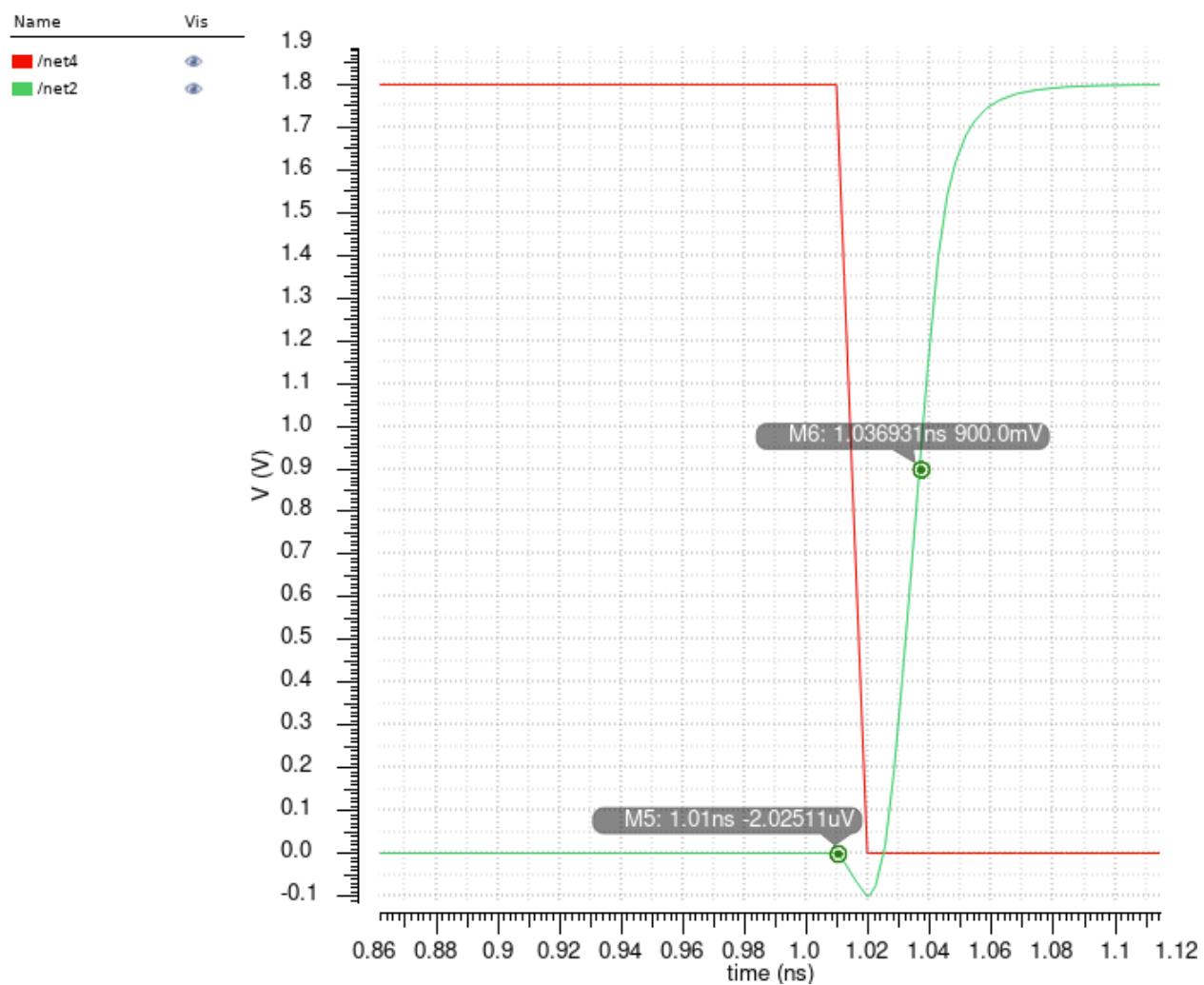
Single Buffer



In order to get the input capacitance, C_{in} , we set up an RC circuit with the first stage of the inverter acting as C. We'll find the delay and solve for C using $T_d = 0.7 \cdot R \cdot C$. Those calculations and the calculation of the stages (N) and the width scale factor (A) are below. The time we are measuring is the 0-50% final value.

Transient Response

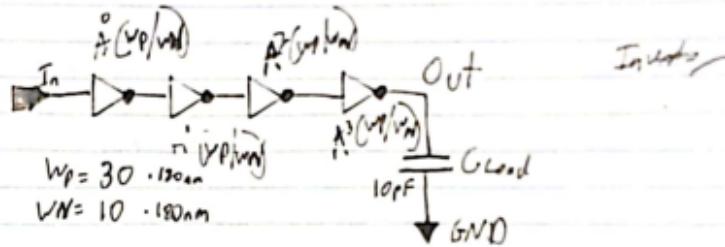
Tue Oct 11 00:53:40 2022 1



Tapered Output Buffer

$C_{Load} = 10 \text{ pF}$ Start $N^{39/10}$
 PMOS/NMOS $30/1$ $10/1$ -

Input = 75 MHz Square Wave $t_d < 2.5 \text{ ns!}$ 10^{-9} s



$$C_{in1}^2 = A_1 \cdot C_{in1}$$

$$C_{in3} = A_3 \cdot C_{in2} = A^2 \cdot C_{in1}$$

Switching Resistance

$$R_n p_1 = \frac{R_n p_1}{A} \quad R_n p_3 = \frac{R_n p_1^2}{A} = \frac{R_n p_1}{A^2}$$

$$\pi = \left[\frac{C_{load}}{C_{in1}} \right]^{1/N} \quad N = \ln \frac{C_{load}}{C_{in1}}$$

We need to start with C_{in1} ,

start with RC Inverter Circuit

$$T_d = 0.7 R C$$

$$C = \frac{T_d}{0.7 R}$$

Solve for C

$$C = \frac{T_d}{0.7(1000)}$$

$$R = 1 \text{ k}\Omega$$

From Graph 50% time

$$1.036931 \text{ ns} - 1.01 \text{ ns}$$

$$0.026931$$

$$C = \frac{0.0^{\text{-9}}}{0.7(1000\text{m}^2)}$$

$$C = 3.84729 \times 10^{-14} \times 10^{-1} \quad 38.4729$$

$$C_m = 38.4729 \text{ aF} \leftarrow$$

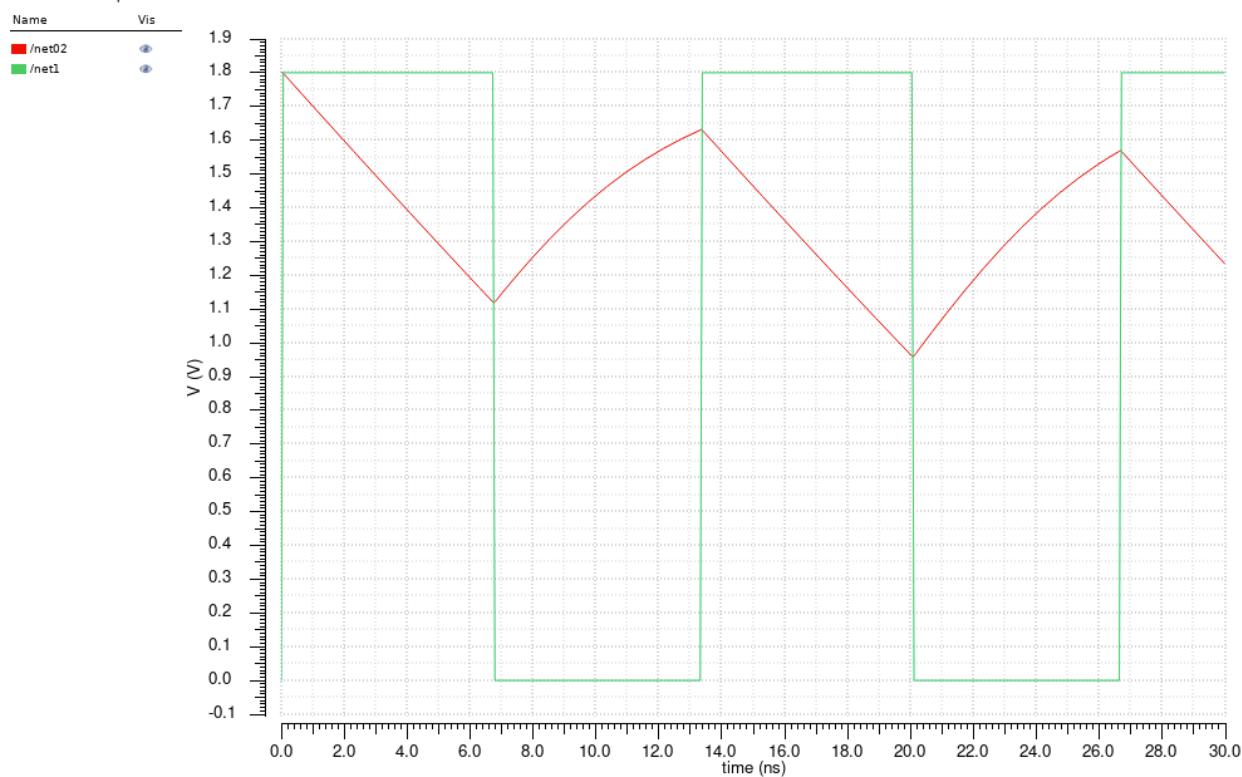
$$N = \left(\frac{10 \times 10^{-12}}{38.4729 \times 10^{-15}} \right)$$

$$N = 5.56039 \quad 5 \text{ stages}$$

$$A = \left[\frac{10 \times 10^{-12}}{38.4729 \times 10^{-15}} \right]^{1/5.56039}$$

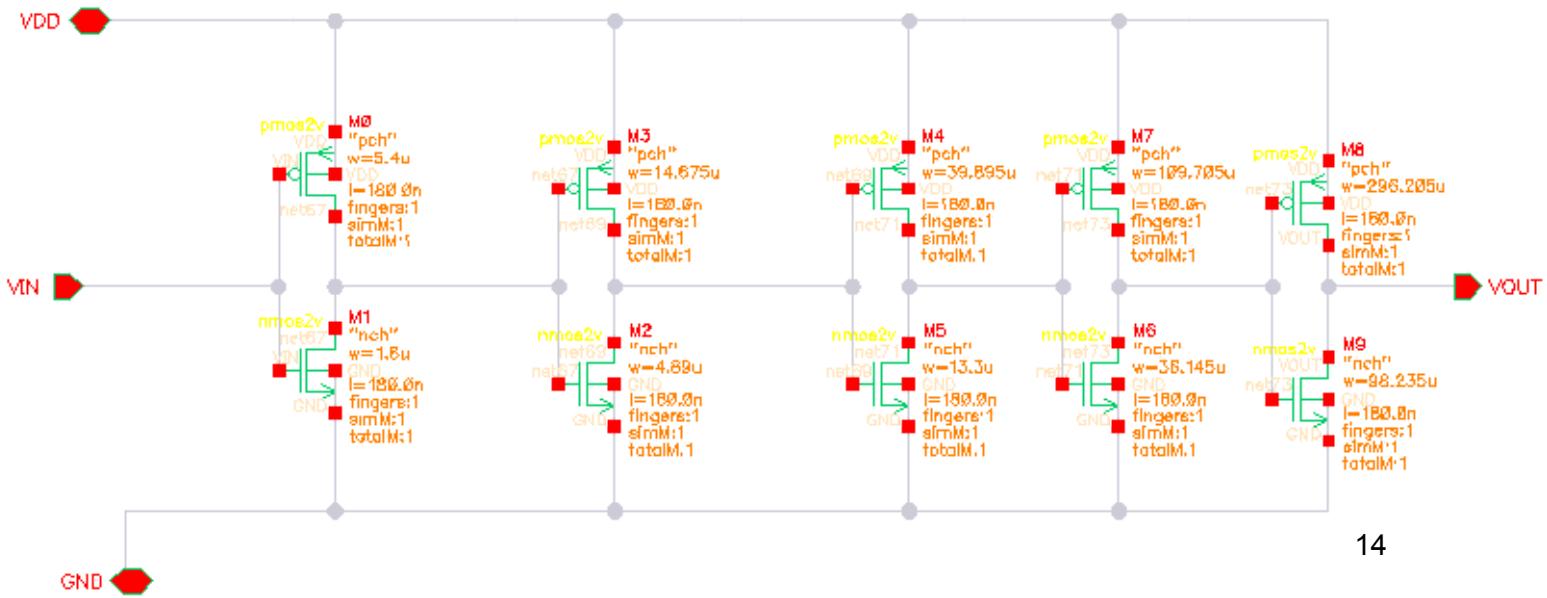
$$A = 27.78 = C \cancel{253}$$

Once A and N were found the construction of the buffer began but first we hooked up the 10pF load capacitance to only the first inverter and checked on the output. This is shown because if you only had 1 inverter it could not drive the load.

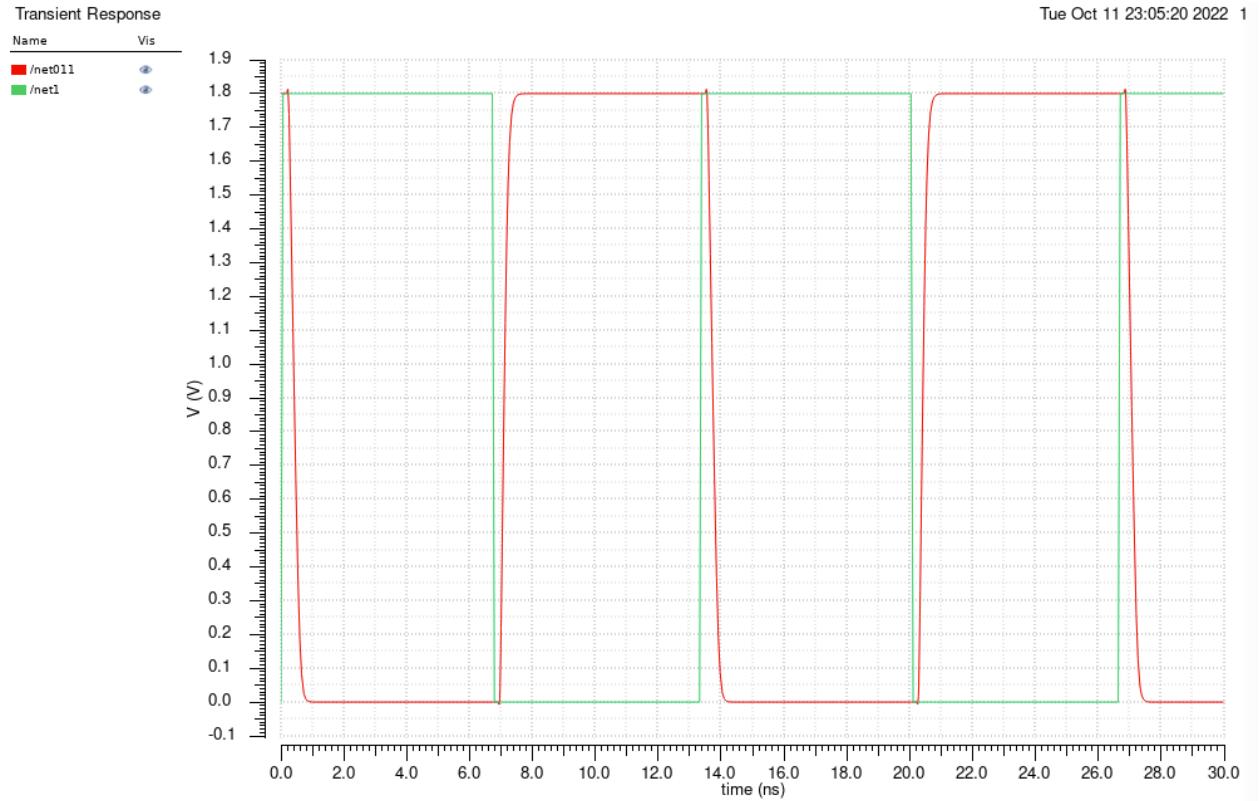


Building the Buffer

As you can see it can not drive the output. With 180nm tech, L and W are quite small. This is problematic when it comes to high current draws. These caps are typically pads used to bring a signal off-chip. Voltage can change very quickly hence the need for large current draws. In order to get this desired output, the tapered buffer is used with more than 1 stage. Width, W, is multiplied by a scale, A, which was found earlier.

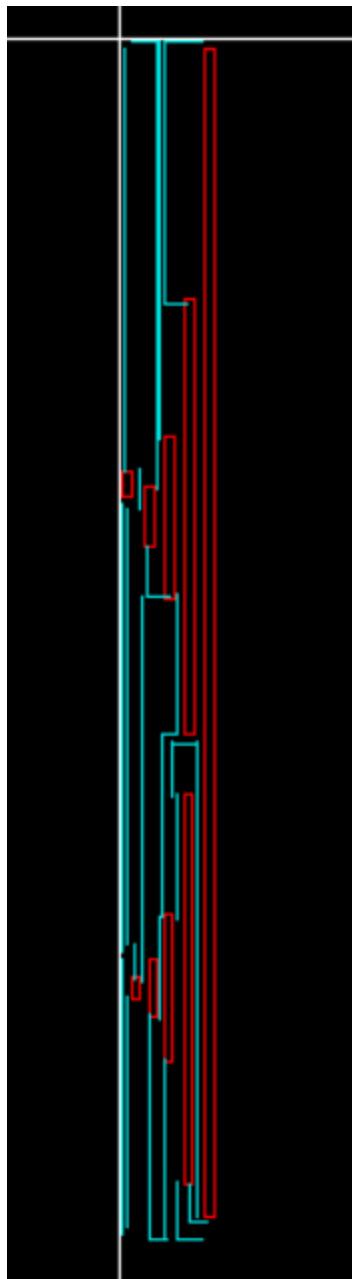


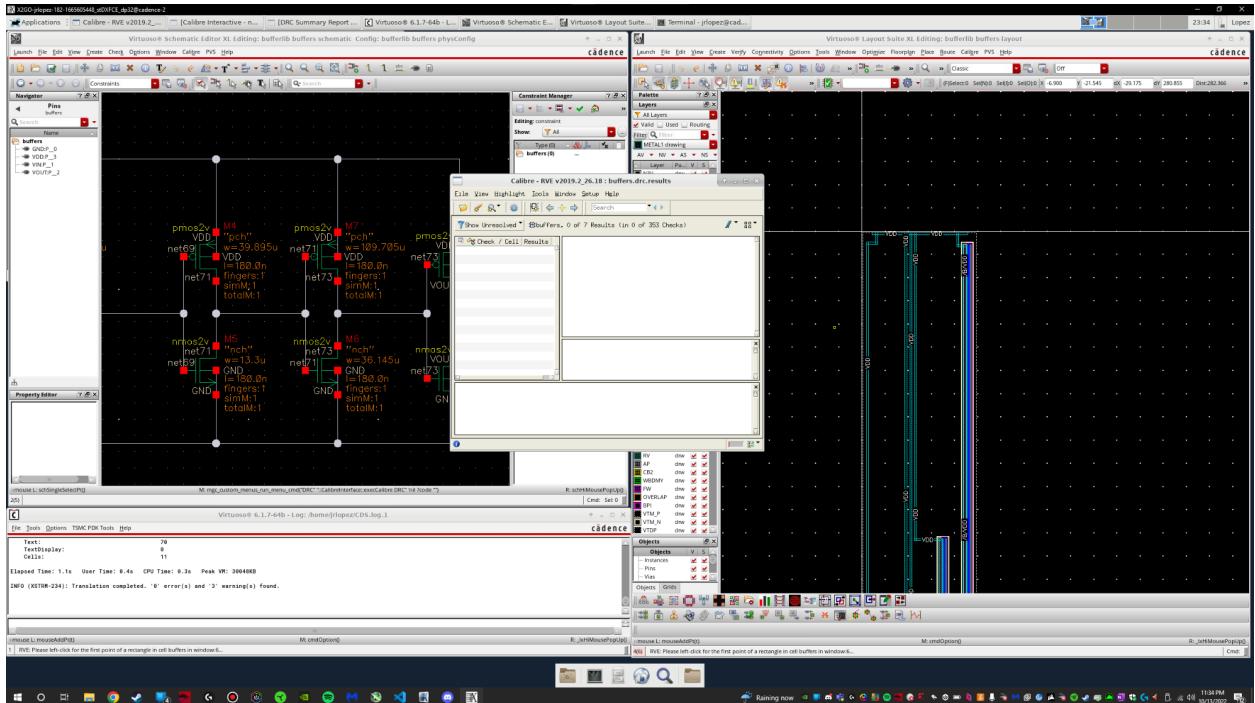
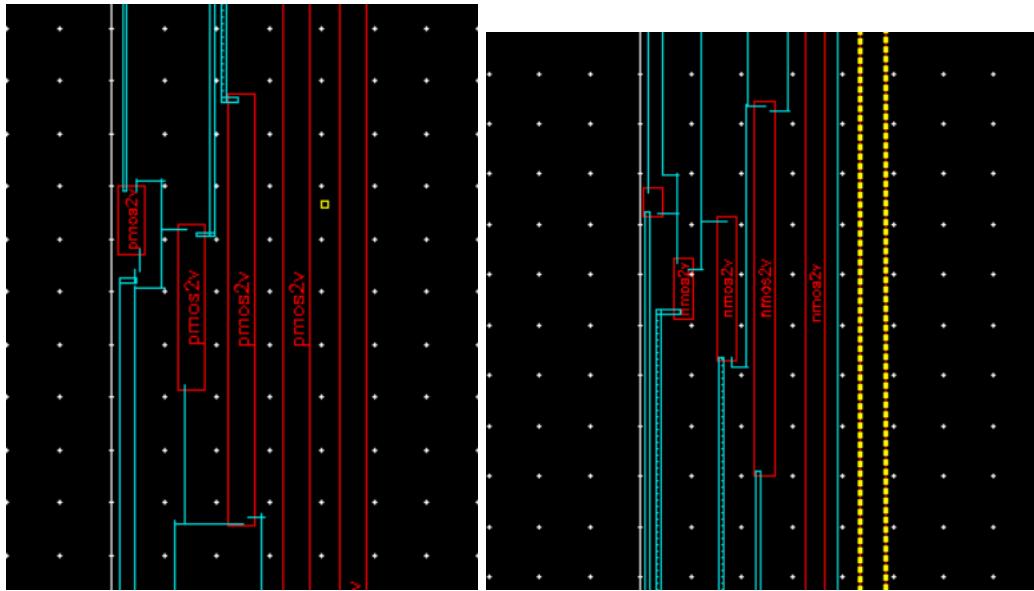
The tapered output buffer is produced with 5 stages and each width is multiplied by a scale factor of A which was about 2.718. After the buffer was built we hooked up the 10pF load capacitance again and checked the output.



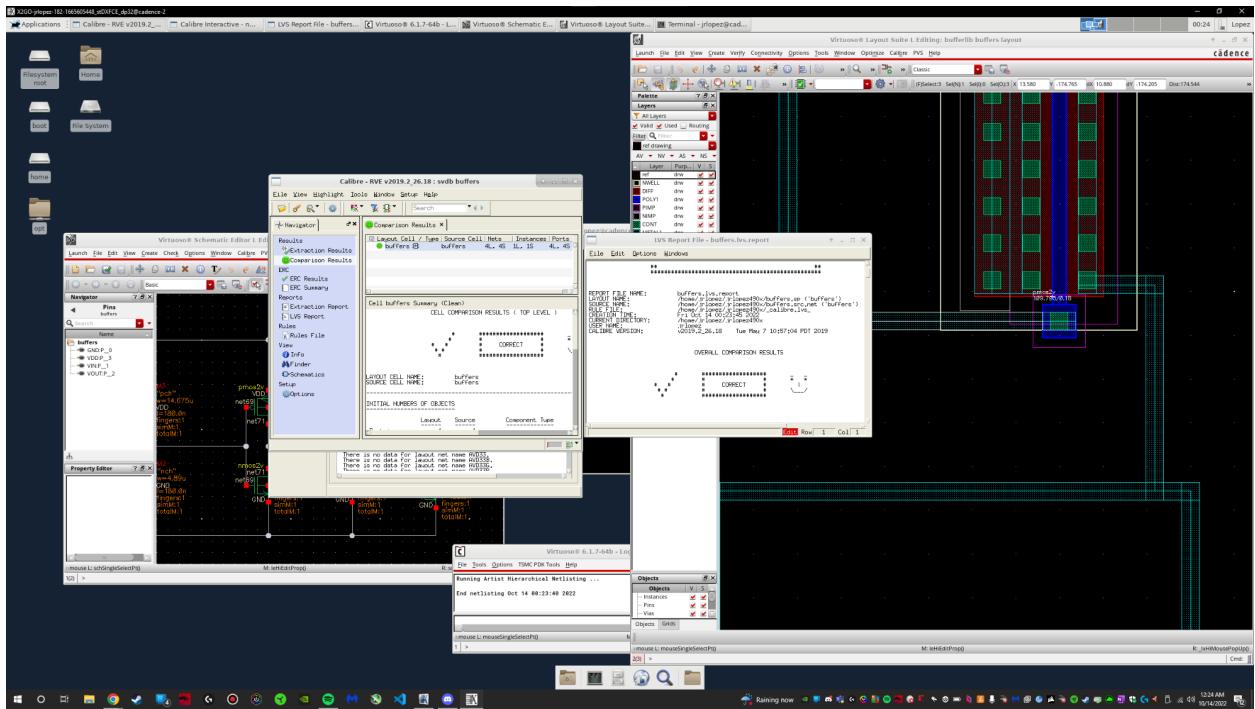
The buffer can now supply the current to the load capacitance with the increased width stages.

Layout





The layout passed DRC with only the only errors being the density of Metal 1-5 staying since we don't use any of them here in this schematic.



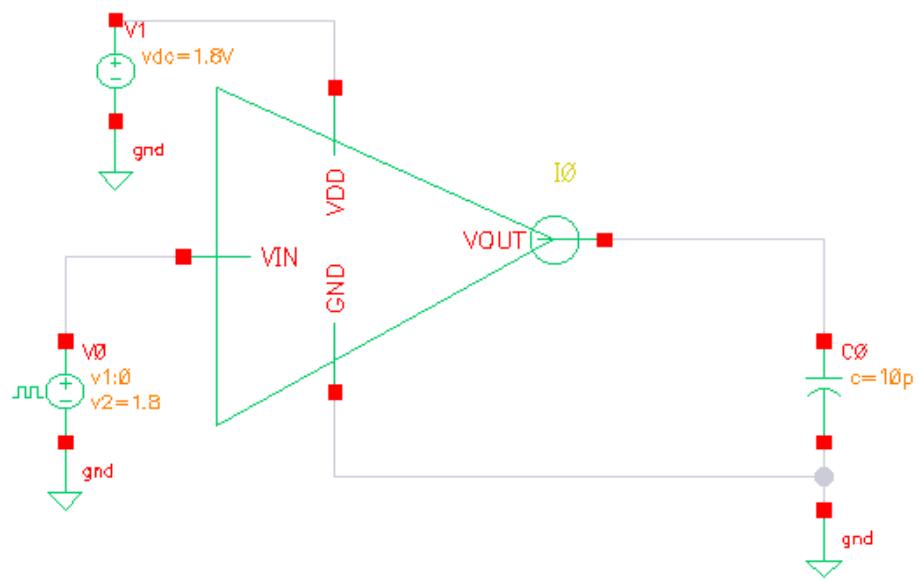
The layout also passed LVS after putting in labels for the pins



As for Parasitic Extraction, it generated a calibre file with no warnings or errors.

Post-Layout Performance

Since it passed DRC, LVS, and PEX, it was time to run a post-layout simulation. A symbol was created for ease of use.



As for the delay of the buffer, it was still within the 2.5ns design parameter.

X2GO-jlopez-182-1665605448_stDXFCE_dp32@cadence-2

Applications [Calibre Interactive - ...] [Library Manager: Wo... [Virtuoso® 6.1.7-64b ...] [Vir...

/home/jlopez/simulation/bufferTB/spectre/schematic/netlist/input.scs

File Edit View Help

```

MM2 (NET69 NET67 GND GND) nch 1=1.8e-07 w=4.89e-06 m=1 nf=1 sd=540.0n \
ad=2.3472e-12 as=2.6406e-12 pd=1.074e-05 ps=1.086e-05 \
nrd=0.0981595 nrs=0.110429 sa=1e-06 sb=4.8e-07 sca=0.133797 \
scb=1.3168e-18 scc=5.09979e-37

MM1 (NET67 VIN GND GND) nch 1=1.8e-07 w=1.8e-06 m=1 nf=1 sd=540.0n \
ad=8.64e-13 as=9.72e-13 pd=4.56e-06 ps=4.68e-06 nrd=0.266667 \
nrs=0.3 sa=1e-06 sb=4.8e-07 sca=0.715662 scb=4.13575e-06 \
scc=1.69345e-11

MM8 (VOUT NET73 VDD VDD) pch 1=1.8e-07 w=0.000296205 m=1 nf=1 \
sd=540.0n ad=1.42178e-10 as=1.59951e-10 pd=0.00059337 \
ps=0.00059349 nrd=0.0016205 nrs=0.00182306 sa=1e-06 sb=4.8e-07 \
sca=1.45819 scb=5.57365e-05 scc=3.30517e-08

MM7 (NET73 NET71 VDD VDD) pch 1=1.8e-07 w=0.000109705 m=1 nf=1 \
sd=540.0n ad=5.26584e-11 as=5.92407e-11 pd=0.00022037 \
ps=0.00022049 nrd=0.00437537 nrs=0.00492229 sa=1e-06 sb=4.8e-07 \
sca=1.48475 scb=6.39912e-05 scc=8.37705e-08

MM4 (NET71 NET69 VDD VDD) pch 1=1.8e-07 w=3.9895e-05 m=1 nf=1 \
sd=540.0n ad=1.91496e-11 as=2.15433e-11 pd=8.075e-05 ps=8.087e-05 \
nrd=0.0120316 nrs=0.0135355 sa=1e-06 sb=4.8e-07 sca=1.55786 \
scb=8.69322e-05 scc=2.24726e-07

MM3 (NET69 NET67 VDD VDD) pch 1=1.8e-07 w=1.4675e-05 m=1 nf=1 \
sd=540.0n ad=7.044e-12 as=7.9245e-12 pd=3.031e-05 ps=3.043e-05 \
nrd=0.0327087 nrs=0.0367973 sa=4.8e-07 sb=1e-06 sca=1.75044 \
scb=0.000148889 scc=6.05493e-07

MM0 (NET67 VIN VDD VDD) pch 1=1.8e-07 w=5.4e-06 m=1 nf=1 sd=540.0n \
ad=2.592e-12 as=2.916e-12 pd=1.176e-05 ps=1.188e-05 nrd=0.0888889 \
nrs=0.1 sa=1e-06 sb=4.8e-07 sca=2.24031 scb=0.000317227 \
scc=1.63971e-06

cc_17 (VDD VOUT) capacitor c=1.7975e-14
cc_16 (GND VOUT) capacitor c=5.95792e-15
cc_15 (NET73 VOUT) capacitor c=7.38565e-15
cc_14 (NET73 VDD) capacitor c=1.28682e-14
cc_13 (NET73 GND) capacitor c=4.31433e-15
cc_12 (NET71 VDD) capacitor c=4.77937e-15
cc_11 (NET71 GND) capacitor c=2.70988e-15
cc_10 (NET71 NET73) capacitor c=2.73721e-15
cc_9 (NET69 VDD) capacitor c=1.81204e-15
cc_8 (NET69 GND) capacitor c=6.67189e-16
cc_7 (NET69 NET71) capacitor c=9.9836e-16
cc_6 (NET67 VDD) capacitor c=6.6539e-16
cc_5 (NET67 GND) capacitor c=2.86466e-16
cc_4 (NET67 NET69) capacitor c=3.97829e-16
cc_3 (VIN VDD) capacitor c=1.13959e-16
cc_2 (VIN GND) capacitor c=9.38737e-17
cc_1 (VIN NET67) capacitor c=1.976e-16
c_42 (VOUT _net0) capacitor c=1.98978e-15
c_38 (VDD _net0) capacitor c=5.13524e-14
c_31 (GND _net0) capacitor c=2.93322e-14
c_24 (NET73 _net0) capacitor c=1.59417e-14
c_19 (NET71 _net0) capacitor c=9.87315e-15
c_14 (NET69 _net0) capacitor c=1.05241e-14
c_9 (NET67 _net0) capacitor c=1.22884e-14
c_4 (VIN _net0) capacitor c=1.04646e-14
ends buffers
// End of subcircuit definition.

// Library name: bufferlib
// Cell name: bufferTB

```

10 L1 C1

```

modelParameter: writing model parameter values to rawfile.
Opening the PSF file ../psf/modelParameter.info ...
element: writing instance parameter values to rawfile.
Opening the PSF file ../psf/element.info ...
outputParameter: writing output parameter values to rawfile.
Opening the PSF file ../psf/outputParameter.info ...
designParamValue: writing netlist parameters to rawfile

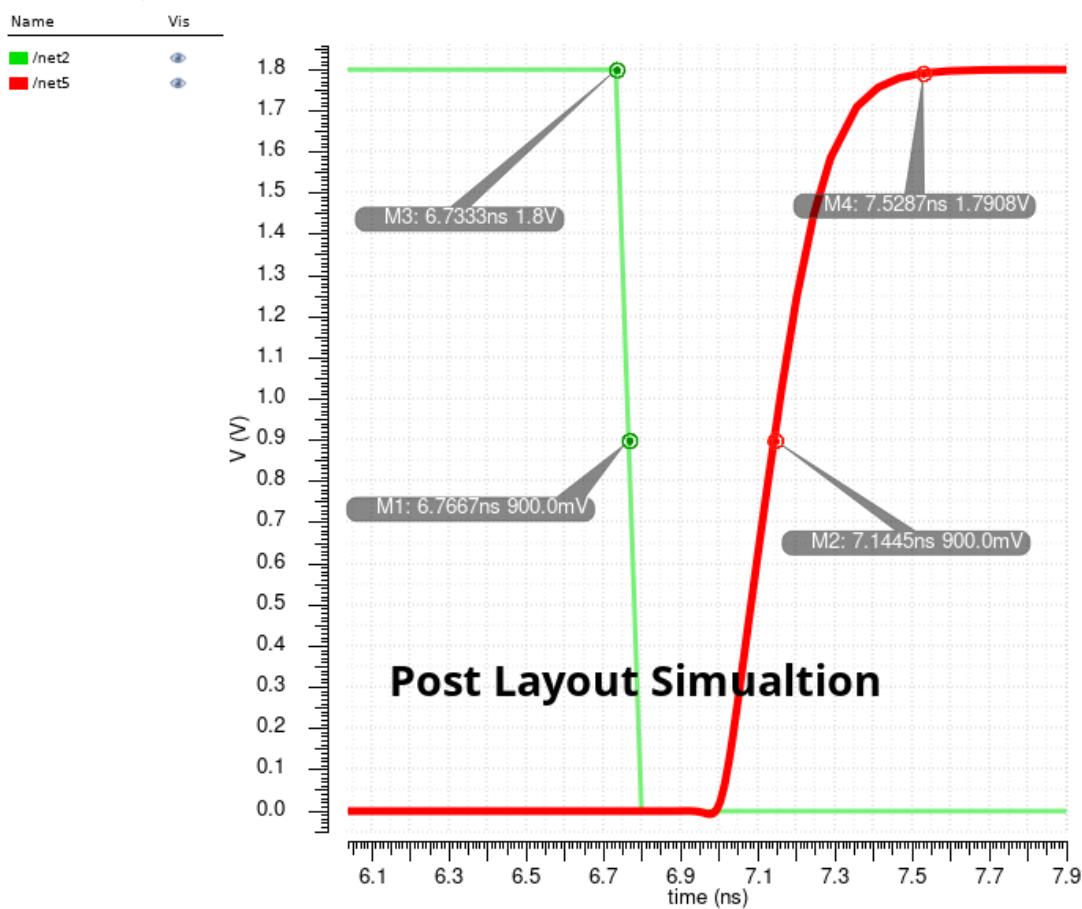
```

Property Editor

It is now using the calibre file as a point of reference for the parasitic capacitances created after the layout.

Transient Response

Sat Oct 15 00:33:56 2022 1



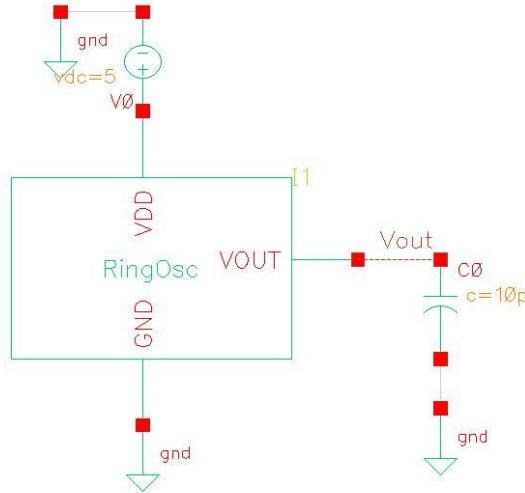
For propagation delay:
50%-50%

$$7.1455\text{ns} - 6.7667\text{ns} = 0.3788\text{ns}$$

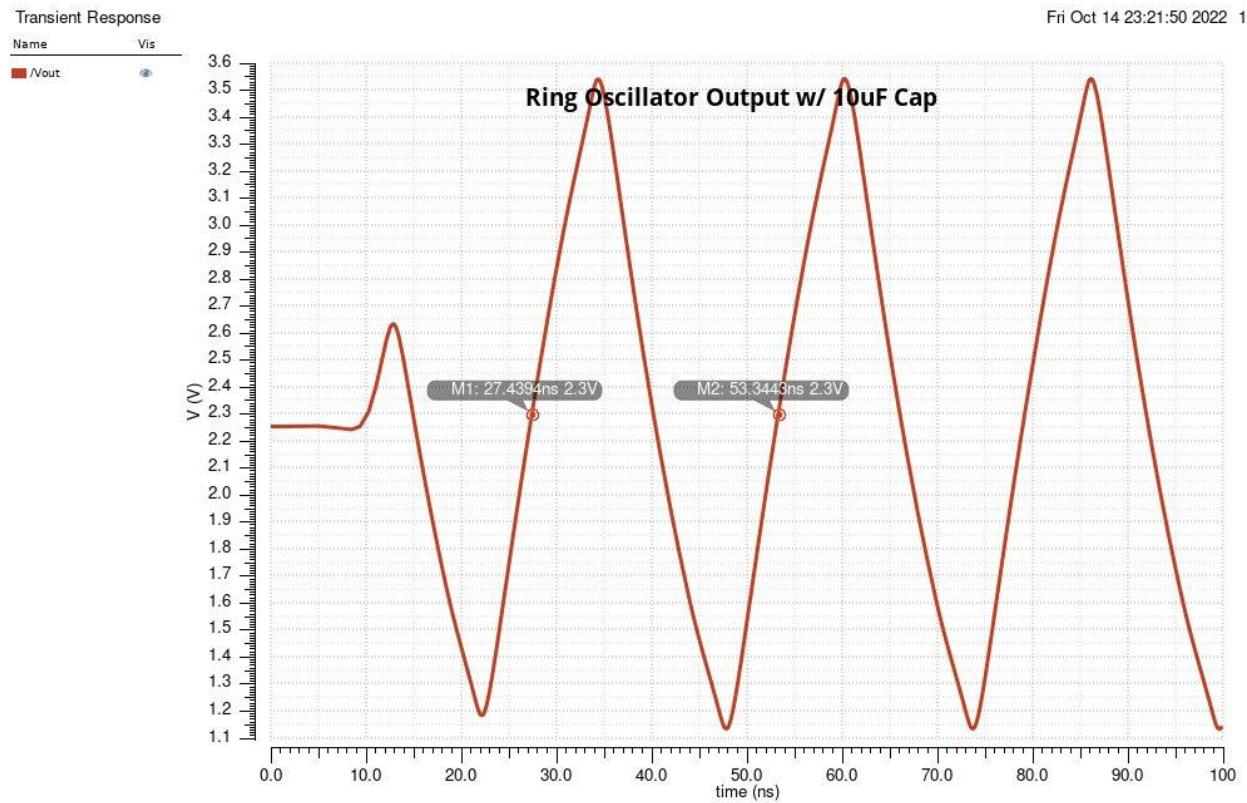
Low to High:

$$7.5387\text{ns} - 6.7333\text{ns} = 0.7954\text{ns}$$

Part 3: Combining Oscillator and Buffer



When a 10pF capacitor is attached to the output of the ring oscillator, the output below is attained:

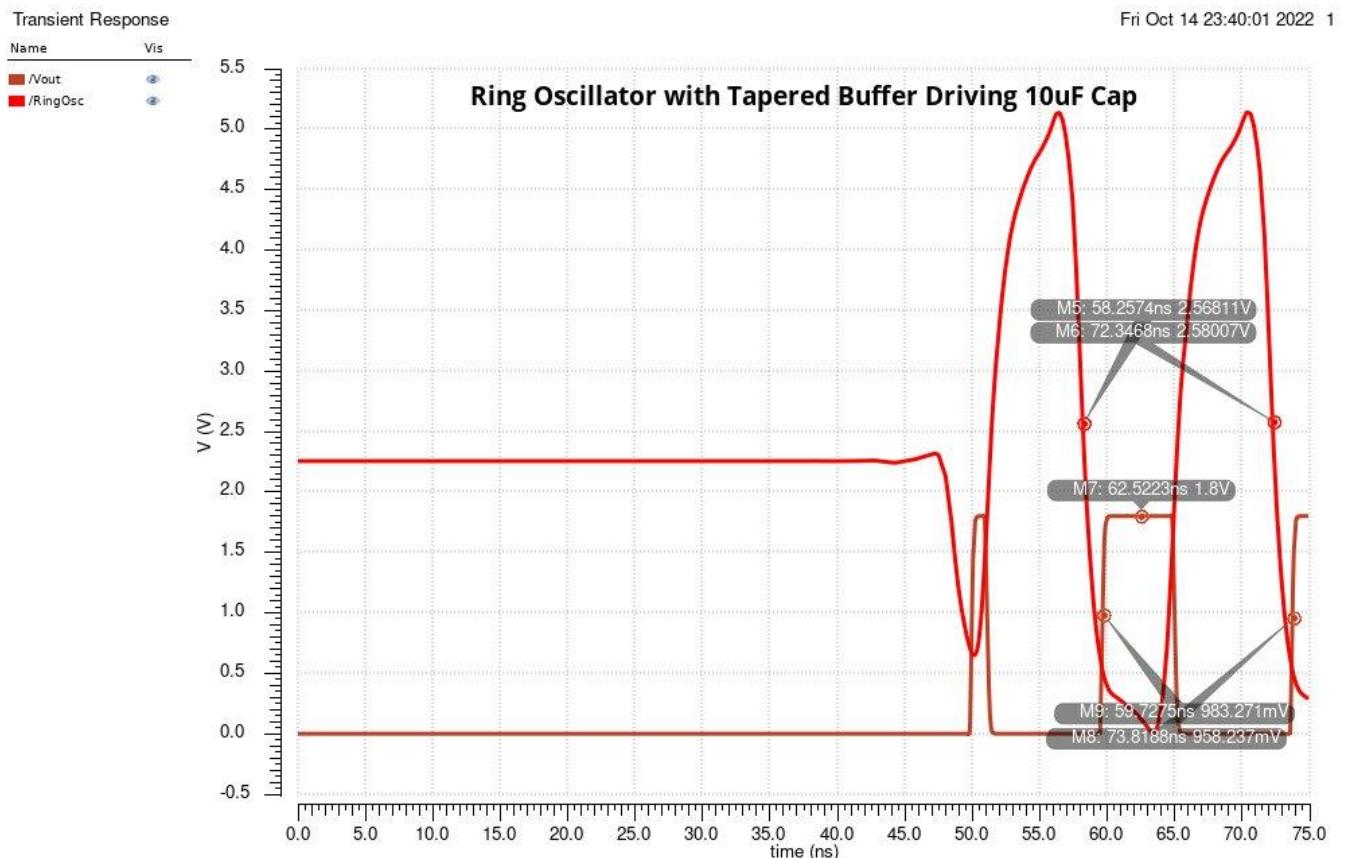
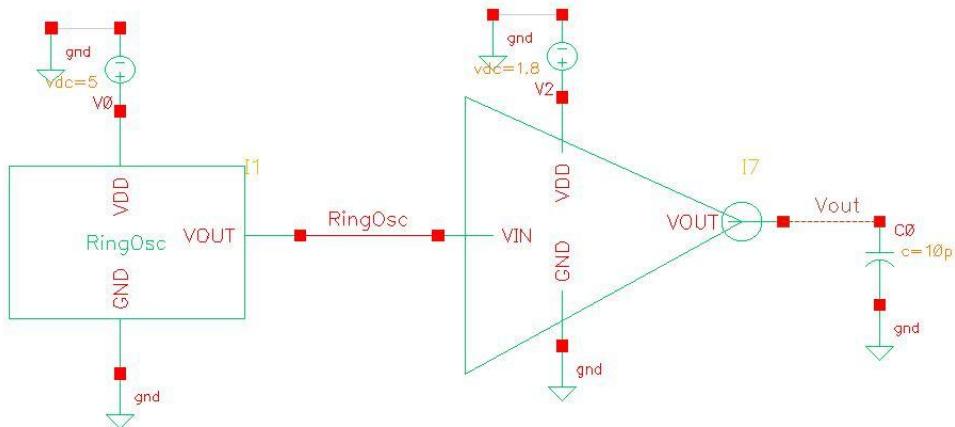


The output of the ring oscillator becomes more sawtooth shaped, although it seems like the period of the oscillation has been greatly increased. The performance as follows:

$$T_{osc} = 53.3443\text{ns} - 27.4394\text{ns} = 25.9049\text{ns}$$

$$F_{osc} = 1/T_{osc} = 38.6\text{MHz}$$

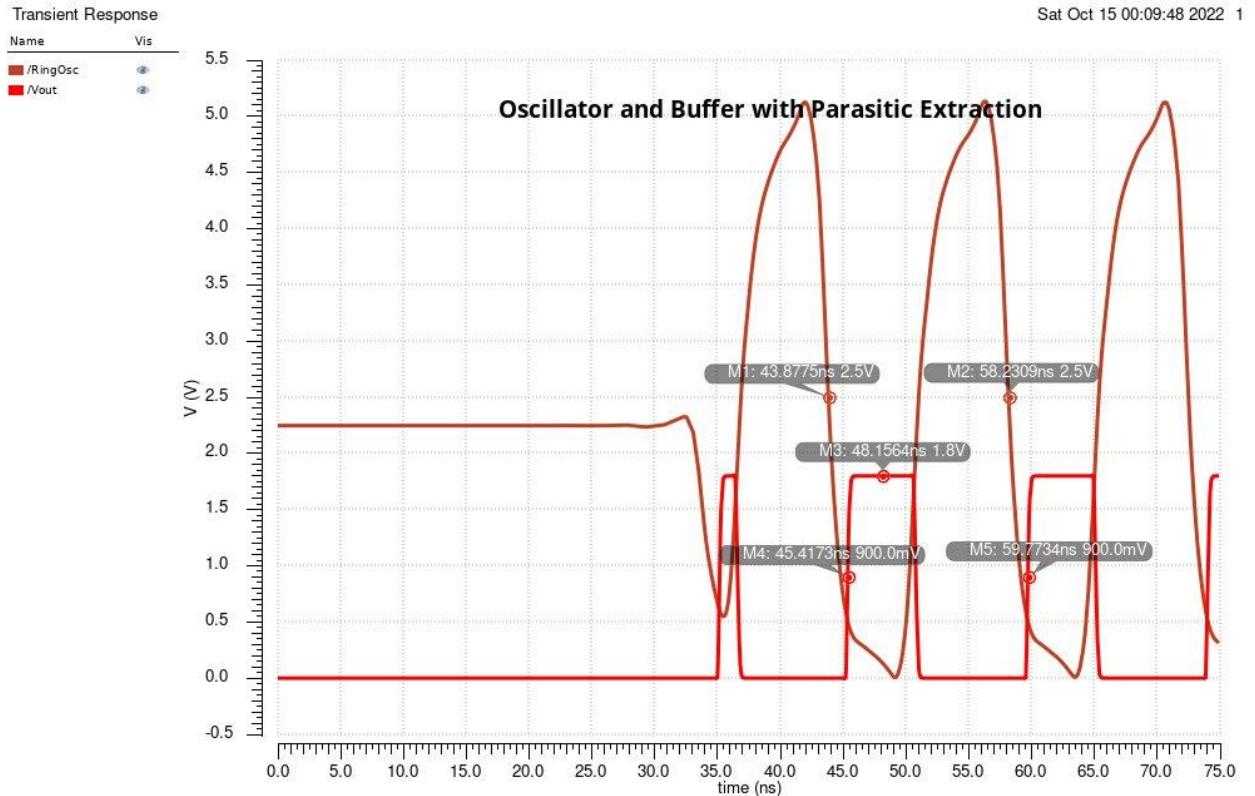
This output frequency is notably about half of the frequency it should be, on account of the capacitor which was added. A tapered buffer is needed between the oscillator and cap to remedy this.



When a tapered buffer is added to the circuit, the output is more like what is expected. In the graph above (with the buffer added now), the performance is as follows:

$$T_{osc} = 72.3486\text{ns} - 58.2574\text{ns} = 14.0912\text{ns}$$

$$F_{osc} = 1/T_{osc} = 70.96\text{MHz}$$



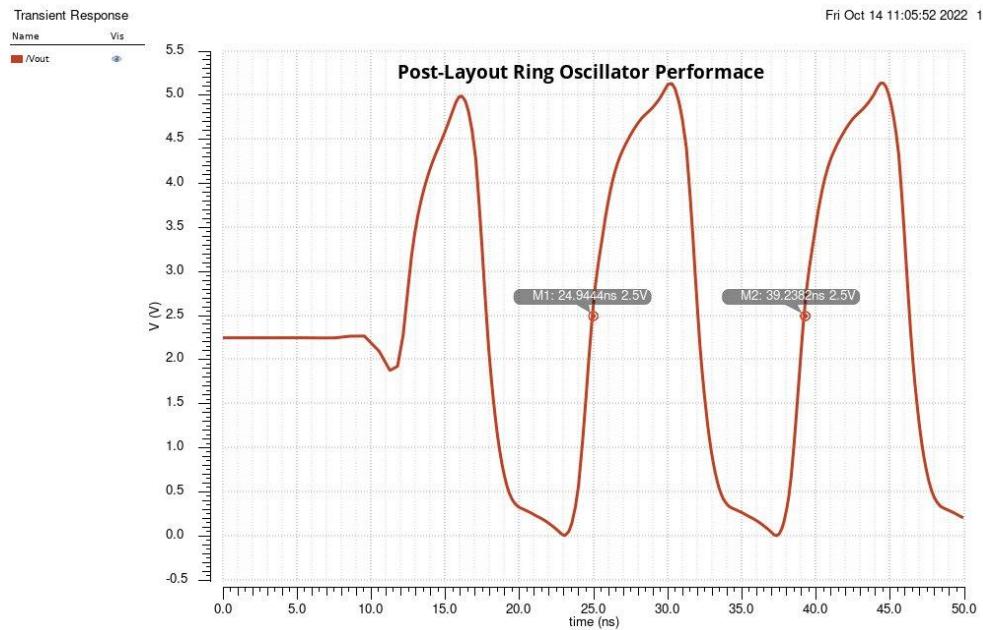
When a parasitic extraction is performed on this circuit, the performance is as follows:

$$T_{osc} = 58.2309\text{ns} - 43.8775\text{ns} = 14.3534\text{ns}$$

$$F_{osc} = 1/T_{osc} = 69.69\text{MHz}$$

After everything, the oscillator and buffer are still working in spec.

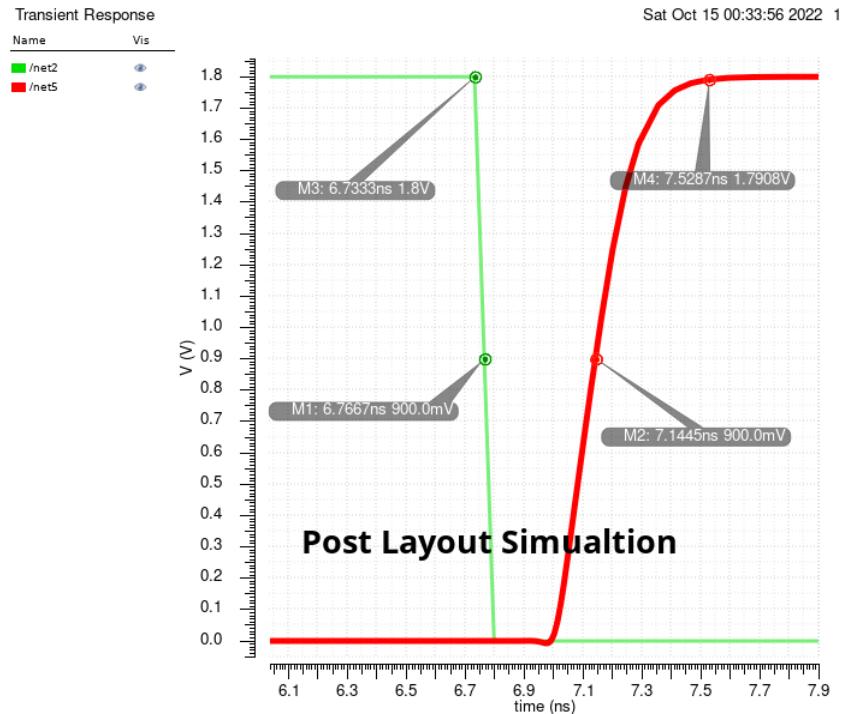
Bonus



The graph above shows the post-layout performance of the ring oscillator, performing within spec. The performance is as follows:

$$T_{osc} = 39.2382\text{ns} - 24.9444\text{ns} = 14.2938\text{ns}$$

$$F_{osc} = 1/T_{osc} = 69.96040241\text{MHz}$$



For propagation delay:

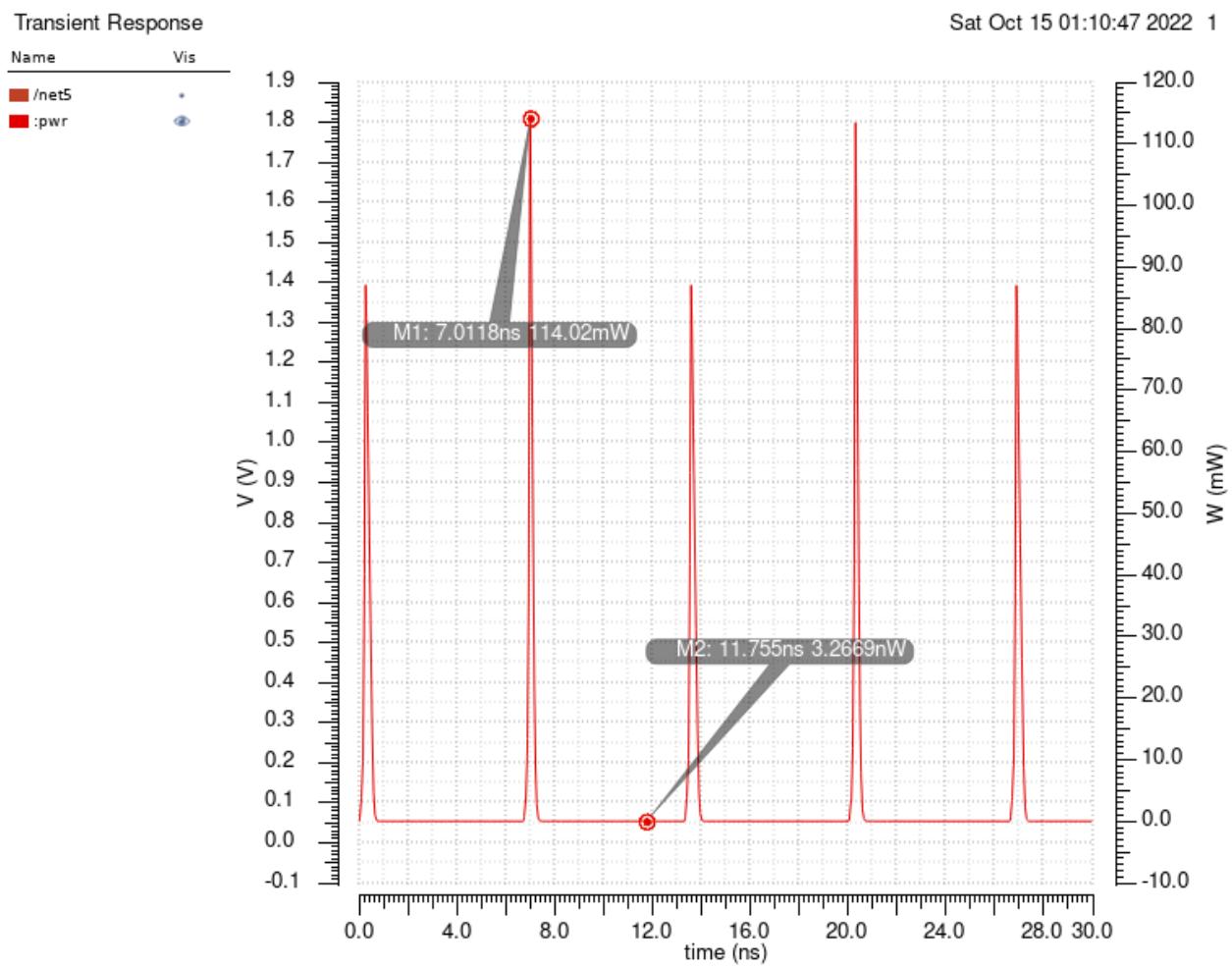
50%-50%

$$7.1455\text{ns} - 6.7667\text{ns} = 0.3788\text{ns}$$

Low to High:

$$7.5387\text{ns} - 6.7333\text{ns} = 0.7954\text{ns}$$

Average Power Consumption Tapered Buffer:



Using the avg function in the calculator:

A screenshot of a mobile application's calculator interface. The screen shows the expression "average(getData(":pwr" ?res...)" followed by the result "3.325...". There are two checkboxes at the bottom: one checked with a red checkmark and one unchecked with a grey square. The background is white with a light grey header bar.

3.325mW