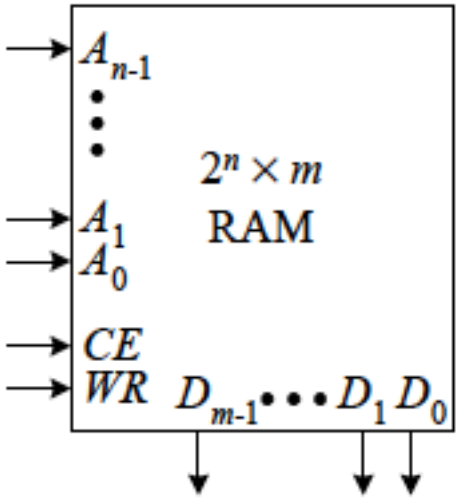
Memória

Paulo Roberto Oliveira Valim

RAM estática



CE	WR	Operation
0	×	None
1	0	Read from memory location selected by address lines
1	1	Write to memory location selected by address lines

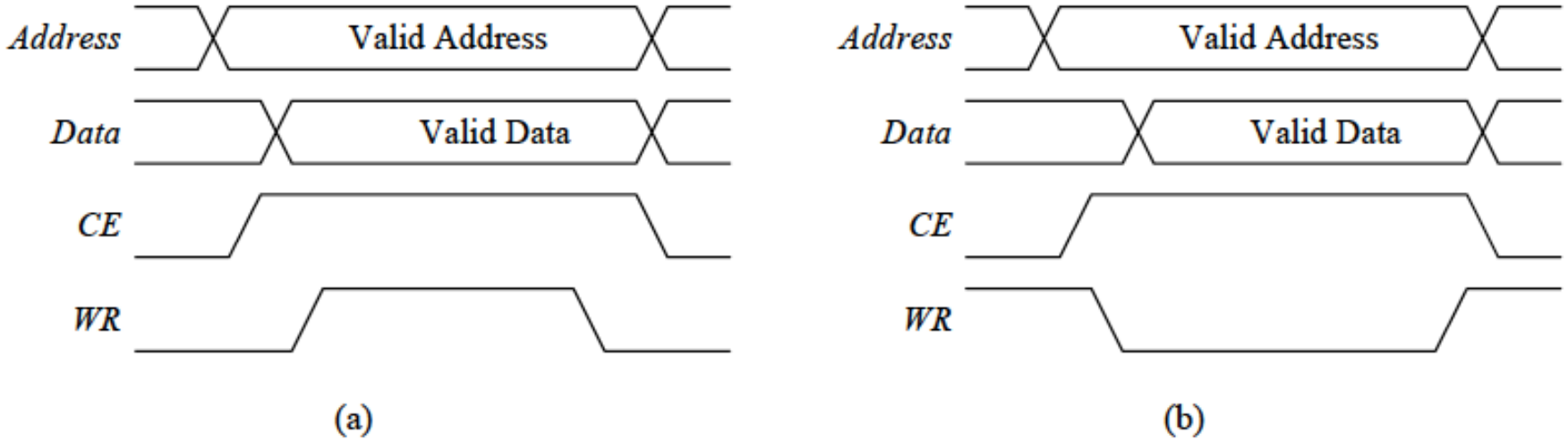
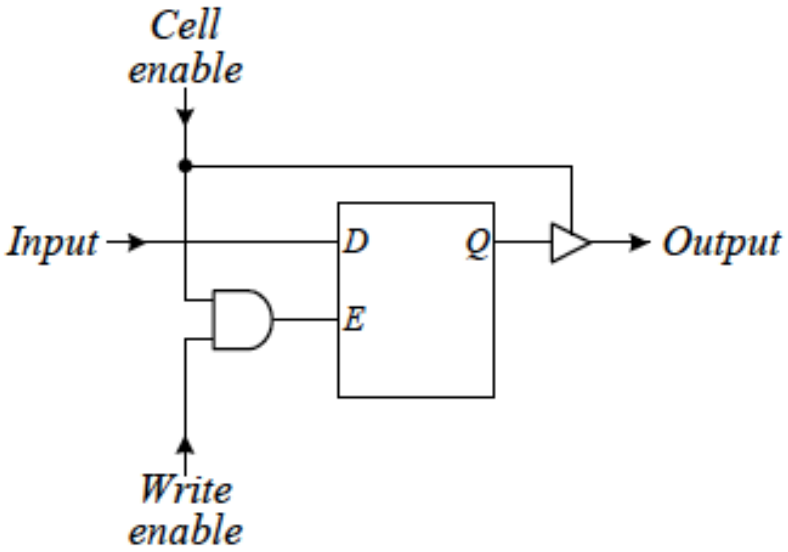
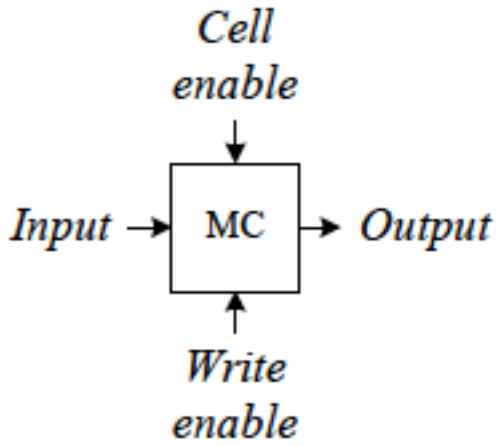
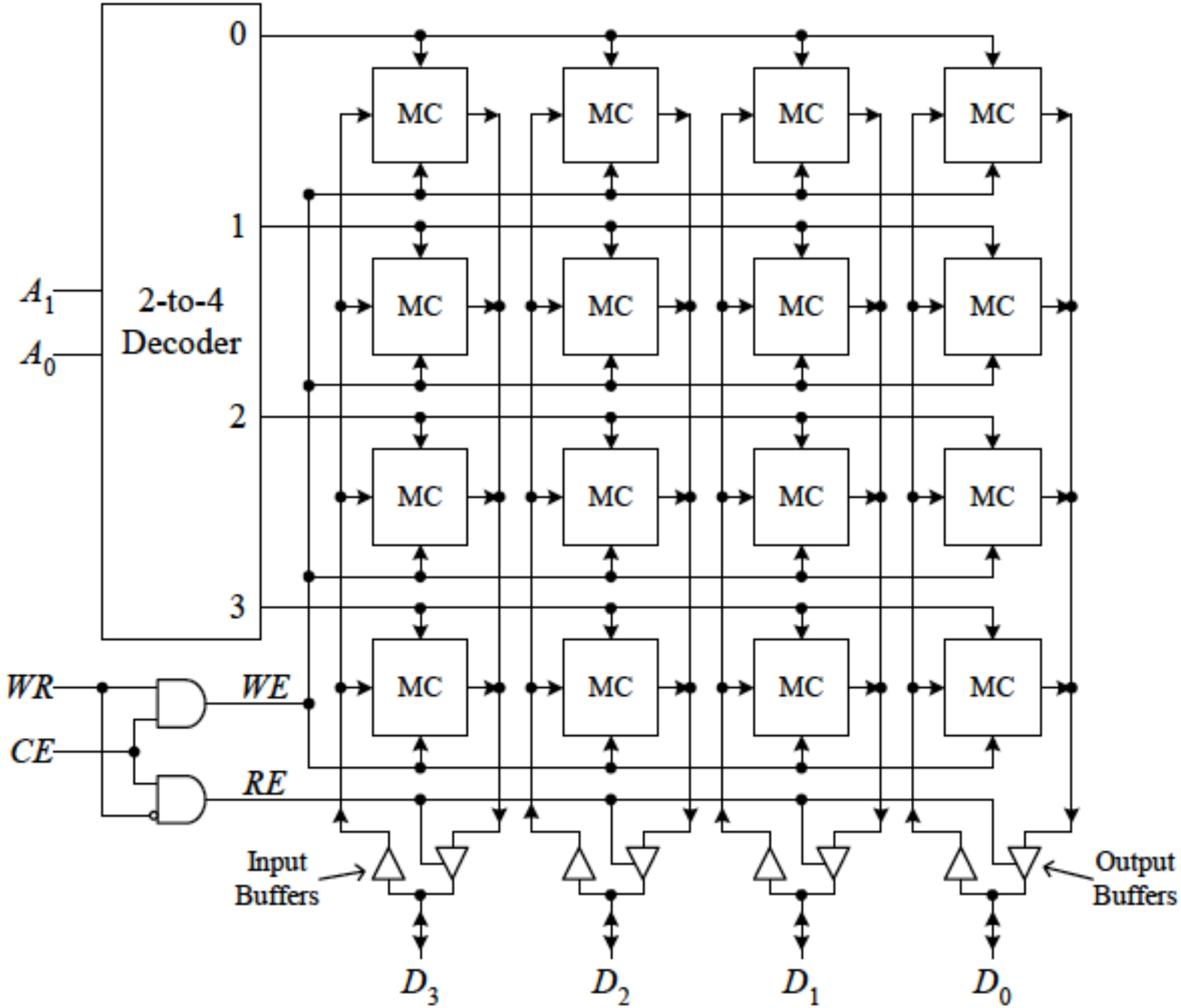


Figure 8.30 Memory timing diagram: (a) read operation; (b) write operation.

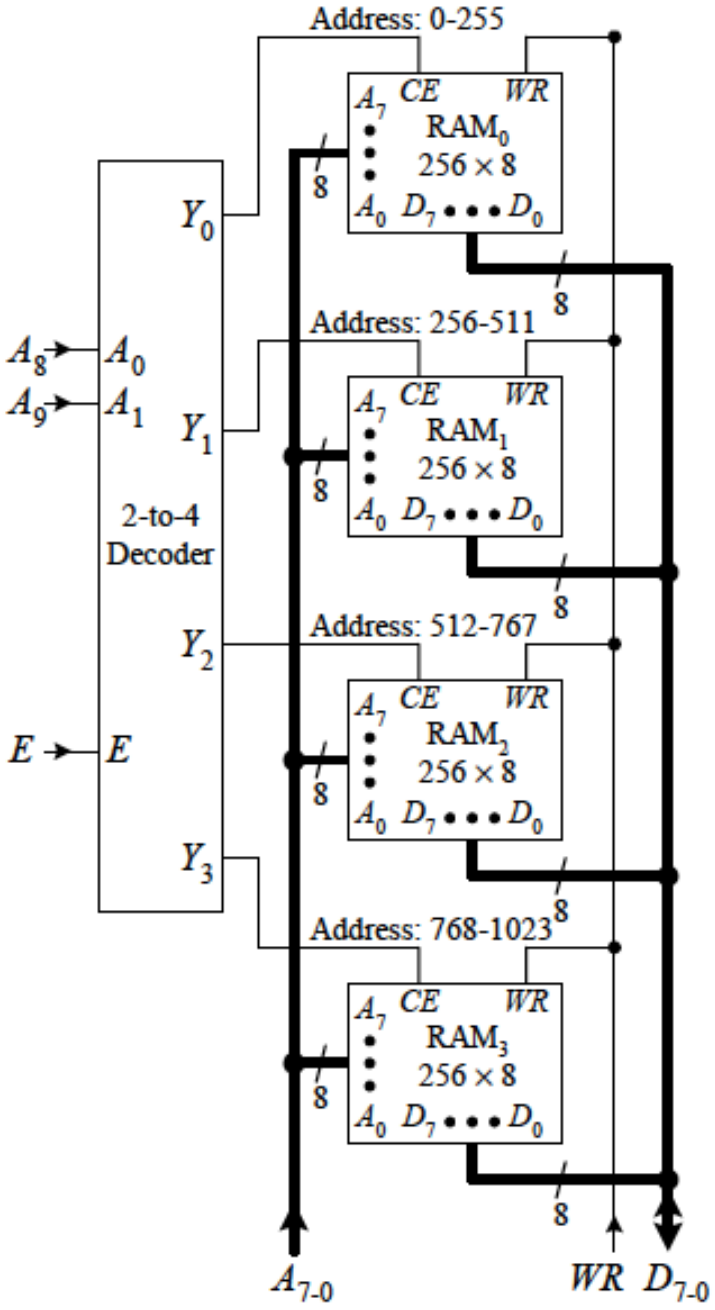

Cell
enable
Input
D
Q
Output
E
Write
enable


Cell
enable
Input
MC
Output
Write
enable

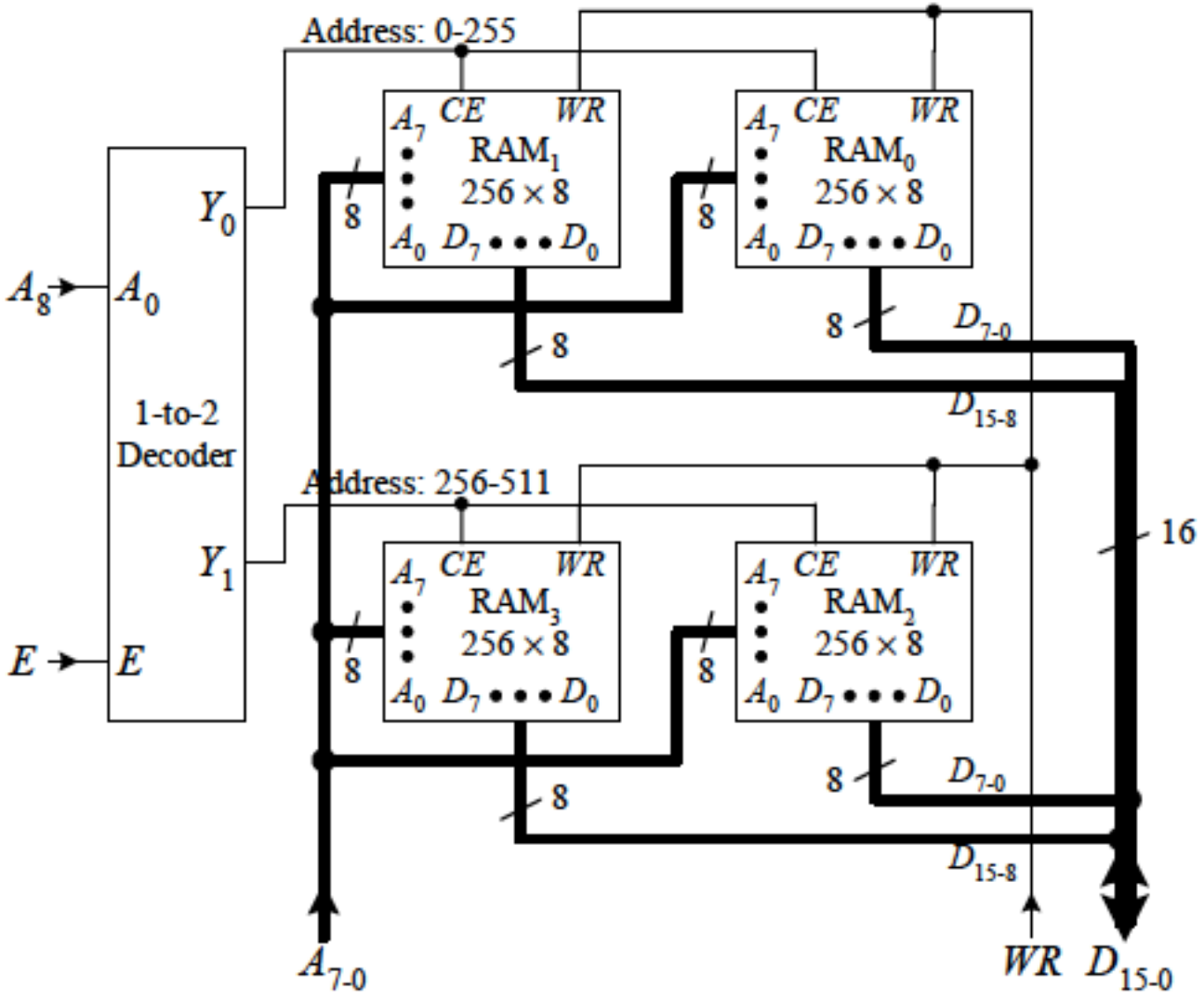


A 4 × 4 RAM chip circuit.

Banco de Memória



(a)


Address: 0-255
Address: 256-511
1-to-2
Decoder
A_8
A_0
E
Y_0
Y_1
A_7
A_0
CE
WR
RAM_1
RAM_0
RAM_3
RAM_2
256 × 8
$D_7 \bullet\bullet\bullet D_0$
8
16
$D_{7\text{-}0}$
$D_{15\text{-}8}$
$A_{7\text{-}0}$
WR
$D_{15\text{-}0}$