

The screenshot displays the Xilinx Vivado IDE interface. The main editor shows a complex logic design with various components and connections. The right-hand pane is open to the 'Clock Tree' summary, which includes a table of clock sources and their properties.

na	sources	is_generated	propagated_clock
clk	false	true	
clk	false	false	
clk	false	true	
clk	false	true	

Below the table, the 'Fanout beyond exception' is set to 'Levels: From: 0'. The 'Show cells by level' and 'Show cells by type' options are checked. The 'Show pins' option is also checked.

The bottom status bar shows the console output, which includes the text: 'Click objects or drag a box to select (Hold Ctrl to add, Shift to remove)'.

A = 89385.7248  
D = 4.08  
L = 3  
ADL = 1094081.272