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DYNAMICS OF FISH

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Abstract

Some nonsense goes here.

Table of Contents

| | |
|---|----------|
| List of Figures | vi |
| List of Tables | viii |
| List of Symbols | ix |
| Acknowledgments | x |
| Chapter 1 | |
| Introduction | 1 |
| Chapter 2 | |
| Background and literature review | 3 |
| 2.1 Semiconductors | 3 |
| 2.1.1 Metal-Semiconductor-Metal conduction | 3 |
| 2.1.2 Field effect transistors (FET) | 7 |
| 2.1.2.1 Band Bending? (TODO) | 10 |
| 2.1.3 Weak localization (TODO) | 11 |
| 2.2 Ferroelectricity | 11 |
| 2.2.1 Piezoelectricity and pyroelectricity | 11 |
| 2.2.2 Domains and polarization | 12 |
| 2.2.3 Phase transitions | 14 |
| 2.2.3.1 First-order, $\beta < 0$ and $\gamma > 0$ | 15 |
| 2.2.3.2 Second-order, $\beta > 0$ | 15 |
| 2.2.4 Ferroelectric field-effect transistors (FeFETs) | 16 |
| 2.2.5 Ferroelectric tunnel junctions (FTJs) | 18 |
| 2.2.6 Polar metals | 19 |
| 2.2.7 FeFETs with ferroelectric channels | 19 |
| 2.3 2D materials | 20 |
| 2.3.1 Trapped charge in 2D FETs? (TODO) | 20 |
| 2.3.2 In-Se compounds | 20 |
| 2.3.2.1 In_2Se_3 polymorphs in literature | 20 |

| | |
|--|-----------|
| Chapter 3 | |
| Sample fabrication and measurement methods | 25 |
| 3.1 Introduction | 25 |
| 3.2 Flake generation | 26 |
| 3.2.1 Alignment marker wafer chips | 26 |
| 3.2.2 Mechanical flake exfoliation | 26 |
| 3.3 Photolithography | 29 |
| 3.3.1 LOR/SPR stack | 29 |
| 3.3.2 PMMA/PMGI/SPR stack for alkali-sensitive materials | 30 |
| 3.4 Thin filament shadow mask | 31 |
| 3.5 Metal evaporation and liftoff | 32 |
| 3.6 Sample wiring | 33 |
| 3.7 Layer Transfer? (TODO after I figure it out) | 34 |
| 3.8 PFM? (TODO, I don't do it but it might be useful) | 34 |
| 3.9 Hall probe (TODO) | 34 |
| Chapter 4 | |
| Electric field induced metallic behavior in thin crystals of ferroelectric $\alpha\text{-In}_2\text{Se}_3$ | 35 |
| 4.1 Introduction | 35 |
| 4.2 Device manufacture | 36 |
| 4.3 Optical crystal measurements | 38 |
| 4.4 FET measurements | 39 |
| 4.5 Discussion | 41 |
| Appendix A | |
| 3D crystal symmetry groups | 45 |
| Appendix B | |
| Additional $\alpha\text{-In}_2\text{Se}_3$ Figures | 50 |

List of Figures

| | | |
|------|---|----|
| 2.1 | Band diagrams of metal in contact with a n-type semiconductor | 5 |
| 2.2 | Current-voltage behavior of various junctions | 7 |
| 2.3 | FET | 9 |
| 2.4 | Polarization | 13 |
| 2.5 | Landau first order transition | 16 |
| 2.6 | Landau second order transition | 17 |
| 2.7 | Ferroelectric field effect transistors | 22 |
| 2.8 | Ferroelectric tunnel junctions | 23 |
| 2.9 | In-Se alloy phase diagram. | 24 |
| 2.10 | In ₂ Se ₃ crystal structure | 24 |
| 3.1 | Device manufacture. | 27 |
| 3.2 | Flake manufacture | 28 |
| 3.3 | Resist stacks | 31 |
| 3.4 | Filament device | 32 |
| 3.5 | Wiring | 34 |
| 4.1 | Device images | 37 |

| | | |
|------|---|----|
| 4.2 | Optical measurements of $\alpha\text{-In}_2\text{Se}_3$. | 39 |
| 4.3 | Sample A: $I_D(V_{DS})$ | 40 |
| 4.4 | Sample A: $I_D(V_G)$ transfer characteristics | 41 |
| 4.5 | Temperature dependence and magnetic field measurements | 43 |
| B.1 | Sample A: $I_D(V_{DS}, V_G)$ | 50 |
| B.2 | Sample B: $I_D(D_{DS}, V_G)$ | 51 |
| B.3 | Sample C: $I_D(V_{DS}, V_G)$ | 52 |
| B.4 | Sample B: $I_D(V_G)$ transfer characteristics | 53 |
| B.5 | Sample C: $I_D(V_G)$ transfer characteristics | 54 |
| B.6 | Sample C: effects of warming and cooling while gated | 55 |
| B.7 | Sample B: $I_D(V_G)$, V_G rate dependence | 55 |
| B.8 | Sample D: contact resistance | 56 |
| B.9 | Sample A and B: annealing | 56 |
| B.10 | Sample A: magnetoconductance | 56 |

List of Tables

| | | |
|-----|--|----|
| 2.1 | <i>In₂Se₃</i> polymorphs | 21 |
| 2.2 | <i>InSe</i> polymorphs | 21 |
| 3.1 | Lithography resists | 30 |
| 4.1 | Device parameters | 38 |
| A.1 | 3D crystal classes [1] | 45 |

List of Symbols

- α The first Landau parameter, p. 14
- β The first Landau parameter, p. 14
- γ The first Landau parameter, p. 14
- E Electric field, p. TODO
- E_c Coercive electric field, p. 13
- P Material polarization, p. 11
- T_0 Landau Curie–Weiss transition temperature, p. 14
- T_C The Curie temperature, p. 11

Acknowledgments

Chapter 1

Introduction

Ferroelectricity was first experimentally observed just over 100 years ago in 1920 by a PhD student at the University of Minnesota, Joseph Valasek [2]. Valasek was originally working with piezoelectric crystals to develop a seismograph when he observed that placing one such material, Rochelle salt, in an electric field showed S-like curve with hysteresis [3]. Ferromagnetism was already known at the time of the discovery so Valasek made the analogous connection showing the relationship between magnetic and electric fields. This gave rise to the term “ferroelectricity” even though such materials rarely contain iron like their ferromagnetic precursors. Ferroelectricity was largely ignored until the discovery of barium titanate (BaTiO_3) during the second world war, where Valasek was seeking to use ferroelectrics to make transducers for submarine detection. Barium titanate had many physical advantages compared to Rochelle salt, it was chemically stable at room temperature, insoluble in water, a high dielectric constant, and more robust ferroelectricity. Its simple structure helped researchers investigate ferroelectricity, eventually resulting in the Landau-Ginzberg-Devonshire phenomenological model of ferroelectricity in 1951 [4]. Barium titanate is still used today in “condensers” and capacitors as its relative permittivity is much greater than most non-ferroelectric dielectrics. [5]

BaTiO_3 showed that oxide crystals could be ferroelectric and in the decades following the Second World War hundreds new ferroelectric compounds were discovered. Ceramics are the most common ferroelectrics in use, due to the ease of manufacture and the ability to build complex configurations in while still behaving like a single ferroelectric crystal. In 1952 lead zirconate-titanate (PZT) was discovered and has become one of the most widely used piezoelectric ceramics, though recent efforts have sought to find lead-free alternatives that are more environmentally friendly. All ferroelectric materials are also piezoelectric and pyroelectric, though the reverse is not true, and many have found

applications in ultrasound, capacitors, transducers, micropositioners, energy harvesters, night vision, sensors, and many other devices.

The applications of ferroelectrics to modern electronics are numerous and diverse, but perhaps the most sought after utilization is enhancing random access memory (RAM) with a ferroelectric dielectric. While the original idea for ferroelectric RAM (FeRAM) was first proposed by Dudley Allen Buck's in his 1952 master's thesis, limitations of the known ferroelectric materials have prevented commercialization. To integrate with silicon transistors, ferroelectrics must be scaled down to a few nanometers in thickness, have a scalable growth processes that is compatible with the temperature limitations of the other materials and lithography processes, all while maintaining their electronic properties. The development of thin ferroelectric films into standard silicon circuits in 1984 was one of the first major milestones approaching practical FeRAM [6] and since then researchers and engineers have continued to push towards this goal. The recent explosive growth in 2D material research, and the subsequent discovery of ferroelectricity down to a few layers of material has opened the possibility of integrating ferroelectric memory with the logic circuits of modern processors.

TODO: discuss what contents of later chapters are.

Chapter 2 | Background and literature review

2.1 Semiconductors

Semiconductors, as their name implies, are characterized by their decreased conduction compared to a metal, while still more than an insulating material. They possess a band gap of a few electron volts (eV), driving this conductivity. Semiconductors come in two flavors, n-type and p-type, that conduct predominately using either electrons or holes respectively. Carriers reside below the Fermi energy in the fully occupied valance band but can be exited to move to an unoccupied higher energy band, the conduction band and thus move thus conduct. This is often through thermal excitation, so most semiconductors have an increased resistance at low temperatures. Photons can also excite electrons giving rise to countless applications such as sensors and LEDs. Furthermore, semiconductor behavior can be altered by introducing other elements or electric fields giving rise to a wide range of potential applications in just about every area of modern electronics.

TODO Add band diagram showing metal, sc, insulator

2.1.1 Metal-Semiconductor-Metal conduction

When constructing electronic devices with multiple materials the physical and chemical properties of the material contact region must be considered. When placed in contact with each other, band structures of the individual crystal is altered as a new preferred energy minimum is reached, chemical reactions between the two materials can take place, and the physical dimensions of one material can shift to accommodate the other. For most electronic transport applications, an ohmic contact is preferred as it takes the least potential to form a current and is an easily predictable behavior. Ohmic contact is

characterized by a linear relationship between the voltage and current given by the usual equation $V = IR$. This typically seen for a metal-metal junction as there is little band bending and metal's ability to conduct at a wide range of energy levels. At the interface between metals and semiconductors a Schottky contact is typically formed instead that is non-ohmic in behavior. The actual nature of Schottky contacts is complicated and no simple model exists for the interface of metal-semiconductors. [7, 8] To predict the behavior of a metal-insulator junction one must numerically calculate the quantum mechanical states of the system, including the materials chemistry, and include the system's geometry. [9]

To provide at least a metal model of the behavior of the system, a simplistic model will be given for the behavior of a Schottky contact that ignores some of the individual details but gives broad predictions. Next to the junction, the electrons in the semiconductor move to (or from) the conduction band of the metal, depleting (accumulating) electrons in the area nearest to the metal. This causes the bands to bend, shown in Figure 2.1a-2.1b. The Schottky-Mott rule gives the energy barrier Φ_B of a charge carrier q between the two materials in terms of the work function of the metal ϕ_M and semiconductor electron affinity χ_{SC}

$$\begin{cases} \Phi_{B,n} = \phi_M - \chi_{SC} & n-type \\ \Phi_{B,p} = \chi_{SC} - \phi_M & p-type \end{cases} \quad (2.1)$$

The bulk of the semiconductor band shifts to accommodate the difference in work functions of both materials $\phi_M - \phi_{SC}$.

Applying a forward voltage bias to the system allows electrons from the semiconductor band to tunnel into the metal forming a current. Applying a bias in reverse causes only a few thermally excited electrons in the metal to tunnel to the semiconductor resulting in almost no current. Taken together, for an n-type semiconductor electrons can more easily flow from the semiconductor to the metal than the reverse. [11] Figure 2.1c-2.1d shows the potential shifting the bands in a forward and reverse bias. However, if a large enough reverse voltage bias is applied the carriers can instead move to the valance band of the semiconductor. This voltage-current curve is used to form diodes that conduct current only in one direction, where the reverse current is considered the breakdown potential of the diode. In order to reduce the band mismatch various techniques are often used to achieve Ohmic contact. Selecting the appropriate metal can reduce the energy band mismatch though it will likely still have a significant barrier. A common solution is to instead dope the semiconductor near the region of contact to provide a smooth transition between the metal and the semiconducting region.

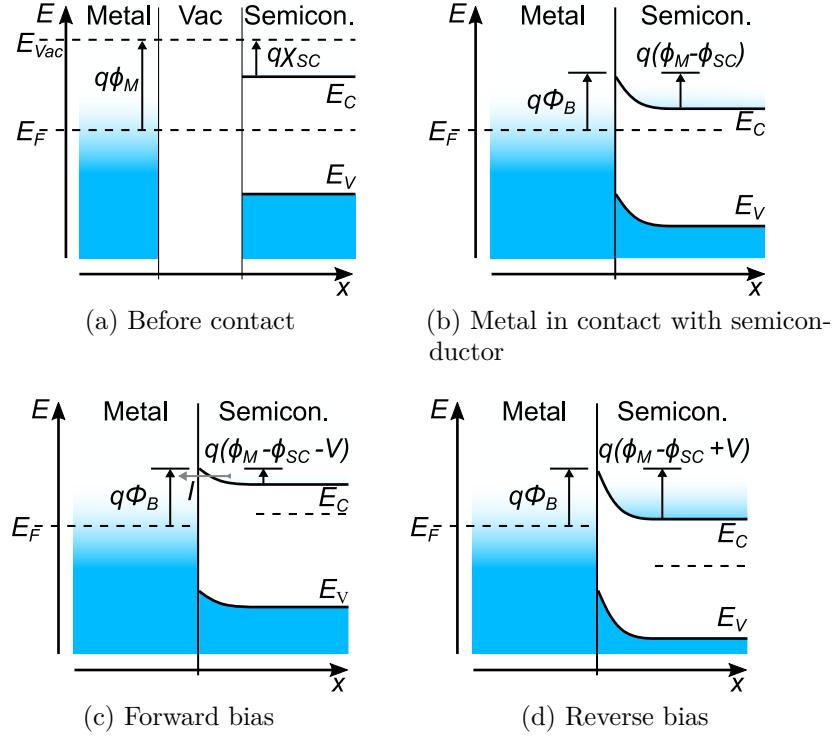


Figure 2.1: Band diagrams of metal in contact with a n-type semiconductor (2.1a) before and (2.1b) after a metal is brought into contact with a n-type semiconductor. [10] Φ_B is the Schottky barrier height, E_F , the Fermi energy, E_C and E_V the conducting and valance bands. 2.1cforward and 2.1d reverse voltage bias applied from right to left. Arrow indicated the direction of current flow.
TODO: Add in boundary layer. Match with FTJ and FeFET

For Schottky contacts behavior can be modeled using thermionic emission theory. The current density is given by

$$J = J_0 \left(\exp \left(\frac{qV}{k_B T} \right) - 1 \right), \quad (2.2)$$

$$J_0 = A^{**} T^2 \exp \left(-\frac{q\Phi_B}{k_B T} \right) \quad (2.3)$$

where J_0 is the saturation current density, q the fundamental charge, k_B Boltzmann constant, T the temperature, and A^{**} the Richardson constant. [12–14] For a complete conduction channel though a semiconductor, both metal contacts must be considered, current in and out, as both are Schottky barriers. If we apply a voltage across the entire structure we have to consider the potential drop across each contact V_n as well as the

material itself V_{SC} . The voltage drop across a single diode is then

$$V_n = \pm \frac{k_B T}{q} \ln \left(\pm \frac{J}{J_{0n}} + 1 \right) \quad (2.4)$$

where the sign corresponds to the direction of current and J_{0n} depends on the individual barrier energy Φ_{Bn} . We may also consider that the contacts may not be ideal and introduce a contact specific parameter $n_n \geq 1$ to take this into account. With this we have the total voltage across the contacts

$$V = V_1 + V_{SC} + V_2 \quad (2.5)$$

$$V = \frac{n_1 k_B T}{q} \ln \left(\frac{J}{J_{01}} + 1 \right) + R A J - \frac{n_2 k_B T}{q} \ln \left(\frac{J}{J_{02}} + 1 \right) \quad (2.6)$$

where A is the surface area and R the resistance of the semiconductor. [12–14] This equation is not directly solvable for the current density but it is possible to numerically model the behavior as shown in figure 2.2. Figure 2.2a shows a typical linear ohmic behavior for large and small resistance. Figure 2.2b and 2.2c shows the behavior of a single diode and attached to a large and small resistance. The increased resistance can be seen in the higher voltages needed to reach the saturation current while the barrier height limits the reverse bias current. Figure 2.2e and 2.2f shows the behavior of both barriers and the semiconductor in this model. Similar to the single contact, the barrier height dictates the saturation current and the resistance the rate at which increasing voltage reaches saturation. The ideality factor n produces a deviation from the ideal curves which can easily be seen with a smaller R , making two contacts that have the same barrier height still produce an asymmetric behavior. This differentiation will decrease as R increases and the semiconductor resistance becomes as large as the contacts.

This non-linear behavior must be taken into account for any electronic transport done on a material as the Schottky contact can have multiple competing effects on a measurement. For a four-terminal device charges may or may not tunnel into a lead in contact with the semiconductor based on the size of the barrier and the resistance of the material being tested. Furthermore by placing a metal in contact with a semiconductor the region around the material is altered so a uniform material can not be assumed if it is near that metal. The ideality factor and barrier height can shift the two terminal resistance of a material so the current produced is not symmetric with respect to the voltage direction.

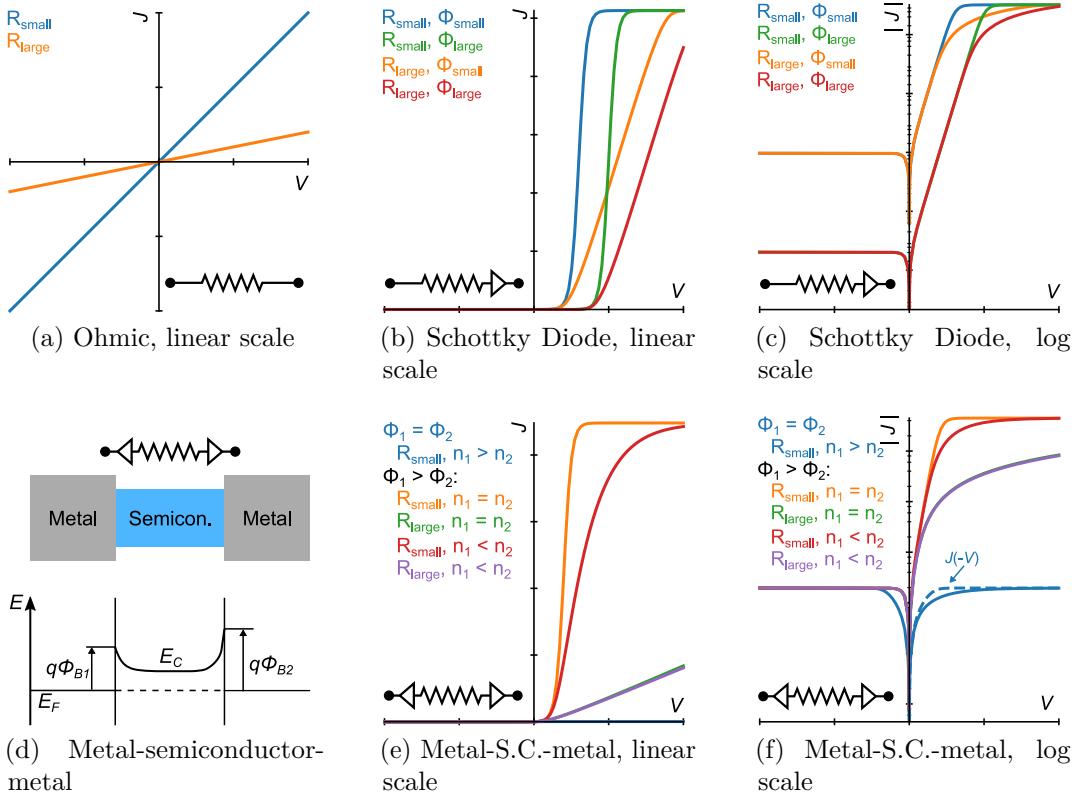


Figure 2.2: Current-voltage behavior of various junctions

Current-voltage graphs of the behaviors of different junction parameters from equation 2.6. (a) ohmic behavior, with no Schottky barrier with large and small resistances. A single Schottky barrier with small and large resistances and barrier heights, in linear (b) and logarithmic (c) plots. (d) simplified band diagram for a double Schottky barrier in a metal-semiconductor-metal device. A double Schottky barrier with large and small resistances, barrier heights, and ideality factors on a linear (e) and log (f) scale. The dashed line shows the asymmetrical nature of a pair of junctions with different ideality factors.

2.1.2 Field effect transistors (FET)

One of the most common applications of semiconductor devices is a field effect transistor (FET). Transistors provide a way to turn a current on or off with a voltage, allowing for controllable states in larger circuits. This forms the basis of digital logic in computers, by defining a threshold current as “on” or “off” we form a binary system. Transistors also allow for circuit elements to be isolated from each other, providing a path for different parts of a circuit to interact with one element while independent of the rest.

The typical structure of a FET is two ohmic contacts on either side of a semiconductor with a metal gate positioned on the semiconductor in between the two contacts.

Between the two contacts a conduction channel is established that majority charge carries, electrons or holes, can pass through. The natural conductivity of this channel can be altered by doping the semiconductor material to change the carrier concentration in the semiconducting material. The gate then provides an electric field that acts on the carriers passing between the two contacts. Removing carriers, known as depletion, will decrease the conductivity, while enhancement adds carriers to increase conductivity. There are two common types of FET, junction gate field-effect transistor (JFET) and metal-oxide-semiconductor FET (MOSFET).

JFET gates are composed of two gates placed on either side of the conduction channel. The gates are opposite in type to the channel, so if the channel is n-type the gate is p-type and vice-versa, figure 2.3a. This junction sets up a depletion region around the gates with a lower carrier concentration. By applying a bias between the source and the gate the depletion region can be expanded, shrinking the conduction channel. This eventually pinches off the entire channel forcing carriers to tunnel across the depletion region and halting most current thus giving an off state to the JFET. Because of this configuration, all JFET must be doped to conduct naturally and operate in depletion mode, as the reverse would generate current though the gate instead.

MOSFET incorporate a thin insulating oxide barrier between the metal gate and the conduction channel channel to isolate each and preventing a junction from forming, as seen in figure 2.3b. This also eliminates almost all current between the gate and the gate and the conduction channel, one of the most important advantages of MOSFET over other types of transistors. The conduction channel contacts are doped to form ohmic contacts opposite to the substrate. MOSFET transistors can operate in either enhancement or depletion mode, another of their significant assets, figure 2.3c shows the different operation modes possible. In enhancement mode the channel region does not have enough carriers to conduct naturally but by applying a gate voltage carriers are added to the region and current flows. Conversely, in depletion mode the channel will conduct without any bias, often though a doped layer, but an external voltage can be used to remove carriers and produce the off state. The bias between the source and drain leads also changes the electric field, and thus carrier density, within the conduction channel. Too large of a voltage causes the channel to start to pinch off, similar to a JFET, and setting a limit on the current that can be sourced between the contacts.

The interplay of drain-source and gate bias on channel behavior in FET lead to a non-trivial relationship between channel current and voltage. Figure 2.3d shows the typical interplay between drain-source voltage and current at different gate voltage

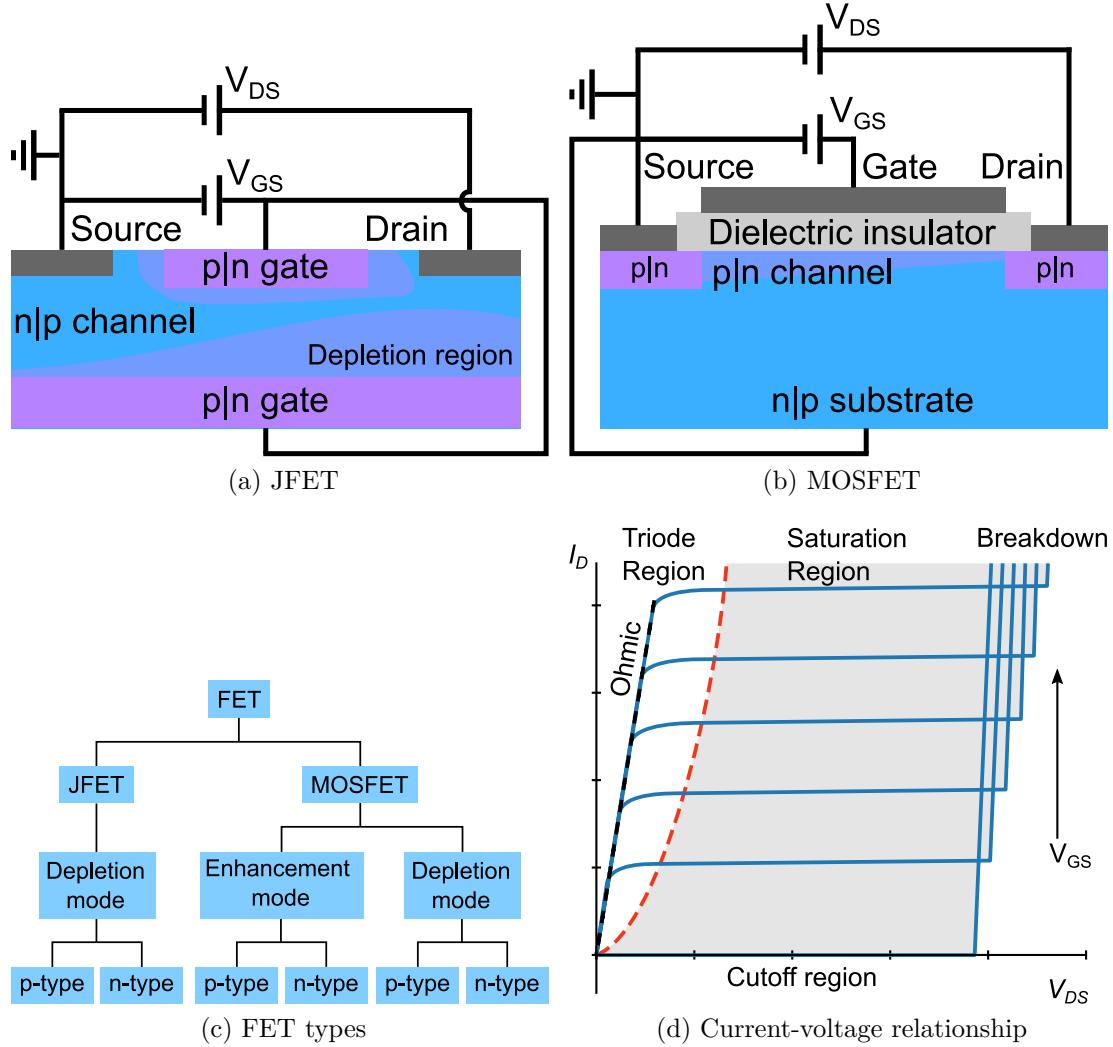


Figure 2.3: FET

Typical (a) JFET and (b) MOSFET devices in n- or p-type configurations. (c) Tree of possible standard FETs used. (d) Source-drain current vs voltage of a generic FET. Different curves show the deviation for increasing gate voltage increments. The transition between ohmic (triode) and saturation occurs near the dotted line. The shown breakdown behavior is a characteristic of a MOSFET rather than most JFET.

intervals. In the cutoff region the channel conduction is exponentially low for almost any current to flow, and is an arbitrary threshold for the off state for a FET. As the channel carrier concentration is raised by the gate voltage the semiconductor has enough free charges for current flow through the channel. For low voltages, $V_{DS} \leq V_G - V_{th}$, the current looks linear and the FET acts like an ohmic resistor. The actual increase more

closely follows

$$I_D = 2\kappa \left((V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right) \quad (2.7)$$

where κ is a scaling factor that depends on multiple factors like temperature, device geometry, and gate capacitance. V_{th} is the threshold voltage at which the gate voltage begins to pinch off the conduction channel, and is also dependent on temperature. Above this limit the current is roughly constant

$$I_D = \kappa (V_{GS} - V_{th})^2 \quad (2.8)$$

and is called the saturation region. The saturation region is what is typically thought of as the on state for a FET, providing an easy binary contrast with the cutoff region. Finally, once V_{DS} is large enough, there is a rapid increase in current known as breakdown, due to the avalanche effect. This typically occurs only in JFET while MOSFET are limited instead by their power dissipation, however MOSFET can suffer an irreversible breakdown in the gate dielectric instead. [15]

Avalanche breakdown starts when a strong enough electric field causes an electron or hole to be propelled into an atom ionizing it and creating a second free charge. The charges can be further driven through the material ionizing more and more atoms along the way. This creates a runaway effect as the ions produce a conduction channel for more current and more free carriers. Avalanche breakdown can occur in both semiconductors and insulators and is usually irreversible as it forms a permanent conduction medium even after the field is removed. The breakdown oftentimes damages the material as rapid heating arises with the current.

As FET gate and channel contacts are within close proximity of each other, the electric fields produced by the gate will influence the channel contact junction behaviors. The electric field will cause the bands to bend at the junction between materials, potentially changing the barrier height, band bending rate, ideality factor, or other properties. Dealing with this often leads to many real world engineering complications and must be accounted for in device design. We must also be wary of assuming all FET device gating response is due to the bulk of the semiconductor alone, but instead recognize it is often a mix of bulk and contact characteristics.

2.1.2.1 Band Bending? (TODO)

TODO: MOSFET band bending?

2.1.3 Weak localization (TODO)

2.2 Ferroelectricity

Ferroelectric crystals will spontaneously polarize below a critical temperature, known as the Curie temperature T_C . Below T_C atoms will create naturally occurring dipoles as they shift to find the lowest overall energy state, sacrificing local electrostatic homogeneity to do so. At higher temperatures the atoms have more energy and space and generally prefer neutrality, forming a paraelectric material instead. When a ferroelectric is exposed to an electric field the dipoles shift to align with the electric field and will remain aligned when that field is removed. Paraelectric materials may form similar dipoles under the electric field but will return to their unpolarized state when the field is removed. Ferroelectrics have many practical applications, as the polarization can be used to enhance capacitors as a dielectric, hold a persistent electronic state, or modify other device properties.

2.2.1 Piezoelectricity and pyroelectricity

Piezoelectricity and pyroelectricity arise from non-linear behaviors in crystal structures [16]. There are 32 crystal classes that make up 3D crystals. Of those 21 are non-centrosymmetric, and 20 of the non-centrosymmetric groups form piezoelectric materials. Furthermore, 10 of those groups are polar, forming dipoles with the material. Crystals from these 10 groups are pyroelectric and possibly ferroelectric. All ferroelectrics possess pyroelectricity and all pyroelectrics are piezoelectric, but not all pyroelectrics are ferroelectric and not all piezoelectrics are pyroelectric. This encircling Venn diagram provides a way for easily screening possible ferroelectrics but also means ferroelectrics materials have other attributes. Appendix A shows a list of classes of each type and the corresponding space groups.

In piezoelectric crystals, mechanical motion and polarization are bound together. Applying mechanical strain or stress that shifts the atom locations in the material shifting the dipole orientation or displacement. This generates an electric field and the aggregate can be measured as a voltage across the material. Applied in reverse, an electric field will cause the dipoles within the materials to displace, and provided they are aligned, alter the the crystal size and shape. This has wide applications, giving rise to rapid, precise electric motors and sensors used throughout modern society [16].

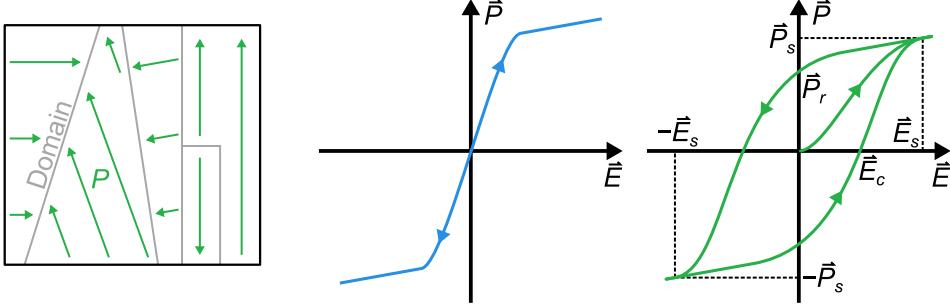
In pyroelectricity crystal polarization is conjoined with changes in temperature [16,17]. If we heat or cool a pyroelectric crystal, the crystal structure is altered slightly allowing it

to spontaneous polarize, or if already polarized, change to a new polarization fitting the new atom placement. This polarization produces a voltage across the bulk of the crystal, providing a method to measure this change and thus the changing temperature that drove the re-polarization. After the temperature is fixed the voltage will generally dissipate through leakage currents. This makes pyroelectrics suitable for changing measurements like thermal imaging cameras and energy generation, but poor for managing persistent states in modern digital electronics [16].

2.2.2 Domains and polarization

A ferroelectric material is differentiated from a pyroelectric by the ability to switch dipole orientation under an electric field, making ferroelectrics a subset of pyroelectrics. \vec{P} is the dipole moment per unit volume, in SI-units as Coulombs per square-meter (C/m^2). The majority of known ferroelectrics are insulating, limiting the movement of charge within the materials. Dipoles in a ferroelectric can have several different origins that depend on the elements and chemical bonds that make up the material. Electronic polarization comes from the electron cloud shifting around an atom so that local charge density forms a positive region around the nucleus and negative with the electron cloud. As electrons are very light this response is quite fast $\sim 10^{15} Hz$. Ionic polarization occurs when cations and anions displace slightly within the crystal to form dipoles. As the nucleus of the atom is much heavier this response is slower, on the order of $\sim 10^{13} Hz$. Polarized molecules may also rotate within a material to align with the field, known as orientation polarization. This is much slower, $\sim 10^7 - 10^9 Hz$, as the larger molecule is again heavier and the competing forces within the material may limit the motion of the dipole. Lastly, space charge polarization takes place when ions move through multiple crystal layers to create positive and negative crystal regions, $\sim 10^4 Hz$ [16]. The rate of the dipole movement can be used to characterize the type of dipole in a material and may limit a materials use in high speed electronics.

As an external electric field is increased the dipoles will move to align with the electric field to minimize the energy of the system. The minimum may include different regions of the materials with different dipole alignments, known as domains, shown in figure 2.4a. These domains often are formed at the defects in crystals such as a lattice mismatch or missing atom, and the dipole walls are typically atomically sharp as there are limited possible dipole configurations. For a crystal with all dipoles aligned in a single direction, an increasing opposing electric field will eventually make a dipole switch. From there the domain will begin to nucleate around the original dipole as the electric field continues to



(a) Ferroelectric crystal domains
(b) Paraelectric polarization
(c) Ferroelectric polarization

Figure 2.4: Polarization

(a) Ferroelectric domains and dipole orientation within a crystal. Polarization vs electric field for a (b) paraelectric and (c) ferroelectric. \vec{E}_c , \vec{E}_s , \vec{P}_s , and \vec{P}_r are the coercive electric field, spontaneous electric field, spontaneous polarization, and remnant polarization.

increase. This can persist until all the dipoles are aligned in a single direction, forming the maximum polarization of the material. This is the spontaneous polarization P_s , and occurs at E_s . A polarized material has excess surface charge on the opposing sides of the material. These charges serve to lessen the field within the material as they produce an electric field within the opposite direction, known as the depolarization field. The depolarization field will cause the dipoles to reorient as thermal fluctuations let the dipoles to find new local energy minimums. As the electric field is reduced to 0 from $\pm\vec{E}_s$ the depolarization field will force some domains to flip directions, but a finite amount will still remain polarized in the original direction as the remnant polarization \vec{P}_r . It is this polarization that gives ferroelectric many uses in low power electronics.

One important characteristic in determining whether a crystal is ferroelectric is the transition to paraelectric above the Curie temperature. Above T_C the temperature fluctuations are enough to destroy any preference the electric charges to remain in a non-neutral configuration. An external electric field may still polarize charges but they will return to electrically neutral when the field is removed. From an energy perspective, two or more local minimums appear for the dipole charges that are offset from each other. Switching the polarization direction requires the electric field must be large enough to overcome this energy barrier, known as the coercive field strength \vec{E}_c . Figures 2.4b and 2.4c show the respective polarization vs electric field behavior for a paraelectric and ferroelectric dielectric.

One of the largest hindrances to ferroelectrics in many applications is the susceptibility

of ferroelectric films to aging and fatigue. Aging is the slow changing of a material's characteristics over time, while fatigue takes place under high electric field. Both take multiple forms and can have similar effects, though the mechanisms are still areas of active research [18]. Crystals may switch to another phase so that the overall stoichiometry does not differ but the elements shift to form a new space group that has a different remnant and spontaneous polarization. Ionic dipoles can form within a crystal that provide a counter electric field within the material or rotate slowly to depolarize. Charged ions, vacancies, or electrons may diffuse through the crystal and later become pinned at domain walls, grain boundaries, or interfaces between materials [19].

2.2.3 Phase transitions

Phase transitions in ferroelectrics is usually modeled with the Landau phenomenological approach, or Landau–Devonshire theory. [16, 20] We can write the free energy F of a ferroelectric in the mean-field approach as

$$F = F_0 + \frac{\alpha}{2}P + \frac{\beta}{4}P^2 + \frac{\gamma}{6}P^6 \dots - EP \quad (2.9)$$

where α , β , γ , etc are the Landau parameters, F_0 is the free energy density of the disordered (high temperature) phase near the transition, and E the external field. In the paraelectric phase the Hamiltonian must be invariant under a transformation from P to $-P$, forcing equation 2.9 to only contain even powers of P . The Landau parameters are pressure and temperature dependent, though usually only the temperature dependence in α is considered. As α should switch sign at the transition, α is generally taken as linear in T near the transition temperature, taking on the form $\alpha = \alpha_0(T - T_0)$, where T_0 is the Curie–Weiss transition temperature ($T_0 \leq T_C$). Equation 2.9 can be modified to fit thin film ferroelectrics by including the boundary conditions [21], but we will keep to the simpler, bulk description and to only three terms in the expansion. To find the local minimums in the free energy we take the derivative

$$\frac{\partial F}{\partial P} = \alpha P + \beta P^3 + \gamma P^5 - E = 0 \quad (2.10)$$

We set $E = 0$ to look at the system in the simplest scenario, without external fields, giving

$$P^2 = \begin{cases} 0 & \text{Paraelectric} \\ \frac{-\beta \pm \sqrt{\beta^2 - 4\alpha\gamma}}{2\gamma} & \text{Ferroelectric} \end{cases} \quad (2.11)$$

We can then look at two separate cases based on the sign of the second term β .

2.2.3.1 First-order, $\beta < 0$ and $\gamma > 0$

For F to remain positive while $\beta < 0$ we need the next term $\gamma > 0$; we will continue to neglect higher order terms as they are increasingly small. As β is negative, we can drop the “ $-$ ” term in equation 2.11. Above T_1 the free energy will have no minimums outside $P_s = 0$ as the term inside the square root becomes negative. Then

$$P_s = \begin{cases} \pm \sqrt{\frac{-\beta + \sqrt{\beta^2 - 4\alpha_0\gamma(T-T_0)}}{2\gamma}} & T < T_0 \\ 0, \pm \sqrt{\frac{-\beta + \sqrt{\beta^2 - 4\alpha_0\gamma(T-T_0)}}{2\gamma}} & T_0 < T < T_1 \\ 0 & T > T_1 \end{cases}$$

where T_1 is the ferroelectric temperature limit. For $T_0 < T < T_C$ the two non-zero terms have lower free energy than $P_s = 0$, while for $T > T_C$ the absolute minima occurs at $P_s = 0$. We can find the Curie temperature T_c by setting $F(P_s = 0) = F(P_s = \pm\sqrt{\cdot}) = 0$ and solving

$$T_C \approx T_0 + \frac{3\beta^2}{16\alpha_0\gamma}$$

We can do the same for T_1 as $F(P_s) = 0$

$$T_1 = T_0 + \frac{\beta^2}{4\alpha_0\gamma}$$

Allowing us to confirm $T_0 < T_C < T_1$. [16, 20] Figure 2.5a shows the free energy as a function of electric fields; as well as 2.6b the progression of the order parameter P_s as T is increased from T_0 , T_C , to above T_1 . Adding the electric field back in will create an asymmetry in the free energy and increase P_s .

2.2.3.2 Second-order, $\beta > 0$

For the second case we assume $\beta > 0$. When $T > T_0$ we neglect the β and higher terms as P is small, there can be only one minimum in equation 2.10 and the shape of F is parabolic. For $T < T_0$ we start with equation 2.11 and Taylor expand the term under

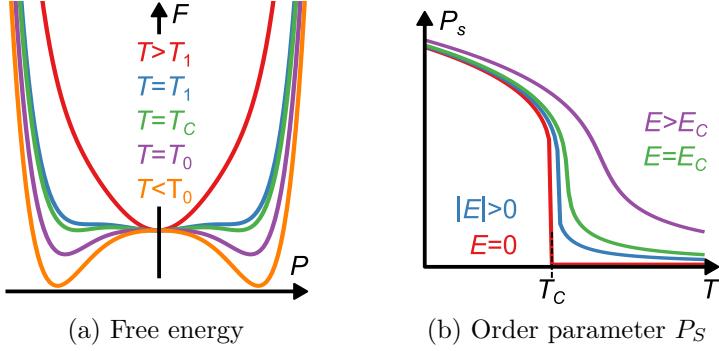


Figure 2.5: Landau first order transition

- (a) The free energy as a function of polarization at constant temperature and zero electric field for a first order transition. As T increases the minimums at finite polarization increase and disappears above T_1 . (b) The value of the parameter P_s as a function of increasing temperature and constant electric fields.

the square root, noting $P^2 > 0$ this gives

$$P = \begin{cases} 0 & T < T_0 \\ \sqrt{\frac{\alpha_0(T_0-T)}{\beta}} & T > T_0 \end{cases} \quad (2.12)$$

we can also find this result dropping the γ and higher terms in equation 2.9. [16, 20] Below T_0 then F becomes quartic in shape with a double well. Figure 2.6 shows the free energy above and below T_0 , and the behavior of the minimum(s) in F with increasing temperature. Above the critical field E_c the minimum polarization transitions from discontinuous to continuous.

2.2.4 Ferroelectric field-effect transistors (FeFETs)

Ferroelectric field-effect transistors (FeFETs), 1T cell, seek to keep a persistent on/off binary state. A ferroelectric dielectric replaces the typical oxide gate dielectric of a (MOS)FET, using the gate to switch the polarization of the crystal, figure 2.7a. The polarization of the material should maintain an electric field along the junction with the semiconductor, providing the normal enhancement or depletion of the channel. As a normal FET, a conducting channel is “on” and conversely, current reduced below a threshold can be considered “off.” While as the polarization persists the channel state should remain on or off, sustaining it without power. This has the potential to replace or

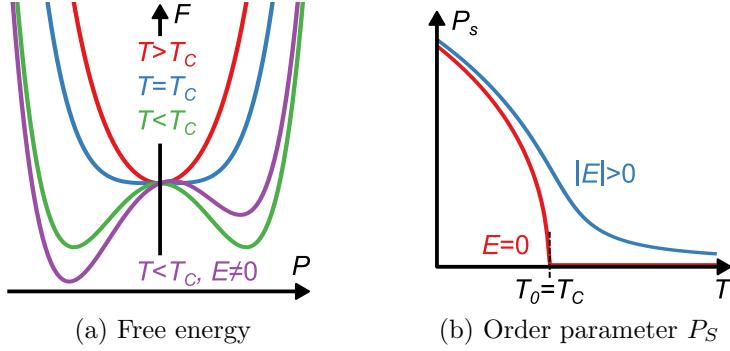


Figure 2.6: Landau second order transition

- (a) The free energy as a function of polarization at constant temperature for a second order transition. All electric fields are zero except for the line indicated. (b) P_s as a function of increasing temperature and constant electric fields.

augment DRAM in computers and low power devices, reducing active energy consumption or possibly allowing electronics to turn on without a lengthy start. FeFETs also offer the possibility of faster switching than traditional capacitor-based RAM [22].

The presence of dipoles within the dielectric layer produces a hysteresis in the current-gate voltage relationship of a FET, figure 2.7b. Increasing the gate voltage to the “on” state of the creates an electric field across the ferroelectric. The electric field increases the carrier concentration within the semiconducting layer, forming a channel between the source and drain contacts [23]. Once the coercive electric field is reached, the dipoles begin to align, creating a larger voltage drop across the ferroelectric dielectric, figure 2.7d. When the voltage across the gate is reduced to 0 V the polarization continues to provide an electric field at the surface and maintaining the conduction channel and the “on” state, figure 2.7c. Further decreasing the gate voltage to the “off” state subsequently polarizes the dielectric in the opposite direction, figure 2.7e. The electric field of the gate depletes the channel of carriers, giving the desired diminutive drain current. When the gate voltage is again returned to 0 V the polarization preserves the depletion field within the channel until the gate is switched to “on” again, figure 2.7f [22, 24]. For both the “on” and “off” states the multiple factors causes the polarization to decay once the electric field is reduced below the threshold of the coercive field, eventually leading to the depolarization of the device.

One of the piratical challenges of FeFETs is increasing the longevity of the polarization state. Often thermal energy may cause the polarization to relax over time as the dipoles

reorient so materials must be chosen to minimize this effect. Likely the largest cause of long term polarization degradation is leakage current through the gate [22]. A common modification of FeFETs is to include a dielectric layer between the ferroelectric and semiconductor to improve the interface between the two (MFIS-FET) and reduce leak currents higher energy electrons from damaging the ferroelectric. Another is to add a floating metal and dielectric layer forming a metal-ferroelectric and channel (MFMIS-FET) to redistribute the electric field evenly over the channel and reduce the effect of domain formation within the ferroelectric. Improving film quality to reduce trapped charges, increasing the metal-ferroelectric Schottky barrier, and using a high-k dielectric can be used to further reduce leak currents in a FeFET [22]. Another common challenge with producing a commercial FeFET RAM is fatigue in the ferroelectric layer as conventional RAM is expected to be able to switch $\sim 10^{12}$ in its lifetime [22].

2.2.5 Ferroelectric tunnel junctions (FTJs)

Ferroelectric tunnel junctions (FTJs) are an alternative to FeFETs being explored for data storage [16]. They consist of a thin ferroelectric in between two metal electrodes, where the ferroelectric polarization is along the axis of the metal-ferroelectric-metal structure, figure 2.8a [25, 26]. The polarization direction will produce a net positive and negative charge distribution in the ferroelectric along the respective electrode junction, figure 2.8c. The electrons in the metal will adjust to screen out the charge at the junction, all together producing a varying potential across the junction. When a voltage is placed across the FTJ some electrons will tunnel though the barrier forming a measurable current. The voltage produces an electric field across the ferroelectric, and if large enough will cause the polarization to switch. The switched polarization will alter the potential across the two junctions and the tunneling current. By measuring the current at a particular voltage it is possible to determine which direction the polarization is orientated giving rise to a binary state that can be used to store information. If the voltage is kept below the coercive field the FTJ will act similar to a non-ferroelectric junction allowing the current state to be read out without being overwritten. Figures 2.8e and 2.8f show two possible resistive switching behaviors, the first with symmetric electrode-ferroelectric interfaces, the second with asymmetric interfaces.

2.2.6 Polar metals

Polar metals, metals that contain dipoles, were first proposed in 1965 [27] to explain the structural transition in V_3Si but only recently seen experimental verification in $LiOsO_3$ [28]. Polar metals must show a continuous phase transition from non-polar to polar at their Curie temperature [29] breaking inversion symmetry. As metals have an abundance of free charge carriers, the electric fields within the material are screened, suggesting that metallicity is the antithesis to both prerequisites in the traditional definition of ferroelectricity. The carrier screening suppresses long-range coulomb interactions necessary for dipole formation and the fields to orient the dipoles. $LiOsO_3$ was shown to shift from $R\bar{3}c$ to $R3c$ at $T = 140\text{ K}$ by the shifting of the Li ion [28], forming a similar structure to several insulating ferroelectrics, and accompanied by several changes in the optical and electronic properties attributed to the dipole formation [28, 30–32]. Similar dipole formation has been seen in $Ca_3Ru_2O_7$ [33], $BaTiO_3$ [34], $LaAuGe$, $LaPtSb$ [35] and other materials. Ferroelectricity was reported in 2-3 layer WTe_2 [36], a 2D Van der Waals chalcogenide metal. The 2D material was stacked between two insulating layers of hexagonal Boron Nitrite (hBN) in a double-gated FeFET. The gating response showed a clear transition behavior in WTe_2 conductivity while the thin graphene layers used to gate the material showed a hysteresis in their conductivity, both are attributed to the polarized electric field from the WTe_2 . Later measurements demonstrated the existence of ferroelectric domains with bulk crystals and thin films [37].

The free carriers in a polar metal may move to the edges of the material, to the excess electrical charge normally found on the surface of insulating ferroelectrics, instead producing a neutral charge distribution. This freedom can remove the depolarization field found in a typical ferroelectric [33] possibly extending the polarized state of the crystal. The charge screening also lowers the system energy from domain walls of different dipole orientations in close proximity, allowing for opposing polarization domains to form 1nm apart with only 10s of meV potential difference [38]. Potential polar metal applications include reducing the size of ferroelectric capacitors [39], FeFETs [36], tunnel barriers [40], and nonreciprocal charge transport [41].

2.2.7 FeFETs with ferroelectric channels

TODO

2.3 2D materials

Started by the discovery of graphene, 2D materials have become a large area of research due to their unique qualities and ability to integrate with conventional electronics. Typically defined by layered nature, many can be mechanically exfoliated to small crystals or grown as thin films. The sharp reduction in one dimension often provides additional fundamental electronic properties from the bulk that can be exploited. Chalcogenides, typically sulfides, selenides, tellurides; often form 2D materials with Van der Waals inter-layer bonding with a semiconductor bandgap. Some of the most studied of these compounds are the transition metal dichalcogenides with the stoichiometry MX_2 , where M is a transition metal such as Mo or W and X a chalcogen S , Se , or Te .

2.3.1 Trapped charge in 2D FETs? (TODO)

2D FETs have a high in-plane to out-of-plane ratio, as devices can be made on several nanometer thick films or flakes, forcing surface properties to play a large role in the behavior of a device. This often manifests in a hysteresis of the source drain current to changes in FET gate voltage, the origin of which is still an area of active research.

TODO

Fermi pinning?

2.3.2 In-Se compounds

Indium-Selenium together can form a variety of binary compounds ranging with completely disparate properties. Depending on the temperature and prevalence of each element it is possible to get different In-Se alloy growth and structure. Figure 2.9 shows a phase diagram compiled from various experimentally published sources up to 2003 as well as calculations. The plethora of compounds, and the sensitivity to both temperature and concentration, makes growth of a single uniform compound harder to control. Alternate configurations of the same stoichiometry have made past literature somewhat inconsistent as each configuration may have unique properties while the specific configuration was not reported.

2.3.2.1 In_2Se_3 polymorphs in literature

In_2Se_3 is perhaps one of the most complicated of the In-Se compounds. Currently there are thought to be α , β , γ , δ , and κ stable phases of In_2Se_3 , in addition to α' , β' , and

| Polymorph | Structure | Space group {number} |
|-----------|-------------------|--|
| α | Rhombohedral [3R] | $R\bar{3}m \{160\}$ [44, 51–55] (or $R\bar{3}m \{166\}$ [56–58]) |
| | Hexagonal [2H] | $P6_3mc \{186\}$ [44, 55] (or $P6_3/mmc \{194\}$ [56]) [59] |
| β | Trigonal [1T] | $P\bar{3}m1 \{162\}$ [44] |
| | Hexagonal [2H] | $P6_3mc \{186\}$ [44] (or $P6_3/mmc \{194\}$ [60]) |
| | Rhombohedral [3R] | $R\bar{3}m \{166\}$ [52, 53, 55, 56, 58, 60, 61] |
| γ | Hexagonal | $P6_1 \{169\}$ [44, 62–64] (or $P6_5 \{170\}$ [44, 59, 62, 65]) [60, 66] |
| δ | Trigonal | $P\bar{3}m1 \{156\}$ [60] or $P3m1 \{164\}$ [56, 61] |
| κ | Hexagonal | [45, 46, 46, 47, 67, 68] |
| α' | Rhombohedral | $R\bar{3}m \{160\}$ [61] |
| β' | Monoclinic | $C2/m \{12\}$ [53] |
| | Rectangular | [69, 70] |

Table 2.1: In_2Se_3 polymorphs

| Polymorph | Structure | Spac group |
|---------------|--------------|------------------|
| β | Hexagonal | $P6_3/mmc$ [71] |
| γ | Rhombohedral | $R\bar{3}m$ [71] |
| ε | Hexagonal | $P6m2$ [71] |

Table 2.2: $InSe$ polymorphs

γ' metastable phases [43]. Ref [44] is likely the most comprehensive single study of the α , β , γ phase structures currently reported. α , β , δ and κ are 2D layered Van der Waals materials while $\gamma - In_2Se_3$ is 3D in nature. α and β are semiconductors and have multiple sub-polymorphic structures with different layer stacking. $\kappa - In_2Se_3$ is typically formed by doping with impurities like Ag, Sb, Te, and Zn, and is similar to the α phase [45, 46, 46, 47]. It is possible to transform among the different polymorphs using pressure, heat, electric potential, or other techniques. This has somewhat added to discrepancies in the literature as one type will be determined then the properties of the material measured after or during annealing when the material changes phases. α' was made by cooling β' [48]. β' forms under pressure from α [49] or at lower temperatures from β [48]. Last, γ' was formed from heating the β polymorph [50]. Table 2.1 lists the different polymorphs reported in literature and the identified space groups.

TODO: Ferroelectricity in In_2Se_3 ? (TODO, maybe leave for later chapter)

Maybe:

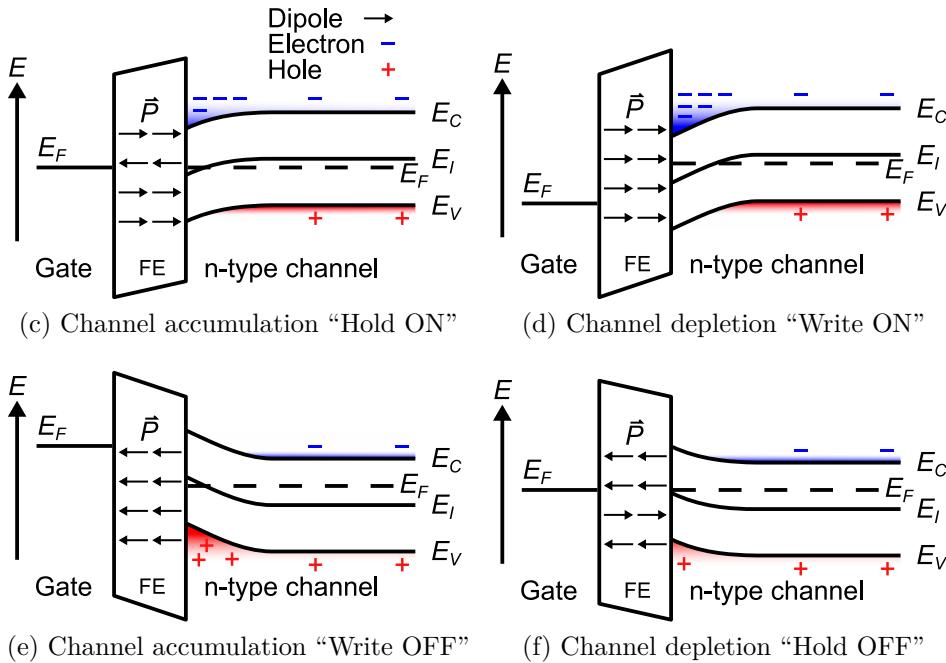
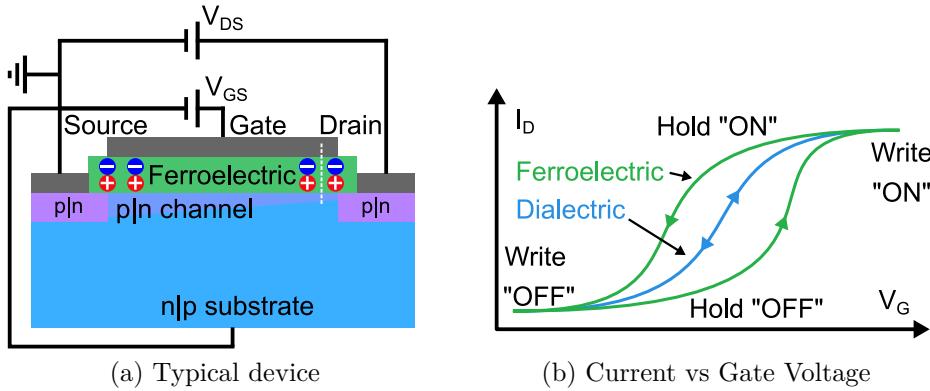


Figure 2.7: Ferroelectric field effect transistors

(a) A typical FeFET device. (b) Source-drain current of the FeFET while increasing the gate voltage from negative to positive and back, a typical FET dielectric response without the ferroelectric deviation is shown in the center. Simplified energy band diagram of the gate-ferroelectric-channel matching the cross section in (a) for "hold ON" (c), "write ON" (d), "write OFF" (e), and "hold OFF" (f) stages of the FeFET show in (b). E_F , E_c , E_I , E_V are the Fermi energy, conduction band, intrinsic band, and valance band respectively.

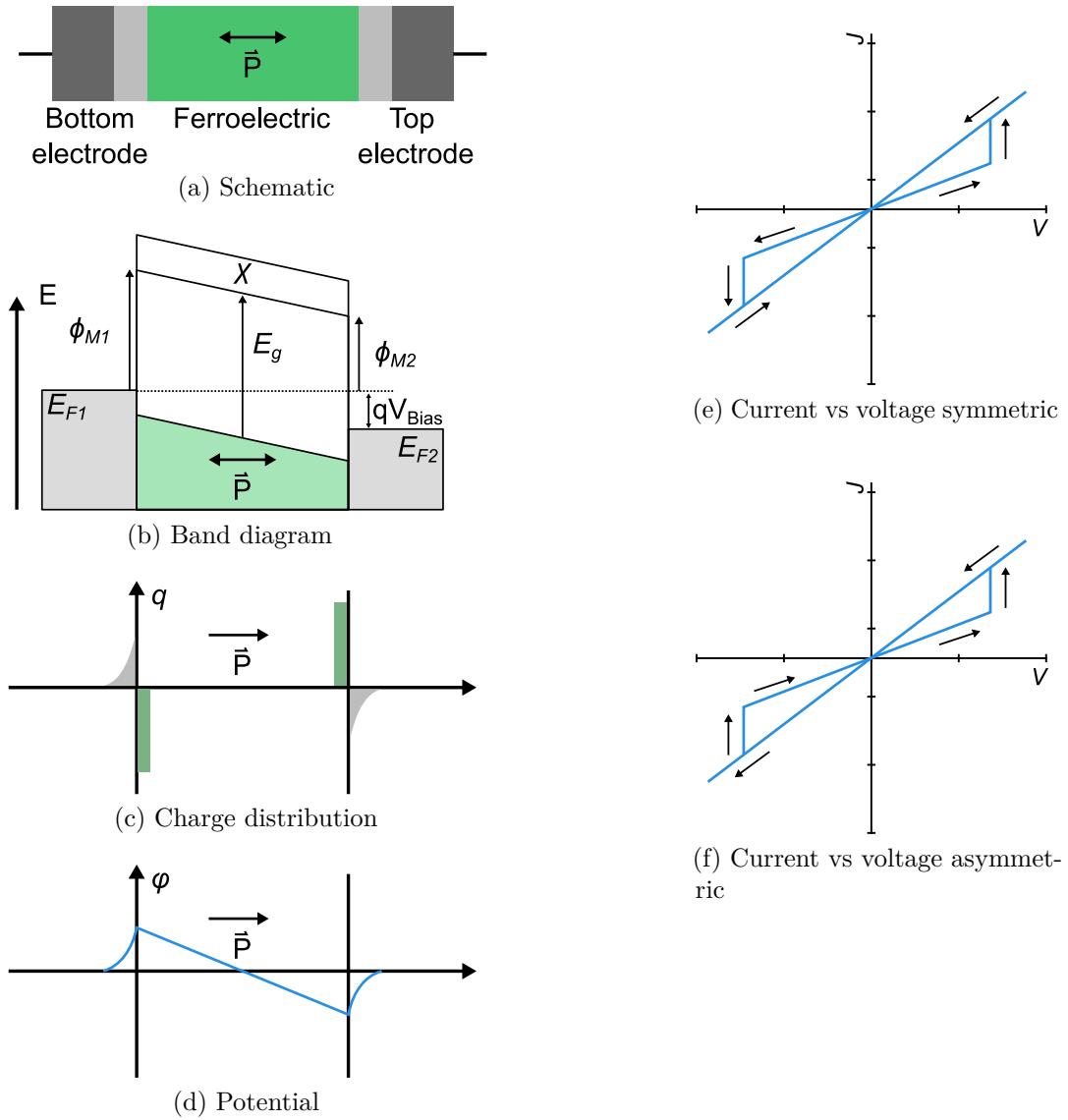


Figure 2.8: Ferroelectric tunnel junctions

FTJ schematic (a) with top and bottom electrodes and depleted regions. Corresponding upward biased band diagram (b) where q is the fundamental charge, V_{bias} is the bias across the electrodes, E_g is the ferroelectric band gap, E_F the Fermi energy, χ is the electron affinity, ϕ_M is the barrier height. (c) charge distribution and (d) potential with the FTJ in an upward polarization. Current density vs voltage of a FTJ with (e) symmetric (f) asymmetric electrode-ferroelectric interfaces.

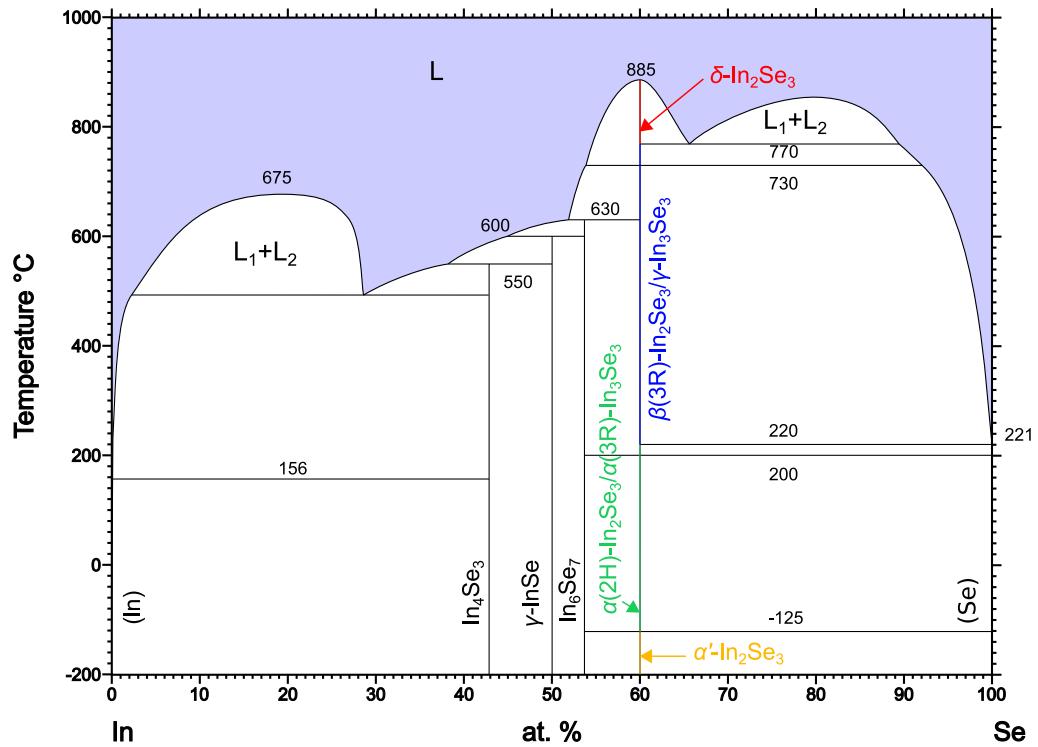


Figure 2.9: In-Se alloy phase diagram.

The various Indium-Selenium compounds grown from literature using both experimental and calculated data. Compiled by ref [42].

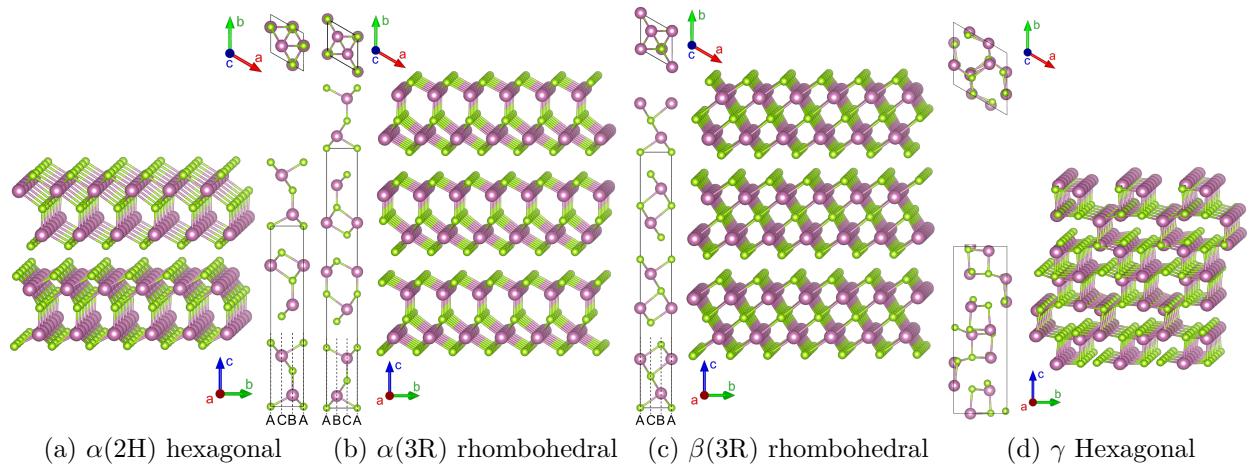


Figure 2.10: In_2Se_3 crystal structure

α ($2\text{H}-P6_3mc$) [51], α ($3\text{R}-R\bar{3}m$) [51], β ($3\text{R}-R\bar{3}m$), and γ ($P6_1$) crystal structures.

Chapter 3 |

Sample fabrication and measurement methods

3.1 Introduction

The introduction of exfoliation of crystals using adhesive tape has spearheaded a boom in 2D material research and driven the development of new techniques to explore these materials. 2D crystals are typically manufactured in one of two methods: films grown on premanufactured substrates or exfoliated flakes from van der Waals crystals. Films are sought for commercialization of materials as they can be incorporated into large-scale manufacturing processes while insuring a level of uniformity and reproducibility. Exfoliated crystals are typically seen in more in initial material development and characterization as they are often easier to produce and faster to work with on small scale device manufacturing. By growing the crystal in isolation, the parameters of the substrate lattice are removed from the development process of the crystal, reducing many complications seen in film growth. Due their self-contained nature, flakes are easier to manipulate when developing a new process. Flakes may additionally be stacked in layered heterostructures to create devices with more unique properties, including interface effects. Advances in flake devices often drive development of film manufacturing to incorporate the 2D crystal properties into commercial devices.

Both flake and film manufactured devices follow similar processes. Films grown on a substrate are covered with a protective resist polymer. The polymer is patterned using lithography to leave only the desired material covered. The remaining resist is etched away using a plasma etch then the polymer is removed. The film and substrate is again covered with a protective polymer and patterned with future metal contact areas now exposed. Metal is evaporated onto the surface to adhere to the film and

substrate wherever resist was removed. The polymer is dissolved taking excess metal with it leaving only desired metal leads. Flakes are exfoliated using tape and placed onto a substrate. The flake is covered with a protective resist and patterned for contacts. In the same manner as the film, the metal is then deposited and unwanted metal then removed. Figure 3.1 shows a overview of the two different processes while the details of each are given below.

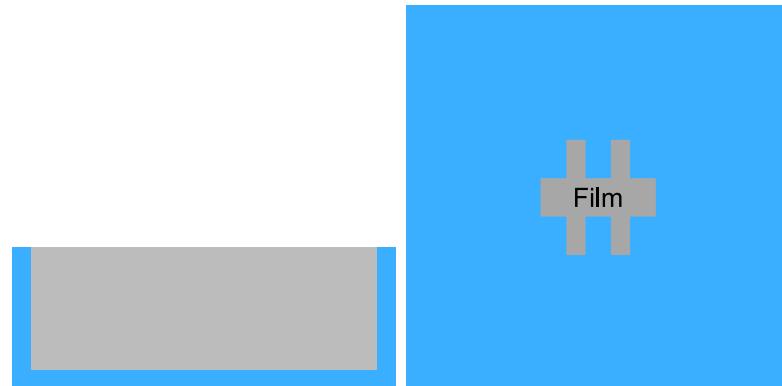
3.2 Flake generation

3.2.1 Alignment marker wafer chips

Before fabricating any devices to test materials we needed a platform to work on that would make it easy to find flakes and manufacture devices. For this 4 inch wafers of $500\mu m$ phosphorus doped silicon with $300nm$ of thermally oxidized SiO_2 was chosen as a substrate (purchased from Si-Tech, <100> thermal oxide allowed us to construct a backgated field effect transistor. The substrate was polished for better adhesion of deposited flakes. Using standard photolithography (see 3.3.1) we patterned the surface with a $\sim 5nm$ thin layer of titanium for adhesion then $\sim 35nm$ of gold. The metals were laid out with a repeating pattern of numbers and lines to easily identify the location of a flake on the substrate when moving between tools. We spun a layer of PMMA resist over the substrate then diced the wafer $8mm$ square chips with a ADT 7100 ProVectus Dicing Saw. This allowed us to make many devices per wafer while customizing their orientation and pattern for each flake. The resist was then removed from the chip using acetone, 2-isopropanol, and deionized (DI) water then dried using a nitrogen blow gun. To remove any residue organics we soaked the chips in Nano-Strip (sulfuric acid and hydrogen peroxide compound, VWR) for 10 minutes, rinsed in DI-water, then repeated the initial solvent clean. After several devices experienced dialectic breakdown across the SiO_2 we changed the residue clean to an oxygen surface treatment. This was done in a M4L Plasma Processing System with 300 sccm oxygen, 100 sccm helium, at 500mTorr of pressure, and 100W for 1 minute.

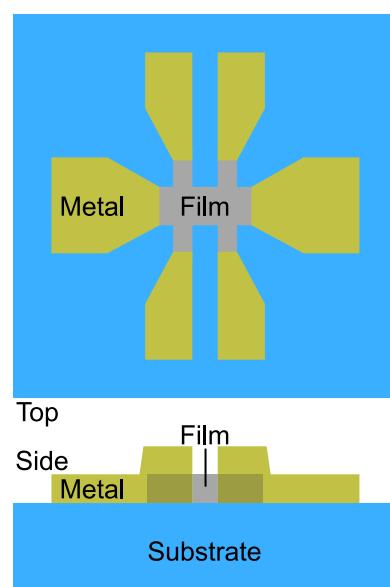
3.2.2 Mechanical flake exfoliation

Flakes of van der Waals materials can be mechanically exfoliated using Scotch 3M Transparent Tape to break the weaker bonds. A piece of tape is pressed into a larger crystal of the material then peeled off, resulting in a few smaller crystals adhered to the

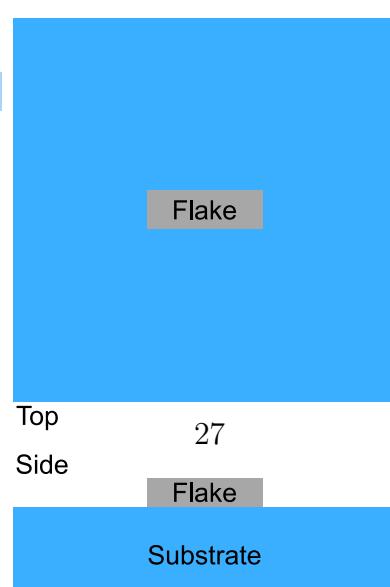
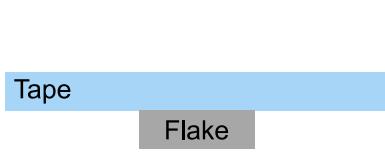


(a) Film on substrate

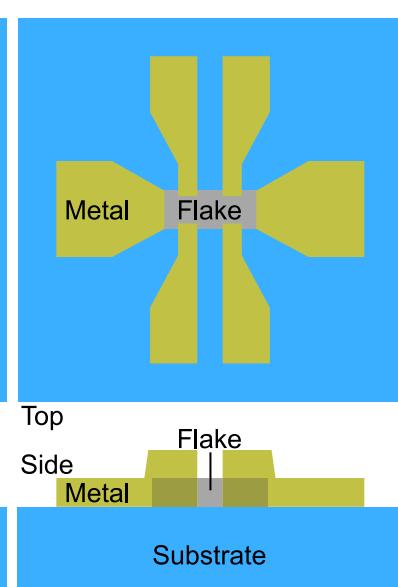
(b) Film etched



(c) Film with leads



27



27

TODO: tape figure, alignment mask? AFM heights



(a) Tape exfoliation

Figure 3.2: Flake manufacture

(a) Starting crystal, tape with thin flakes of crystal, and final substrate with flakes.

tape. The tape is then folded over itself so the crystals are pressed into different areas of tape, ideally without coming into contact with each other. The tape is then peeled apart, breaking the weaker van der Waals bond, so that the crystals are pulled apart into smaller crystal layers. This process is repeated several times to provide a region roughly 8 to 10mm in diameter of crystal coverage. This region is then pressed into a fresh region of tape, providing a new exposed surface of crystals with less tape residue. This can be repeated to thin the layers of crystal repeatedly until the desired thickness is reached. The tape and crystals are then placed on a cleaned aliment marker chip, ideally maximizing the amount of crystals within the center of the chip. The tape is lightly pressed into the chip so that the crystals would be in contact with the surface of the chip. To promote adhesion to the surface, the chip can then be heated for 1-2 minutes at 100C to improve van der Walls adhesion to the substrate. [72] The chips are then allowed to cool and the tape peeled off, leaving a freshly cleaved surface on both the substrate and top of the flakes.

After exfoliation we scanned each chip for flakes using a Nikon Eclipse LV150 microscope. We chose 300nm of thermally oxidized SiO_2 to increase visibility of 2D materials under white light. [73] Flakes choice was optimized for uniformity, thinness, and lateral sizes large enough for photolithography processing. A Bruker Icon Atomic Force Microscope was used to measure flake height and develop a thickness color-code to compare new exfoliated flakes against.

3.3 Photolithography

Photolithography is a common technique used by industry and academia alike. In most variants of photolithography, a series of photosensitive polymers, or resists, are spread over a surface then exposing the polymer to light to change the chemical makeup of the polymer. This can be done by spinning a solution of the desired polymer, dissolved within a compatible solvent, at high speeds over a substrate. The solution is dripped on the substrate either statically or dynamically, under a slower rotation. The substrate is then rotated at high speeds until the desired thickness of polymer is left on the surface, the excess being flung off the substrate edges. The solvent can then be removed by baking the substrate and polymer for a short time until a desired durability is achieved. After exposure the resist is then removed by soaking the substrate in a chemical developer. Developer selection must take into account any chemistry between the developer and flake material as some developers can react with the exposed material. For negative resists, light exposed regions of polymer are removed when developed, positive resists will only have non-exposed regions removed. For devices that change based on the flake, the resist pattern is generated on a computer and then written by a moving laser to fit the device dimensions. In commonly used patterns, a mask of chrome on quartz is prefabricated. The mask is moved over the flake then the entire surface is flooded with light at once, exposing the regions with the desired resist pattern. We typically choose a multiple layer resist stack as allowing the bottom layer dissolve long enough to undercut the top allows for easier liftoff when removing evaporated metals (See 3.5). Resist can also be used to protect part of a sample when etching allowing a patterned etch of the substrate or testing device.

3.3.1 LOR/SPR stack

The LOR/SPR negative resist stack is easy to use and allows for high resolution patterns down to $2\mu m$. Before any resist is added the substrate is given a dehydration bake of $115C$ for $60s$ to remove any water. A layer of LOR-2A is statically deposited as the first layer of the stack. The substrate is then spun at $4000RPM$ for $45s$ reducing the LOR-2A to a $\sim 200nm$ thick coating. [74] Finally we bake it at $180C$ for $60s$ on a hot plate to remove some solvent. Next a layer of SPR-3012 is dynamically dispensed at $900RPM$. The substrate is then sped up and spun again at $4000RPM$ for $45s$ flattening the SPR-3012 to $\sim 1.3\mu m$ thick. [75] This is then baked for $95C$ for $60s$ on a hot plate. The resist stack and flake is then exposed using a MA/BA Gen4 or Gen2 Contact Aligner

(SUSS MicroTec) with 54mW of light. The patterned resist is then developed for 60s in Microposit CD-26 (Tetramethylammonium hydroxide 1-5% and water, Shipley).

Table 3.1: Lithography resists

| Resist | Developer | Liftoff |
|----------|-----------|--------------------|
| LOR-2A | CD-26 | Remover-PG |
| SPR-3012 | CD-26 | Remover-PG |
| PMMA | MIBK | Acetone/Remover-PG |
| SF6-slow | 101A | Remover-PG |

Resists, developers, and liftoff solvents used in various lithography processes.

3.3.2 PMMA/PMGI/SPR stack for alkali-sensitive materials

Some chalcogenides react with alkali developers such as CD-26 [76] so we developed an alternate photolithography resist stack with a solvent used to develop the layer closest to the material. First a layer of Polymethyl methacrylate (PMMA-2A) (Microchem) is statically deposited, spun at 2500*RPM* for 45s to give a $\sim 600\text{nm}$ layer, then baked at 180°C for 180s. [77] Next a layer of PMGI SF6-slow is dynamically spun at 900*RPM*, then 4000*RPM* for 45s to reduce the thickness to $\sim 300\text{nm}$, and baked at 180°C for 60s. [78] Finally, a top-coat of SPR-3012 is dynamically dispensed at 900RPM. This is then spun at 4000*RPM* for 45s for a thickness $\sim 1.3\mu\text{m}$ and baked for 95°C for 60s. The SPR-3012 is then exposed using a MA/BA Contact aligner with 54mW of light (peak 365nm), developed for 60s in in Microposit CD-26 from Shipley (3.3.1), then rinsed in water. The PMMA and SF6 under-layers are exposed for 30 minutes in a Deep UV (peak 270nm, OAI Deep UV Flood Exposure) at 5.3mW ($\sim 9.5\text{ J}$). The SF6 is developed in 101A developer (Microchem) for 90s then rinsed in water. Finally the PMMA is developed for 10 minutes in methyl isobutyl ketone (MIBK) and a trace amount of water. The substrate is moved though the water for 5 – 10s then to the MIBK, where a thin bubble of water continues to adhere to the resist near the exposed region. After allowing the water to sit on the sample for another 10 – 30s, the substrate is gently shaken back and forth with tweeters to dislodge the SPR layer from the top of the sample. This prevents the SPR from later partially peeling up then adhering to the substrate, ruining the lithography pattern. The sample is left in the MIBK for another 5 – 10m to develop the PMMA down to the substrate. The MIBK is then removed with 2-propanol.

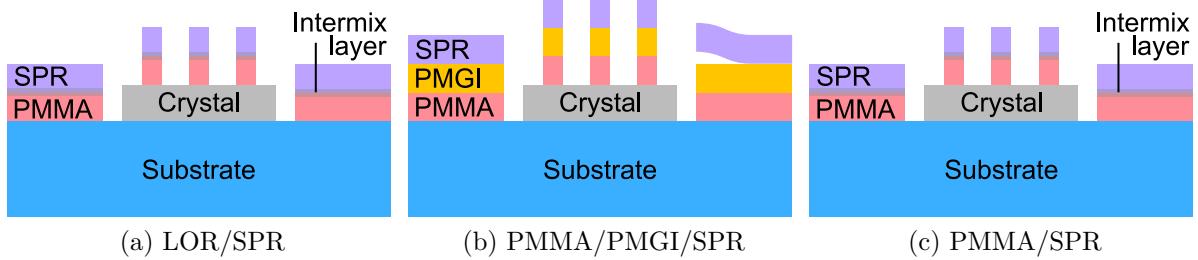


Figure 3.3: Resist stacks

Three of the resist stacks used in device manufacture. (a) LOR/SPR used in most of our devices, (b) PMMA/PMGI/SPR used in devices with alkali-sensitive materials, (c) PMMA/SPR alternative stack used initially in some of our alkali-sensitive materials before the previous stack was developed.

An alternate version of this process used a thicker PMMA (6A) with SPR-3012 on top. Because the SPR uses a PMMA-compatible solvent (Cyclopentanone) the two layers would intermix and form a layer that was unable to be dissolved in either developer. This was removed by ashing the layer for 515 seconds in the M4L with 250 sccm oxygen, 50 sccm helium, 500mTorr pressure, 450W power. This process varied greatly depending on polymer uniformity and location of device on the substrate so later devices included the PMGI SF6 layer to eliminate the inconsistency.

3.4 Thin filament shadow mask

As an alternative to lithography, we used an all-dry quartz filament shadow mask for metal evaporation (3.5). This allowed us to test contact resistance of an underlying material without introducing the polymers, chemicals, and processing to the material that may damage the surface or leave a residue between the material and metal contacts. We heated two quartz rod ends with an acetylene torch until semi-molten. We then lightly touched the two ends together and quickly pulled the ends apart within the flame. If done correctly, this produced several $2 - 10\text{cm}$ long strands of quartz that were $< 2\mu\text{m}$ in diameter. These were identified under a fluorescent light by their thread-like behavior, losing most stiffness and free to float in the air when $\lesssim 2\mu\text{m}$ in diameter. These filaments were then caught on glass forks by dragging the filament across the opening and snapping the end attached to the quartz rod. The forks were cut to fit over the sides of our sample

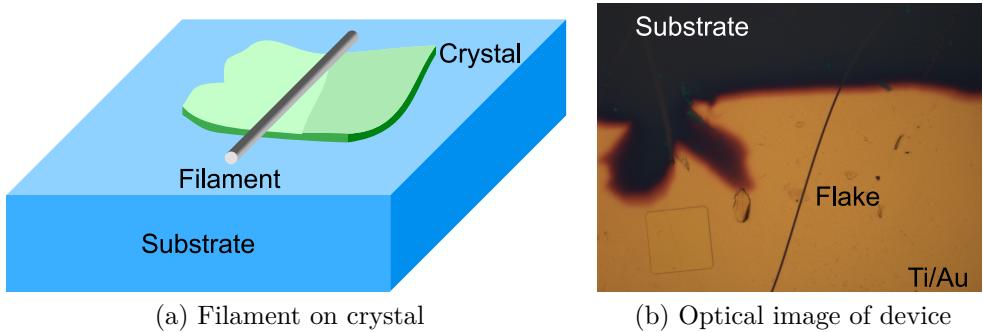


Figure 3.4: Filament device

(a) Filament shadow mask and (b) flake filament device made to test dry contact process.

chip substrates and reinforced with metal for durability. The sample chip was attached to a glass slide with double-sided tape. These filaments were then draped over the sample material with the glass fork. The ends of the filament were then cut with a tungsten needle and the glass fork removed. The filament could be adjusted by pulling it gently with a thin copper wire until it was in place and laying flat against the surface. This often caused the quartz to snap so the range of movement was limited to within a few 10s of microns from where it started. Once the filament was maneuvered it was fixed in place by wrapping the ends in Teflon tape that wrapped around the glass slide. Teflon tape was chosen as it is unlikely to scratch the material and has no adhesive that would cause the filament to move when securing it. The tape was also used to reduce the exposed area so only a small region around the material was included and reduce the risk of a short between the two sides. We found a filament less than $.5\mu$ tended to cause a short between the two sides while greater than $3\mu m$ would not sit flush against the surface. Metal choice is similarly important as certain metals like indium tended to “wet” across the surface and short at any diameter.

3.5 Metal evaporation and liftoff

Metal deposition was done using the Lab-18 Thin Film Deposition System (Kurt J. Lesker Co.). This was used to add contacts to a lithography-patterned flake by covering a substrate with layers of metal. We used electron beam evaporated titanium and gold for the uniform deposition and high conductivity. First $\sim 5nm$ of titanium was deposited at $\sim 1\text{\AA}/s$ as titanium adheres well to SiO_2 . Next a layer of $35 - 50nm$ of gold was evaporated at $\sim 1\text{\AA}/s$ on top of the titanium. The gold provided a highly conductive

protective layer that was inert in atmosphere and safe to use when wiring samples.

The Lab-18 Thin Film Deposition System also had an in situ ion source that could be used to clean and roughen the surface of a material before deposition occurred. A typical process used 10sccm of argon gas flowed over a metal coil with 2.5A of emission current and 150V between the coil and the substrate. The ion source is undirected which caused trace amounts of iron from the chamber itself to be knocked loose and deposited on the surface of the sample.

To remove excess metals from the substrate the lithography resist was then removed through a 'lift-off' process. The resist stacks were designed to have a small undercut between the top and bottom layer to allow solvents to dissolve the resists from the edges even if metal had deposited on the sides of the upper layers. For LOR-based (see 3.3.1) stacks the substrate was soaked in heated Remover-PG (Microchem) for 10 minutes at 60°C . The Remover-PG was then gently blown with a pipette over the surface of the substrate to push away any metals that were no longer adhered to resist. This process was repeated until all of the resist and metal adhered to it were removed. As smaller features had less surface area of resist for the solvent to resolve, more forceful streams were sometimes needed. If this was not enough to peel off the resist, sonication in a water bath was sometimes used. This often pulled off the metals deposited on the substrate, flake, or even the flake itself, so was used only when necessary. The Remover-PG was then removed by soaking the material in 2-proponal for 5 minutes and blow-dried with a nitrogen gun. For PMMA based stacked unheated acetone was used in the place of Remover-PG while the rest of the process was the same.

3.6 Sample wiring

Lithography wiring patterns were designed with $.5 - 1\text{mm}$ square pads that connected to metal leads on the sample material. To connect this to a preexisting wiring system we used a series of indium dots and thin gold wires (99.95% Au, $25\mu\text{m}$, Alfa Aesar). To avoid any currents damaging the sample, we first adhered the wire to the wiring structure with lead-free solder. Next we placed an indium dot (TODO source) on each of the sample wiring pads using a modified tweezer. The tweezer was cut so that only one prong remained, then the tip cut flat and further sanded smooth with the side of a razor blade. This allowed the indium dot to adhere to the tip easily and for the modified tweezer to be held similar to a pen for increased dexterity and use with samples in recessed mounts. The gold wire was then bent down and pushed into the indium dot and a second indium

Figure 3.5: Wiring

TODO: figure, wiring

dot was pressed into the first, forming a sandwich-like structure, that held the gold wire in place. The gold wire was then bent from the sample to prevent it from coming into contact with any part of the sample or other wires. This process was repeated for each of the wiring pads on the device.

To prevent static discharge from damaging the flake several measures were taken. A ionizing fan (Chapman VSE3000 static eliminator) was constantly blown across the sample and wiring station at all times. The person wiring was grounded with a static wrist strap to the building ground at all times when touching the device. The modified tweezer was held without gloves to connect it to the building ground though the body. The wiring station used a rubber floor mat with metal stool to isolate the person from the floor and prevent any charge buildup from the ground. Finally, clothing was chosen to reduce the buildup of static, especially in winter as the dryer air made hazardous amounts of static buildup fairly frequent. [15]

3.7 Layer Transfer? (TODO after I figure it out)

3.8 PFM? (TODO, I don't do it but it might be useful)

3.9 Hall probe (TODO)

The hall effect uses the Lorentz Force to measure the properties of carriers in a material.

Chapter 4 |

Electric field induced metallic behavior in thin crystals of ferroelectric $\alpha\text{-In}_2\text{Se}_3$

4.1 Introduction

Ferroelectric field effect transistors (FeFETs, see 2.2.4) are a natural evolution to field effect transistors (FET), providing a means of maintaining the transistor state without the need for a constant gate voltage. Typically this is achieved as a standard FET with a ferroelectric replacing gate dielectric. [79, 80] Further engineering for use in devices like ferroelectric random access memory add a metal layer in between the ferroelectric and channel to enhance the field, and adapt the FinFET design to utilize this design. [81] FeFET commercialization, in FRAM and beyond, still faces many engineering challenges including retention duration, finding an optimal coercive field and polarization strength, leakage current through the ferroelectric dielectric, material interface mismatches, limits to minimization of the ferroelectric. [81,82] With the discovery of conductive ferroelectric compounds, see 2.2.6, we can construct a new variation of the FeFET, where the ferroelectric acts the role of the semiconductor device channel. [83] Ferroelectric semiconductor field effect transistors (FeSmFETs) opens up many new possibilities for future devices and may one day answer the aforementioned obstacles.

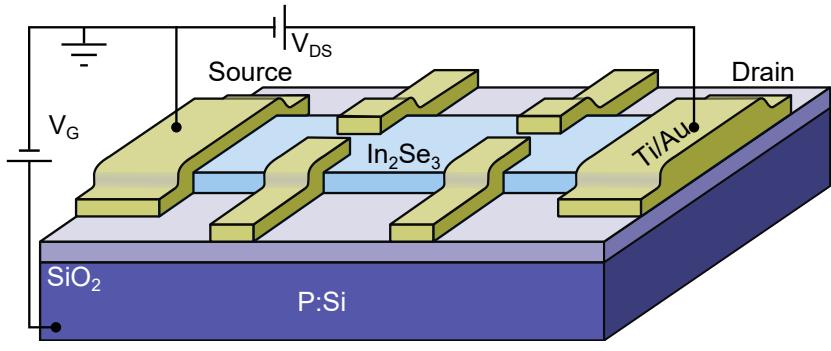
In 2017 α (3R)- and $\beta\text{-In}_2\text{Se}_3$ were first predicted to be ferroelectric down to one unit cell. [84] The α -phase prediction indicated a combined binary in-plane (IP) and out-of-plane (OOP) polarization as the selenium atom shifted in the lattice, while the β -phase showed only binary IP polarization. Due to the conductive nature of polar metals it is

difficult to preform traditional capacitance-polarization methods on a crystal as much of the capacitance voltage simply leaks though the material. In lieu of those measurements many distinct experiments form a pool of evidence for the existence of ferroelectricity in α -In₂Se₃. Second harmonic generation (SHG) shows a breaking of inversion symmetry [85–87], a necessary requirement for ferroelectricity. Piezoelectric force microscopy (PFM) has also shown evidence supporting ferroelectricity [85,88–91], though PFM can often give false positives as similar responses arise from other phenomena. [92] To counter this some authors have looked at both IP and OOP PFM response correlation [44,85,86,88,90,91], as well as observing the effect IP electric fields to alter the OOP polarization measured by PFM [90], narrowing the possibilities of what may be producing false positives.

The largest experimental verification of ferroelectricity in α -In₂Se₃ comes from several disparate devices designs that show signs of polarization. The most explicit example was from an α -In₂Se₃/graphene heterostructure FET. The graphene channel fermi-level shifts from the electric field produced by the FET gate and the α -In₂Se₃ polarization, forming two peaks in the channel resistance as gate voltage is swept and the fermi-level passes though the charge neutral point. [93] The authors use this to estimate a polarization value of 0.92 $\mu\text{C}/\text{cm}^2$, similar to the original theoretical prediction of 0.6 $\mu\text{C}/\text{cm}^2$ [84]. Extensive work has been carried out by multiple group using α -In₂Se₃ to create IP [85,88,91] and OOP [89,94] rectifying devices. For V_{DS} sweeps below the coercive field threshold, the devices act as a typical semiconductor channel. Above the threshold voltage the device current shows a significant change in slope, and a large hysteresis between increasing and decreasing voltage sweeps, see figure 4.3c and f. Finally, the recent pioneering of the first FeSmFET using thin crystals of α -In₂Se₃ with gate dielectric of 90-nm-thick SiO₂ or 15-nm-thick HfO₂. When gated, the channel current showed a large hysteresis, forming clockwise and counterclockwise loops with the respective gate dielectric, and persisting down to liquid helium temperatures. [83] Below we discuss the manufacture and measurement of similar α -In₂Se₃ FeSmFET devices that show a metallic transition when gated though a SiO₂ dialectic.

4.2 Device manufacture

Thin crystals of α -In₂Se₃ were grown by a modified Bridgman method. Transport measurements were carried out on both bulk and thin mechanically-exfoliated crystals. For bulk resistivity measurements, silver paint was used to form conductive terminals. In-plane resistivity measurements were carried out using a hall bar pattern along the



(a) Hall bar schematic

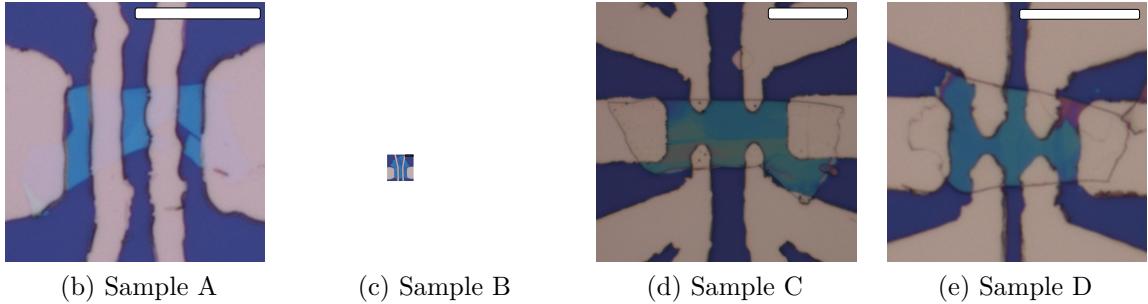


Figure 4.1: Device images

(a) Schematic of the Hall bar device with used in flake measurements, samples A and B had connected voltage leads for four-point measurements while C and D had separated leads for hall measurements. (b-e) Optical images of sample devices following this design with $10 \mu m$ scale bars.

longest axis of the bulk crystal. For out-of-plane measurements, to ensure a fresh surface, the previous leads were removed with a razor before new leads were added on. A modified four-point pattern was used to accommodate the thin c-axis of the crystal: a current lead was placed in the center of the crystal on the opposing sides of the c-axis with a voltage lead encircling each current lead.

Flakes of thin crystals of α -In₂Se₃ on Si:P/SiO₂ were manufactured using mechanical exfoliation as described in 3.2.2. Flakes were identified using an optical microscope and atomic force microscopy was used to establish a rough microscope color code to judge the thickness of the flakes. Below 20nm, flakes hue was unchanged but appeared increasingly transparent as thickness decreased. To promote better van der Walls adhesion of the flake to the substrate, the latter was first cleaned in Nanostrip, Acetone, 2-Propanol, and DI-water, before flake exfoliation, and the substrate was heated to 100C while in contact with the tape prior to the final removal. After optical identification, flake-substrates were kept in a drybox, or later in vacuum, to avoid water contamination and oxidation.

Flakes of crystal were made into four-point probe and Hall bar FET devices using

| Sample | t (nm) | L_{volt} (μm) | $L_{current}$ (μm) | w (μm) | Device pattern |
|--------|----------|------------------------|---------------------------|-----------------|------------------|
| A | 20 | 2 | 12 | 5 | four-point probe |
| B | 13 | 4 | 16 | 30 | four-point probe |
| C | 110 | 5 | 15 | 10 | Hall bar |
| D | 110 | 2 | 12 | 9 | Hall bar |

Table 4.1: Device parameters

Physical dimensions of the α -In₂Se₃ crystals used in the sample devices and the lead configuration. L_{volt} and $L_{current}$ are the distance between the respective voltage and current leads, w the channel width of the crystal, and t the thickness of the crystal.

photolithography and e-beam metal deposition. Similar to many other van der Waals chalcogenide materials, In₂Se₃ is sensitive to the alkali (base) developers used in many photodevelopment processes. [95, 96] Initial Hall bar devices with thinner crystal flakes were completely inoperative after manufacture, while thicker devices showed substantial Schottky barriers on various contacts. Milling away crystal material between the lithography and metal evaporation produced better contacts, but inconsistently, and only worked with thicker devices. To circumvent this effect, we modified our lithography step to only allow solvent developers in contact with the flake material, with the procedure described in section 3.3.2. 5 nm of titanium and 45 nm of gold was evaporated using either a Lab-18 Thin Film Deposition System (Kurt J. Lesker Co.) or a Temescal FC2000 (Ferrotec). The excess material was removed using the solvent Remover-PG (Microchem). Figure 4.1 shows the layout and optical images of the devices measured in this chapter, table 4.1 the corresponding parameters of those devices. All measurements were carried out in low vacuum, less than 1 mTorr, in a Model 6000 Physical Properties Measurement System (PPMS, Quantum Design). A Keithley 6340 was used as the current and voltage bias source as well as the corresponding two-point voltage and current measurements, two Keithley 2182A were used for four-point and hall measurements across the voltage leads, and a Keithley 2400 was used to provide the gate voltage bias.

4.3 Optical crystal measurements

Indium and selenium can form a variety of compounds, and the growth process is complicated and may result in crystals with mixed polymorphs, see section 2.3.2. [44] Because of this, several optical measurements were used to confirm the stoichiometry and lattice stacking of the material used in our devices. X-Ray diffraction measurements

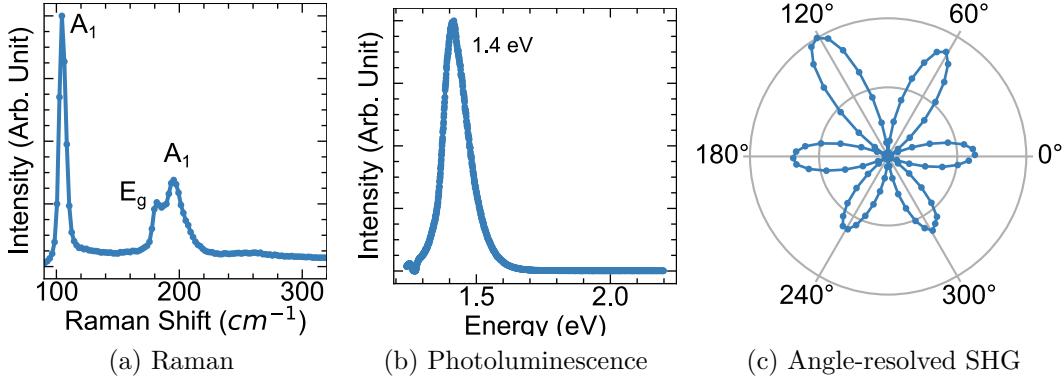


Figure 4.2: Optical measurements of $\alpha\text{-In}_2\text{Se}_3$.

Raman (a), photoluminescence (b), and angle-resolved SHG (c) of exfoliated $\alpha\text{-In}_2\text{Se}_3$ flakes on Si-SiO₂ substrate.

displayed peaks corresponding to the $R3m$ or $R\bar{3}m$ space groups, indicating α - or β -phase. Raman showed peaks near 104 , 179 , and 193 cm^{-1} corresponding to the A_1^1 , E^3 , and A_1^4 peaks of $\alpha\text{-In}_2\text{Se}_3$. [44, 97] Photoluminescence showed an energy gap of 1.4 eV , consistent with previous $\alpha\text{-In}_2\text{Se}_3$ optical measurements. [97] Finally, angle-resolved SHG showed a six-fold symmetry establishing the material as stacking in a $R3m$ (166) space group lattice. [85, 86, 91] Figure 4.2 shows the Raman, photoluminescence, and SHG measurements performed on exfoliated flakes of crystal on Si:P/SiO₂ wafer chips.

4.4 FET measurements

Thin crystals of $\alpha\text{-In}_2\text{Se}_3$ were manufactured into Hall bar and four-point probe FETs. Devices were made on conductive substrates of doped silicon with an insulating layer of 300nm thermally grown Si:P/SiO₂, allowing us to use the substrate as the gate in the FETs. Figure 4.3 shows sample A source-drain current I_D measured against voltage bias V_{DS} from 0 to 5 V, and separately for 0 to -5 V, for fixed back gate voltages. Gate voltages were fixed in 25 V intervals from -75 V to 75 V for each sequence. The rapid increase in I_D at low voltages is indicative of two back-to-back Schottky diodes, see section 2.1.1. Samples B and C showed a similar measurement with both the increasing and decreasing V_{DS} bias for fixed gate voltages, figures B.2 and B.3. None of the samples measured were seen to saturate within $\pm 10 \text{ V}$ for any gate bias. The lower I_D for negative V_{DS} bias than positive is typical of n-type semiconductors, which is seen in most reports of $\alpha\text{-In}_2\text{Se}_3$ [98, 99]. Sample A V_{DS} was cycled from 0 V, 10 V,

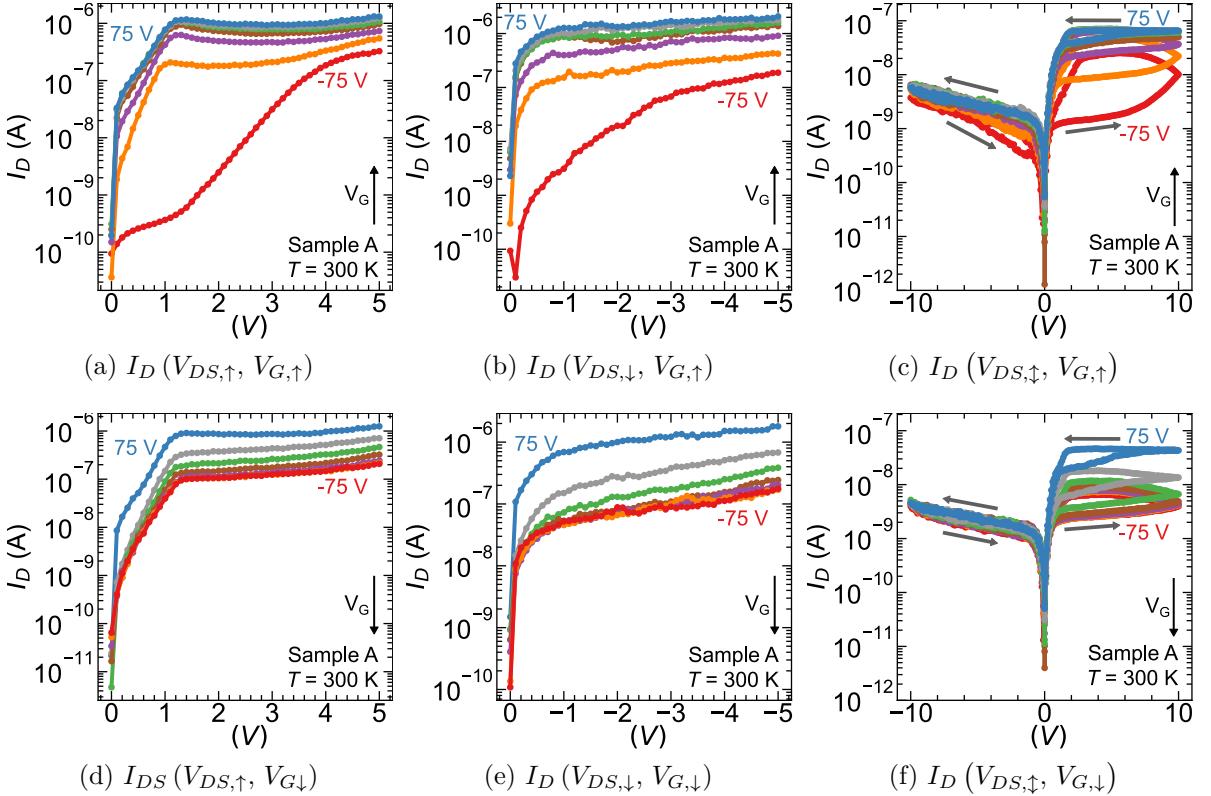


Figure 4.3: Sample A: $I_D (V_{DS})$

$I_D (V_{DS})$ of sample A with positive-increasing (a & d) and negative-decreasing (b & e) V_{DS} . (c & f) hysteresis in I_D as V_{DS} is cycled from 0 V, 10 V, -10 V, to 0 V. Measurements (a - c) are taken while V_G is held at 25 V intervals that increase sequentially for each curve, and (d - f) decreasing for V_G intervals. All measurements were done at 300 K.

-10V, to 0 V, forming asymmetric hysteresis in the current. The switching behavior is similar to previous reports of $\alpha\text{-In}_2\text{Se}_3$ rectifying devices, where the ferroelectric polarization field is thought to modify the Schottky barrier between the material and the metal leads. [85, 88, 89, 94] The increasing drain current with positive gate voltages is indicative of a *n*-type semiconductor [15], consistent with previous measurements on $\alpha\text{-In}_2\text{Se}_3$ [98, 100].

FET transistor transfer curves, current as a function of gate voltage V_G , were measured for each device. All measurements shown were performed with a fixed $V_{DS} = .1V$, with the V_G cycled from 0 V, to -75 V, 75 V, -75 V, to 0 V, shown in figure 4.4. For clarity, only the data between -75 V, 75 V, to -75 V is shown, as that behavior is persistent across multiple loops. The measurement was repeated at various, fixed temperatures from 300 K to 2-4 K, the lowest temperature reached is sample dependent due to ice blockages in the PPMS

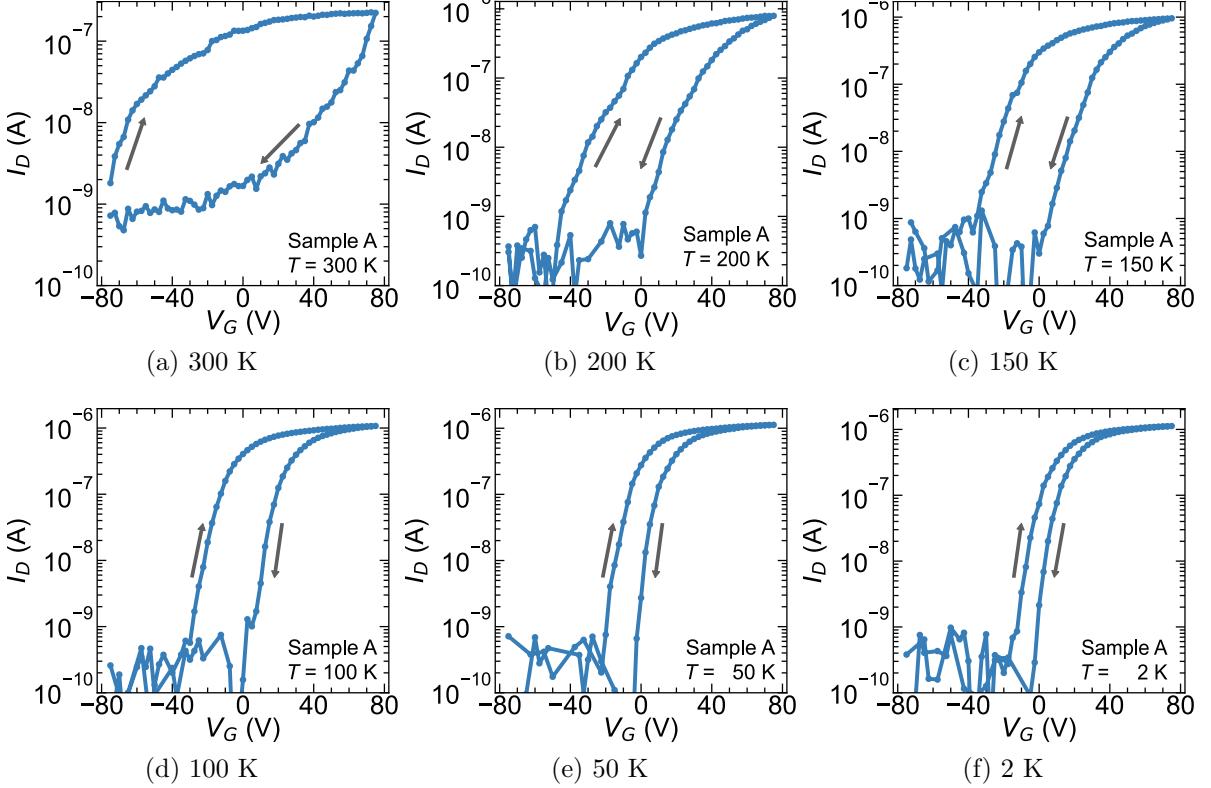


Figure 4.4: Sample A: $I_D (V_G)$ transfer characteristics $I_D (V_G)$ of sample A at the indicated fixed temperatures. Each was measured with $V_{DS} = 0.1 \text{ V}$ as V_G was cycled, a clockwise hysteresis current loop was seen at all temperatures.

cooling. For each gate voltage sweep sweep the current formed a clockwise hysteresis loop. In all samples the width of the loop decreased with decreasing temperature, though each sample still exhibited a finite hysteresis at the lowest temperature. Samples B and C showed similar clockwise hysteresis behavior, shown in B.4 and B.5. This behavior is consistent with previous work with *n*-type $\alpha\text{-In}_2\text{Se}_3$ on SiO_2 FeSmFETs. [83]

4.5 Discussion

When cooled from 300 to 2 K, the $\alpha\text{-In}_2\text{Se}_3$ bulk crystal showed an increase in resistivity emblematic of most semiconductors, seen in figure 4.5a, with variable range hopping conduction appearing below approximately 40 K. In contrast thin gated crystals of $\alpha\text{-In}_2\text{Se}_3$ showed a more positive dR/dT slope for increasing positive gate voltages. Figure 4.5b-d show a cross section of the $I_D (V_G)$ transport measurements taken at different

temperatures of samples A, B, and C, shown in figures 4.4, B.4, and B.5. $V_G = 0$ shows a similar behavior to the bulk crystal, while 50 V and 75 V have a dR/dT slope indicative of a metallic state. The cross section of $I_D(V_G)$ is used to examine the metallic transition of the devices as the increased conductivity state was quickly destroyed with changing temperatures, and was sensitive to the previous state of the system, see figure B.6. In all samples the onset of the uptick in conductivity occurs at higher voltages as temperatures decrease, leading to a shrinking but finite hysteresis loop. These behaviors seem to be independent of ramping rate of V_G (B.7) and contact resistance does not appear to play a significant role in sample resistance (figures B.6 and B.8). The magnetoconductance of sample A displayed weak localization even while gated to the metallic state at 1.8 K (figure 4.5d), as well as 10 and 50 K (figure B.10). The MC data was quantitatively fit to the Hikami-Larkin-Nagaoka theory of 2D weak localization with spin-orbital coupling [101]

$$\Delta\sigma(B) = \alpha \frac{e^2}{2\pi^2\hbar} \left[\ln\left(\frac{B_\phi}{B}\right) - \psi\left(\frac{1}{2} + \frac{B_\phi}{B}\right) \right] \quad (4.1)$$

where ψ is the digamma function, B_ϕ is the dephasing magnetic field, $\alpha = 1/2$ for weak anti-localization and 1 for weak localization. Sample C shows a small uptick in cross-section resistance near liquid helium temperatures, this is likely a result of disorder in the sample C crystal. Weak localization in a 2D system can manifest a non-metallic, negative dR/dT at low temperatures. [102]

FIXME: Max 2D electric conductivity? No idea where the $80\sigma_0$ (quantum conductance) calculation comes from.

FIXME: hysteresis shrink, polarization exists at 2K (invoke 6?)

FIXME: discuss how polarization may change metallic transition

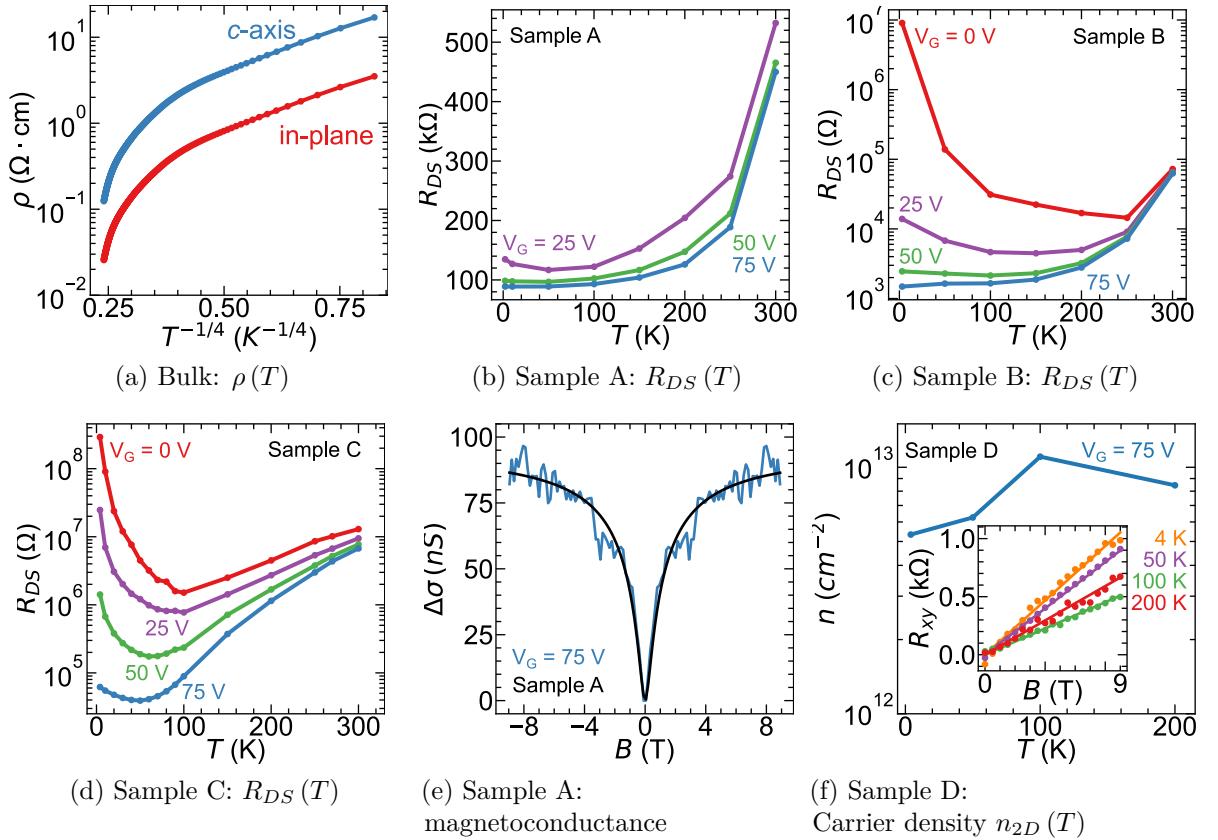


Figure 4.5: Temperature dependence and magnetic field measurements

(a) Bulk crystal resistivity along the c-axis and in-plane. (b-d) Temperature cross-section of the $I_D(V_G)$ transfer characteristics for samples A, B, and C for the curves shown in figures 4.4, B.4, and B.5 respectively. Each data-point is taken from the increasing V_G (top) portion of the respective $I_D(V_G)$ curves for 0, 25, 50, and 75 V. (e) The magnetoconductance of sample A taken at 1.8 K. The data was symmetrized to remove odd-term magnetic field dependence, and normalized to the difference from the measured value at zero-field. (f) Sample D carrier density at various temperatures, the inset shows the hall data used the the carrier density calculations.

Appendix A |

3D crystal symmetry groups

There are a total of 32 possible 3D crystal point groups. The following table lists the groups and are colored according to related phenomena:

- Pyroelectrics, possible ferroelectrics: 1, 2, m, mm2, 3, 3m, 4, 4mm, 6, 6mm
- Piezoelectrics only: 222, 4, 422, 42m, 32, 6, 622, 6m2, 23, 43m
- Non-centrosymmetric and non-piezoelectric: O
- Centrosymmetric: $\bar{1}$, $2/m$, mmm , $4/m$, $4/mmm$, $\bar{3}$, $\bar{3}m$, $6/m$, $6/mmm$, $m3$, $m\bar{3}m$

Table A.1: 3D crystal classes [1]

| Crystal system # | Point group | | | Space groups | |
|------------------|---------------------|-----------|------------------|--------------|------------------------------|
| | Hermann– Mauguin | | Schoen- flies | Order | |
| | 1 | 1 | C_1 | 1 | P1 |
| Triclinic | 2 | $\bar{1}$ | C_i | 2 | $P\bar{1}$ |
| | 3–5 | 2 | C_2 | 2 | $P2$, $P2_1$, $C2$ |
| Monoclinic | 6–9 | m | C_s | 2 | Pm , Pc , Cm , Cc |
| | | | | | |

| | | | | | |
|--------------|-----------|----------|---|--|---|
| | | | | | $P2/m, P2_1/m,$ |
| 10–15 | $2/m$ | C_{2h} | 4 | | $C2/m, P2/c, P2_1/c,$ |
| | | | | | $C2/c$ |
| 16–24 | 222 | D_2 | 4 | | $P222, P222_1, P2_12_12_1, C222_1,$ $C222, F222, I222, I2_12_12_1$ |
| 25–46 | mm2 | C_{2v} | 4 | | $Pmm2, Pmc2_1, Pcc2, Pma2, Pca2_1, Pnc2,$ $Pmn2_1, Pba2, Pna2_1, Pnn2,$ $Cmm2, Cmc2_1, Ccc2, Amm2, Aem2,$ $Ama2, Aea2,$ |
| Orthorhombic | | | | | |
| | | | | | $Fmm2, Fdd2,$ |
| | | | | | $Imm2, Iba2, Im2$ |
| 47–74 | mmm | D_{2h} | 8 | | $Pmmm, Pnnn, Pccm, Pban, Pmma, Pnna,$ $Pmna, Pcca, Pbam, Pccn, Pbcm, Pnnm,$ $Pmmn, Pbcn, Pbca, Pnma,$ $Cmcm, Cmce, Cmmm, Cccm, Cmme, Ccce,$ $Fmmm, Fddd,$ |
| | | | | | $Immm, Ibam, Ibca, Imma$ |
| 75–80 | 4 | C_4 | 4 | | $P4, P4_1, P4_2, P4_3, I4, I4_1$ |
| 81–82 | $\bar{4}$ | S_4 | 4 | | $P\bar{4}, I\bar{4}$ |
| 83–88 | $4/m$ | C_{4h} | 8 | | $P4/m, P4_2/m, P4/n, P4_2/n,$ $I4/m, I4_1/a$ |
| 89–98 | 422 | D_4 | 8 | | $P422, P4_212, P4_122, P4_12_12, P4_222,$ $P4_212, P4_322, P4_32_12,$ $I422, I4_122$ |
| Tetragonal | | | | | |
| 99–110 | 4mm | C_{4v} | 8 | | $P4mm, P4bm, P4cm, P4_2nm, P4cc, P4nc,$ $P4_2mc, P4_2bc,$ $I4mm, I4cm, I4_1md, I4_1cd$ |

| | | | | | |
|-----------|-------------|----------|-------|---|---|
| | | | | | $P\bar{4}2m, P\bar{4}2c, P\bar{4}2_1m, P\bar{4}2_1c, P\bar{4}m2, P\bar{4}c2,$ |
| 111–122 | $\bar{4}2m$ | D_{2d} | 8 | $P\bar{4}b2, P\bar{4}n2,$ | |
| | | | | $I\bar{4}m2, I\bar{4}c2, I\bar{4}2m, I\bar{4}2d$ | |
| | | | | | $P4/mmm, P4/mcc, P4/nbm, P4/nnc,$ |
| | | | | | $P4mbm, P4/mnc, P4/nmm, P4/ncc,$ |
| 123–142 | $4/mmm$ | D_{4h} | 16 | $P4_2/mmc, P4_2/mcm, P4_2/nbc, P4_2/nnm,$ | |
| | | | | $P4_2/mbc, P4_2/mnm, P4_2/nmc, PP4_2/ncm,$ | |
| | | | | $I4/mmm, I4/mcm, I4_1/amd, I4_1/acd$ | |
| 143–146 | 3 | C_3 | 3 | $P3, P3_1, P3_2,$ | |
| | | | | $R3$ | |
| 147–148 | $\bar{3}$ | S_6 | 6 | $P\bar{3}, R\bar{3}$ | |
| Trigonal | 149–155 | 32 | D_3 | 6 | $P312, P321, P3_112, P3_121, P3_212, P3_221,$ |
| | | | | $R32$ | |
| 156–161 | 3m | C_{3v} | 6 | $P3m1, P31m, P3cl, P31c$ | |
| | | | | $R3m, R3c$ | |
| 162–167 | $\bar{3}m$ | D_{3d} | 12 | $P\bar{3}1m, P\bar{3}1c, P\bar{3}m1, P\bar{3}c1,$ | |
| | | | | $R\bar{3}m, R\bar{3}c$ | |
| 168–173 | 6 | C_6 | 6 | $P6, P6_1, P6_5, P6_2, P6_4, P6_3,$ | |
| 174 | $\bar{6}$ | C_{3h} | 6 | $P\bar{6}$ | |
| 175–176 | $6/m$ | C_{6h} | 12 | $P6/m, P6_3/m$ | |
| Hexagonal | 177–182 | 622 | D_6 | 12 | $P622, P6_122, P6_522, P6_222, P6_422,$ |
| | | | | $P6_322$ | |
| 183–186 | 6mm | C_{6v} | 12 | $P6mm, P6cc, P6_3cm, P6_3mc$ | |
| 187–190 | $\bar{6}m2$ | D_{3h} | 12 | $P6\bar{m}2, P\bar{6}m2, P\bar{6}2m, P\bar{6}2c$ | |
| 191–194 | $6/mmm$ | D_{6h} | 24 | $P6/mmm, P6/mcc, P6_3/mcm, P6_3/mmc$ | |

| | | | |
|--|---------------------------------|----------------------------|--|
| 195–199 23 <hr/> 200–206 $m\bar{3}$ <hr/> Cubic 207–214 432 | T <hr/> T_h <hr/> O | 12 <hr/> 24 <hr/> 24 | $P23, F23, I23,$ $P2_13, I2_13$ <hr/> $P432, P4_232,$ $F432, F4_132,$ $I432,$ $P4_332, P4_132, I4_132$ <hr/> $P\bar{4}3m, F\bar{4}3m, I\bar{4}3m,$ $P\bar{4}3n, F\bar{4}3c, I\bar{4}3d$ <hr/> $Pm\bar{3}m, Pn\bar{3}n, Pm\bar{3}n, Pn\bar{3}m,$ $Fm\bar{3}m, Fm\bar{3}c, Fd\bar{3}m, Fd\bar{3}c,$ $Im\bar{3}m, Ia\bar{3}d$ |
|--|---------------------------------|----------------------------|--|

Appendix B | Additional α -In₂Se₃ Figures

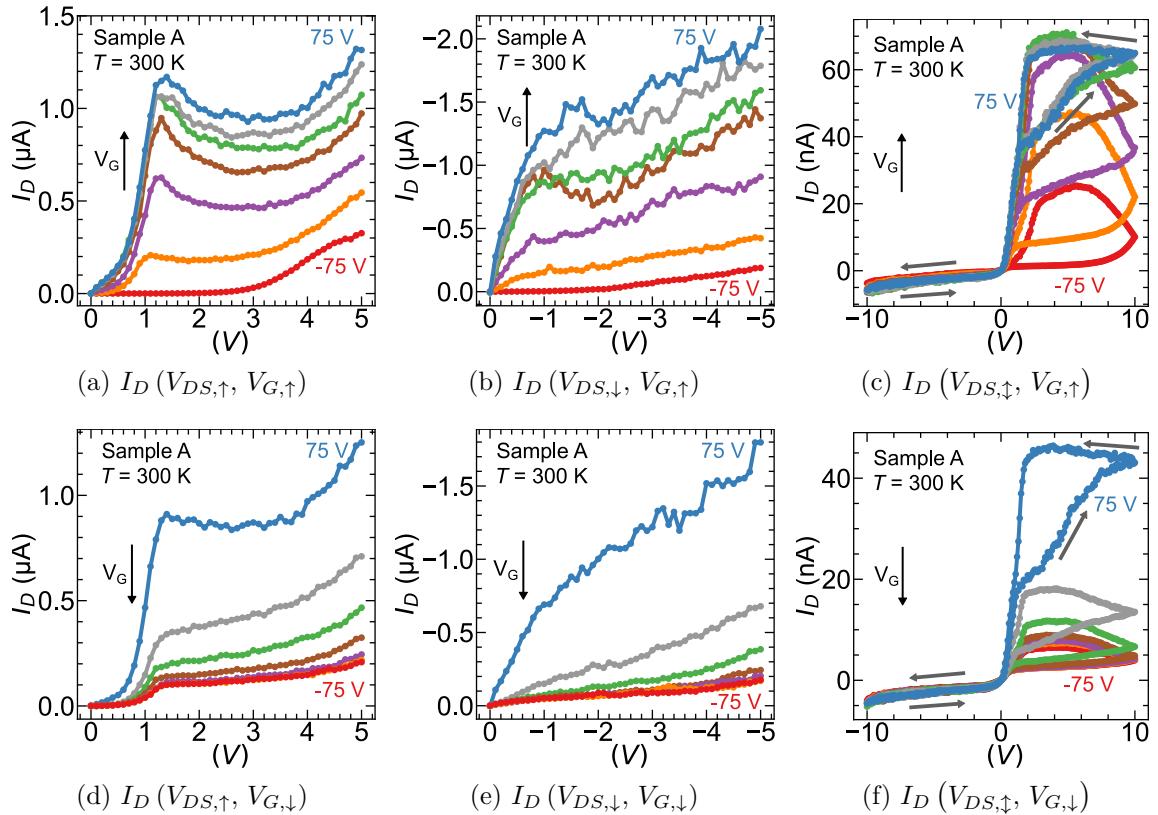


Figure B.1: Sample A: $I_D (V_{DS}, V_G)$

$I_D (V_{DS})$ of sample A, linear scaling of data shown in figure 4.3. (a & d) Show positive-increasing V_{DS} and (b & e) negative-decreasing V_{DS} . (c & f) hysteresis in I_D as V_{DS} is cycled from 0 V, 10 V, -10 V, to 0 V. Measurements (a - c) are taken while V_G is held at 25 V intervals that increase sequentially for each curve, and (d - f) decreasing for V_G intervals. All measurements were done at 300 K.

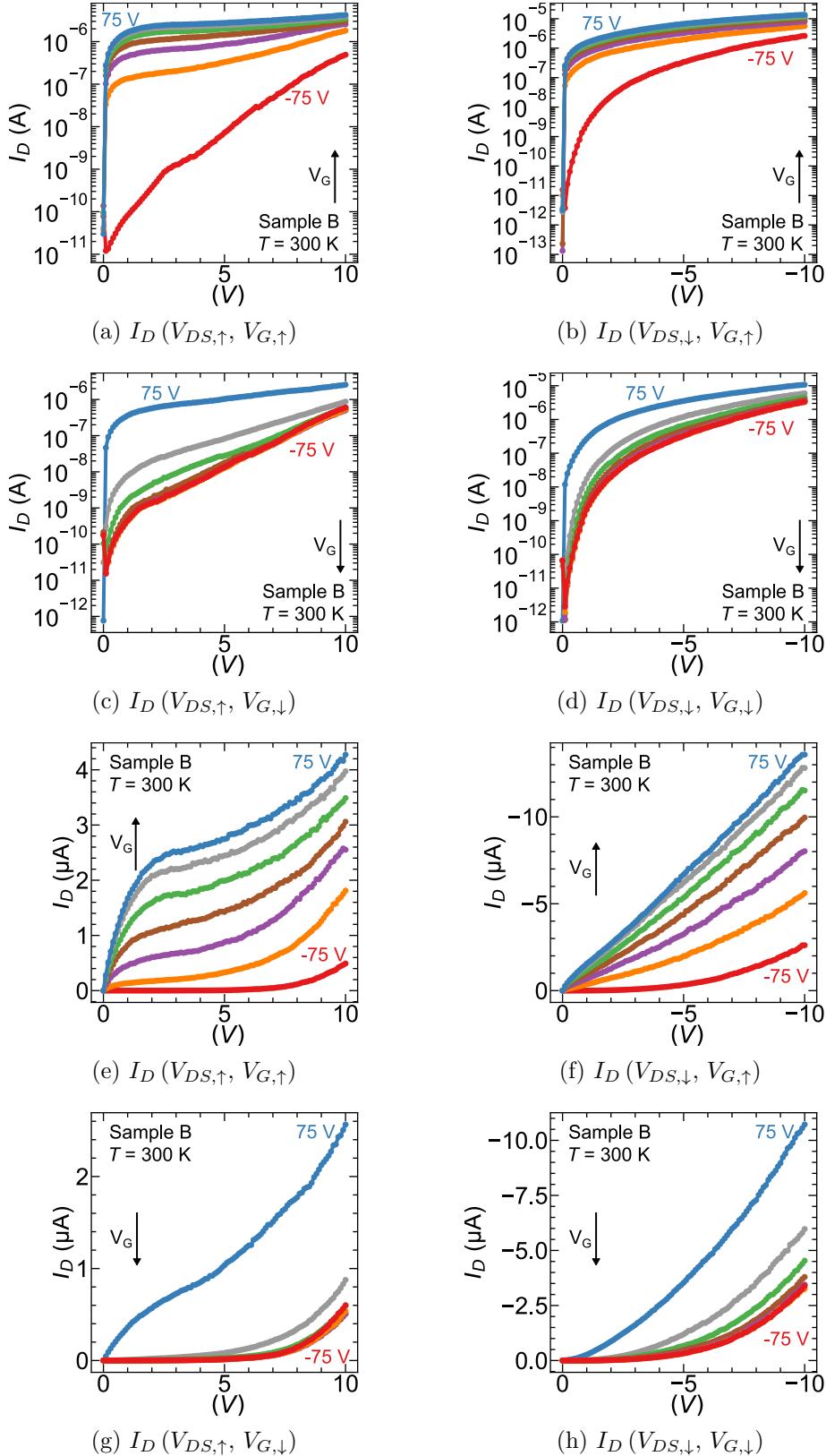


Figure B.2: Sample B: $I_D (D_{DS}, V_G)$

$I_D (V_{DS})$ of sample B with positive-increasing (a, c, e, & g) and negative-decreasing (b, d, f, & h) V_{DS} . Measurements (a, b, e, & f)⁵¹ are taken while V_G is held at 25 V intervals that increase sequentially for each curve, and (c, d, g, & h) decreasing for V_G intervals. All measurements were done at 300 K.

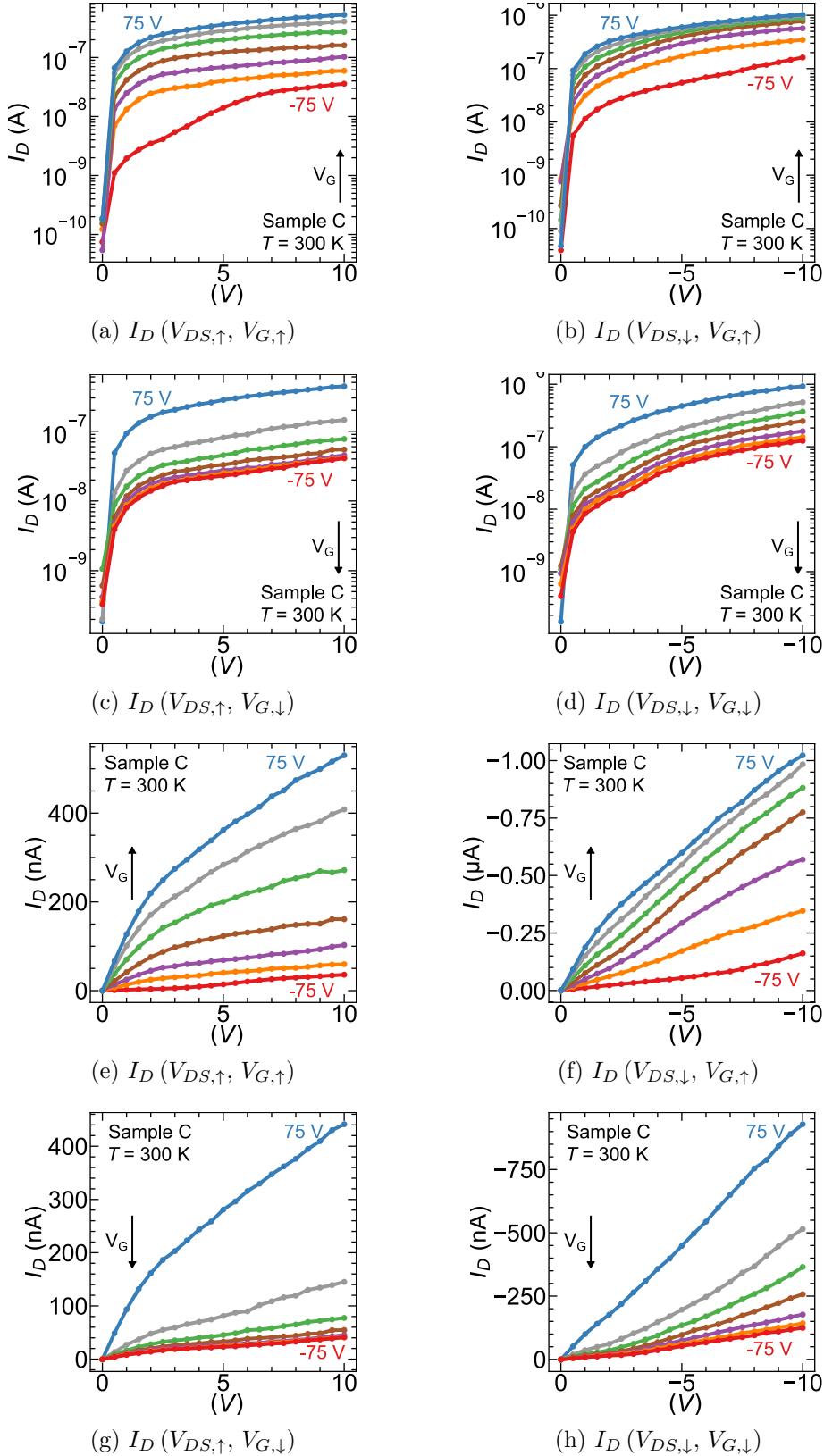


Figure B.3: Sample C: $I_D (V_{DS}, V_G)$

$I_D (V_{DS})$ of sample C with positive-increasing (a, c, e, & g) and negative-decreasing (b, d, f, & h) V_{DS} . Measurements (a, b, e, & f)⁵² are taken while V_G is held at 25 V intervals that increase sequentially for each curve, and (c, d, g, & h) decreasing for V_G intervals. All measurements were done at 300 K.

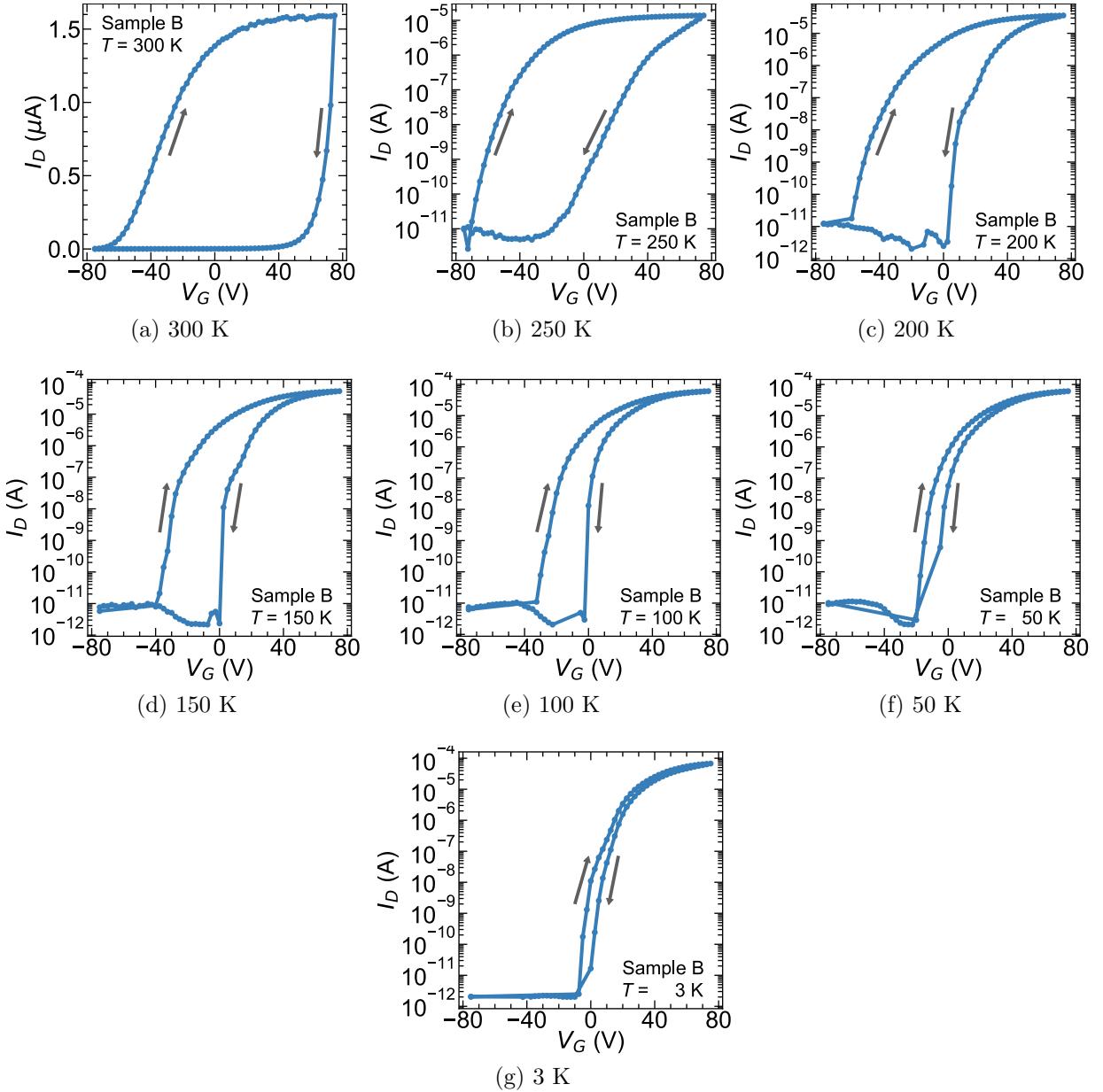


Figure B.4: Sample B: I_D (V_G) transfer characteristics
 I_D (V_G) of sample B at the indicated fixed temperatures. Each was measured with $V_{DS} = 0.1$ V as V_G was cycled, a clockwise hysteresis loop was seen at all temperatures.

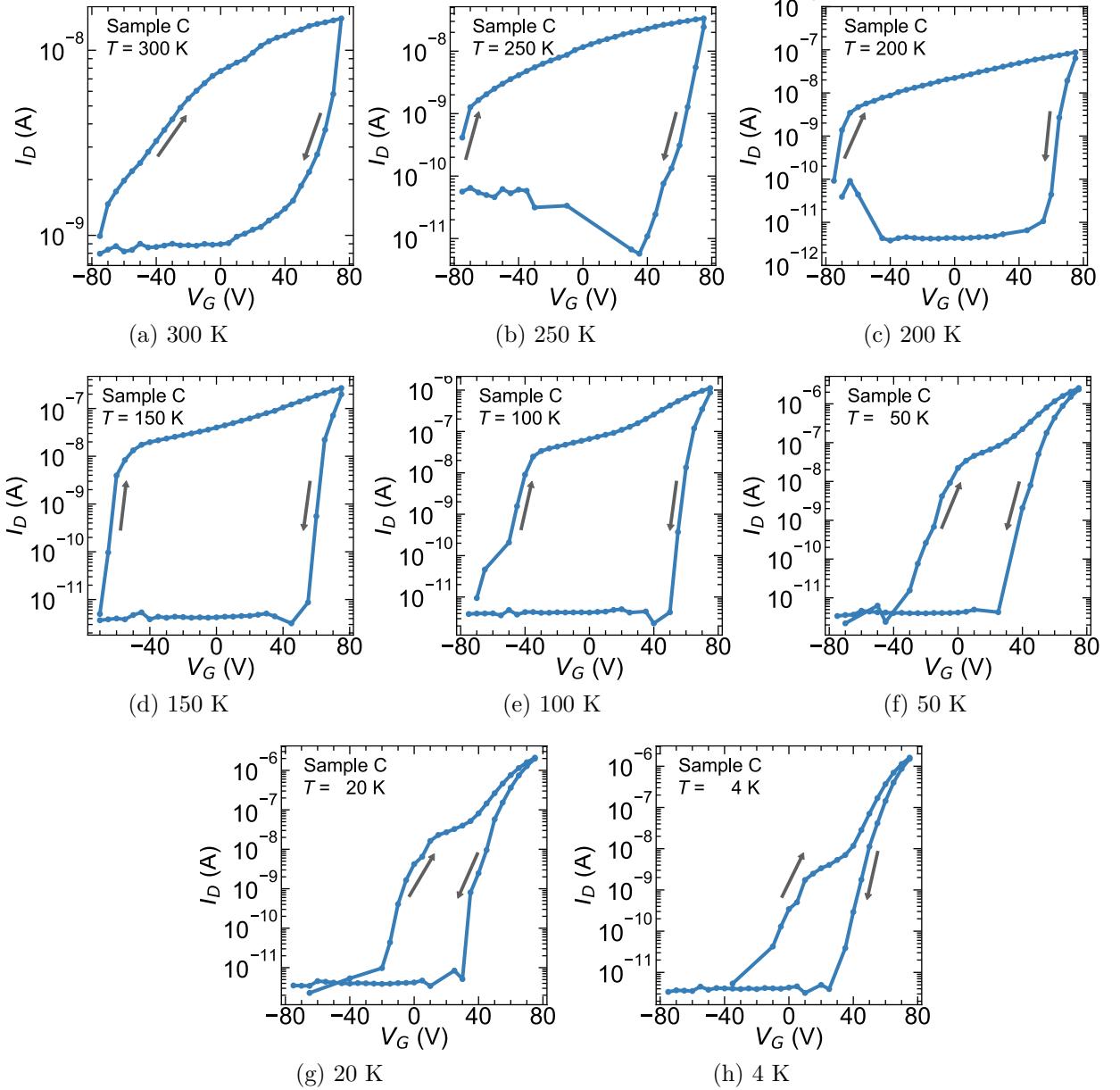


Figure B.5: Sample C: I_D (V_G) transfer characteristics
 I_D (V_G) of sample C at the indicated fixed temperatures. Each was measured with $V_{DS} = 0.1 \text{ V}$ as V_G was cycled, a clockwise hysteresis loop was seen at all temperatures.

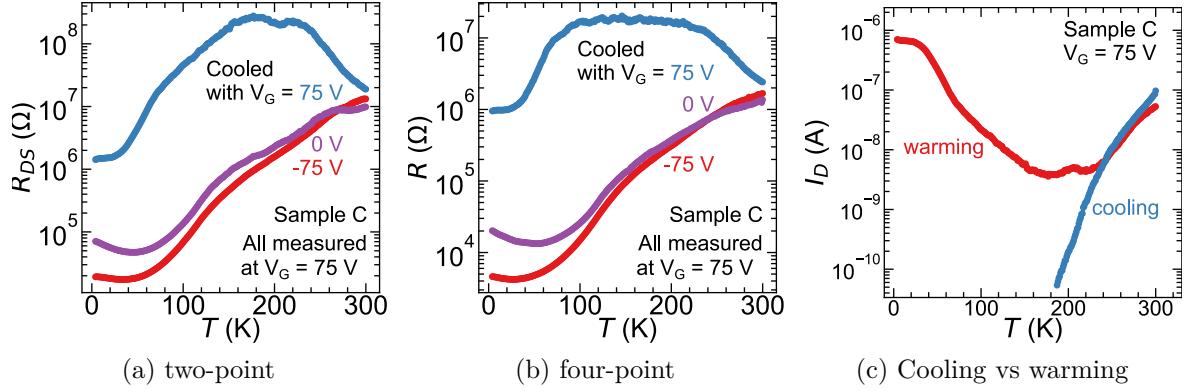


Figure B.6: Sample C: effects of warming and cooling while gated

Sample C (a) two-point and (b) four-point resistance measured at $V_G = 75 V$ with increasing temperature from 2 to 300 K. Before each measurement, sample were cycled at 300 K to $V_G = -75 V$, then fixed at 25, 50, and 75 V as indicated, then finally cooled from 300 to 2 K with the V_G still held constant. (c) Sample was cycled at 2 K (300 K) to $V_G = -75 V$ then to 75 V and held fixed. I_D was measured while sample was warmed (cooled) with constant V_G and $V_{DS} = 1 V$.

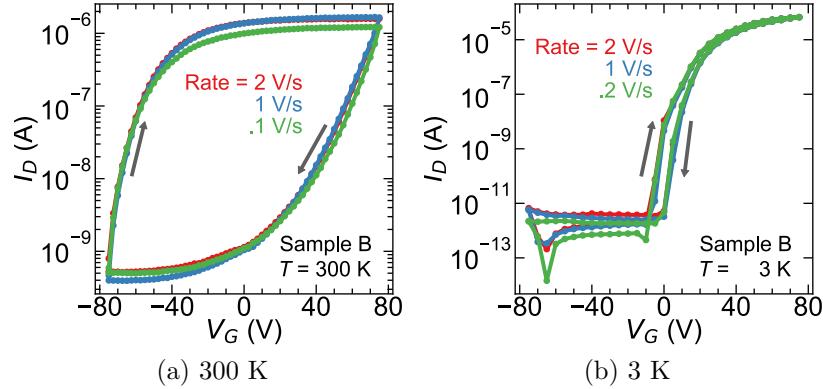


Figure B.7: Sample B: $I_D (V_G)$, V_G rate dependence
 $I_D (V_G)$ of sample C taken at (a) 300 K and (b) 3 K. Each curve was taken with $V_{DS} = 0.1 V$.

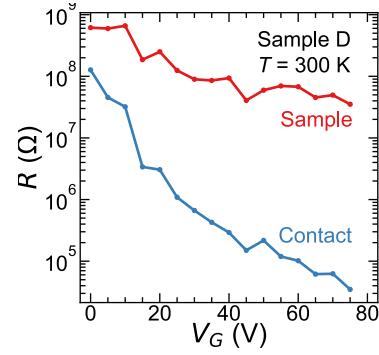


Figure B.8: Sample D: contact resistance

Sample D $R(V_G)$ contact and four-point sample resistance, taken at 300 K with increasing V_G .

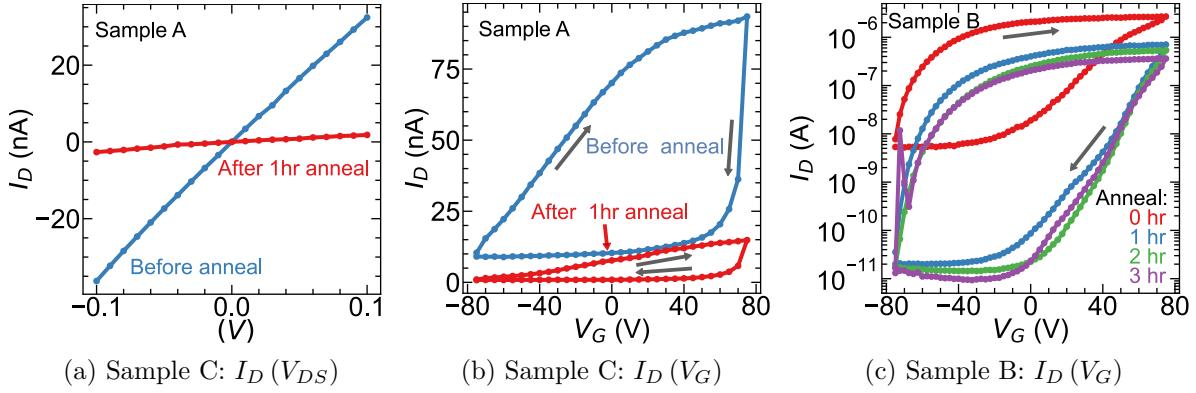


Figure B.9: Sample A and B: annealing

Samples A (a & b) and B (c) were annealed in vacuum at 400 K in 1 hour intervals. (a) Show $I_D(V_{DS})$ measurements and (b & c) $I_D(V_G)$, each taken at 300 K.

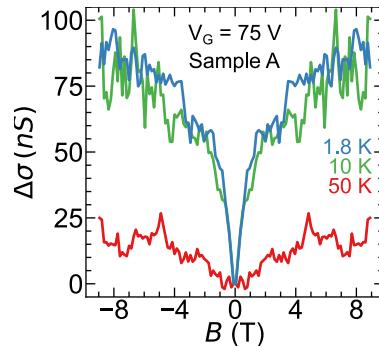


Figure B.10: Sample A: magnetoconductance

The magnetoconductance of sample A taken at 1.8, 10, and 50 K.

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Vita

Your Name

The details of my childhood are inconsequential.