Chapter 1

Sample Fabrication

1.1 Introduction

TODO: Explain about the 2D fad. Overall device construction.

1.2 Flake generation

1.2.1 Alignment marker wafer

Before fabricating any devices to test materials we needed a platform to work on that would make it easy to find flakes and manufacture devices. For this 4 inch wafers of $500\mu m$ phosphorus doped silicon with $300nm$ of thermally oxidized SiO_2 was chosen as a substrate (purchased from Si-Tech, <100> face, $\rho 5m\omega \cdot cm$). The high conductivity and thermal oxide allowed us to construct a backgated field effect transistor (see: FIXME). The substrate was polished for better adhesion of deposited flakes. Using standard photolithography (see 1.3.1) we patterned the surface with a $\sim 5nm$ thin layer of titanium for adhesion then $\sim 35nm$ of gold. The metals were laid out with a repeating pattern of numbers and lines to easily identify the location of a flake on the substrate when moving between tools. We spun a layer of PMMA resist over the substrate then diced the wafer $8mm$ square chips with a ADT 7100 ProVectus Dicing Saw. This allowed us to make many devices per wafer while customizing their orientation and pattern for each flake. The resist was then removed from the chip using acetone, 2-isoproponal, and deionized (DI) water then dried using a nitrogen blow gun. To remove any residue organics we soaked the chips in Nano-Strip (sulfuric acid and hydrogen peroxide compound, VWR) for 10 minutes, rinsed in DI-water, then repeated the initial solvent clean. After several devices experienced dialectic breakdown across the SiO_2 we changed the residue clean to an oxygen surface treatment. This was done in a M4L Plasma Processing System with 300 sccm oxygen, 100 sccm helium, at 500mTorr of pressure, and 100W for 1 minute.

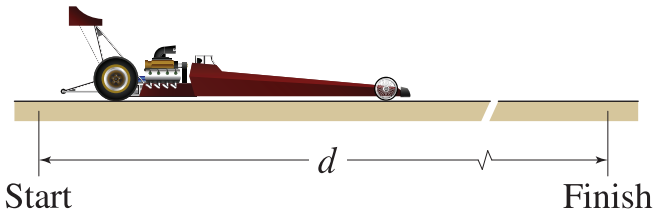

Figure 1.1. TODO: Device manufacture.

1.2.2 Mechanical flake exfoliation

Flakes were exfoliated using Scotch 3M Transparent Tape. The tape was pressed into a crystal of the desired material then peeled off, resulting in a few smaller chunks of crystals adhered to the tape. The tape was then folded over itself so the crystals were pressed into two different areas of tape. The tape was then peeled apart so that the crystals would be pulled apart into multiple chunks. This process was repeated several times to provide a region roughly 8 to 10mm in diameter with crystal coverage. This region was then pressed into a fresh region of tape so the exposed surface of crystals was free of tape residue. The tape and crystals was then placed on a cleaned aliment marker chip to maximize the amount of crystals within the center of the chip. The tape was lightly pressed into the chip so that the crystals would be in contact with the surface of the chip. To promote adhesion to the surface, the chip was then heated for 2 minutes at 100C.[**?**] The chips were then allowed to cool and the tape peeled off.

After exfoliation we scanned each chip for flakes using a Nikon Eclipse LV150 microscope. We chose 300nm of thermally oxidized SiO_2 to increase visibility of 2D materials under white light.[**?**] Flakes choice was optimized for uniformity, thinness, and lateral sizes large enough for photolithography processing. A Bruker Icon Atomic Force Microscope was used to measure flake height and develop a thickness color-code to compare new exfoliated flakes against.

TODO: tape figure, alingment mask?

1.3 Photolithography

Photolithography is a common technique used by industry and academia alike. In most variants of photolithography, a series of photosensitive polymers, or resists, are spread over a surface then exposing the polymer to light to change the chemical makeup of the polymer. This can be done by spinning a solution of the desired polymer, dissolved within a compatible solvent, at high speeds over a substrate. The solution is dripped on the substrate either statically or dynamically, under a slower rotation. The substrate is then rotated at high speeds until the desired thickness of polymer is left on the surface, the excess being flung off the substrate edges. The solvent can then be removed by baking the substrate and polymer for a short time until a desired durability is achieved. After exposure the resist is then removed by soaking the substrate in a chemical developer. Developer selection must take into account any chemistry between the developer and flake material as some developers can react with the exposed material. For negative resists, light exposed regions of polymer are removed when developed, positive resists will only have non-exposed regions removed. For devices that change based on the flake, the resist pattern is generated on a computer and then written by a moving laser to fit the device dimensions. In commonly used patterns, a mask of chrome on quartz is prefabricated. The mask is moved over the flake then the entire surface is flooded with light at once, exposing the regions with the desired resist pattern. We typically choose a multiple layer resist stack as allowing the bottom layer dissolve long enough to undercut the top allows for easier liftoff when removing evaporated metals (See 1.5). Resist can also be used to protect part of a sample when etching allowing a patterned etch of the substrate or testing device.

1.3.1 LOR+SPR stack

The LOR+SPR negative resist stack is easy to use and allows for high resolution patterns down to 2μm. Before any resist is added the substrate is given a dehydration bake of 115C for 60s to remove any water. A layer of LOR-2A is statically deposited as the first layer of the stack. The substrate is then spun at 4000RPM for 45s reducing the LOR-2A to a $\sim$ 200nm thick coating.[**?**] Finally we bake it at 180C for 60s on a hot plate to remove some solvent. Next a layer of SPR-3012 is dynamically dispensed at 900RPM. The substrate is then sped up and spun again at 4000RPM for 45s flattening the SPR-3012 to $\sim$ 1.3μm thick.[**?**] This is then baked for 95C for 60s on a hot plate. The resist stack and flake is then exposed using a MA/BA Gen4 or Gen2 Contact Aligner (SUSS MicroTec) with 54mW of light. The patterned resist is then developed for 60s in Microposit CD-26 (Tetramethylammonium hydroxide 1-5% and water, Shipley).

TODO resist stack

Table 1.1. TODO: Lithography resists

Resist	Solvent	Developer	Liftoff
LOR-2A		CD-26	Remover-PG
SPR-3012		CD-26	Remover-PG
PMMA		MIBK	Acetone/Remover-PG
SF6-slow		101A	Remover-PG

1.3.2 PMMA+PMGI+SPR stack

We found some chalcogenides reacted to alkali developers such as CD-26[**?**] so we developed an alternate photolithography resist stack with a solvent used to develop the material layer. First a layer of Polymethyl methacrylate (PMMA) (-2A Microchem) is statically deposited, spun at $2500RPM$ for $45s$ to give a $\sim 600nm$ layer, then baked at $180C$ for $180s$.[**?**] Next a layer of PMGI SF6-slow is dynamically spun at $900RPM$, then $4000RPM$ for $45s$ to reduce the thickness to $\sim 300nm$, and baked at $180C$ for $60s$.[**?**] Finally, a top-coat of SPR-3012 is dynamically dispensed at 900RPM. This is then spun at $4000RPM$ for $45s$ for a thickness $\sim 1.3\mu m$ and baked for $95C$ for 60s. The SPR-3012 is then exposed using a MA/BA Contact aligner with 54mW of light (peak $365nm$), developed for $60s$ in in Microposit CD-26 from Shipley (1.3.1), then rinsed in water. The PMMA and SF6 under-layers are exposed for 30 minutes in a Deep UV (peak $270nm$, FIXME WHO) at 5.4W (FIXME wavelength and energy). The SF6 is developed in 101A developer (Microchem) for $90s$ then rinsed in water. Finally the PMMA is developed for 10 minutes in methyl isobutyl ketone (MIBK) and a trace amount of water. The substrate is moved though the water for $30 - 60s$ to remove a thin film that forms, causing the film to pull off. The MIBK is then removed with 2-proponal.

An alternate version of this process used a thicker PMMA (6A) with SPR-3012 on top. Because the SPR uses a PMMA-compatible solvent (Cyclopentanone) the two layers would intermix and form a layer that was unable to be dissolved in either developer. This was removed by ashing the layer for 8:35 minutes in the M4L with 250 sccm oxygen, 50 sccm helium, 500mTorr pressure, 450W power. This process varied greatly depending on polymer uniformity and location of device on the substrate so later devices included the PMGI SF6 layer to eliminate the inconsistency.

TODO: figure resist stack

1.4 Thin filament shadow mask

As an alternative to lithography, we used an all-dry quartz filament shadow mask for metal evaporation (1.5). This allowed us to test contact resistance of an underlying material without introducing the polymers, chemicals, and processing to the material that may damage the surface or leave a residue between the material and metal contacts. We heated two quartz rod ends with an acetylene torch until semi-molten. We then lightly touched the two ends together and quickly pulled the ends apart within the flame. If done correctly, this produced several $2 - 10cm$ long strands of quartz that were $< 2\mu m$ in diameter. These were identified under a florescent light by their thread-like behavior, losing most stiffness and free to float in the air when $2\mu m$ in diameter. These filaments were then caught on glass forks by dragging the filament across the opening and snapping the end attached to the quartz rod. The forks were cut to fit over the sides of our sample chip substrates and reinforced with metal for durability. The sample chip was attached to a glass slide with double-sided tape. These filaments were then draped over the sample material with the glass fork. The ends of the filament were then cut with a tungsten needle and the glass fork removed. The filament could be adjusted by pulling it gently with a thin copper wire until it was in place and laying flat against the surface. This often caused the

quartz to snap so the range of movement was limited to within a few 10s of microns from where it started. Once the filament was maneuvered it was fixed in place by wrapping the ends in Teflon tape that wrapped around the glass slide. Teflon tape was chosen as it is unlikely to scratch the material and has no adhesive that would cause the filament to move when securing it. The tape was also used to reduce the exposed area so only a small region around the material was included and reduce the risk of a short between the two sides. We found a filament less than $.5\mu$ tended to cause a short between the two sides while greater than $3\mu m$ would not sit flush against the surface. Metal choice is similarly important as certain metals like indium tended to "wet" across the surface and short at any diameter.

TODO: figure filiment device, undercut with indium

1.5 Metal evaporation and liftoff

Metal deposition was done using the Lab-18 Thin Film Deposition System (Kurt J. Lesker Co.). This was used to add contacts to a lithography-patterned flake by covering a substrate with layers of metal. We used electron beam evaporated titanium and gold for the uniform deposition and high conductivity. First $\sim 5nm$ of titanium was deposited at $\sim 1\mathring{A}/s$ as titanium adheres well to SiO_2. Next a layer of $35-50nm$ of gold was evaporated at $\sim 1\mathring{A}/s$ on top of the titanium. The gold provided a highly conductive protective layer that was inert in atmosphere and safe to use when wiring samples.

The Lab-18 Thin Film Deposition System also had an in situ ion source that could be used to clean and roughen the surface of a material before deposition occurred. A typical process used $10sccm$ of argon gas flowed over a metal coil with $2.5A$ of emission current and $150V$ between the coil and the substrate. The ion source is undirected which caused trace amounts of iron from the chamber itself to be knocked loose and deposited on the surface of the sample.

To remove excess metals from the substrate the lithography resist was then removed though a 'liftoff' process. The resist stacks were designed to have a small undercut between the top and bottom layer to allow solvents to dissolve the resists from the edges even if metal had deposited on the sides of the upper layers. For LOR-based (see 1.3.1) stacks the substrate was soaked in heated Remover-PG (Microchem) for 10 minutes at $60C$. The Remover-PG was then gently blown with a pipette over the surface of the substrate to push away any metals that were no longer adhered to resist. This process was repeated until all of the resist and metal adhered to it were removed. As smaller features had less surface area of resist for the solvent to resolve, more forceful streams were sometimes needed. If this was not enough to peel off the resist, sonication in a water bath was sometimes used. This often pulled off the metals deposited on the substrate, flake, or even the flake itself, so was used only when necessary. The Remover-PG was then removed by soaking the material in 2-proponal for 5 minutes and blow-dried with a nitrogen gun. For PMMA based stacked unheated acetone was used in the place of Remover-PG while the rest of the process was the same.

1.6 Wiring

Lithography wiring patterns were designed with $.5-1mm$ square pads that connected to metal leads on the sample material. To connect this to a preexisting wiring system we used a series of indium dots and thin gold wires (99.95% Au, $25\mu m$, Alfa Aesar). To avoid any currents damaging the sample, we first adhered the wire to the wiring structure with lead-free solder. Next we placed an indium dot (FIXME source) on each of the sample wiring pads using a modified tweezer. The tweezer was cut so that only one prong remained, then the tip cut flat and further sanded smooth with the side of a razor blade. This allowed the indium dot to adhere to the tip easily and for the modified tweezer to be held similar to a pen for increased dexterity and use with samples in recessed mounts. The gold wire was then bent down and pushed into the indium dot and a second indium dot was pressed into the first, forming a sandwich-like structure, that held the gold wire in place. The gold wire was then bent from the sample to prevent it from coming into contact with any part of the sample or other wires. This process was repeated for each of the wiring pads on the device.

To prevent static discharge from damaging the flake several measures were taken. A ionizing fan (Chapman VSE3000 static eliminator) was constantly blown across the sample and wiring station at all times. The person wiring was grounded with a static wrist strap to the building ground at all times when touching the device. The modified tweezer was held without gloves to connect it to the building ground though the body. The wiring station used a rubber floor mat with metal stool to isolate the person from the floor and prevent any charge buildup from the ground. Finally, clothing was chosen to reduce the buildup of static, especially in winter as the dryer air made hazardous amounts of static buildup fairly frequent.

TODO: figure, wiring

1.7 Layer Transfer?