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The Graduate School
College of Engineering

DYNAMICS OF FISH

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Abstract

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Acknowledgments

Chapter 1
Background

1.1 Semiconductors

Semiconductors, as their name implies, are characterized by their decreased conduction compared to a metal while still conducting more than an insulating material. They possess a band gap of a few electron volts (eV), driving this conductivity. Semiconductors come in two flavors, n-type and p-type, that conduct using either electrons or holes respectively. Carriers reside below the Fermi energy in the fully occupied valance band but can be exited to move to an unoccupied higher energy band, the conduction band and thus move thus conduct. This is often through thermal excitation, so most semiconductors have an increased resistance at low temperatures. Photons can also excite electrons giving rise to countless applications such as sensors and LEDs. Furthermore, semiconductor behavior can be altered by introducing other elements or electric fields giving rise to a wide range of potential applications in just about every area of modern electronics.

1.1.1 Metal-Semiconductor-Metal conduction

When constructing electronic devices with multiple materials the physical and chemical properties of the material contact region must be considered. When placed in contact with each other, band structures of the individual crystal is altered as a new preferred energy minimum is reached, chemical reactions between the two materials can take place, and the physical dimensions of one material can shift to accommodate the other. For most electronic transport applications, an ohmic contact is preferred as it takes the least potential to form a current and is an easily predictable behavior. Ohmic contact is characterized by a linear relationship between the voltage and current given by the usual equation $V = IR$. This typically seen for a metal-metal junction as there is little band

bending and metal's ability to conduct at a wide range of energy levels. At the interface between metals and semiconductors a Schottky contact is typically formed instead that is non-ohmic in behavior. The actual nature of Schottky contacts is complicated and no simple model exists for the interface of metal-semiconductors. [2, 3] To predict the behavior of a metal-insulator junction one must numerically calculate the quantum mechanical states of the system, including the materials chemistry, and include the system's geometry. [4]

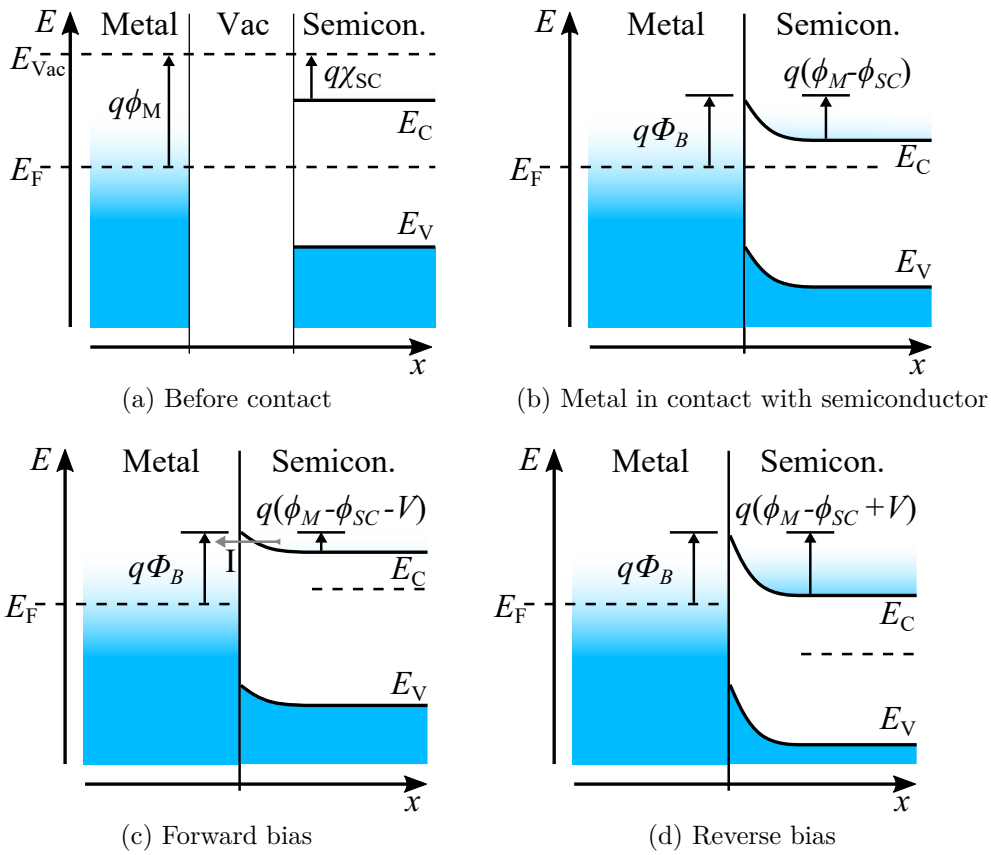
To provide at least a metal model of the behavior of the system, a simplistic model will be given for the behavior of a Schottky contact that ignores some of the individual details but gives broad predictions. Next to the junction, the electrons in the semiconductor move to (or from) the conduction band of the metal, depleting (accumulating) electrons in the area nearest to the metal. This causes the bands to bend, shown in Figure 1.1a-1.1b. The Schottky-Mott rule gives the energy barrier Φ_B of a charge carrier q between the two materials in terms of the work function of the metal ϕ_M and semiconductor electron affinity χ_{SC}

$$\begin{cases} \Phi_{B,n} = \phi_M - \chi_{SC} & n - type \\ \Phi_{B,p} = \chi_{SC} - \phi_M & p - type \end{cases} \tag{1.1}$$

The bulk of the semiconductor band shifts to accommodate the difference in work functions of both materials $\phi_M - \phi_{SC}$.

Applying a forward voltage bias to the system allows electrons from the semiconductor band to tunnel into the metal forming a current. Applying a bias in reverse causes only a few thermally excited electrons in the metal to tunnel to the semiconductor resulting in almost no current. Taken together, for an n-type semiconductor electrons can more easily flow from the semiconductor to the metal than the reverse. [6] Figure 1.1c-1.1d shows the potential shifting the bands in a forward and reverse bias. However, if a large enough reverse voltage bias is applied the carriers can instead move to the valance band of the semiconductor. This voltage-current curve is used to form diodes that conduct current only in one direction, where the reverse current is considered the breakdown potential of the diode. In order to reduce the band mismatch various techniques are often used to achieve Ohmic contact. Selecting the appropriate metal can reduce the energy band mismatch though it will likely still have a significant barrier. A common solution is to instead dope the semiconductor near the region of contact to provide a smooth transition between the metal and the semiconducting region.

For Schottky contacts behavior can be modeled using thermionic emission theory.



(a) Before contact

(b) Metal in contact with semiconductor

(c) Forward bias

(d) Reverse bias

Figure 1.1: Band diagrams of metal in contact with a n-type semiconductor (1.1a) before and (1.1b) after a metal is brought into contact with a n-type semiconductor. [5] Φ_B is the Schottky barrier height, E_F, the Fermi energy, E_C and E_V the conducting and valance bands. 1.1cforward and 1.1d reverse voltage bias applied from right to left. Arrow indicated the direction of current flow.

The current density is given by

$$J = J_0 \left(\exp\left(\frac{qV}{k_B T} \right) - 1 \right), \tag{1.2}$$

$$J_0 = A^{**} T^2 \exp\left(-\frac{q\Phi_B}{k_B T} \right) \tag{1.3}$$

where J_0 is the saturation current density, q the fundamental charge, k_B Boltzmann constant, T the temperature, and A^{**} the Richardson constant. [7–9] For a complete conduction channel though a semiconductor, both metal contacts must be considered, current in and out, as both are Schottky barriers. If we apply a voltage across the entire structure we have to consider the potential drop across each contact V_n as well as the

material itself V_{SC}. The voltage drop across a single diode is then

$$V_n = \pm \frac{k_B T}{q} \ln\left(\pm \frac{J}{J_{0n}} + 1\right) \tag{1.4}$$

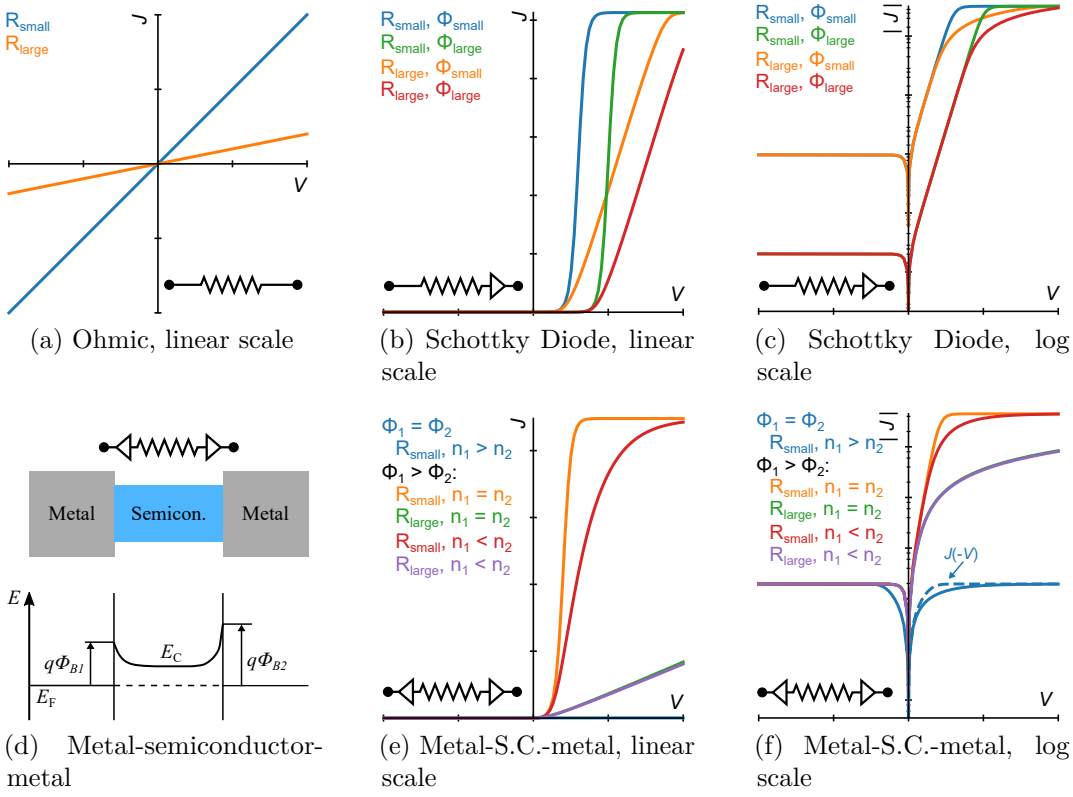
where the sign corresponds to the direction of current and J_{0n} depends on the individual barrier energy Φ_{Bn}. We may also consider that the contacts may not be ideal and introduce a contact specific parameter $n_n \geq 1$ to take this into account. With this we have the total voltage across the contacts

$$V = V_1 + V_{SC} + V_2 \tag{1.5}$$

$$V = \frac{n_1 k_B T}{q} \ln\left(\frac{J}{J_{01}} + 1\right) + RAJ - \frac{n_2 k_B T}{q} \ln\left(-\frac{J}{J_{02}} + 1\right) \tag{1.6}$$

where A is the surface area and R the resistance of the semiconductor. [7–9] This equation is not directly solvable for the current density but it is possible to numerically model the behavior as shown in figure 1.2. Figure 1.2a shows a typical linear ohmic behavior for large and small resistance. Figure 1.2b and 1.2c shows the behavior of a single diode and attached to a large and small resistance. The increased resistance can be seen in the higher voltages needed to reach the saturation current while the barrier height limits the reverse bias current. Figure 1.2e and 1.2f shows the behavior of both barriers and the semiconductor in this model. Similar to the single contact, the barrier height dictates the saturation current and the resistance the rate at which increasing voltage reaches saturation. The ideality factor n produces a deviation from the ideal curves which can easily be seen with a smaller R, making two contacts that have the same barrier height still produce an asymmetric behavior. This differentiation will decrease as R increases and the semiconductor resistance becomes as large as the contacts.

This non-linear behavior must be taken into account for any electronic transport done on a material as the Schottky contact can have multiple competing effects on a measurement. For a four-terminal device charges may or may not tunnel into a lead in contact with the semiconductor based on the size of the barrier and the resistance of the material being tested. Furthermore by placing a metal in contact with a semiconductor the region around the material is altered so a uniform material can not be assumed if it is near that metal. The ideality factor and barrier height can shift the two terminal resistance of a material so the current produced is not symmetric with respect to the voltage direction.



(a) Ohmic, linear scale

(b) Schottky Diode, linear scale

(c) Schottky Diode, log scale

(d) Metal-semiconductor-metal

(e) Metal-S.C.-metal, linear scale

(f) Metal-S.C.-metal, log scale

Figure 1.2: Current-voltage behavior of various junctions
Current-voltage graphs of the behaviors of different junction parameters from equation 1.6. (a) ohmic behavior, with no Schottky barrier with large and small resistances. A single Schottky barrier with small and large resistances and barrier heights, in linear (b) and logarithmic (c) plots. (d) simplified band diagram for a double Schottky barrier in a metal-semiconductor-metal device. A double Schottky barrier with large and small resistances, barrier heights, and ideality factors on a linear (e) and log (f) scale. The dashed line shows the asymmetrical nature of a pair of junctions with different ideality factors.

1.1.2 Field effect transistors

One of the most common applications of semiconductor devices is a field effect transistor (FET). Transistors provide a way to turn a current on or off with a voltage, allowing for controllable states in larger circuits. This forms the basis of digital logic in computers, by defining a threshold current as "on" or "off" we form a binary system. Transistors also allow for circuit elements to be isolated from each other, providing a path for different parts of a circuit to interact with one element while independent of the rest.

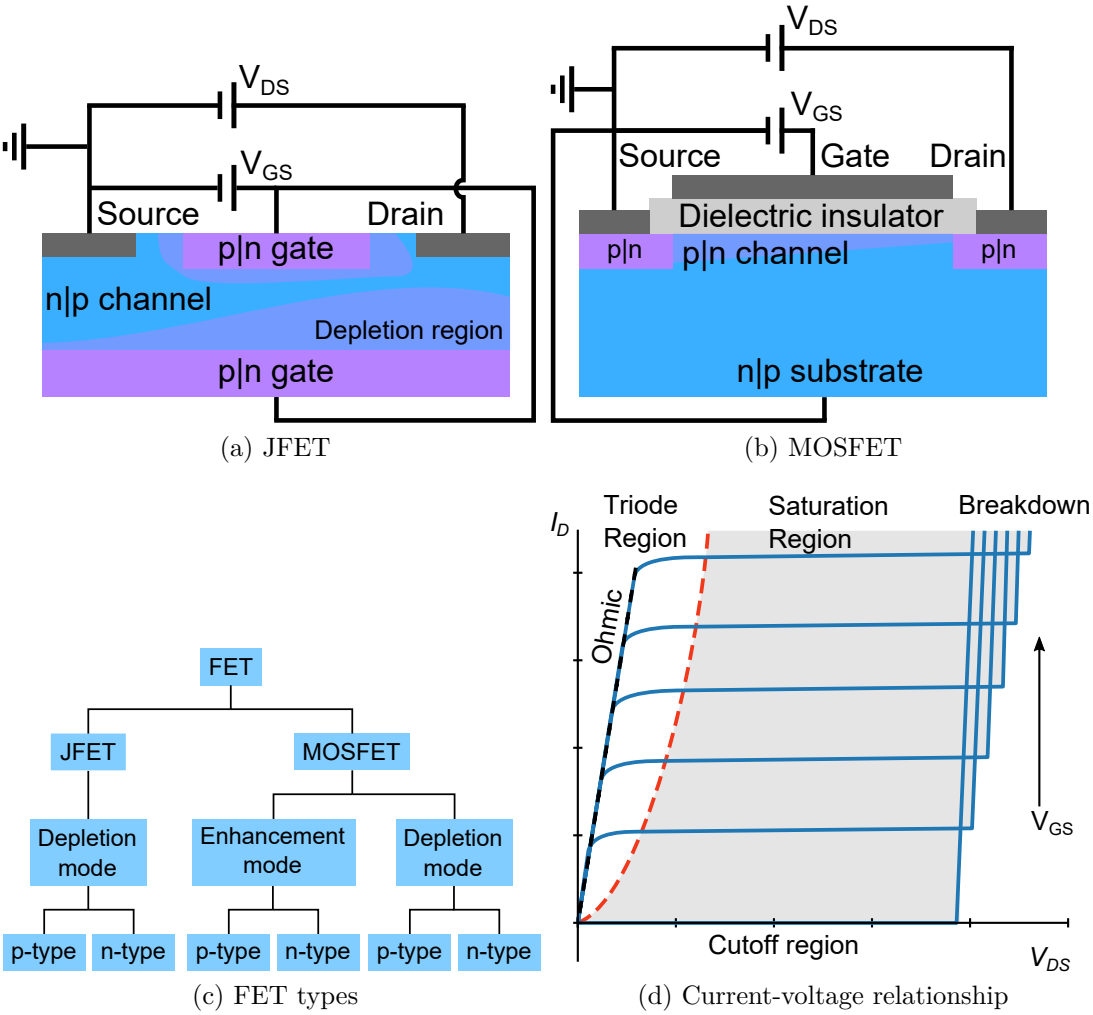
The typical structure of a FET is two ohmic contacts on either side of a semiconductor with a metal gate positioned on the semiconductor in between the two contacts.

Between the two contacts a conduction channel is established that majority charge carries, electrons or holes, can pass through. The natural conductivity of this channel can be altered by doping the semiconductor material to change the carrier concentration in the semiconducting material. The gate then provides an electric field that acts on the carriers passing between the two contacts. Removing carriers, known as depletion, will decrease the conductivity, while enhancement adds carriers to increase conductivity. There are two common types of FET, junction gate field-effect transistor (JFET) and metal-oxide-semiconductor FET (MOSFET).

JFET gates are composed of two gates placed on either side of the conduction channel. The gates are opposite in type to the channel, so if the channel is n-type the gate is p-type and vise-versa, figure 1.3a. This junction sets up a depletion region around the gates with a lower carrier concentration. By applying a bias between the source and the gate the depletion region can be expanded, shrinking the conduction channel. This eventually pinches off the entire channel forcing carriers to tunnel across the depletion region and halting most current thus giving an off state to the JFET. Because of this configuration, all JFET must be doped to conduct naturally and operate in depletion mode, as the reverse would generate current though the gate instead.

MOSFET incorporate a thin insulating oxide barrier between the metal gate and the conduction channel channel to isolate each and preventing a junction from forming, as seen in figure 1.3b. This also eliminates almost all current between the gate and the gate and the conduction channel, one of the most important advantages of MOSFET over other types of transistors. The conduction channel contacts are doped to form ohmic contacts opposite to the substrate. MOSFET transistors can operate in either enhancement or depletion mode, another of their significant assets, figure 1.3c shows the different operation modes possible. In enhancement mode the channel region does not have enough carriers to conduct naturally but by applying a gate voltage carriers are added to the region and current flows. Conversely, in depletion mode the channel will conduct without any bias, often though a doped layer, but an external voltage can be used to remove carriers and produce the off state. The bias between the source and drain leads also changes the electric field, and thus carrier density, within the conduction channel. Too large of a voltage causes the channel to start to pinch off, similar to a JFET, and setting a limit on the current that can be sourced between the contacts.

The interplay of drain-source and gate bias on channel behavior in FET lead to a non-trivial relationship between channel current and voltage. Figure 1.3d shows the typical interplay between drain-source voltage and current at different gate voltage



(a) JFET (b) MOSFET

(c) FET types (d) Current-voltage relationship

Figure 1.3: FET

intervals. In the cutoff region the channel conduction is exponentially low for almost any current to flow, and is an arbitrary threshold for the off state for a FET. As the channel carrier concentration is raised by the gate voltage the semiconductor has enough free charges for current flow through the channel. For low voltages, $V_{DS} \leq V_G - V_{th}$, the current looks linear and the FET acts like an ohmic resistor. The actual increase more closely follows

$$I_D = 2\kappa \left((V_{GS} - V_{th})\, V_{DS} - \frac{V_{DS}^2}{2} \right) \tag{1.7}$$

where κ is a scaling factor that depends on multiple factors like temperature, device geometry, and gate capacitance. V_{th} is the threshold voltage at which the gate voltage begins to pinch off the conduction channel, and is also dependent on temperature. Above

this limit the current is roughly constant

$$I_D = \kappa \left(V_{GS} - V_{th}\right)^2 \tag{1.8}$$

and is called the saturation region. The saturation region is what is typically thought of as the on state for a FET, providing an easy binary contrast with the cutoff region. Finally, once V_{DS} is large enough, the there is a rapid increase in current known as breakdown, due to the avalanche effect. This typically occurs only in JFET while MOSFET are limited instead by their power dissipation, however MOSFET can suffer an irreversible breakdown in the gate dialectic instead. [10]

Avalanche breakdown starts when a strong enough electric field causes an electron or hole to be propelled into an atom ionizing it and creating a second free charge. The charges can be further driven though the material ionizing more and more atoms along the way. This creates a runaway effect as the ions produce a conduction channel for more current and more free carriers. Avalanche breakdown can occur in both semiconductors and insulators and is usually irreversible as it forms a permanent conduction medium even after the field is removed. The breakdown oftentimes damages the material as rapid heating arises with the current.

As FET gate and channel contacts are within close proximity of each other, the electric fields produced by the gate will influence the channel contact junction behaviors. The electric field will cause the bands to bend at the junction between materials, potentially changing the barrier height, band bending rate, ideality factor, or other properties. Dealing with this often leads to many real world engineering complications and must be accounted for in device design. We must also be wary of assuming all FET device gating response is due to the bulk of the semiconductor alone, but instead recognize it is often a mix of bulk and contact characteristics.

1.1.3 Charge trapping

something

1.2 Ferroelectricity

Ferroelectric crystals will spontaneously polarize when below a critical temperature (T_C). Below T_C atom locations will create naturally occurring dipoles as they shift to find the lowest overall energy state, sacrificing local electrostatic homogeneity to do so. At higher

temperatures the atoms have more energy and space and generally prefer neutrality, forming a paraelectric material instead. When a ferroelectric is exposed to an electric field the dipoles shift to align with the electric field and will remain aligned when that field is removed. Paraelectric materials may form similar dipoles under the electric field but will return to their natural state when the field is removed. Ferroelectrics have many applications, as the polarization can be used to enhance capacitors, hold a persistent electronic configuration, or enhance other device properties.

1.2.1 Piezoelectricity and pyroelectricity

Piezoelectricity and pyroelectricity arise from non-linear behaviors in crystal structures. There are 32 crystal classes that make up 3D crystals. Of those 21 are non-centrosymmetric, and 20 of the non-centrosymmetric groups form piezoelectric materials. Furthermore, 11 of those groups can form pyroelectric and ferroelectrics materials. All ferroelectrics possess pyroelectricity and all pyroelectrics are piezoelectric, but not all pyroelectrics are ferroelectric and not all piezoelectrics are pyroelectric. This encircling Venn diagram provides a way for easily screening possible ferroelectrics but also means ferroelectrics materials have other attributes. Appendix A shows a list of classes of each type and the corresponding space groups.

In piezoelectric crystals, mechanical motion and polarization are bound together. Under mechanical strain and stress a voltage across the crystal. The movement changes the locations of the atoms within the crystal dipole.

In pyroelectricity crystal polarization is conjoined with changes in temperature. If we heat or cool a pyroelectric crystal, the crystal structure is altered slightly allowing it to spontaneously polarize, or if already polarized, change to a new polarization fitting the new atom placement. This polarization produces a voltage across the bulk of the crystal, providing a method to measure this change and thus the changing temperature that drove the re-polarization. After the temperature is fixed the voltage will generally dissipate though leakage currents. This makes pyroelectrics suitable for changing measurements like thermal imaging cameras and energy generation, but poor for managing persistent states in modern digital electronics.

- strain
- Formulas?

1.2.2 P-E diagram

figures here, paraelectric, dielectric, resistor?

1.2.3 FeFET

two types, behaviors of each, applicatons

1.3 2D materials

probably makes more sense under In-Se

1.3.1 In-Se phases

Indium-Selenium together can form a variety of binary compounds ranging with completely disparate properties. Depending on the temperature and prevalence of each element it is possible to get different phases of In-Se alloy growth and structure. Figure 1.4 shows a phase diagram compiled from various experimentally published sources up to 2003 as well as calculations. The plethora of compounds, and the sensitivity to both temperature and concentration, makes growth of a single uniform compound harder to control. Alternate configurations of the same stoichiometry have made past literature somewhat inconsistent as each configuration may have unique properties while the specific configuration was not reported.

1.3.2 In_2Se_3 in literature

In_2Se_3 is perhaps one of the most complicated of the In-Se compounds. Currently there are thought to be α, β, γ, δ, and κ phases of In_2Se_3, in addition to α', β', and γ' metastable phases. [12]

1.3.3 α and $\beta - In_2Se_3$

α and $\beta - In_2Se_3$are both 2D Van der Waal materials. α phase comes in 2H (Hexagonal, P63/mmc) and 3R (Rhombohedral, R3m [12,13]) stacking with indium atoms surrounded by selenium in a tetrahedral structure. There has also been a few reports of a $R\bar{3}m$ phase but they may be a misclassification of R3m with similar lattice parameters. [12, 14–16] β

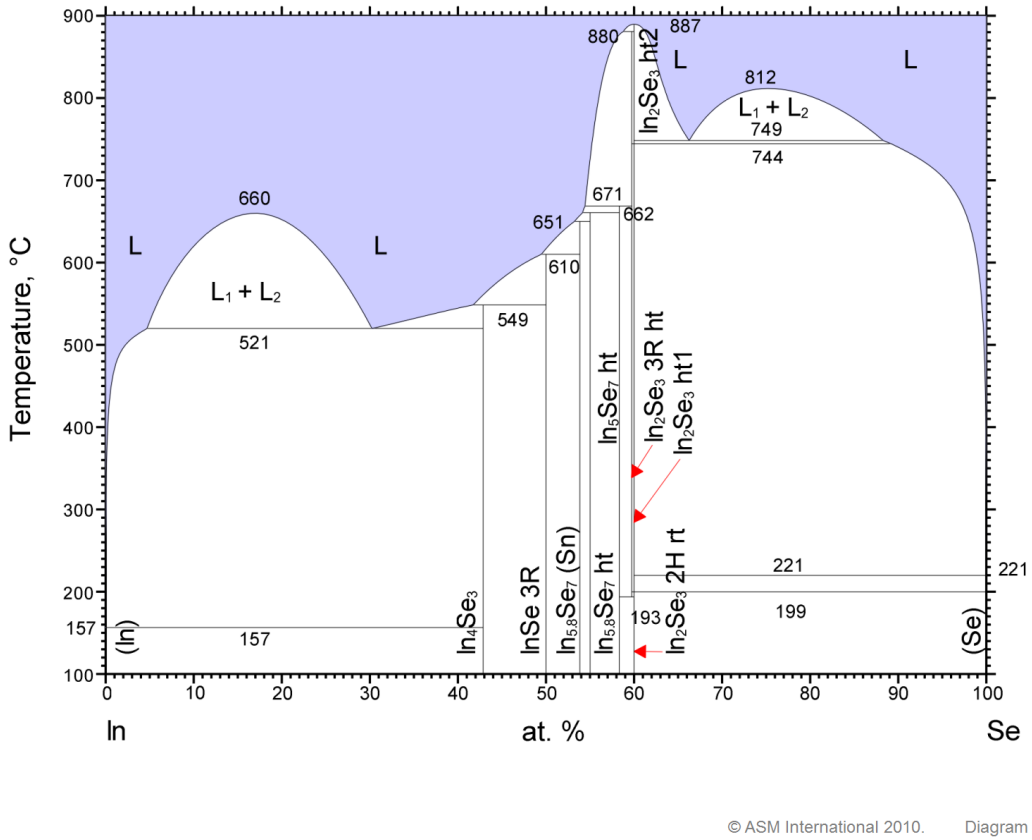


Figure 1.4: In-Se alloy phase diagram.
The various Indium-Selenium compounds grown from literature using both experimental and calculated data. Compiled by J.-B. Li, M.-C. Record, and and J.-C. Tedenac. [11]

phase also forms the 2H and 3R ($R\bar{3}m$) configuration, though the surrounding selenium in an octahedral structure.

	P63/mmc (2H)	R3m	$R\bar{3}m$	
α	x	x	x	
β	x		x	
		FE-ZB'		

Chapter 2
Sample Fabrication

2.1 Introduction

TODO: Explain about the 2D fad. Overall device construction.

2.2 Flake generation

2.2.1 Alignment marker wafer

Before fabricating any devices to test materials we needed a platform to work on that would make it easy to find flakes and manufacture devices. For this 4 inch wafers of $500\mu m$ phosphorus doped silicon with $300nm$ of thermally oxidized SiO_2 was chosen as a substrate (purchased from Si-Tech, <100> face, $\rho \lesssim 5m\omega{\cdot}cm$). The high conductivity and thermal oxide allowed us to construct a backgated field effect transistor (see: FIXME). The substrate was polished for better adhesion of deposited flakes. Using standard photolithography (see 2.3.1) we patterned the surface with a $\sim 5nm$ thin layer of titanium for adhesion then $\sim 35nm$ of gold. The metals were laid out with a repeating pattern of numbers and lines to easily identify the location of a flake on the substrate when moving between tools. We spun a layer of PMMA resist over the substrate then diced the wafer $8mm$ square chips with a ADT 7100 ProVectus Dicing Saw. This allowed us to make many devices per wafer while customizing their orientation and pattern for each flake. The resist was then removed from the chip using acetone, 2-isoproponal, and deionized (DI) water then dried using a nitrogen blow gun. To remove any residue organics

Figure 2.1: TODO: Device manufacture.

we soaked the chips in Nano-Strip (sulfuric acid and hydrogen peroxide compound, VWR) for 10 minutes, rinsed in DI-water, then repeated the initial solvent clean. After several devices experienced dialectic breakdown across the SiO_2 we changed the residue clean to an oxygen surface treatment. This was done in a M4L Plasma Processing System with 300 sccm oxygen, 100 sccm helium, at 500mTorr of pressure, and 100W for 1 minute.

2.2.2 Mechanical flake exfoliation

Flakes were exfoliated using Scotch 3M Transparent Tape. The tape was pressed into a crystal of the desired material then peeled off, resulting in a few smaller chunks of crystals adhered to the tape. The tape was then folded over itself so the crystals were pressed into two different areas of tape. The tape was then peeled apart so that the crystals would be pulled apart into multiple chunks. This process was repeated several times to provide a region roughly 8 to $10mm$ in diameter with crystal coverage. This region was then pressed into a fresh region of tape so the exposed surface of crystals was free of tape residue. The tape and crystals was then placed on a cleaned aliment marker chip to maximize the amount of crystals within the center of the chip. The tape was lightly pressed into the chip so that the crystals would be in contact with the surface of the chip. To promote adhesion to the surface, the chip was then heated for 2 minutes at $100C$. [17] The chips were then allowed to cool and the tape peeled off.

After exfoliation we scanned each chip for flakes using a Nikon Eclipse LV150 microscope. We chose $300nm$ of thermally oxidized SiO_2 to increase visibility of 2D materials under white light. [18] Flakes choice was optimized for uniformity, thinness, and lateral sizes large enough for photolithography processing. A Bruker Icon Atomic Force Microscope was used to measure flake height and develop a thickness color-code to compare new exfoliated flakes against.

TODO: tape figure, alingment mask?

2.3 Photolithography

Photolithography is a common technique used by industry and academia alike. In most variants of photolithography, a series of photosensitive polymers, or resists, are spread over a surface then exposing the polymer to light to change the chemical makeup of the polymer. This can be done by spinning a solution of the desired polymer, dissolved within a compatible solvent, at high speeds over a substrate. The solution is dripped on

the substrate either statically or dynamically, under a slower rotation. The substrate is then rotated at high speeds until the desired thickness of polymer is left on the surface, the excess being flung off the substrate edges. The solvent can then be removed by baking the substrate and polymer for a short time until a desired durability is achieved. After exposure the resist is then removed by soaking the substrate in a chemical developer. Developer selection must take into account any chemistry between the developer and flake material as some developers can react with the exposed material. For negative resists, light exposed regions of polymer are removed when developed, positive resists will only have non-exposed regions removed. For devices that change based on the flake, the resist pattern is generated on a computer and then written by a moving laser to fit the device dimensions. In commonly used patterns, a mask of chrome on quartz is prefabricated. The mask is moved over the flake then the entire surface is flooded with light at once, exposing the regions with the desired resist pattern. We typically choose a multiple layer resist stack as allowing the bottom layer dissolve long enough to undercut the top allows for easier liftoff when removing evaporated metals (See 2.5). Resist can also be used to protect part of a sample when etching allowing a patterned etch of the substrate or testing device.

2.3.1 LOR+SPR stack

The LOR+SPR negative resist stack is easy to use and allows for high resolution patterns down to $2\mu m$. Before any resist is added the substrate is given a dehydration bake of $115C$ for $60s$ to remove any water. A layer of LOR-2A is statically deposited as the first layer of the stack. The substrate is then spun at $4000RPM$ for $45s$ reducing the LOR-2A to a $\sim 200nm$ thick coating. [19] Finally we bake it at $180C$ for $60s$ on a hot plate to remove some solvent. Next a layer of SPR-3012 is dynamically dispensed at 900RPM. The substrate is then sped up and spun again at $4000RPM$ for $45s$ flattening the SPR-3012 to $\sim 1.3\mu m$ thick. [20] This is then baked for $95C$ for $60s$ on a hot plate. The resist stack and flake is then exposed using a MA/BA Gen4 or Gen2 Contact Aligner (SUSS MicroTec) with 54mW of light. The patterned resist is then developed for $60s$ in Microposit CD-26 (Tetramethylammonium hydroxide 1-5% and water, Shipley).

TODO resist stack

Table 2.1: TODO: Lithography resists

Resist	Solvent	Developer	Liftoff
LOR-2A		CD-26	Remover-PG
SPR-3012		CD-26	Remover-PG
PMMA		MIBK	Acetone/Remover-PG
SF6-slow		101A	Remover-PG

2.3.2 PMMA+PMGI+SPR stack

We found some chalcogenides reacted to alkali developers such as CD-26 [21] so we developed an alternate photolithography resist stack with a solvent used to develop the material layer. First a layer of Polymethyl methacrylate (PMMA) (-2A Microchem) is statically deposited, spun at $2500RPM$ for $45s$ to give a $\sim 600nm$ layer, then baked at $180C$ for $180s$. [22] Next a layer of PMGI SF6-slow is dynamically spun at $900RPM$, then $4000RPM$ for $45s$ to reduce the thickness to $\sim 300nm$, and baked at $180C$ for $60s$. [23] Finally, a top-coat of SPR-3012 is dynamically dispensed at 900RPM. This is then spun at $4000RPM$ for $45s$ for a thickness $\sim 1.3\mu m$ and baked for $95C$ for 60s. The SPR-3012 is then exposed using a MA/BA Contact aligner with 54mW of light (peak $365nm$), developed for $60s$ in in Microposit CD-26 from Shipley (2.3.1), then rinsed in water. The PMMA and SF6 under-layers are exposed for 30 minutes in a Deep UV (peak $270nm$, OAI Deep UV Flood Exposure) at 5.3mW (~9.5J). The SF6 is developed in 101A developer (Microchem) for $90s$ then rinsed in water. Finally the PMMA is developed for 10 minutes in methyl isobutyl ketone (MIBK) and a trace amount of water. The substrate is moved though the water for $30 - 60s$ to remove a thin film that forms, causing the film to pull off. The MIBK is then removed with 2-proponal.

An alternate version of this process used a thicker PMMA (6A) with SPR-3012 on top. Because the SPR uses a PMMA-compatible solvent (Cyclopentanone) the two layers would intermix and form a layer that was unable to be dissolved in either developer. This was removed by ashing the layer for 8:35 minutes in the M4L with 250 sccm oxygen, 50 sccm helium, 500mTorr pressure, 450W power. This process varied greatly depending on polymer uniformity and location of device on the substrate so later devices included the PMGI SF6 layer to eliminate the inconsistency.

TODO: figure resist stack

2.4 Thin filament shadow mask

As an alternative to lithography, we used an all-dry quartz filament shadow mask for metal evaporation (2.5). This allowed us to test contact resistance of an underlying material without introducing the polymers, chemicals, and processing to the material that may damage the surface or leave a residue between the material and metal contacts. We heated two quartz rod ends with an acetylene torch until semi-molten. We then lightly touched the two ends together and quickly pulled the ends apart within the flame. If done correctly, this produced several $2 - 10cm$ long strands of quartz that were $< 2\mu m$ in diameter. These were identified under a florescent light by their thread-like behavior, losing most stiffness and free to float in the air when $\lesssim 2\mu m$ in diameter. These filaments were then caught on glass forks by dragging the filament across the opening and snapping the end attached to the quartz rod. The forks were cut to fit over the sides of our sample chip substrates and reinforced with metal for durability. The sample chip was attached to a glass slide with double-sided tape. These filaments were then draped over the sample material with the glass fork. The ends of the filament were then cut with a tungsten needle and the glass fork removed. The filament could be adjusted by pulling it gently with a thin copper wire until it was in place and laying flat against the surface. This often caused the quartz to snap so the range of movement was limited to within a few 10s of microns from where it started. Once the filament was maneuvered it was fixed in place by wrapping the ends in Teflon tape that wrapped around the glass slide. Teflon tape was chosen as it is unlikely to scratch the material and has no adhesive that would cause the filament to move when securing it. The tape was also used to reduce the exposed area so only a small region around the material was included and reduce the risk of a short between the two sides. We found a filament less than $.5\mu$ tended to cause a short between the two sides while greater than $3\mu m$ would not sit flush against the surface. Metal choice is similarly important as certain metals like indium tended to "wet" across the surface and short at any diameter.

TODO: figure filiment device, undercut with indium

2.5 Metal evaporation and liftoff

Metal deposition was done using the Lab-18 Thin Film Deposition System (Kurt J. Lesker Co.). This was used to add contacts to a lithography-patterned flake by covering a substrate with layers of metal. We used electron beam evaporated titanium and gold

for the uniform deposition and high conductivity. First $\sim 5nm$ of titanium was deposited at $\sim 1\mathring{A}/s$ as titanium adheres well to SiO_2. Next a layer of $35 - 50nm$ of gold was evaporated at $\sim 1\mathring{A}/s$ on top of the titanium. The gold provided a highly conductive protective layer that was inert in atmosphere and safe to use when wiring samples.

The Lab-18 Thin Film Deposition System also had an in situ ion source that could be used to clean and roughen the surface of a material before deposition occurred. A typical process used $10sccm$ of argon gas flowed over a metal coil with $2.5A$ of emission current and $150V$ between the coil and the substrate. The ion source is undirected which caused trace amounts of iron from the chamber itself to be knocked loose and deposited on the surface of the sample.

To remove excess metals from the substrate the lithography resist was then removed though a 'liftoff' process. The resist stacks were designed to have a small undercut between the top and bottom layer to allow solvents to dissolve the resists from the edges even if metal had deposited on the sides of the upper layers. For LOR-based (see 2.3.1) stacks the substrate was soaked in heated Remover-PG (Microchem) for 10 minutes at $60C$. The Remover-PG was then gently blown with a pipette over the surface of the substrate to push away any metals that were no longer adhered to resist. This process was repeated until all of the resist and metal adhered to it were removed. As smaller features had less surface area of resist for the solvent to resolve, more forceful streams were sometimes needed. If this was not enough to peel off the resist, sonication in a water bath was sometimes used. This often pulled off the metals deposited on the substrate, flake, or even the flake itself, so was used only when necessary. The Remover-PG was then removed by soaking the material in 2-proponal for 5 minutes and blow-dried with a nitrogen gun. For PMMA based stacked unheated acetone was used in the place of Remover-PG while the rest of the process was the same.

2.6 Wiring

Lithography wiring patterns were designed with $.5 - 1mm$ square pads that connected to metal leads on the sample material. To connect this to a preexisting wiring system we used a series of indium dots and thin gold wires (99.95% Au, $25\mu m$, Alfa Aesar). To avoid any currents damaging the sample, we first adhered the wire to the wiring structure with lead-free solder. Next we placed an indium dot (FIXME source) on each of the sample wiring pads using a modified tweezer. The tweezer was cut so that only one prong remained, then the tip cut flat and further sanded smooth with the side of a razor blade.

This allowed the indium dot to adhere to the tip easily and for the modified tweezer to be held similar to a pen for increased dexterity and use with samples in recessed mounts. The gold wire was then bent down and pushed into the indium dot and a second indium dot was pressed into the first, forming a sandwich-like structure, that held the gold wire in place. The gold wire was then bent from the sample to prevent it from coming into contact with any part of the sample or other wires. This process was repeated for each of the wiring pads on the device.

To prevent static discharge from damaging the flake several measures were taken. A ionizing fan (Chapman VSE3000 static eliminator) was constantly blown across the sample and wiring station at all times. The person wiring was grounded with a static wrist strap to the building ground at all times when touching the device. The modified tweezer was held without gloves to connect it to the building ground though the body. The wiring station used a rubber floor mat with metal stool to isolate the person from the floor and prevent any charge buildup from the ground. Finally, clothing was chosen to reduce the buildup of static, especially in winter as the dryer air made hazardous amounts of static buildup fairly frequent. [10]

TODO: figure, wiring

2.7 Layer Transfer?

Appendix A
3D crystal symmetry groups

There are a total of 32 possible 3D crystal point groups. The following table lists the groups and are colored according to related phenomena:

- Pyroelectrics, possible ferroelectrics: 1, 2, m, mm2, 3, 3m, 4, 4mm, 6, 6mm
- Piezoelectrics only: 222, $\bar{4}$, 422, $\bar{4}2\mathrm{m}$, 32, $\bar{6}$, 622, $\bar{6}\mathrm{m}2$, 23, $\bar{4}3\mathrm{m}$
- Non-centrosymmetric and non-piezoelectric: O
- Centrosymmetric: $\bar{1}$, 2/m, mmm, 4/m, 4/mmm, $\bar{3}$, $\bar{3}\mathrm{m}$, 6/m, 6/mmm, m3, $\mathrm{m}\bar{3}\mathrm{m}$

Table A.1: 3D crystal classes [1]

Crystal system	#	Point group			Space groups
		Hermann–Mauguin	Schoen-flies	Order	
Triclinic	1	1	C_1	1	$P1$
	2	$\bar{1}$	C_i	2	$P\bar{1}$
Monoclinic	3–5	2	C_2	2	$P2$, $P2_1$, $C2$
	6–9	m	C_s	2	Pm, Pc, Cm, Cc
	10–15	2/m	C_{2h}	4	$P2/m$, $P2_1/m$,

					$C2/m$, $P2/c$, $P2_1/c$, $C2/c$
Orthorhombic	16–24	222	D_2	4	$P222$, $P222_1$, $P2_12_12_1$, $C222_1$, $C222$, $F222$, $I222$, $I2_12_12_1$
	25–46	mm2	C_{2v}	4	$Pmm2$, $Pmc2_1$, $Pcc2$, $Pma2$, $Pca2_1$, $Pnc2$, $Pmn2_1$, $Pba2$, $Pna2_1$, $Pnn2$, $Cmm2$, $Cmc2_1$, $Ccc2$, $Amm2$, $Aem2$, $Ama2$, $Aea2$, $Fmm2$, $Fdd2$, $Imm2$, $Iba2$, $Ima2$
	47–74	mmm	D_{2h}	8	$Pmmm$, $Pnnn$, $Pccm$, $Pban$, $Pmma$, $Pnna$, $Pmna$, $Pcca$, $Pbam$, $Pccn$, $Pbcm$, $Pnnm$, $Pmmn$, $Pbcn$, $Pbca$, $Pnma$, $Cmcm$, $Cmce$, $Cmmm$, $Cccm$, $Cmme$, $Ccce$, $Fmmm$, $Fddd$, $Immm$, $Ibam$, $Ibca$, $Imma$
Tetragonal	75–80	4	C_4	4	$P4$, $P4_1$, $P4_2$, $P4_3$, $I4$, $I4_1$
	81–82	$\bar{4}$	S_4	4	$P\bar{4}$, $I\bar{4}$
	83–88	4/m	C_{4h}	8	$P4/m$, $P4_2/m$, $P4/n$, $P4_2/n$, $I4/m$, $I4_1/a$
	89–98	422	D_4	8	$P422$, $P42_12$, $P4_122$, $P4_12_12$, $P4_222$, $P4_22_12$, $P4_322$, $P4_32_12$, $I422$, $I4_122$
	99–110	4mm	C_{4v}	8	$P4mm$, $P4bm$, $P4_2cm$, $P4_2nm$, $P4cc$, $P4nc$, $P4_2mc$, $P4_2bc$, $I4mm$, $I4cm$,$I4_1md$, $I4_1cd$
	111–122	$\bar{4}$2m	D_{2d}	8	$P\bar{4}2m$, $P\bar{4}2c$, $P\bar{4}2_1m$, $P\bar{4}2_1c$, $P\bar{4}m2$, $P\bar{4}c2$,

					$P\bar{4}b2$, $P\bar{4}n2$, $I\bar{4}m2$, $I4\bar{c}2$, $I\bar{4}2m$, $I\bar{4}2d$
	123–142	4/mmm	D_{4h}	16	$P4/mmm$, $P4/mcc$, $P4/nbm$, $P4/nnc$, $P4mbm$, $P4/mnc$, $P4/nmm$, $P4/ncc$, $P4_2/mmc$, $P4_2/mcm$, $P4_2/nbc$, $P4_2/nnm$, $P4_2/mbc$, $P4_2/mnm$, $P4_2/nmc$, $PP4_2/ncm$, $I4/mmm$, $I4/mcm$, $I4_1/amd$, $I4_1/acd$
Trigonal	143–146	3	C_3	3	$P3$, $P3_1$, $P3_2$, $R3$
	147–148	$\bar{3}$	S_6	6	$P\bar{3}$, $R\bar{3}$
	149–155	32	D_3	6	$P312$, $P321$, $P3_112$, $P3_121$, $P3_212$, $P3_221$, $R32$
	156–161	3m	C_{3v}	6	$P3m1$, $P31m$, $P3c1$, $P31c$ $R3m$, $R3c$
	162–167	$\bar{3}$m	D_{3d}	12	$P\bar{3}1m$, $P\bar{3}1c$, $P\bar{3}m1$, $P\bar{3}c1$, $R\bar{3}m$, $R\bar{3}c$
Hexagonal	168–173	6	C_6	6	$P6$, $P6_1$, $P6_5$, $P6_2$, $P6_4$,$P6_3$,
	174	$\bar{6}$	C_{3h}	6	$P\bar{6}$
	175–176	6/m	C_{6h}	12	$P6/m$, $P6_3/m$
	177–182	622	D_6	12	$P622$, $P6_122$, $P6_522$, $P6_222$, $P6_422$, $P6_322$
	183–186	6mm	C_{6v}	12	$P6mm$, $P6cc$, $P6_3cm$, $P6_3mc$
	187–190	$\bar{6}$m2	D_{3h}	12	$P6\bar{m}2$,$P\bar{6}m2$, $P\bar{6}2m$, $P\bar{6}2c$
	191–194	6/mmm	D_{6h}	24	$P6/mmm$, $P6/mcc$, $P6_3/mcm$, $P6_3/mmc$
Cubic	195–199	23	T	12	$P23$, $F23$, $I23$,

				$P2_13$, $I2_13$
200–206	m$\bar{3}$	T_h	24	$Pm\bar{3}$, $Pn\bar{3}$, $Fm\bar{3}$, $Fd\bar{3}$, $Im\bar{3}$, $Pa\bar{3}$, $Ia\bar{3}$
207–214	432	O	24	$P432$, $P4_232$, $F432$, $F4_132$, $I432$, $P4_332$, $P4_132$, $I4_132$
215–220	$\bar{4}$3m	T_d	24	$P\bar{4}3m$, $F\bar{4}3m$, $I\bar{4}3m$, $P\bar{4}3n$, $F\bar{4}3c$, $I\bar{4}3d$
221–230	m$\bar{3}$m	O_h	48	$Pm\bar{3}m$, $Pn\bar{3}n$, $Pm\bar{3}n$, $Pn\bar{3}m$, $Fm\bar{3}m$, $Fm\bar{3}c$, $Fd\bar{3}m$, $Fd\bar{3}c$, $Im\bar{3}m$, $Ia\bar{3}d$

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Vita

Your Name

The details of my childhood are inconsequential.