Design Project 4: Simple Computer Assembly Language Programming

Jamahl Savage Last Four Digits of Student ID: 3855

ECE 2504: Introduction to Computer Engineering

December 3, 2018

The Source Code: *Comments are in green

```
// Starter source code program for ECE 2504
// Project 4
//
// File: starter-program FINAL VER.txt
// Description: This text file implements the small assembly language program to process
// the values stored in an array in the data memory. The program uses two for loops to find the maximum
// and the minimum value in n length array
//
// The code will be used to display:
// 1. The location of the first array element (pointer to the array) (Data Memory Location: 00)
// 2. The length of the array (Data Memory Location: 01)
// 3. The Maximum value in the array (Data Memory Location: 02)
// 4. The Minimum value in the array (Data Memory Location: 03)
// 5. The Last four digits of my Student ID (Data Memory Location: 04)
// The registers used in this program are used as follows:
// r0 - Mainly as the zero register. At times was used for controlling when the program needed to skip over
// parts of code.( Act like an if-else)
// r1 - x (the for loop counter)
// r2 - y (the array pointer)
// r3 - the data memory pointer. Was also used to hold the result of some of the comparisons (brz
// statements)
// r4 - used to hold the current max or min
// r5 - used as the bit mask. Was also used to hold the result of whether the bits during a comparison
// were the same (brz statements)
// r6 - used to hold the next value in the array element
// r7 - was free to use for many purpose (No specific role)
// Created: 11/28/2018, Jamahl Savage, Virginia Tech
// Student ID Last Four Digits: 3855
ldi r0, 4
shl r0, r0
```

```
shl r0, r0
jmp r0
// The following set of load instructions read the final values of the variables in
// memory locations into r1-r5 so that we can see them on the LEDs.
// Your code must jump to this point after it has stored the results in data memory.
// You should jump to location 4.
// address 0x04
xor r0, r0, r0
ld r1, r0
                          //r1 < -M[0x00]
inc r0, r0
ld r2, r0
                          //r2 < -M[0x01]
inc r0, r0
ld r3, r0
                          //r3 < -M[0x02]
inc r0, r0
ld r4, r0
                          //r4 < -M[0x03]
inc r0, r0
ld r5, r0
                          //r5 < -M[0x04]
                          // Now loop forever
ldi r0, 0
                          //The address of this brz is the one used in validation: Address 0x0F.
brz r0, 0
                          // Your last instruction should be a jump to location 4
                          // in order to read the variables into registers r1-r5.
                          // address 0x10
//creating the last 4 digits of the student ID (3855) and storing them while using register 5 as a pointer to
memory location 4
ldi r6, 3
shl r6, r6
shl r6, r6
shl r6, r6
shl r6, r6
adi r6, r6, 7
adi r6, r6, 1
                          //this will now make it 8
shl r6, r6
```

```
shl r6, r6
shl r6, r6
shl r6, r6
adi r6, r6, 5
shl r6, r6
shl r6, r6
shl r6, r6
shl r6, r6
adi r6, r6, 5
ldi r3, 4
                         //r3 points to the memory address 4, which the student id should be stored in
st r3, r6
//Create a zero register: r0
ldi r0, 0
//derive a for loop counter (x): r1
// derive a general DM pointer: r3
ldi r3, 1
ld r1, r3
                         //r1 = x
                //This allows us to start with the comparison of the current max and the next
dec r1, r1
                 // value without over iterating
//derive an array poiner(y): r2
ldi r3, 0
                         //r2 = y
ld r2, r3
//derive a max and min: r4
ld r4, r2
                         //register 4(the max holder) is initialized to be the first value in the array
//START OF THE FOR LOOP
                         // i = 1
inc r2, r2
ld r6, r2
                         //r6 = a[i] the next value in the array
//CREATE THE MASK USED FOR ONLY COMPARING THE SIGN OF THE FPs
ldi r5, 7
                         //Now is the value 8
adi r5,r5, 1
shl r5, r5
shl r5, r5
shl r5, r5
shl r5, r5
```

adi r5, r5, 0	
shl r5, r5	
adi r5, r5, 0	
shl r5, r5	
adi r5, r5, 0	//the mask is now equal to 8000 in hex which is 16'b1000 0000 0000 0000
and r7, r4, r5	//Using a selective hold or mask to only maintain the sign bit of the current max. It // will be held in r7 for later comparison
shr r7, r7	//We will have to shift the bit to the right one so that it is at location 15 of the 16 bit // number (therefore there will only be positive values for comparing)
	//r5 will no longer be need for bit masking at this point so we can use for holding the // result of the bit masking of the next value in the array
and r5, r6, r5	//Using a selective hold or mask to only maintain the sign bit of the next value in // the array. It will be held in r5 for later comparison
shr r5, r5	//We will also have to shift the bit to the right so that it is at location 15 of the 16 bit // number (therefore there will only be positive values for comparing)
	//Next we will check to make sure the max and the next value in the array DON'T have // the same sign and the result of the comparison will be stored in r3
xor r3, r5, r7	
	//Now we use brz to determine whether the max and the next value in the array have the // same sign
brz r3, 8	//IF they have the same sign as each other $(r3 = 0)$ then we must continue checking the // rest of the bits
	//ELSE we will check whether the max or the next value in the array is greater through // means of subtraction
sub r3, r7, r5	
brn r3, 3	// If this fails then that means the current max had a 1 as it's sign, thus meaning it was // negative. Therefore not the max.
add r4, r0, r6	// This means that brn failed and that the next value in the array was the one with a 0 as // its sign, thus meaning it was positive.
brz r0, 2	// TO THE END OF ALL THE IF ELSE STATEMENTS SO THAT SKIPS TO THE // INCREMENTING AND DECREMENTING

add r4, r0, r4 // If brn passes that means that the current max had a 0 as its sign, thus meaning it was // positive. There the current max remains the max

brz r0, 30 // TO THE END OF ALL THE IF ELSE STATEMENTS SO THAT SKIPS TO THE // INCREMENTING AND DECREMENTING

brz r0, -30 // TO THE BEGINNING OF ALL THE IF ELSE STATEMENTS SO THAT IT CONTINUES // THE LOOP

//THIS WILL MARK THE END OF CHECKING THE SIGNS OF THE MAX AND THE NEXT VALUE IN //THE ARRAY. WE WILL NOW PROCEED TO CHECKING THE 4 BITS OF THE EXPONENT OF THE //CURRENT MAX AND THE NEXT VALUE IN THE ARRAY IF NECESSARY

ldi r0, 1

ldi r5, 7

shl r5, r5

shl r5, r5

shl r5, r5

shl r5, r5

adi r5, r5, 7

adi r5, r5, 1 //Now the value is 8

shl r5, r5

shl r5, r5

shl r5, r5

shl r5, r5

adi r5, r5, 0

shl r5, r5

shl r5, r5

shl r5, r5

shl r5, r5

adi r5, r5, 0 //the mask is now equal to 7800 in hex which is 16'b0111 1000 0000 0000

and r7, r4, r5 //Using a selective hold or mask to only maintain the exponent bits of the current max. It // will be held in r7 for later comparison

//r5 will no longer be need for bit masking at this point so we can use for maintaining the // result of the bit masking of the next value in the array

and r5, r6, r5 //Using a selective hold or mask to only maintain the exponent bits of the next value in // the array. It will be held in r5 for later comparison

//Next we will check to make sure the max and the next value in the array DON'T have // the same exponent bits and the result of the comparison will be stored in r3

xor r3, r5, r7

//Now we use brz to determine whether the max and the next value in the array have the // same exponent bits brz r3, 9 //IF they have the same exponent bits as each other (r3 = 0) then we must continue // checking the rest of the bits //ELSE we will check whether the max or the next value in the array is greater through // means of subtraction ldi r0, 0 sub r3, r7, r5 brn r3, 3 //If this fails then that means the current max has a larger exponent thus it stays as the // max add r4, r0, r4 //The max shall stay the new max // TO THE END OF ALL THE IF ELSE STATEMENTS SO THAT SKIPS TO THE brz r0, 2 // INCREMENTING AND DECREMENTING //If brn passed then that means the next value in the array had a larger exponent and add r4, r0, r6 // thus should become the max brz r0, 3 // TO THE END OF ALL THE IF ELSE STATEMENTS SO THAT SKIPS TO THE // INCREMENTING AND DECREMENTING // TO THE BEGINNING OF ALL THE IF ELSE STATEMENTS SO THAT IT CONTINUES brz r0. -30 // THE LOOP //THIS WILL MARK THE END OF CHECKING THE 4 BITS OF THE EXPONENT OF THE MAX AND //THE NEXT VALUE IN THE ARRAY. WE WILL NOW PROCEED TO CHECKING THE 11 BITS OF THE //MANTISSA OF THE CURRENT MAX AND THE NEXT VALUE IN THE ARRAY IF NECESSARY ldi r0, 1 brz r0, 30 // TO THE END OF ALL THE IF ELSE STATEMENTS SO THAT SKIPS TO THE // INCREMENTING AND DECREMENTING brz r0, -3 // TO THE BEGINNING OF ALL THE IF ELSE STATEMENTS SO THAT IT CONTINUES // THE LOOP ldi r5, 0 shl r5, r5 shl r5, r5 shl r5, r5 shl r5, r5 adi r5, r5, 7 shl r5, r5 shl r5, r5 shl r5, r5 shl r5, r5 adi r5, r5, 7

adi r5, r5, 1 shl r5, r5 adi r5, r5, 7 adi r5, r5, 7 adi r5, r5, 1 //Now the value 15 //the mask is now equal to 07FF in hex which is 16'b0000 0111 1111 1111 and r7, r4, r5 //the mask is now equal to 07FF in hex which is 16'b0000 0111 1111 1111 and r7, r4, r5 //Using a selective hold or mask to only maintain the mantissa bits of the current // max. It will be held in r7 for later comparison //r5 will no longer be need for bit masking at this point so we can use for // maintaining the result of the bit masking at this point so we can use for // maintaining the result of the bit masking at this point so we can use for // maintaining the result of the bit masking at this point so we can use for // maintaining the result of the bit masking at this point so we can use for // walue in the array and r5, r6, r5 //Using a selective hold or mask to only maintain the mantissa bits of the next // value in the array. It will be held in r5 for later comparison //Next we will check to make sure the max and the next value in the array DONT have // the same mantissa bits and the result of the comparison will be stored in r3 xor r3, r5, r7 //Now we use brz to determine whether the max and the next value in the array have the // same mantissa bits brz r3, 9 ///IF they have the same mantissa bits as each other (r3 = 0) then the current max and the // next value in the array must be the same, thus we can just maintain the same max //ELSE we will check whether the max or the next value in the array is greater through // max ame mantissa bits as each other (r3 = 0) then the current max and the // next value in the array must be the same, thus we can just maintain the same max ///ELSE we will check whether the max or the next value in the array is greater through // max ame mantissa bits as each other (r3 = 0) then the current max and the // next value in the array had a larger mantissa the // max ame mantissa bits of the current max has a la	adi r5, r5, 7	
shl r5, r5 adi r5, r5, 7 adi r5, r5, 7 adi r5, r5, 7 adi r5, r5, 11 //Now the value 15 //the mask is now equal to 07FF in hex which is 16'b0000 0111 1111 1111 and r7, r4, r5 //Using a selective hold or mask to only maintain the mantissa bits of the current // max. It will be held in r7 for later comparison //r5 will no longer be need for bit masking at this point so we can use for // maintaining the result of the bit masking of the next value in the array and r5, r6, r5 //Using a selective hold or mask to only maintain the mantissa bits of the next // value in the array. It will be held in r5 for later comparison //Next we will check to make sure the max and the next value in the array DON'T have // the same mantissa bits and the result of the comparison will be stored in r3 xor r3, r5, r7 //Now we use brz to determine whether the max and the next value in the array have the // same mantissa bits brz r3, 9 ///F they have the same mantissa bits as each other (r3 = 0) then the current max and the // next value in the array must be the same, thus we can just maintain the same max // ELSE we will check whether the max or the next value in the array is greater through // means of subtraction Idi r0, 0 sub r3, r7, r5 brn r3, 3 ///If this fails then that means the current max has a larger mantissa thus it remains the // max add r4, r0, r4 // The current max shall remain as the max brz r0, 4 // TO THE END OF ALL THE IF ELSE STATEMENTS SO THAT SKIPS TO THE // INCREMENTING AND DECREMENTING add r4, r0, r6 /// If brn passed then that means the next value in the array had a larger mantissa and thus // should be made the new max // TO THE END OF ALL THE IF ELSE STATEMENTS SO THAT SKIPS TO THE // INCREMENTING AND DECREMENTING brz r0, -32 // TO THE BEGINNING OF ALL THE IF ELSE STATEMENTS SO THAT SKIPS TO THE // INCREMENTING AND DECREMENTING	adi r5, r5, 1	//Now the value is 15
shl r5, r5 shl r5, r5 adi r5, r5, 7 adi r5, r5, 7 adi r5, r5, 1 //Now the value 15 //the mask is now equal to 07FF in hex which is 16'b0000 0111 1111 1111 and r7, r4, r5 //Using a selective hold or mask to only maintain the mantissa bits of the current // max. It will be held in r7 for later comparison //r5 will no longer be need for bit masking at this point so we can use for // maintaining the result of the bit masking of the next value in the array and r5, r6, r5 //Using a selective hold or mask to only maintain the mantissa bits of the next // value in the array. It will be held in r5 for later comparison //Next we will check to make sure the max and the next value in the array DON'T have // the same mantissa bits and the result of the comparison will be stored in r3 xor r3, r5, r7 XNOW we use brz to determine whether the max and the next value in the array have the // same mantissa bits brz r3, 9 /// F they have the same mantissa bits as each other (r3 = 0) then the current max and the // next value in the array must be the same, thus we can just maintain the same max //ELSE we will check whether the max or the next value in the array is greater through // means of subtraction Idi r0, 0 sub r3, r7, r5 brn r3, 3 /// this fails then that means the current max has a larger mantissa thus it remains the // max add r4, r0, r4 // The current max shall remain as the max brz r0, 4 // TO THE END OF ALL THE IF ELSE STATEMENTS SO THAT SKIPS TO THE // INCREMENTING AND DECREMENTING brz r0, -32 // TO THE END OF ALL THE IF ELSE STATEMENTS SO THAT SKIPS TO THE // INCREMENTING AND DECREMENTING brz r0, -32 // TO THE END OF ALL THE IF ELSE STATEMENTS SO THAT SKIPS TO THE // INCREMENTING AND DECREMENTING brz r0, -32 // TO THE END OF ALL THE IF ELSE STATEMENTS SO THAT SKIPS TO THE // INCREMENTING AND DECREMENTING brz r0, -32 // TO THE BEGINNING OF ALL THE IF ELSE STATEMENTS SO THAT IT CONTINUES	shl r5, r5	
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and r7, r4, r5 //Using a selective hold or mask to only maintain the mantissa bits of the current // max. It will be held in r7 for later comparison //r5 will no longer be need for bit masking at this point so we can use for // maintaining the result of the bit masking of the next value in the array and r5, r6, r5 //Using a selective hold or mask to only maintain the mantissa bits of the next // value in the array. It will be held in r5 for later comparison //Next we will check to make sure the max and the next value in the array DON'T have // the same mantissa bits and the result of the comparison will be stored in r3 xor r3, r5, r7 //Now we use brz to determine whether the max and the next value in the array have the // same mantissa bits brz r3, 9 //IF they have the same mantissa bits as each other (r3 = 0) then the current max and the // next value in the array must be the same, thus we can just maintain the same max //ELSE we will check whether the max or the next value in the array is greater through // means of subtraction Idi r0, 0 sub r3, r7, r5 brn r3, 3 //If this fails then that means the current max has a larger mantissa thus it remains the // max add r4, r0, r4 // The current max shall remain as the max brz r0, 4 // TO THE END OF ALL THE IF ELSE STATEMENTS SO THAT SKIPS TO THE // INCREMENTING AND DECREMENTING brz r0, -32 // TO THE BEGINNING OF ALL THE IF ELSE STATEMENTS SO THAT SKIPS TO THE // INCREMENTING AND DECREMENTING brz r0, -32 // TO THE BEGINNING OF ALL THE IF ELSE STATEMENTS SO THAT SKIPS TO THE	adi r5, r5, 1	//Now the value 15
// max. It will be held in r7 for later comparison //r5 will no longer be need for bit masking at this point so we can use for // maintaining the result of the bit masking of the next value in the array and r5, r6, r5 //Using a selective hold or mask to only maintain the mantissa bits of the next // value in the array. It will be held in r5 for later comparison //Next we will check to make sure the max and the next value in the array DON'T have // the same mantissa bits and the result of the comparison will be stored in r3 xor r3, r5, r7 //Now we use brz to determine whether the max and the next value in the array have the // same mantissa bits brz r3, 9 //IF they have the same mantissa bits as each other (r3 = 0) then the current max and the // next value in the array must be the same, thus we can just maintain the same max //ELSE we will check whether the max or the next value in the array is greater through // means of subtraction ldi r0, 0 sub r3, r7, r5 brn r3, 3 //If this fails then that means the current max has a larger mantissa thus it remains the // max add r4, r0, r4 // The current max shall remain as the max brz r0, 4 // TO THE END OF ALL THE IF ELSE STATEMENTS SO THAT SKIPS TO THE // INCREMENTING AND DECREMENTING add r4, r0, r6 /// TO THE END OF ALL THE IF ELSE STATEMENTS SO THAT SKIPS TO THE // INCREMENTING AND DECREMENTING brz r0, -32 // TO THE BEGINNING OF ALL THE IF ELSE STATEMENTS SO THAT SKIPS TO THE		//the mask is now equal to 07FF in hex which is 16'b0000 0111 1111 1111
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// value in the array. It will be held in r5 for later comparison //Next we will check to make sure the max and the next value in the array DON'T have // the same mantissa bits and the result of the comparison will be stored in r3 xor r3, r5, r7 //Now we use brz to determine whether the max and the next value in the array have the // same mantissa bits brz r3, 9 //IF they have the same mantissa bits as each other (r3 = 0) then the current max and the // next value in the array must be the same, thus we can just maintain the same max //ELSE we will check whether the max or the next value in the array is greater through // means of subtraction Idi r0, 0 sub r3, r7, r5 brn r3, 3 //If this fails then that means the current max has a larger mantissa thus it remains the // max add r4, r0, r4 //The current max shall remain as the max brz r0, 4 // TO THE END OF ALL THE IF ELSE STATEMENTS SO THAT SKIPS TO THE // INCREMENTING AND DECREMENTING add r4, r0, r6 //If brn passed then that means the next value in the array had a larger mantissa and thus // should be made the new max brz r0, 2 // TO THE END OF ALL THE IF ELSE STATEMENTS SO THAT SKIPS TO THE // INCREMENTING AND DECREMENTING brz r0, -32 // TO THE BEGINNING OF ALL THE IF ELSE STATEMENTS SO THAT SKIPS TO THE // INCREMENTING AND DECREMENTING		
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// next value in the array must be the same, thus we can just maintain the same max //ELSE we will check whether the max or the next value in the array is greater through // means of subtraction Idi r0, 0 sub r3, r7, r5 brn r3, 3 //If this fails then that means the current max has a larger mantissa thus it remains the // max add r4, r0, r4 //The current max shall remain as the max brz r0, 4 // TO THE END OF ALL THE IF ELSE STATEMENTS SO THAT SKIPS TO THE // INCREMENTING AND DECREMENTING add r4, r0, r6 //If brn passed then that means the next value in the array had a larger mantissa and thus // should be made the new max brz r0, 2 // TO THE END OF ALL THE IF ELSE STATEMENTS SO THAT SKIPS TO THE // INCREMENTING AND DECREMENTING brz r0, -32 // TO THE BEGINNING OF ALL THE IF ELSE STATEMENTS SO THAT IT CONTINUES		·
Idi r0, 0 sub r3, r7, r5 brn r3, 3	brz r3, 9	
sub r3, r7, r5 brn r3, 3		
brn r3, 3 //If this fails then that means the current max has a larger mantissa thus it remains the // max add r4, r0, r4 //The current max shall remain as the max brz r0, 4 // TO THE END OF ALL THE IF ELSE STATEMENTS SO THAT SKIPS TO THE // INCREMENTING AND DECREMENTING add r4, r0, r6 //If brn passed then that means the next value in the array had a larger mantissa and thus // should be made the new max brz r0, 2 // TO THE END OF ALL THE IF ELSE STATEMENTS SO THAT SKIPS TO THE // INCREMENTING AND DECREMENTING brz r0, -32 // TO THE BEGINNING OF ALL THE IF ELSE STATEMENTS SO THAT IT CONTINUES	ldi r0, 0	
add r4, r0, r4 //The current max shall remain as the max brz r0, 4 // TO THE END OF ALL THE IF ELSE STATEMENTS SO THAT SKIPS TO THE // INCREMENTING AND DECREMENTING add r4, r0, r6 //If brn passed then that means the next value in the array had a larger mantissa and thus // should be made the new max brz r0, 2 // TO THE END OF ALL THE IF ELSE STATEMENTS SO THAT SKIPS TO THE // INCREMENTING AND DECREMENTING brz r0, -32 // TO THE BEGINNING OF ALL THE IF ELSE STATEMENTS SO THAT IT CONTINUES	sub r3, r7, r5	
brz r0, 4 // TO THE END OF ALL THE IF ELSE STATEMENTS SO THAT SKIPS TO THE // INCREMENTING AND DECREMENTING add r4, r0, r6 //If brn passed then that means the next value in the array had a larger mantissa and thus // should be made the new max brz r0, 2 // TO THE END OF ALL THE IF ELSE STATEMENTS SO THAT SKIPS TO THE // INCREMENTING AND DECREMENTING brz r0, -32 // TO THE BEGINNING OF ALL THE IF ELSE STATEMENTS SO THAT IT CONTINUES	brn r3, 3	
## INCREMENTING AND DECREMENTING add r4, r0, r6 ## Increment with the interval of the array had a larger mantissa and thus ## should be made the new max brz r0, 2 ## TO THE END OF ALL THE IF ELSE STATEMENTS SO THAT SKIPS TO THE ## INCREMENTING AND DECREMENTING brz r0, -32 ## TO THE BEGINNING OF ALL THE IF ELSE STATEMENTS SO THAT IT CONTINUES	add r4, r0, r4	//The current max shall remain as the max
// should be made the new max brz r0, 2 // TO THE END OF ALL THE IF ELSE STATEMENTS SO THAT SKIPS TO THE // INCREMENTING AND DECREMENTING brz r0, -32 // TO THE BEGINNING OF ALL THE IF ELSE STATEMENTS SO THAT IT CONTINUES	brz r0, 4	
// INCREMENTING AND DECREMENTING brz r0, -32 // TO THE BEGINNING OF ALL THE IF ELSE STATEMENTS SO THAT IT CONTINUES	add r4, r0, r6	
·	brz r0, 2	
	brz r0, -32	

//THIS WILL MARK THE END OF COMPARISON ALGORITHM.

//Decrement the counter to indicate that I have completed an iteration also increment // second counter (register 6) for going through the values in the array

inc r2, r2 //ptr++ (array pointer++)

dec r1, r1 //loop counter--

//Check the value of the counter register to see if it's done with the for loop. If it's done go // 2 spots forward in the instructions and continue,

//else move forward once in the instructions (brz r0 will cause it to repeat the loop)

brz r1, 2

brz r0, -4 //DON'T FORGET TO SET THE OFFSET SO THAT IT REPEATS THE COMPARISON // ALGORITHM IF THE LOOP IS NOT DONE!!!!!!

//The following will occur after the for loop has ended

//Now we store the max (register 4) into its appropriate location in data memory

ldi r3, 2

st r3, r4

//derive a for loop counter (x): r1
// derive a general DM pointer: r3

ldi r3, 1

ld r1, r3 //r1 = x

dec r1, r1 //This allows us to start with the comparison of the current min and the

// next value without over iterating

//derive an array poiner(y): r2

ldi r3, 0

Id r2, r3 //r2 = y

//derive a max and min: r4

ld r4, r2 //register 4(the max holder) is initialized to be the first value in the array

//START OF THE FOR LOOP

inc r2, r2 // i = 1

ld r6, r2 //r6 = a[i] the next value in the array

//CREATE THI	E MASK USED FOR ONLY COMPARING THE SIGN OF THE FPs////////////////////////////////////
ldi r5, 7	
adi r5,r5, 1	//Now is the value 8
shl r5, r5	
adi r5, r5, 0	
shl r5, r5	
adi r5, r5, 0	
shl r5, r5	
adi r5, r5, 0	//the mask is now equal to 8000 in hex which is 16'b1000 0000 0000 0000
and r7, r4, r5	//Using a selective hold or mask to only maintain the sign bit of the current min. It // will be held in r7 for later comparison
shr r7, r7	//We will have to shift the bit to the right one so that it is at location 15 of the 16 bit // number (therefore there will only be positive values for comparing)
	//r5 will no longer be need for bit masking at this point so we can use for holding the // result of the bit masking of the next value in the array
and r5, r6, r5	//Using a selective hold or mask to only maintain the sign bit of the next value in the // array. It will be held in r5 for later comparison
shr r5, r5	//We will have to shift the bit to the right one so that it is at location 15 of the 16 bit // number (therefore there will only be positive values for comparing)
	//Next we will check to make sure the min and the next value in the array DON'T have the // same sign and the result of the comparison will be stored in r3
xor r3, r5, r7	
	//Now we use brz to determine whether the min and the next value in the array have the // same sign
brz r3, 8	//IF they have the same sign as each other ($r3 = 0$) then we must continue checking the // rest of the bits

//ELSE we will check whether the min or the next value in the array is lesser through // means of subtraction

CII	h	r3.	r7	r5
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- brn r3, 3 // If this fails then that means the current min had a 1 as it's sign, thus meaning it was // negative. Therefore, it is the min.
- add r4, r0, r4 // This means that brn failed and that the next value in the array was the one with a 0 as // its sign, thus meaning it was positive.
- brz r0, 2 // TO THE END OF ALL THE IF ELSE STATEMENTS SO THAT SKIPS TO THE // INCREMENTING AND DECREMENTING
- add r4, r0, r6 // If brn passes that means that the current min had a 0 as its sign, thus meaning it was // positive. Therefore, the next value in the array is the new min
- brz r0, 30 // TO THE END OF ALL THE IF ELSE STATEMENTS SO THAT SKIPS TO THE // INCREMENTING AND DECREMENTING
- brz r0, -30 // TO THE BEGINNING OF ALL THE IF ELSE STATEMENTS SO THAT IT CONTINUES // THE LOOP

//THIS WILL MARK THE END OF CHECKING THE SIGNS OF THE MIN AND THE NEXT VALUE IN //THE ARRAY. WE WILL NOW PROCEED TO CHECKING THE 4 BITS OF THE EXPONENT OF THE //CURRENT MIN AND THE NEXT VALUE IN THE ARRAY IF NECESSARY

ldi r0, 1

ldi r5, 7

shl r5, r5

shl r5, r5

shl r5, r5

shl r5, r5

adi r5, r5, 7

adi r5, r5, 1 //Now the value is 8

shl r5, r5

shl r5, r5

shl r5, r5

shl r5, r5

adi r5, r5, 0

shl r5, r5

shl r5, r5

shl r5, r5

shl r5, r5

adi r5, r5, 0 //the mask is now equal to 7800 in hex which is 16'b0111 1000 0000 0000

//Using a selective hold or mask to only maintain the exponent bits of the current min. It and r7, r4, r5 // will be held in r7 for later comparison //r5 will no longer be need for bit masking at this point so we can use for maintaining the // result of the bit masking of the next value in the array //Using a selective hold or mask to only maintain the exponent bits of the next value in and r5. r6. r5 // the array. It will be held in r5 for later comparison //Next we will check to make sure the min and the next value in the array DON'T have the // same exponent bits and the result of the comparison will be stored in r3 xor r3, r5, r7 //Now we use brz to determine whether the min and the next value in the array have the // same exponent bits brz r3, 9 //IF they have the same exponent bits as each other (r3 = 0) then we must continue // checking the rest of the bits //ELSE we will check whether the min or the next value in the array is lesser through // means of subtraction ldi r0, 0 sub r3, r7, r5 // If this fails then that means the current min has a smaller exponent thus it is the min brn r3. 3 add r4, r0, r4 //The current min shall remain the min // TO THE END OF ALL THE IF ELSE STATEMENTS SO THAT SKIPS TO THE brz r0. 2 // INCREMENTING AND DECREMENTING add r4, r0, r6 //If brn passed then that means the next value in the array had a smaller exponent and // thus it should be the new min brz r0, 3 // TO THE END OF ALL THE IF ELSE STATEMENTS SO THAT SKIPS TO THE // INCREMENTING AND DECREMENTING // TO THE END OF ALL THE IF ELSE STATEMENTS SO THAT SKIPS TO THE brz r0. -30 // INCREMENTING AND DECREMENTING //THIS WILL MARK THE END OF CHECKING THE 4 BITS OF THE EXPONENT OF THE MIN AND THE //NEXT VALUE IN THE ARRAY. WE WILL NOW PROCEED TO CHECKING THE 11 BITS OF THE //MANTISSA OF THE CURRENT MIN AND THE NEXT VALUE IN THE ARRAY IF NECESSARY ldi r0, 1 brz r0, 30 // TO THE END OF ALL THE IF ELSE STATEMENTS SO THAT SKIPS TO THE // INCREMENTING AND DECREMENTING // TO THE BEGINNING OF ALL THE IF ELSE STATEMENTS SO THAT IT CONTINUES brz r0, -3 // THE LOOP ldi r5, 0 shl r5, r5 shl r5, r5 shl r5, r5

```
shl r5, r5
adi r5, r5, 7
shl r5, r5
shl r5, r5
shl r5, r5
shl r5, r5
adi r5, r5, 7
adi r5, r5, 7
adi r5, r5, 1
                         //Now the value is 15
shl r5, r5
shl r5, r5
shl r5, r5
shl r5, r5
adi r5, r5, 7
adi r5, r5, 7
                         //Now the value is 15
adi r5, r5, 1
                         //the mask is now equal to 07FF in hex which is 16'b0000 0111 1111 1111
and r7, r4, r5
                         //Using a selective hold or mask to only maintain the mantissa bits of the current
                         // min. It will be held in r7 for later comparison
                //r5 will no longer be need for bit masking at this point so we can use for
                // maintaining the result of the bit masking of the next value in the array
and r5, r6, r5
                //Using a selective hold or mask to only maintain the mantissa bits of the next value in the
                // array. It will be held in r5 for later comparison
                //Next we will check to make sure the min and the next value in the array DON'T have the
                // same mantissa bits and the result of the comparison will be stored in r3
xor r3, r5, r7
                //Now we use brz to determine whether the min and the next value in the array have the
                // same mantissa bits
brz r3, 9
                //IF they have the same mantissa bits as each other (r3 = 0) then the current min and the
                // next value in the array must be the same, Thus we can just maintain the same min
                //ELSE we will check whether the min or the next value in the array is lesser through
                // means of subtraction
ldi r0, 0
sub r3, r7, r5
brn r3, 3
                //If this fails then that means the current min has a larger mantissa thus it should NOT
                // stay the min
```

add r4, r0, r6 //The current min is replaced by the next value in the array as the new min

brz r0, 4 // TO THE END OF ALL THE IF ELSE STATEMENTS SO THAT SKIPS TO THE // INCREMENTING AND DECREMENTING

add r4, r0, r4 //If brn passed then that means the next value in the array had a larger mantissa and thus // the current min REMAINS as the min

brz r0, 2 // TO THE END OF ALL THE IF ELSE STATEMENTS SO THAT SKIPS TO THE // INCREMENTING AND DECREMENTING

brz r0, -32 // TO THE BEGINNING OF ALL THE IF ELSE STATEMENTS SO THAT IT CONTINUES // THE LOOP

//THIS WILL MARK THE END OF COMPARISON ALGORITHM.

//Decrement the counter to indicate that I have completed an iteration also increment // second counter (register 6) for going through the values in the array

inc r2, r2 //ptr++ (array pointer++)

dec r1, r1 //loop counter--

//Check the value of the counter register to see if it's done with the for loop. If it's done go // 2 spots forward in the instructions and continue, else move forward once in the // instructions (brz r0 will cause it to repeat the loop)

brz r1, 2

brz r0, -4 //DON'T FORGET TO SET THE OFFSET SO THAT IT REPEATS THE COMPARISON // ALGORITHM IF THE LOOP IS NOT DONE!!!!!!

//The following will occur after the for loop has ended

//Now we store the max (register 4) into its appropriate location in data memory

ldi r3, 3

st r3, r4

//Give the register 0 the location in the instructions (Stating from 0 aka the top of the instructions)

ldi r0, 4

jmp r0 // to jump back to where the final data will be stored in the specified registers for viewing // on the DE0 Nano Board

Test 1:

Floating Point values used in the test and their decimal values:

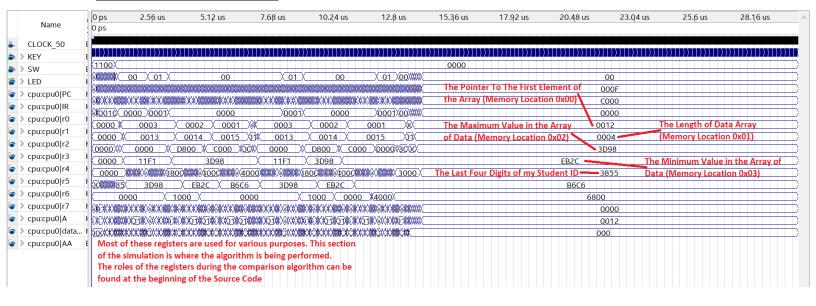
11F1: 0.038833618

3D98: 1.69921875 (This should be the Maximum Value)

EB2C: -89.375 (This should be the Minimum Value)

B6C6: -0.923339844

Full Simulation Results:



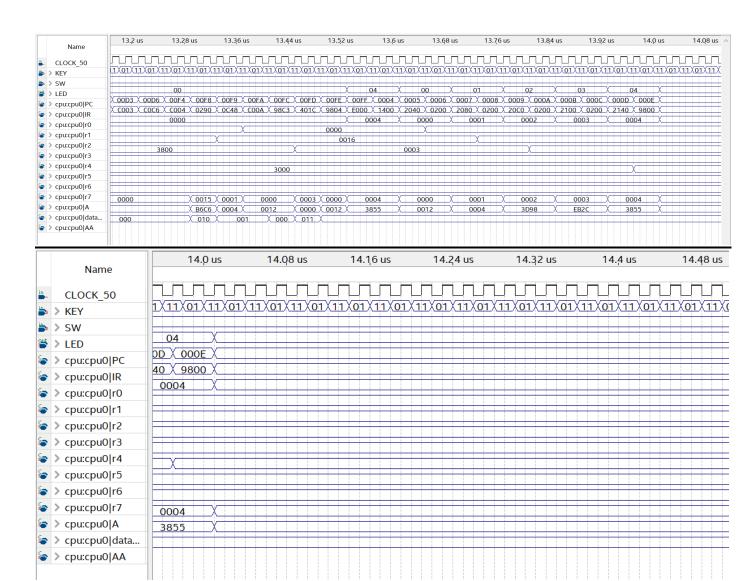
<u>Test 1 Zoomed in Until Final Results of Simulation Are Generated:</u>

	Name	0 ps 80.0 ns 0 ps	160,0 ns	240 ₁ 0 ns 3	320,0 ns 400),0 ns 4	30,0 ns 5	660,0 ns €	640 _r 0 ns	720 _r 0 ns	800 _r 0 ns	880 _r 0 ns
in_	CLOCK_50											
	KEY	10\(\times\00\(\times\00\(\times\0	X10X00X10X00X1	1X01X11X01X11X	01X11X01X11X01	X11X01X11X0	1X11X01X11X0 1100	01X11X01X11X	01 X 11 X 01 X 11	01 X 11 X 01 X	11 X01 X 11 X01 X	(11X01X11X01X11
≥ 3	SW LED	00	X		03 X 10 X 11					19 X 1A	X 1B X 1C	
	cpu:cpu0 PC	0000	X8C		003 X 0010 X 001 000 X 9983 X	1 X 0012 X 00 1D86		015 X 0016 X 0 5B7 X 85B1 X	017 X 0018 X 0		X 001B X 001C X 85B5 X	X 001D X 001E X 1D86
	cpu:cpu0 IR cpu:cpu0 r0	0000		0004 X 0008 X	000 A 3903 A	1000		3B7 A 03B1 A		0010	V 62B3 V	1000
	cpu:cpu0 r1							0000	0000			
	cpu:cpu0 r2						0000		0000			
	cpu:cpu0 r3 cpu:cpu0 r4								0000			
	cpu:cpu0 r5		0000		X 000	3 × 0006 × 00	OC X 0018 X 00	030 × 0037 × 0	038 × 0070 × 0	0000 00F0 X 01C0	X 0380 X 0385	5 X 070A X 0E14 X
	cpu:cpu0 r6											
	cpu:cpu0 r7	0000		0004 X 0008 X		0010 B470	X oc	030 X 0037 X	0010 B470		X 0380 X X 0000 X	0010 B470
	cpu:cpu0 data			000		U-1, U		110	000		X 110 X	000
	Name	880,0 ns 960,		·	1.2 us	1.28 us	1.36 us	1.44 us	1.52 us	1.6 us	1.68 us	
<u>in</u>	CLOCK_50	11X01X11X01X11X01X	11X01X11X01X11									
	KEY SW		X									
	LED	X 1D X 1E X 1F X 001D X 001E X 001F		10 X 0022 X 0023 X 003	24 × 0025 × 0026	X 0027 X 002	3 X 0029 X 002	A X 002B X 002	C X 002D X 002	2E X 002E X 0	0030 X 0031 X	00
	cpu:cpu0 PC	1D86		401E × 9800 × 980						1D45		8568 X
> 3	cpu:cpu0 r0			 	X 0004	} 						0000
	cpu:cpu0 r1						X 0012	X				
	cpu:cpu0 r3			0004	0001		<u> </u>					
	cpu:cpu0 r4								X 0007 X 000	08 X 0010 X 0	0020 X 0040 X	0080 X (
	cpu:cpu0 r6	X 070A X 0E14 X 1C28	X 3850 X		3855			X		0000		
	cpu:cpu0 r7	0010		0004 X 0010 X 000			X 0012	X 0013 X 000	0 X 0007 X	0000		0080 X
	cpu:cpu0 A cpu:cpu0 data	B470 000	X 0000 X B470 X X 110 X 000 X	0000 X B470 X 00°		X 0012 X 000 X 011	X 11F1 X 010	X 3D98 X 001	2 X 0000 X	0012		0000 X
* 3	cpu:cpu0 AA											
	Name	1.76 us 1.84 u	ıs 1.92 us	2.Q us	2.08 us	2.16 us	2.24 us	2.32 us	2.4 us	2.48 us	2.56 us	2.64 us
in												
<u>_</u> ,	CLOCK_50	1X01X11X01X11X01X1										
S	KEY SW	1X01X11X01X11X01X1										
> :	KEY SW LED		1X01X11X01X11X0)1X11X01X11X01	(11)(01)(11)(01)(11	X01X11X01X		 11X01X11X01X	11X01X11X01	(11X01X11X0)1X11X01X11X	01X11X01X11XC
□ 3 □ 3 □ 3	KEY SW	1X01X11X01X11X01X1 00 0033 X 0034 X 0035 X 1D45	1X01X11X01X11X0)1X11X01X11X01	(11X01X11X01X11 X 003B X 003C X	003D X 003E)	 11X01X11X01X	11X01X11X01 11X01X11X01 X 004A X 004E	(11X01X11X0 3 X 004C X 00)1X11X01X11X	01X11X01X11XC
	kEY SW LED cpu:cpu0 PC cpu:cpu0 IR cpu:cpu0 r0	00 0033 \ 0034 \ 0035 \	1X01X11X01X11X0	01X11X01X11X01) 038 X 0039 X 003A	(11X01X11X01X11 X 003B X 003C X	003D X 003E)	11X01X11X01X X 0041 X 0042	11X01X11X01 11X01X11X01 X 004A X 004E	11X01X11X0 3 X 004C X 00	01X11X01X11X 04D X 004E X 0	01X11X01X11XC
	KEY SW LED cpu:cpu0 PC cpu:cpu0 IR	1X01X11X01X11X01X1 00 0033 X 0034 X 0035 X 1D45	1X01X11X01X11X0	01X11X01X11X01) 038 X 0039 X 003A	(11X01X11X01X11 X 003B X 003C X	003D X 003E	X 003F X 0040 X 1175 X 1845	11X01X11X01X X 0041 X 0042	11X01X11X01X 11X01X11X01X X 004A X 004E X 9801 X 9947	11X01X11X0 3 X 004C X 00	01X11X01X11X 04D X 004E X 0	01X11X01X11XC
	KEY	1X01X11X01X11X01X1 00 0033 X 0034 X 0035 X 1D45	1X01X11X01X11X0	01X11X01X11X01) 038 X 0039 X 003A	(11X01X11X01X11 X 003B X 003C X	003D X 003E)	11X01X11X01X X 0041 X 0042	11X01X11X01X 11X01X11X01X X 004A X 004E X 9801 X 9947	(11X01X11X0 3 X 004C X 00	01X11X01X11X 04D X 004E X 0	01X11X01X11XC
	SW LED Councille	1X01X11X01X11X01X1 00 0033 X 0034 X 0035 X 1D45	1X01X11X01X11X(0036 X 0037 X 00 X 8568 X	01X11X01X11X01) 038 X 0039 X 003A	(11\x\01\x\11\x\01\x\11 \x\\\\\\\\\\\\\\\	003D X 003E	X 003F X 0040 X 1175 X 1845	11X01X11X01X X 0041 X 0042	11X01X11X01X 11X01X11X01X X 004A X 004E X 9801 X 9947 X 00003	(11X01X11X0 3X 004C X 00 1X 0013)1X11X01X11X)4D X 004E X 0 1D45	01X11X01X11XC
	KEY SW LED cpuscpu0 PC cpuscpu0 r0 cpuscpu0 r1 cpuscpu0 r2 cpuscpu0 r3 cpuscpu0 r4 cpuscpu0 r6 cpuscpu0 r6	1\(01\(11\) \(01\) \(11\) \(01\) \(11\) \(01\) \(11\) \(01\) \(11\) \(01\) \(11\) \(001\) \(11\) \(0033\) \(0033\) \(0034\) \(0035\) \(0000\) \(1045\) \(0000\) \(0000\)	1X01X11X01X11X(0036 X 0037 X 00 X 8568 X	01X11X01X11X01X 038 X 0039 X 003A 1D45	(11 \(\)\(\)\(\)\(\)\(\)\(\)\(\)\	003D X 003E 11E5 X 18C7	X 003F X 0040 X 1175 X 1845 0000	11X01X11X01X X 0041 X 0042 X 14FF X C058	11X01X11X01X 11X01X11X01X X 004A X 004E X 9801 X 9947 X 00003	(11X01X11X0 3X 004C X 00 1X 0013)1X11X01X11X)4D X 004E X 0 1D45	01X11X01X11X0 004F X 0050 X 00 X 856F X 85 0038 X 0070 X 00 30
	KEY	1\(01\(11\) \(01\) \(11\) \(01\) \(11\) \(01\) \(11\) \(01\) \(11\) \(01\) \(11\) \(001\) \(11\) \(0033\) \(0033\) \(0034\) \(0035\) \(0000\) \(1045\) \(0000\) \(0000\)	1X01X11X01X11X(0036 X 0037 X 00 X 8568 X	01X11X01X11X01X 038 X 0039 X 003A 1D45	(11 \(\)\(\)\(\)\(\)\(\)\(\)\(\)\	003D X 003E 11E5 X 1BC7 8000	X 003F X 0040 X 1175 X 1845 0000	11X01X11X01X X 0041 X 0042 X 14EF X C058 0000	11X01X11X01X 11X01X11X01X X 004A X 004E X 9801 X 9947 X 00003	0013 0007 X 00	D1X11X01X11X D1AD X 004E X 0 1D45 D0E X 001C X 0	01X11X01X11X0 004F X 0050 X 00 X 856F X 85 0038 X 0070 X 00 30 X 0070 X 00
	KEY SW LED cpuscpu0 PC cpuscpu0 r0 cpuscpu0 r1 cpuscpu0 r2 cpuscpu0 r4 cpuscpu0 r5 cpuscpu0 r5 cpuscpu0 r5 cpuscpu0 r5 cpuscpu0 r6 cpuscpu0 r6 cpuscpu0 r6 cpuscpu0 r6 cpuscpu0 r6 cpuscpu0 r7 cpuscpu0 A	1\(01\)\(11\)\(01\)\(11\)\(01\)\(11\)\(01\)\(11\)\(01\)\(11\)\(0033\)\(0034\)\(0035\)\(0033\)\(0004\)\(0000\)\(0	1X01X11X01X11X(0036 X 0037 X 0(X 8568 X	01X11X01X11X01X 038 X 0039 X 003A 1D45 X 1000 X 2000	(11 \(\)\(\)\(\)\(\)\(\)\(\)\(\)\	003D X 003E 11E5 X 1BC7 8000 11F1 X 0000 0000 X 0012	X 003F X 0040 X 1175 X 1845 0000	11X01X11X01X X 0041 X 0042 X 14EF X C058 0000 0000 0012	11X01X11X01X 11X01X11X01X X 004A X 004E X 9801 X 9947 X 00003	0013 0007 X 00	D1X11X01X11X D1AD X 004E X 0 1D45 D0E X 001C X 0	01X11X01X11X0 004F X 0050 X 00 X 856F X 85 0038 X 0070 X 00 30
	KEY	1\(01\)\(11\)\(01\)\(11\)\(01\)\(11\)\(01\)\(11\)\(01\)\(11\)\(001\)\(11\)\(0031\)\(0033\)\(0034\)\(0035\)\(0000	1X01X11X01X11X(0036 X 0037 X 0(01X11X01X11X01X 038 X 0039 X 0034 1D45 X 1000 X 2000	(11 \(\)\(\)\(\)\(\)\(\)\(\)\(\)\	003D X 003E 11E5 X 1BC7 8000 11F1 X 0000 0000 X 0012	11X01X11X01X X 003F X 0040 X 1175 X 1845 0000 X X 3098 X X 0000 X	11X01X11X01X X 0041 X 0042 X 14EF X C058 0000 0000 0012	11X01X11X01X 11X01X11X01X X 004A X 004E X 9801 X 9947 X 00003	0013 0007 X 0000 X	D1X11X01X11X D1AD X 004E X 0 1D45 D0E X 001C X 0	001X11X01X11XC 0004F X 0050 X 00
	KEY SW LED cpuscpu0 PC cpuscpu0 r0 cpuscpu0 r1 cpuscpu0 r2 cpuscpu0 r4 cpuscpu0 r5 cpuscpu0 r5 cpuscpu0 r5 cpuscpu0 r5 cpuscpu0 r6 cpuscpu0 r6 cpuscpu0 r6 cpuscpu0 r6 cpuscpu0 r6 cpuscpu0 r7 cpuscpu0 A	1\(01\)\(11\)\(01\)\(11\)\(01\)\(11\)\(01\)\(11\)\(01\)\(11\)\(001\)\(11\)\(0031\)\(0033\)\(0034\)\(0035\)\(0000	1X01X11X01X11X(20036 X 0037 X 0(X 8568 X 200400 X 0800 X 0800 X 0012 X 101 X	01X11X01X11X01X 038 X 0039 X 0034 1D45 X 1000 X 2000	(11 \(\)\(\)\(\)\(\)\(\)\(\)\(\)\	003D X 003E 11E5 X 1BC7 8000 11F1 X 0000 0000 X 0012	11X01X11X01X X 003F X 0040 X 1175 X 1845 0000 X X 3098 X X 0000 X	11X01X11X01X X 0041 X 0042 X 14EF X C058 0000 0000 0012	11X01X11X01X 11X01X11X01X X 004A X 004E X 9801 X 9947 X 00003	0013 0007 X 0000 X	D1X11X01X11X D1AD X 004E X 0 1D45 D0E X 001C X 0	001X11X01X11XC 0004F X 0050 X 00
	KEY	1\(01\)\(11\)\(01\)\(11\)\(01\)\(11\)\(01\)\(11\)\(01\)\(11\)\(033\)\(0034\)\(0035\)\(0000\)\(00	1X01X11X01X11X(0036 X 0037 X 0(X 8568 X 0400 X 0800 X 0800 X 0012 X 101 X us 2.8 us	21X11X01X11X01X 238 X 0039 X 003A 1D45 X 1000 X 2000 0000 2.8β us	(11 \(\)\(\)\(\)\(\)\(\)\(\)\(\)\	8000 11F1 X 0000 0000 X 0012 100 X 000	X 3D98 X X 0000 X 110 X 0000 X 0000 X 110 X 0000 X 0000 X 110 X 0000	0000 0000 0012 03.2 us	111X01X11X01X X 004A X 004E X 9801 X 9947 0003 11F1 3.28 us	0013 0007 X 00 000 3.36 us	D1X11X01X11X D1AD X 004E X 0 1D45 D0E X 001C X 0 1001 D04 3.44 us	01X11X01X11XC 004F X 0050 X 00
	KEY SW LED Cpurcpu0 PC cpurcpu0 PC cpurcpu0 IR cpurcpu0 IR cpurcpu0 IT cpurcpu0 A cpurcpu0 A cpurcpu0 AA	1\(01\)\(11\)\(01\)\(11\)\(01\)\(11\)\(01\)\(11\)\(01\)\(11\)\(01\)\(11\)\(0035\)\(1045\)\(0000\	1X01X11X01X11X(0036 X 0037 X 0(X 8568 X 0400 X 0800 X 0800 X 0012 X 101 X us 2.8 us	21X11X01X11X01X 238 X 0039 X 003A 1D45 X 1000 X 2000 0000 2.8β us	(11 \(\)\(\)\(\)\(\)\(\)\(\)\(\)\	8000 11F1 X 0000 0000 X 0012 100 X 000	X 3D98 X X 0000 X 110 X 0000 X 0000 X 110 X 0000 X 0000 X 110 X 0000	0000 0000 0012 03.2 us	111X01X11X01X X 004A X 004E X 9801 X 9947 0003 11F1 3.28 us	0013 0007 X 00 000 3.36 us	D1X11X01X11X D1AD X 004E X 0 1D45 D0E X 001C X 0 1001 D04 3.44 us	01X11X01X11XC 004F X 0050 X 00
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	KEY SW LED cpurcpuo PC cpurcpuo IR cpurcpuo IR cpurcpuo I7 cpurcpuo IA Cpurcpuo A Name CLOCK_50 KEY SW LED	1\(01\)\(11\)\(01\)\(11\)\(01\)\(11\)\(01\)\(11\)\(01\)\(11\)\(033\)\(0034\)\(0035\)\(0000\)\(00	1X01X11X01X11X(00) 1X0036 X 0037 X 00 1X 8568 X 1X0800 X 1X0800 X 1X01X11X 1X01X11X 1X01X11X 1X01X11X	21X11X01X11X01X 238 X 0039 X 003A 1D45 X 1000 X 2000 0000 0000 2.8β us	(11\(01\(11\(01\(11\))\)1\(11\(01\)1\(11\)1\	8000 11F1 \ 0000 0000 \ 00012 100 \ 0000 3.04 us	X 003E X 0040 X 1175 X 1845 0000 X 3D98 X X 0000 X X 110 X 000 3.12 us 11X01X11X01X	0000 0000 0012 011001X11X01X	111 (O1 (11 (O1 (O1 (O1 (O1 (O1 (O1 (O1	0013 0007 X 00 000 3.36 us X 00062 X 00	201X11X01X11X 204D X 004E X 0 1D45 200E X 001C X 0 2001 2004 201X11X01X11X 201X11X01X11X	01X11X01X11XC 00X11X01X11XC 004F X 0050 X 00
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	KEY SW LED Cputcpu0 PC Cputcpu0 r3 Cputcpu0 r5 Cputcpu0 r5 Cputcpu0 r6 Cputcpu0 r6 Cputcpu0 r7 Cputcpu0 r7 Cputcpu0 r6 Cputcpu0 r7 Cputcpu0 AA Cputcpu0 AA Cputcpu0 R6 Cputcpu0 R6 Cputcpu0 R7 Cputcpu0 R6 Cputcpu0 R7 Cputcpu0 R7 Cputcpu0 R7 Cputcpu0 R7 Cputcpu0 R1 Cputcpu0 r1 Cputcpu0 r2 Cputcpu0 r3 Cputcpu0 r4 Cputcpu0 r5	1X01X11X01X11X01X11 00 00 0033 X 0034 X 0035 X 1D45 0000 B0 X 0100 X 0200 X 0000 2.64 us 2.72 u 11X01X11X01X11X01X1 X 0050 X 0051 X 0052 X 8 56F X 8 569 X	1X01X11X01X11X(0) 1X01X11X(0) 1X036X X X X X X X X X X X X X X X X X X X	21X11X01X11X01X 238 X 0039 X 003A 1D45 X 1000 X 2000 0000 0000 2.8β us 01X11X01X11X01 01 055 X 0056 X 005: X 8568 X 0001	(11\(01\)\(11\)\(01\)\(1	8000 11F1 X 0000 8000 11F1 X 0000 0000 X 0012 100 X 000 3.04 us 1X01X11X01X 005A X 005B X 8568	X 003F X 0040 X 1175 X 1845 0000 X 3098 X X 0000 X X 110 X 000 3.12 us 11X01X11X01X X 005C X 005D X 1155 X 1175	11X01X11X01X X 0041 X 0042 X 14FF X C058 0000 0000 0012 X 101 X 011 3.2 us 11X01X11X01X X 005E X 005F	3.2β us 3.2β us 3.2β us X 0060 X 0061 X 9800 X 0AFD	0013 0007 X 00 000 3.36 us X 00062 X 00	201X11X01X11X 204D X 004E X 0 1D45 200E X 001C X 0 2001 2004 201X11X01X11X 201X11X01X11X	01X11X01X11XC 00X11X01X11XC 004F X 0050 X 00
	KEY SW LED Cpurcpu0 PC Cpurcpu0 r3 Cpurcpu0 r4 Cpurcpu0 r5 Cpurcpu0 r6 Cpurcpu0 r7 Cpurcpu0 r7 Cpurcpu0 r7 Cpurcpu0 r7 Cpurcpu0 r8 Cpurcpu0 r8 Cpurcpu0 r8 Cpurcpu0 r8 Cpurcpu0 r8 Cpurcpu0 R4 Cpurcpu0 R4 Cpurcpu0 R4 Cpurcpu0 R4 Cpurcpu0 R4 Cpurcpu0 R5 Cpurcpu0 r1 Cpurcpu0 r2 Cpurcpu0 r3 Cpurcpu0 r4 Cpurcpu0 r5 Cpurcpu0 r6 Cpurcpu0 r6 Cpurcpu0 r6 Cpurcpu0 r6 Cpurcpu0 r6 Cpurcpu0 r7 Cpurcpu0 r7 Cpurcpu0 r7 Cpurcpu0 r6 Cpurcpu0 r7	1X01X11X01X11X01X11 00 00333 X 0034 X 0035 X 1D45 0000 80 X 0100 X 0200 X 0000 2.64 us 2.72 x 11X01X11X01X11X01X1 X 0030 X 0051 X 0052 X 856F X 8569 X	1X01X11X01X11X(0) 1X01X11X(0) 1X036X X X X X X X X X X X X X X X X X X X	21X11X01X11X01X 238 X 0039 X 003A 1D45 X 1000 X 2000 0000 0000 2.8β us 01X11X01X11X01 01 055 X 0056 X 005: X 8568 X 0001	(11\(01\)\(11\)\(01\)\(1	8000 11F1 X 0000 8000 11F1 X 0000 0000 X 0012 100 X 000 3.04 us 1X01X11X01X 005A X 005B X 8568	X 003F X 0040 X 1175 X 1845 0000 X 3098 X X 0000 X X 110 X 000 3.12 us 11X01X11X01X X 005C X 005D X 11E5 X 1175	11X01X11X01X X 0041 X 0042 X 14FF X C058 0000 0000 0012 X 101 X 011 3.2 us 11X01X11X01X X 005E X 005F	3.28 us 11/01/11/01/11/01/ X 0046 X 0046 3.28 us X 0060 X 0061 X 0060 X 0061	11X01X11X0 3X 004C X 00 3X 0004C X 00 3X 0007 X 00 000 000 000 3.36 us 11X01X11X0 X 00062 X 00 0 X C21B X 05	201X11X01X11X 204D X 004E X 0 1D45 200E X 001C X 0 2001 2004 201X11X01X11X 201X11X01X11X	0004F \ 0050 \ \ 00 \ \ 856F \ \ 85 \ 0038 \ \ 0070 \ \ 00 \ \ 0000 \ \ 101 \ 0000 \ \ 101 \ 00069 \ \ 0087 \ \ 0 \ 0006 \ \ 0004 \ 0
	KEY SW LED Cputcpu0 PC cputcpu0 AA cputcpu0 AA Cputcpu0 PC	1X01X11X01X11X01X11 00 00 0033 X 0034 X 0035 X 1D45 0000 80 X 0100 X 0200 X 0000 2.64 us 2.72 11X01X11X01X11X01X1 X 0050 X 0051 X 0052 X 856F X 8569 X X 0070 X 0077 X 0078 3 098 X 0070 X 0077 X X 0000 X	1X01X11X01X11X0 (0036 X 0037 X 00 X 8568 X (0400 X 0800 X 0800 X 0012 X 101 X us 2.8 us 1X01X11X01X11X (0053 X 0054 X 0 1D45 (0001 0001 0004	21X11X01X11X01X 238 X 0039 X 0034 1D45 X 1000 X 2000 0000 0000 2.8β us 01X11X01X11X01 01X11X01X11X01 01X11X01X11X01 01X11X01X11X01 355 X 0056 X 0051 X 8568 X 0001	(11\(01\)\(11\)\(01\)\(11\)\(01\)\(11\)\(01\)\(11\)\(11\)\(01\)\(1	8000 11F1 \ 0000 0000 \ 0012 100 \ 0000 3.04 us 1\(\text{CO}\) \ 11\(\text{CO}\) \ 0058 \(\text{X}\) \ 8568 3C00 \(\text{X}\)	X 3D98 X X 0000 X 11F5 X 11F5 X 11F5 X 11F5 X 11F5 X 1090 X X 11F1 X 3D98 X X 0000 X 11F5 X 11F5 X 11F5 X 11F5 X 1000 X 11F5 X 11F5 X 1000 X 1	11X01X11X01X X 0041 X 0042 X 14EF X C058 0000 0012 X 101 X 011 3.2 us 11X01X11X01X X 005E X 005E X 14EF X C059 X 3800 X 2800 X 0012	3.28 us 3.28 us 3.28 us 2800 X 0001 X 1000 X 0001 X 1000 X 0004 X	3.36 us 0.0052 00 0.0002 00 0.	201X11X01X11X 204D X 004E X 0 1D45 200E X 001C X 0 200E X 0 2	01X11X01X11XC 00X11X01X11XC 004F X 0050 X 0C
	KEY SW LED Cpurcpu0 PC Cpurcpu0 r3 Cpurcpu0 r4 Cpurcpu0 r5 Cpurcpu0 r6 Cpurcpu0 r7 Cpurcpu0 r7 Cpurcpu0 r7 Cpurcpu0 r7 Cpurcpu0 r8 Cpurcpu0 r8 Cpurcpu0 r8 Cpurcpu0 r8 Cpurcpu0 r8 Cpurcpu0 R4 Cpurcpu0 R4 Cpurcpu0 R4 Cpurcpu0 R4 Cpurcpu0 R4 Cpurcpu0 R5 Cpurcpu0 r1 Cpurcpu0 r2 Cpurcpu0 r3 Cpurcpu0 r4 Cpurcpu0 r5 Cpurcpu0 r6 Cpurcpu0 r6 Cpurcpu0 r6 Cpurcpu0 r6 Cpurcpu0 r6 Cpurcpu0 r7 Cpurcpu0 r7 Cpurcpu0 r7 Cpurcpu0 r6 Cpurcpu0 r7	1X01X11X01X11X01X11 00 00 0033 X 0034 X 0035 X 1D45 0000 B0	1X01X11X01X11X0 (0036 X 0037 X 00 X 8568 X (0400 X 0800 X 0012 X 101 X 1X01X11X01X11X (0053 X 0054 X 0 1D45 (0000 X 01E0 X 0 0001	21X11X01X11X01X 238 X 0039 X 003A 1D45 X 1000 X 2000 0000 2.88 us 01X11X01X11X01 01 055 X 0056 X 005: X 8568 X 0001 3C0 X 0780	(11\(01\)\(11\)\(01\)\(1	8000 11F1 \ 0000 0000 \ 0012 100 \ 0000 3.04 us 1\(\text{CO}\) \ 11\(\text{CO}\) \ 0058 \(\text{X}\) \ 8568 3C00 \(\text{X}\)	X 3D98 X X 0000 X 11F5 X 11F5 X 11F5 X 11F5 X 11F5 X 1090 X X 11F1 X 3D98 X X 0000 X 11F5 X 11F5 X 11F5 X 11F5 X 1000 X 11F5 X 11F5 X 1000 X 1	0000 0000 0000 0012 X 101 X 011 3.2 us 11X01X11X01X X 003E X 003F X 14FF X C039	3.28 us 3.28 us 3.28 us 2800 X 0001 X 1000 X 0001 X 1000 X 0004 X	3.36 us 0.0052 00 0.0002 00 0.	201X11X01X11X 204D X 004E X 0 1D45 200E X 001C X 0 200E X 001C X 0 2001 2001 2001 2004 2005 2006 X 0006 X 0006 2006 X 0003 X C	01X11X01X11XC 004F X 0050 X 0C X 856F X 85 0038 X 0070 X 0C X 0000 X 101 3.52 us 01X11X01X11X 0069 X 0087 X 0 0066 X C004 X 0

Name	3.44 us	3.52 us	3.6 us	3.68 us	3.76 us	3.84 us	3.92 us	4.0 us	4.08 us	4.16 us	4.24 us	4.32 us
L CLOCK 50	Іпппп	пппп	пппп	ппппг		пппп		пппп	ппппп	ппппп	ппппп	пппп
> KEY							01X11X01X11X0					
⇒ > SW												
⇒ > LED		V										
> cpu:cpu0 PC							02B × 002C × 002		1D45	X 8568 X	1D45	X 8!
> cpu:cpu0 IR	C003 \ C0C0	A C004 A 0290	7 A UC48 A COC	DA A CIC4 A CIC	JO A CICS A	C102 A 2	190 / 9947 / 830	J9 ^	1043	A 8308 A	1043	
> cpu:cpu0 r0			х									
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> cpu:cpu0 r6	1					1	000					
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> cpu:cpu0 A	112	X 3D98	3 X 0000	X	0012	ΧE	32C X 0012 X 000	00 X	0012	X 0000 X		
> cpu:cpu0 data	000	X 010	X 001	X	000	X_c	10 X 000 X 10	1 X	000	X 101 X	000	X1
> cpu:cpu0 AA	1											
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Name	4.32 us	4.4 us	4.48 us	4.56 us	4.64 us	4.72 us	4.8 us	4.88 us	4.96 us	5.04 us	5.12 us	5.2 us
b 01001150	hana		пппг			1			ппппп		пппп	пппп
L CLOCK_50 KEY							1X11X01X11X01					
⇒ > SW												
⇒ > LED												
> cpu:cpu0 PC							41 X 0042 X 004					
> cpu:cpu0 IR	X 8568	11	D45	↑ 8568 ↑ 11E:	5 X 1BC/ X 11/	5 X 1B45 X 14	EF X CO58 X OAFI) X C21B X 05	04 1 0006 1 000	13 X COC6 X COO2	1 X 0290 X 0C48	X COOA X C1
> cpu:cpu0 r0		0002										X
> cpu:cpu0 r1	0014										X	
> cpu:cpu0 r2 > cpu:cpu0 r3							X 4000	X				
> cpu:cpu0 r4			V									
> cpu:cpu0 r5	0400 X 08	00 X 1000	X 2000 X 4000	0 X	8000 EB2	, X					4000	
> cpu:cpu0 r6					Y							
🍲 > cpu:cpu0 r7	X 0800	00	000	X 8000 X 3D98	8 X 0000 X EB2	c X 0000 X	4000 X 000	0 X C000 X	000	00	X 0014 X 0002	X 0001 X
> cpu:cpu0 A	00	12			0 X 0012 X 000			0012			X EB2C X 0000	X 0004 X
> cpu:cpu0 data	101	0	100	X 101 X 100	X 000 X 110	O X 000 X 10)1 X 011 X 111	X 011 X	000	0	X 010 X (D01 X
> cpu:cpu0 AA												
			E 26									
	5.2 us	5.28 us	2.36 US	5.44 us	5.52 us	5.6 us	5.68 us	5.76 us	5.84 us	5.92 us	6.0 us	6.08 us \land
Name	5.2 us	5.28 us	5.36 us	5.44 us	5.52 us	5.6 us	5.68 us	5.76 us	5.84 us	5.92 us	6.Q us	6.08 us
LCLOCK_50							· · · · · · · · · · · · · · · · · · ·					
CLOCK_50 KEY SW							01X11X01X11X0	1X11X01X11X				
CLOCK_50 KEY SW LED	11X01X11X01	X11X01X11X01	X11X01X11X0	1X11X01X11X0	1X11X01X11X0	 p1X11X01X11X		1X11X01X11X	01X11X01X11X0)1X11X01X11X0	1X11X01X11X01	\\ X11X01X11\
CLOCK_50 KEY SW LED cpu:cpu0 PC	11X01X11X01 11X01X11X01	X11X01X11X01	X11X01X11X0 A X 0067 X 00	1X11X01X11X0	11X11X01X11X0 2C X 002D X 00	 p1X11X01X11X	01X11X01X11X0	1X11X01X11X 0 32 X 0033 X 0	01X11X01X11X0)1X11X01X11X0	1X11X01X11X01	\\ X11X01X11\
CLOCK_50 KEY SW LED cpucpu0 PC cpucpu0 IR	11X01X11X01 11X01X11X01	X11X01X11X01 X 008A X 006	X11X01X11X0 A X 0067 X 00	11X11X01X11X0	11X11X01X11X0 2C X 002D X 00	D1X11X01X11X	01X11X01X11X0 01X01X11X0 0030 X 0031 X 00	1X11X01X11X 0 32 X 0033 X 0	01X11X01X11X0 0034 X 0035 X 00	036 X 0037 X 003 X 8568 X	1X11X01X11X01 38 X 0039 X 003, 1D45	\\ X11X01X11\
CLOCK_50 KEY SW LED cpu:cpu0 PC	11X01X11X01 11X01X11X01	X11X01X11X01 X 008A X 006	X11X01X11X0 A X 0067 X 00	11X11X01X11X0	11X11X01X11X0 2C X 002D X 00	D1X11X01X11X	01X11X01X11X0 01X11X01X11X0 0 030 X 0031 X 00 030 X 85	1X11X01X11X 0 32 X 0033 X 0	01X11X01X11X0 0034 X 0035 X 00	01X11X01X11X0 036 X 0037 X 003 X 8568 X	1X11X01X11X01 38 X 0039 X 003, 1D45	\\ X11X01X11\
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CLOCK_50 NEY NEY NED LED Cpuccpuol PC Cpuccpuol ri Cpuccpuol	11\(01\\11\\01\\01	X11X01X11X01 X 008A X 006. 4 X C100 X C1C 3D98	X11X01X11X0 A X 0067 X 00 5 X C102	249 X 0028 X 000 X 2190 X 99	X 0007 X 00	D1X11X01X11X D2E X 002F X C 1D45 C000 008 X 0010 X C	01\(\text{11\times01\times11\times0}\) 01\(\text{11\times01\times11\times0}\) 030\(\times00331\times0\) 030\(\times00331\times0\) 030\(\times00331\times0\) 040\(\times00331\times0\) 020\(\times00400\times)	0 332 X 0033 X 0 68 X 00 0080 X 0	01X11X01X11X0 0034 X 0035 X 00 1045	01X11X01X11X0 036 X 0037 X 00 0 X 8568 X 0005	1X11X01X11X01 38 X 0039 X 003, 1D45	X11X01X11 A X 003B X (
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CLOCK_50 NEY NEY CUCK_50 NEY NED CPUCCPUO PC CPUCCPUO A CPUCCPUO AA Name CLOCK_50	X 0001 X X 0004 X 0004 X 0004 X 0004 X 0001 X 10004 X 0001 X 10004 X 00001 X 00004 X 00001 X 00004 X 00001 X	X11X01X11X01 X 008A X 006A 1 X C100 X C1C 3098 0000 001 0000 6.16 us	X11X01X11X0 A X 0067 X 00 5 X C102 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	11 11 1 11 1 1 1 1 1 1 1 1 1 1 1 1 1 1	X 0007 X 000 X 000 X 000 X 000 X 000 X 101	D1X11X01X11X D2E X 002F X C 1D45 C000 008 X 0010 X C 0000 0012 000 6.48 us	01X11X01X11X0 0030 X 0031 X 00 030 X 0031 X 00 00 020 X 0040 X 00 020 X 0040 X	0 332 X 0033 X 0 668 X 00 0080 X 0 80 X 000 X	01X11X01X11X0 1034 X 0035 X 00 1045 1000 X 0200 X 04 0000 0000 6.72 us	010 X 0800 X 0012 X 101	38 X 0039 X 003 1045 31 31 32 33 33 34 35 36 37 38 37 38 38 38 38 38 38 38 38 38 38	X11X01X11) AX 003B X(X 8 0 X 4000 X 6.96 us
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CLOCK_50	X 0001 X X 0004 X 2001 X X 0001 X X 0001 X X 0004 X 201 X 2003B X 003C X 003B X 003C X 003C X 003B X 003C	X11X01X11X01 X 008A X 006 1 X C100 X C1C 3098 000 001 000 6.16 us 1 X01X11X01X1 003D X 003E	X11X01X11X0 A X 0067 X 00 5 X C102 0 2 0 6.24 us 1X01X11X01X	11\(11\)\(01\)\(11\)\(01\)\(11\)\(01\)\(11\)\(01\)\(11\)\(01\)\(11\)\(01\)\(11\)\(01\)\(11\)\(01\)\(11\)\(01\)\(11\)\(01\)\(11\)\(01\)\(11\)\(01\)\(11\)\(01\)\(11\)\(01\)\(11\)\(01\)\(11\)\(01\)\(11\)\(01\)\(11	X 0007 X 0000 X 1011 X 111 X 111 X 111 X 111 X 11 X	22E X 002F X C 1045 C000 008 X 0010 X C 0000 0012 000 6.48 us (11X01X11X01	01X11X01X11X0 0030 X 0031 X 00 030 X 0031 X 00 00 020 X 0040 X 00 020 X 0040 X 00 020 X 10	1X11X01X11X 0 32 X 0033 X 0 68 X 00 0080 X 0 0080 X 0 00 X 01 X 6.64 us 11X01X11X01	01X11X01X11X01 1034 X 0035 X 00 1045 1000 X 0200 X 04 0000 0000 0000 6.72 us 11X01X11X01X11X01X B X 008C X 008D	036 X 0037 X 00 036 X 0037 X 00 036 X 0037 X 00 0015 000 X 0800 0015 000 X 0800 0012 X 101 X 6.8 us 111 X 01 X 11 X 01 X 11 000 X 000	1 (1) (1) (1) (1) (1) (1) (1) (1) (1) (1	0 X 4000 X 6.96 us 1 X 11 X 12 X 8
CLOCK_50 SKEY SW SED CUCCPUO PC PC PC PC PC PC PC PC	X 0001 X X 0004 X 2001 X X 0001 X X 0001 X X 0004 X 201 X 2003B X 003C X 003B X 003C X 003C X 003B X 003C	X11X01X11X01 X 008A X 006 1 X C100 X C1C 3098 000 001 000 6.16 us 1 X01X11X01X1 003D X 003E	X11X01X11X0 A X 0067 X 00 5 X C102 0 2 0 6.24 us 1X01X11X01X	11\(11\)\(01\)\(11\)\(01\)\(11\)\(01\)\(11\)\(01\)\(11\)\(01\)\(11\)\(01\)\(11\)\(01\)\(11\)\(01\)\(11\)\(01\)\(11\)\(01\)\(11\)\(01\)\(11\)\(01\)\(11\)\(01\)\(11\)\(01\)\(11\)\(01\)\(11\)\(01\)\(11\)\(01\)\(11	X 0007 X 0000 X 1011 X 111 X 111 X 111 X 111 X 11 X	22E X 002F X C 1045 C000 008 X 0010 X C 0000 0012 000 6.48 us (11X01X11X01	01X11X01X11X0 01X11X01X11X0 0030 X 0031 X 00 020 X 0040 X 020 X 0040 X 020 X 10	1X11X01X11X 0 32 X 0033 X 0 68 X 00 0080 X 0 0080 X 0 00 X 01 X 6.64 us 11X01X11X01	01X11X01X11X01 1034 X 0035 X 00 1045 1000 X 0200 X 04 0000 0000 0000 6.72 us 11X01X11X01X11X01X B X 008C X 008D	000 X 0800 X 00012 X 101 X 11 X 01 X 11 X 01 X 11 X 01 X 10 X 10 X 0800 X 00012 X 101 X 10	38 × 0039 × 003 1045 21 × 1000 × 200 0000 000 6.8β us 11×01×11×01×1 × 0091 × 0092 × × 98C1 × 2058 ×	X11X01X11 AX 003B X (X (0 X 4000 X (X (0 X 4000 X (X (1 X (
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CLOCK_50	X 0001 X X 0004 X 2001 X X 0001 X X 0001 X X 0004 X 201 X 2003B X 003C X 003B X 003C X 003C X 003B X 003C	X11X01X11X01 X 008A X 006 1 X C100 X C1C 3098 000 001 000 6.16 us 1 X01X11X01X1 003D X 003E	X11X01X11X0 A X 0067 X 00 5 X C102 0 2 0 6.24 us 1X01X11X01X	11\(\)11\(\)01\(\)11\(\)002\(\)2\(\)002\(\)8\(\)002\(\)8\(\)002\(\)8\(\)002\(\)8\(\)002\(\)8\(\)9\(\)9\(\)9\(\)9\(\)9\(\)9\(\)9	X 0007 X 0000 X 1011 X 111 X 111 X 111 X 111 X 11 X	22E X 002F X C 1045 C000 008 X 0010 X C 0000 0012 0000 6.48 us	01X11X01X11X0 0030 X 0031 X 00 030 X 0031 X 00 020 X 0040 X 00 020 X 0040 X 00 020 X 10 6.56 us 11X01X11X01X 8 X 0066 X 0069 6 X C003 X C0C6	1X11X01X11X 0 32 X 0033 X 0 68 X 00 0080 X 0 0080 X 0 00 X 01 X 6.64 us 11X01X11X01	01X11X01X11X01 1034 X 0035 X 00 1045 1000 X 0200 X 04 0000 0000 0000 6.72 us 11X01X11X01X11X01X B X 008C X 008D	036 X 0037 X 00. 0015 000 X 0800 X 0015 0012 0012 0014 6.8 us 111\(01\)\(01\	38 × 0039 × 003 1045 21 × 1000 × 200 0000 000 6.8β us 11×01×11×01×1 × 0091 × 0092 × × 98C1 × 2058 ×	X11X01X11 AX 003B X (X (0 X 4090 X (X (0 X 4090 X (X (0 X 4090 X (0 X 4
CLOCK_50 S KEY S W	X 0001 X X 0004 X 0004 X 0001 X X 00001 X 000001 X 00001 X 000	X11X01X11X01 X 008A X 006 A X C100 X C1C 3098 000 001 001 001 001 001 001	X11X01X11X0 A X 0067 X 00 5 X C102 0 2 0 6.24 us 1X01X11X01X	11\(\)11\(\)01\(\)11\(\)002\(\)2\(\)002\(\)8\(\)002\(\)8\(\)002\(\)8\(\)002\(\)8\(\)002\(\)8\(\)9\(\)9\(\)9\(\)9\(\)9\(\)9\(\)9	X 0007 X 00 00 X 0007 X 00 00 X 0007 X 12 X 0000 X 101 X 101 X 101 X 11 X 01 X 11 X 01 X 11 X 01 X 004 X 004 D X 004	22E X 002F X C 1045 C000 008 X 0010 X C 0000 0012 0000 6.48 us	01X11X01X11X0 0030 X 0031 X 00 030 X 0031 X 00 020 X 0040 X 00 020 X 0040 X 00 020 X 10 6.56 us 11X01X11X01X 8 X 0066 X 0069 6 X C003 X C0C6	1X11X01X11X 0 32 X 0033 X 0 68 X 00 0080 X 0 80 X 00 X 01 X 6.64 us 11X01X11X01 X 0087 X 008 X C004 X 029	01X11X01X11X01 1034 X 0035 X 00 1045 1045 1000 X 0200 X 04 0000 0000 6.72 us 11X01X11X01X B X 008C X 008D 0 X 0C48 X CO9A	00000 X 0000 X 0	1X11X01X11X01 38 X 0039 X 003 1D45 201 2 X 1000 X 200 0000 000 000 6.88 us 11X01X11X01X1 2 X 0091 X 0092 X 98C1 X 2058 X 0016	0 X 4000 X 6.96 us 1 X 1 X 1 X 2 X 2 X 2 X 2 X 2 X 2 X 2 X
CLOCK_50 SKEY SW SED COUNCEDUOIS	X 0001 X X 0004 X 2001 X X 0001 X X 0001 X X 0004 X 201 X 2003B X 003C X 003B X 003C X 003C X 003B X 003C	X11X01X11X01 X 008A X 006 1 X C100 X C1C 3098 000 001 000 6.16 us 1 X01X11X01X1 003D X 003E	X11X01X11X0 A X 0067 X 00 5 X C102 0 2 0 6.24 us 1X01X11X01X	11X11X01X11X01 149 X 0028 X 00 X 2190 X 99 X 2190 X 99 X 0015 X 00 X B6C6 X 00 X 010 X 00 4.32 us 11X01X11X01X X 0041 X 0042 X 14EF X C058	X 0007 X 00 00 X 0007 X 00 00 X 0007 X 12 X 0000 X 101 X 101 X 101 X 11 X 01 X 11 X 01 X 11 X 01 X 004 X 004 D X 004	22E X 002F X C 1045 C000 008 X 0010 X C 0000 0012 0000 6.48 us	01X11X01X11X0 0030 X 0031 X 00 030 X 0031 X 00 020 X 0040 X 00 020 X 0040 X 00 020 X 10 6.56 us 11X01X11X01X 8 X 0066 X 0069 6 X C003 X C0C6	1X11X01X11X 0 32 X 0033 X 0 68 X 00 0080 X 0 80 X 00 X 01 X 6.64 us 11X01X11X01 X 0087 X 008 X C004 X 029	01X11X01X11X01 1034 X 0035 X 00 1045 1000 X 0200 X 04 0000 0000 0000 6.72 us 11X01X11X01X11X01X B X 008C X 008D	00000 X 0000 X 0	1X11X01X11X01 38 X 0039 X 003 1D45 201 2 X 1000 X 200 0000 000 000 6.88 us 11X01X11X01X1 2 X 0091 X 0092 X 98C1 X 2058 X 0016	0 X 4000 X 6.96 us 1 X 1 X 1 X 1 X 2 X 2 X 2 X 2 X 2 X 2 X
CLOCK_50 S KEY S W S VED CONCEPTION CONCEPTIO	X 0001 X X 0004 X 0004 X 0001 X X 00001 X 000001 X 00001 X 000	X11X01X11X01 X 008A X 006 A X C100 X C1C 3098 000 001 001 001 001 001 001	X11X01X11X0 A X 0067 X 00 5 X C102 0 2 0 6.24 us 1X01X11X01X	11\(\)11\(\)01\(\)11\(\)002\(\)2\(\)002\(\)8\(\)002\(\)8\(\)002\(\)8\(\)002\(\)8\(\)002\(\)8\(\)9\(\)9\(\)9\(\)9\(\)9\(\)9\(\)9	X 0007 X 00 00 X 0007 X 00 00 X 0007 X 12 X 0000 X 101 X 101 X 101 X 11 X 01 X 11 X 01 X 11 X 01 X 004 X 004 D X 004	22E X 002F X C 1045 C000 008 X 0010 X C 0000 0012 0000 6.48 us	01X11X01X11X0 0030 X 0031 X 00 030 X 0031 X 00 020 X 0040 X 00 020 X 0040 X 00 020 X 10 6.56 us 11X01X11X01X 8 X 0066 X 0069 6 X C003 X C0C6	1X11X01X11X 0 32 X 0033 X 0 68 X 00 0080 X 0 80 X 00 X 01 X 6.64 us 11X01X11X01 X 0087 X 008 X C004 X 029	01X11X01X1X01X11X01X11X01X11X01X11X01X11X01X11X01X1X01X1X01X1X01X1X01X1X01X1X01X1X01X1X01X1X01X1X01X1X01X1X01X1X01X1X01X1X01X1X01X1X01X0	00000 X 0000 X 0	1X11X01X11X01 38 X 0039 X 003 1D45 201 2 X 1000 X 200 0000 000 000 6.88 us 11X01X11X01X1 2 X 0091 X 0092 X 98C1 X 2058 X 0016	0 X 4000 X 6.96 us 1 X 1 X 1 X 1 X 2 X 2 X 2 X 2 X 2 X 2 X
CLOCK_50	X 0001 X X 0004 X 301 X 003B X 003C X 8568 X 4000 X	(11X01X11X01 (11X01X11X01 (11X01X11X01 (11X01X11X01 (11X01X11X01X1 (11X01X11X01X1 (11X01X11X01X1 (11X01X11X01X1 (11X01X1 (11X01X1 (11X01	X11X01X11X0 AX 0067 X 00 5 X C102 0 0 2 1 X01X11X01X C003F X 0040 C1175 X 1845	11X11X01X11X01 149 X 002B X 00 X 2190 X 99 X 2190 X 99 X 0015 X 00 X B6C6 X 00 X 010 X 00 43 Z us 11X01X11X01X X 0041 X 0042 X 14EF X C058 X 4 X B6C6	1X11X01X11X0 2C X 002D X 00 47 X 8569 X X 0007 X 00 00 X 0007 X 112 X 0000 X 112 X 0000 X 101 X 6.4 us 11X01X11X01X X 0043 X 0044 X 0045 X C218	201X11X01X11X 202E X 002F X C 1D45 2000 2008 X 0010 X C 2000 2012 2000 6.4β us 211X01X11X01 X 0047 X 004 X 0504 X COC	01X11X01X11X0 0030 X 0031 X 00 030 X 0031 X 00 000 020 X 0040 X 000 X 00 X 10 6.56 us 111X01X11X01X 8 X 0066 X 0069 6 X C003 X C0C6	1)X11X01X11X01X11X01X11X01X11X01X11X01X11X01X11X01X11X01X11X01X11X01X11X01X11X01X10000	01X11X01X11X01 1034 X 0035 X 00 1045 1045 1000 X 0200 X 04 0000 0000 6.72 us 11X01X11X01X11X01X B X 008C X 008D 0 X 0C48 X C09A X 1 X 0000 0000	0000 X 00000 X 0000 X 0	1X11X01X11X01 38 X 0039 X 003 1045 21 X 1000 X 200 0000 6.8β us 11X01X11X01X1 X 0091 X 0092 X X 98C1 X 2058 X 0016	X11X01X11) AX 003B X (
CLOCK_50 S KEY S W S V KEY S V S V K	X 0001 X 0004 X 0004 X 0004 X 0004 X 00038 X 003C X 8568 X 4000 X 8000 X	(11/01/11/01 (11/01/11/01 (100/11/01) (100/11/01/11 (100/11/01	A X 0067 X 00 A X 0067 X 00 5 X C102 0 0 2 0 1X01X11X01X (003F X 0040 (1175 X 1845)	11X11X01X11X01 149 X 002B X 00 X 2190 X 99 X 2190 X 99 X 0015 X 00 X B6C6 X 00 X 010 X 00 43 Z us 11X01X11X01X X 0041 X 0042 X 14EF X C058 X 4 X B6C6	2C X 002D X 00 47 X 8569 X X 0007 X 00 00 X 0007 X 112 X 0000 X 10 X 101 X 6.4 us 11X01X11X01X X 0043 X 0044 X 0045 X C21B	201X11X01X11X 202E X 002F X C 1D45 2000 2008 X 0010 X C 2000 2012 2000 6.4β us 11X01X11X01 X 0047 X 004 X 0504 X COC	01X11X01X11X0 0030 X 0031 X 00 030 X 0031 X 00 020 X 0040 X 00 020 X 0040 X 00 020 X 10 6.56 us 11X01X11X01X 8 X 0066 X 0069 6 X C003 X C0C6	1)X11X01X11X 0 332 X 0033 X 0 68 X 00 0080 X 0 80 X 00 X 11 X 6.64 us 11 X 11X01X11X01 X 0087 X 008 X C004 X 029	01X11X01X11X01 1034 X 0035 X 00 1045 1000 X 0200 X 04 1000 X 0	0000 X 0000	38 × 0039 × 003 38 × 1045 31 31 × 1000 × 200 3000 3000 3000 3000 3000 3000 3000	X11X01X11 AX 003B X (X 8 0 X 4000 X 0 X 4000 X X 8 1 X 1 X 1 X 1 X 1 X 1 X 1 X 1 X 1 X 1 X
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Name	6.96 us	7.04 us	7.12 us	7.2 us	7.28 us	7.36 us	7.44 us	7.52 us	7.6 us	7.68 us	7.76 us	7.84 us
CLOCK_50			1X11X01X11X01									
⇒ > SW												
> LED > cpu:cpu0 PC			96 X 0097 X 009									
> cpu:cpu0 IR > cpu:cpu0 r0		1 1 2098 1 21	10 X 0290 X 219	0 1 9947 1 856	,	1D45	X 8568 X	1D45	X 8568	3 .	1D45	X 8568 X 1
> cpu:cpu0 r1	X 0004 X	ж	0012 X									
> cpu:cpu0 r2 > cpu:cpu0 r3	0001	X										
> cpu:cpu0 r4 > cpu:cpu0 r5				X 000	7 X 0008 X 00)10 X 0020 X 00	40 X 0080	X 0100 X 020	0 X 0400 X (0800 X 1000	0 X 2000 X 4	000 X
> cpu:cpu0 r6												
> cpu:cpu0 r7 > cpu:cpu0 A		0000 X 0012 X		3 X 0000 X 000 8 X 0012 X 0000		0000 0012	X 0000 X	0000	X 0800	0012	0000	X 8000 X 1 X 0
> cpu:cpu0 data > cpu:cpu0 AA	X 001 X 000	X 011 X	010	X 000 X 101	X	000	X 101 X	000	X 101	X	000	X 101 X 1
Name	7.84 us	7.92 us	8.0 us	8.08 us	8.16 us	8.24 us	8.32 us	8.4 us	8.48 us	8.56 us	8.64 us	8.72 us ^
CLOCK_50			01X11X01X11X0									
> SW					- V					01		
> LED > cpu:cpu0 PC			0AC X 00AD X 00							1 X 00C2 X 00C		
> cpu:cpu0 IR > cpu:cpu0 r0	X 8568 X 11E	-5 X 1BC/ X 1	175 X 1B45 X 14	EF X C058 X 980		1D45	X 85	6F X 8569 X	1D45	X 856 0001	8 1	1D45
> cpu:cpu0 r1					0003	0013						
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> cpu:cpu0 r6								3D98				
> cpu:cpu0 r7 > cpu:cpu0 A	X 8000 X 11F	1 X 0000 X 3 00 X 0012 X 0		0000	±X	0001 0004	X 00	70 X 0077 X 0000 X	0001	X 078 X 000		0001
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	Name	10.56 us	10.64 us	10.7,2 us	10.8 us	10.88 us	10.96 us	11.Q4 us	11.12 us	11.2 us	11.28 us	11.36 us	11.44 us ^
in	CLOCK_50	пппп	пппп		ппппп	пппг	пппг		ппппп			тппг	ппп
<u> </u>	KEY							X11X01X11X01X1	1X01X11X01X1	1X01X11X01X1	X01X11X01X1	X01X11X01	(11X01X11X(
	SW												
* >	LED	00	V and V and	V anna V anna V	/ 00F4 V 00F0 V		/ 00ED V 00E	V ASST V ASST	V agas V agas V	/ 0000 V 000 V	0000 V 0000 V	0000 V 0000	Vaceva
	cpu:cpu0 PC							7 X 00D7 X 00D4 D X C1C5 X C1			1D4		X 8568 Y
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		44.00		11.50	44.0	11.00	44.70	44.04	11.00	100	10.00	1010	10.01
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	cpu:cpu0 r5 cpu:cpu0 r6 cpu:cpu0 r7 cpu:cpu0 A cpu:cpu0 A cpu:cpu0 AA Name CLOCK_50	12.24 us	X 0080 X X 0000 X X 101 X	0000 000 12,4 us	(0800) 00 (101) 12.48 us	12.56 us	12.64 us	X 8000 X EB2C X 0000 X 101 X 100 12.72 us	X 8000 X X 0000 X 86C6 X 0012 X 0000 X 000 X 110 12.8 us	X 000 X 101 12.88 us	0000 112 011 X 12.96 us	13.Q4 us	0001 0004 000 13.12 us ^
	cpu:cpu0 r5 cpu:cpu0 r6 cpu:cpu0 r7 cpu:cpu0 r7 cpu:cpu0 A cpu:cpu0 data cpu:cpu0 AA Name CLOCK_50 KEY	12.24 us	X 0080 X X 0000 X X 101 X	0000 000 12,4 us	(0800) 00 (101) 12.48 us	12.56 us	12.64 us	X 8000 X FB2C X 00000 X 101 X 100 12.7,2 us	X 8000 X X 0000 X 86C6 X 0012 X 0000 X 000 X 110 12.8 us	X 000 X 101 12.88 us	0000 112 011 X 12.96 us	13.Q4 us	0001 0004 000 13.12 us ^
등) 등) 등) 등)	cpu:cpu0 r5 cpu:cpu0 r6 cpu:cpu0 r7 cpu:cpu0 A cpu:cpu0 AA Name CLOCK_50 KEY SW	12.24 us	X 0080 X X 0000 X X 101 X 12.32 us	0000 000 12.4 us 11.101X11X01X	12.48 us	12.56 us	12.64 us	X 8000 X EB2C	X 8000 X X 0000 X 8606 X 0012 X 0000 X 000 X 110 12,8 us 11X01X11X01X	X 000 X 101 12.88 us 11.01 X 1	12.96 us	13.Q4 us	0001 0004 000 13.12 us ^
	cpu:cpu0 r5 cpu:cpu0 r6 cpu:cpu0 r7 cpu:cpu0 r7 cpu:cpu0 A cpu:cpu0 data cpu:cpu0 AA Name CLOCK_50 KEY	12.24 us 11.01\(11\(10\)) 11.00\(11\(10\))	X 0080 X X 0000 X X 1011 X 12.32 us 17.17 V11 X 11 X 11 X 11 X 11 X 11 X 11 X 1	0000 000 12.4 us X11X01X11X01X	12.48 us 11.01\(\text{11}\(\text{01}\) \(\text{10}\) \(\text{12}\) \(\text{0000}\) \(\text{0000}\) \(\text{0000}\) \(\text{0000}\) \(\text{0000}\)	12.56 us 12.56 us 11.X01X11X01X 01 X 00C2 X 00C3	12.54 us 11.X01 X11X0 X 00C4 X 00C	X 8000 X EB2C X 00000 X 101 X 100 12.72 us 12.72 us 12.72 us 13.73 X 11.70 1 X 12.72 us 15.74 X 12.75 X 0006 X 0007	X 8000 X X 0000 X 8606 X 0012 X 0000 X 000 X 110 12.8 us 11.X01X11X01X X 0008 X 0009	X 000 X 101 12.88 us 11X01X11X01X1 X 00CA X 00CB	12.96 us 1/01/11/01/11 100CC X 00CD	13.Q4 us 1.X01.X11.X01 X.X00CE X.00CE X.00CE	0001 0004 000 13.12 us ^
	cpu:cpu0 r5 cpu:cpu0 r6 cpu:cpu0 r7 cpu:cpu0 A cpu:cpu0 AA Name CLOCK_50 KEY SW LED	12.24 us	X 0080 X X 0000 X X 1011 X 12.32 us 17.17 V11 X 11 X 11 X 11 X 11 X 11 X 11 X 1	0000 000 12.4 us 11.101X11X01X	12.48 us	12.56 us 12.56 us 11.01\(11.01\) 01 \(\times 0.0022 \times 0.0033 \) \(\times 0.568 \)	12.54 us 11.X01 X11X0 X 00C4 X 00C	X 8000 X EB2C	X 8000 X X 0000 X 8606 X 0012 X 0000 X 000 X 110 12.8 us 11.X01X11X01X X 0008 X 0009	X 000 X 101 12.88 us 11.01 X 1	12.96 us 1/01/11/01/11 100CC X 00CD	13.Q4 us 1.X01.X11.X01 X.X00CE X.00CE X.00CE	0001 0004 000 13.12 us ^
	cpu:cpu0 r5 cpu:cpu0 r6 cpu:cpu0 r7 cpu:cpu0 A cpu:cpu0 AA Name CLOCK_50 KEY SW LED cpu:cpu0 PC cpu:cpu0 R cpu:cpu0 PC cpu:cpu0 R cpu:cpu0 R cpu:cpu0 R	12.24 us 11.01\(\text{11}\(\text{01}\) \(\text{00BA}\(\te	X 0080 X X 0000 X X 1011 X 12.32 us 17.17 V11 X 11 X 11 X 11 X 11 X 11 X 11 X 1	0000 000 12.4 us X11X01X11X01X	12.48 us 11.01\(\text{11}\(\text{01}\) \(\text{10}\) \(\text{12}\) \(\text{0000}\) \(\text{0000}\) \(\text{0000}\) \(\text{0000}\) \(\text{0000}\)	12.56 us 12.56 us 11.X01X11X01X 01 X 00C2 X 00C3	12.54 us 11.X01 X11X0 X 00C4 X 00C	X 8000 X EB2C X 00000 X 101 X 100 12.72 us 12.72 us 12.72 us 13.72 x 1	X 8000 X X 0000 X 8606 X 0012 X 0000 X 000 X 110 12.8 us 11.X01X11X01X X 0008 X 0009	X 000 X 101 12.88 us 11X01X11X01X1 X 00CA X 00CB	12.96 us 1/01/11/01/11 100CC X 00CD	13.Q4 us 1.X01.X11.X01 X.X00CE X.00CE X.00CE	0001 0004 000 13.12 us ^
	cpu:cpu0 r5 cpu:cpu0 r6 cpu:cpu0 r6 cpu:cpu0 A cpu:cpu0 AA Name CLOCK_50 KEY SW LED cpu:cpu0 PC cpu:cpu0 IR cpu:cpu0 IR cpu:cpu0 IR cpu:cpu0 r0 cpu:cpu0 r1	12.24 us 11.01\(\text{11}\(\text{01}\) \(\text{00BA}\(\te	X 0080 X X 0000 X X 1011 X 12.32 us 17.17 V11 X 11 X 11 X 11 X 11 X 11 X 11 X 1	0000 000 12.4 us X11X01X11X01X	12.48 us 11.01\(\text{11}\(\text{01}\) \(\text{10}\) \(\text{12}\) \(\text{0000}\) \(\text{0000}\) \(\text{0000}\) \(\text{0000}\) \(\text{0000}\)	12.56 us 12.56 us 11.01\(11.01\) 01 \(\times 0.0022 \times 0.0033 \) \(\times 0.568 \)	12.54 us 11.X01 X11X0 X 00C4 X 00C	X 8000 X EB2C X 00000 X 101 X 100 12.72 us 12.72 us 12.72 us 13.72 x 1	X 8000 X X 0000 X 8606 X 0012 X 0000 X 000 X 110 12.8 us 11.X01X11X01X X 0008 X 0009	X 000 X 101 12.88 us 11X01X11X01X1 X 00CA X 00CB	12.96 us 1/01/11/01/11 100CC X 00CD	13.Q4 us 1.X01.X11.X01 X.X00CE X.00CE X.00CE	0001 0004 000 13.12 us ^
	Cpu:cpu0 r5	12.24 us 11.01\(\text{11}\(\text{01}\) \(\text{00BA}\(\te	X 0080 X X 0000 X X 1011 X 12.32 us 17.17 V11 X 11 X 11 X 11 X 11 X 11 X 11 X 1	0000 000 12.4 us X11X01X11X01X	12.48 us 11.01\(\text{11}\(\text{01}\) \(\text{10}\) \(\text{12}\) \(\text{0000}\) \(\text{0000}\) \(\text{0000}\) \(\text{0000}\) \(\text{0000}\)	12.56 us 12.56 us 11.01\(11.01\) 01 \(\times 0.0022 \times 0.0033 \) \(\times 0.568 \)	12.54 us 11.X01 X11X0 X 00C4 X 00C	X 8000 X EB2C X 00000 X 101 X 100 12.72 us 12.72 us 12.72 us 13.72 x 1	X 8000 X X 0000 X 8606 X 0012 X 0000 X 000 X 110 12.8 us 11.X01X11X01X X 0008 X 0009	X 000 X 101 12.88 us 11X01X11X01X1 X 00CA X 00CB	12.96 us 1/01/11/01/11 100CC X 00CD	13.Q4 us 1.X01.X11.X01 X.X00CE X.00CE X.00CE	0001 0004 000 13.12 us ^
	cpu:cpu0 r5 cpu:cpu0 r6 cpu:cpu0 r7 cpu:cpu0 A cpu:cpu0 AA Name CLOCK_50 KEY SW LED cpu:cpu0 PC cpu:cpu0 R cpu:cpu0 r1 cpu:cpu0 r2 cpu:cpu0 r2 cpu:cpu0 r2 cpu:cpu0 r3	12.24 us 11.200 11.200 11.201 11.211.211.201 11.212.24 us 11.212.24 us 11.222.24 us 11.2222.24 us 11.222.24 us 12.222.24 u	X 0080 X X 0000 X X 1011 X 12.32 us (11.V01.X11.V01 8 X 0080 X 008 X 856	0000 000 12,4 us X11X01X11X01X D X 00BE X 00BF F X 8569 X	12.48 us 12.48 us 111X01X11X01X1 X 00C0 X 00C1 1D45	12.56 us 12.56 us 11.01\(11\)\(01\)\(11\)\(01\)\(11\)\(01\)\(11\)\(01\)\(01\)\(000\)\(12.64 us 11.01 \(\text{11.01} \) \(\text{200c4} \) \(\text{200c4} \) \(\text{200c4} \) \(\text{200c4} \)	X 8000 X EB2C X 0000 X 101 X 100 12.72 us 111X01X11X01X 25 X 0006 X 0007 1D45	X 8000 X X 0000 X 8566 X 0012 X 0000 X 000 X 110 12,8 us 11X01X11X01X X 00068 X 0009 X 8568 X 11E5	X 000 X 101 12.88 us 11X01X11X01X1 X 00CA X 00CB	12.96 us 12.011 X 12.96 us 1/01/11/01/1	13.Q4 us 1.X01.X11.X01 X.X00CE X.00CE X.00CE	0001 0004 000 13.12 us ^
	Cpu:cpu0 r5	12.24 us 11.200 11.200 11.201 11.211.211.201 11.212.24 us 11.212.24 us 11.222.24 us 11.2222.24 us 11.222.24 us 12.222.24 u	X 0080 X X 0000 X X 1011 X 12.32 us (11.V01.X11.V01 8 X 0080 X 008 X 856	0000 000 12.4 us 11\(1\)\(1\)\(1\)\(1\)\(1\)\(1\)\(1\)\(12.48 us 12.48 us 111X01X11X01X1 X 00C0 X 00C1 1D45	12.56 us 12.56 us 11.01\(11\)\(01\)\(11\)\(01\)\(11\)\(01\)\(11\)\(01\)\(01\)\(000\)\(12.64 us 11.01 \(\text{11.01} \) \(\text{200c4} \) \(\text{200c4} \) \(\text{200c4} \) \(\text{200c4} \)	X 8000 X EB2C X 00000 X 101 X 100 12.72 us 12.72 us 12.72 us 13.72 x 1	X 8000 X X 0000 X 8566 X 0012 X 0000 X 000 X 110 12,8 us 11X01X11X01X X 00068 X 0009 X 8568 X 11E5	X 000 X 101 12.88 us 11X01X11X01X1 X 00CA X 00CB	12.96 us 12.011 X 12.96 us 1/01/11/01/1	13.Q4 us 1.X01.X11.X01 X.X00CE X.00CE X.00CE	0001 0004 000 13.12 us ^
	cpu:cpu0 r5 cpu:cpu0 r6 cpu:cpu0 r6 cpu:cpu0 A cpu:cpu0 AA Name CLOCK_50 KEY SW LED cpu:cpu0 PC cpu:cpu0 R cpu:cpu0 r1 cpu:cpu0 r1 cpu:cpu0 r2 cpu:cpu0 r3 cpu:cpu0 r4	12.24 us 11.200 11.200 11.201 11.211.211.201 11.212.24 us 11.212.24 us 11.222.24 us 11.2222.24 us 11.222.24 us 12.222.24 u	X 0080 X X 0000 X X 1011 X 12.32 us (11.V01.X11.V01 8 X 0080 X 008 X 856	0000 12.4 us 11.4 us 11.4 us 11.4 us 12.5 us 12.5 us 12.6 u	12.48 us 12.48 us 111X01X11X01X1 X 00C0 X 00C1 1D45	12.56 us 12.56 us 11.01\(11\)\(01\)\(11\)\(01\)\(11\)\(01\)\(11\)\(01\)\(01\)\(000\)\(12.64 us 11.01 \(\text{11.01} \) \(\text{200c4} \) \(\text{200c4} \) \(\text{200c4} \) \(\text{200c4} \)	X 8000 X EB2C X 0000 X 101 X 100 12.72 us 111X01X11X01X 25 X 0006 X 0007 1D45	X 8000 X X 0000 X 8566 X 0012 X 0000 X 000 X 110 12,8 us 11X01X11X01X X 00068 X 0009 X 8568 X 11E5	X 000 X 101 12.88 us 11X01X11X01X1 X 00CA X 00CB	12.96 us 12.011 X 12.96 us 1/01/11/01/1	13.Q4 us 1.X01.X11.X01 X.X00CE X.00CE X.00CE	0001 0004 000 13.12 us ^
	Cpu:cpu0 r5	12.24 us 11.200 11.200 11.201 11.211.211.201 11.212.24 us 11.212.24 us 11.222.24 us 11.2222.24 us 11.222.24 us 12.222.24 u	X 0080 X X 0000 X X 1011 X 12.32 us 11.01 X11/01 3 X 00BC X 00B X 856	0000 000 12,4 us X11X01X11X01X D X 00BE X 00BF F X 8569 X	12.48 us 12.48 us 111X01X11X01X1 X 00C0 X 00C1 1D45	12.56 us 12.56 us 11.01\(11\)\(01\)\(11\)\(01\)\(11\)\(01\)\(11\)\(01\)\(01\)\(000\)\(12.64 us 11X01X11X01 X 00C4 X 000 X	X 8000 X EB2C X 0000 X 101 X 100 12.72 us 111X01X11X01X 25 X 0006 X 0007 1D45	X 8000 X X 0000 X 8506 X 0012 X 0000 X 000 X 110 12,β us 11X01X11X01X X 00068 X 0009 X 8568 X 11E5 X 7800	X 000 X 101 12.88 us 11X01X11X01X1 X 00CA X 00CB	12.96 us 12.96 us 12.011 \(\text{1.01} \text{1.01} \) 1000C \(\text{0.00CD} \) (000C \(\text{0.00CD} \) (000C \(\text{0.00CD} \) (000C \(\text{0.00CD} \) (000C \(\text{0.00CD} \)	13.Q4 us 13.Q4 us 1X01X11X01 X X X X X X X X X X X X X	0001 0004 000 13.12 us ^
	cpu:cpu0 r5 cpu:cpu0 r6 cpu:cpu0 r6 cpu:cpu0 A cpu:cpu0 AA Name CLOCK_50 KEY SW LED cpu:cpu0 PC cpu:cpu0 r0 cpu:cpu0 r1 cpu:cpu0 r1 cpu:cpu0 r2 cpu:cpu0 r3 cpu:cpu0 r4 cpu:cpu0 r5 cpu:cpu0 r7 cpu:cpu0 r7 cpu:cpu0 r7 cpu:cpu0 r7 cpu:cpu0 r7	12.24 us 11./01/11/01/11/01/ X 000BA X 000BE 1D45 X 000E X 0010	X 0080 X X 0090 X X 1011 X 12.32 us (11X01X11X01 3 X 008¢ X 008 X 856	0000 12,4 us 11,101 \ 11,01 \ 11,01 \ 11,01 \ 10,008E \ 0,008E \ 0,008E \ 0,008E \ 0,008E \ 0,007E \ 0,0000	X 0800	12.56 us 12.56 us 12.56 us 13.01\(11\)\(01	12.64 us 11.01 \text{\text{1.64 us}} \text{\tinx{\text{\ti}\text{\texi{\text{\texi\text{\texi}\tint{\text{\text{\text{\text{\text{\text{\text{\text{\texi}\text{\text{\texi{\text{\texi{\texi{\texi{\text{\texi{\texi{\texi}\ti\tint{\texi{\texi}\texi{\texi{\texi{\texi{\texi{\texi{\texi	X 8000 X EB2C X 00000 X 101 X 100 D 12.72 us	X 8000 X X 0000 X 8606 X 0012 X 0000 X 000 X 110 12.8 us 11X01X11X01X X 0008 X 0009 X 8568 X 11E5 X 7800 X 7800 X 682 X 0012 X 00	X 000 X 101 12.88 us 11.01X11X01X11X01X11X01X11X01X11X01X1X00CA X 00CB X 1175 X 14EF 11.01X1X1X00CA X 00CB	12.96 us 12.96 us 1/01/11/01/0	13.Q4 us 1.X01.X11.X01 X OOCE X OOCE X OOCE X OAFD X C21	0001 0004 000 13.12 us ^
	Cpu:cpu0 r5	12.24 us 11.21 voi 11.20 voi 11.20 voi 11.20 voi 11.20 voi 2.24 us 2.2	X 0080 X X 0090 X X 1011 X 12.32 us (11X01X11X01 3 X 008¢ X 008 X 856	0000 12.4 us 12.7 us 12.7 us 12.8 us 12.8 us 12.8 us 12.8 us 12.9 u	X 0800 X 000 X 101 X 0000 X 0000 X 0000 X 0010 0001	12.56 us 12.56 us 11.01\(11\)\(01\)\(11\)\(01\)\(11\)\(01\)\(01\)\(01\)\(00\)\	12.64 us 11.01 \text{\text{1.64 us}} \text{\tinx{\text{\ti}\text{\texi{\text{\texi\text{\texi}\tint{\text{\text{\text{\text{\text{\text{\text{\text{\texi}\text{\text{\texi{\text{\texi{\texi{\texi{\text{\texi{\texi{\texi}\ti\tint{\texi{\texi}\texi{\texi{\texi{\texi{\texi{\texi{\texi	X 8000 X EB2C X 00000 X 101 X 100 12.72 us 12.72	X 8000 X X 0000 X 8606 X 0012 X 0000 X 000 X 110 12.8 us 11X01X11X01X X 0008 X 0009 X 8568 X 11E5 X 7800 X 7800 X 682 X 0012 X 00	X 000 X 101 12.88 us 11.701 X 11.701 X 11.701 X 14EF	12.96 us 12.96 us 1/01/11/01/0	13.Q4 us 1.X01.X11.X01 X OOCE X OOCE X OOCE X OAFD X C21	0001 0004 000 13.12 us ^



Test 2:

Floating Point values used in the test and their decimal values:

4AEC: 5.4609375

1DA0: 0.106445313

A75B: -0.239929199

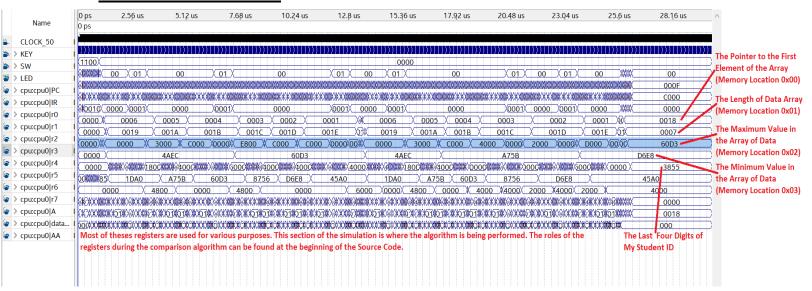
60D3: 35.296875 (This should be the Maximum Value)

8756: -0.014976501

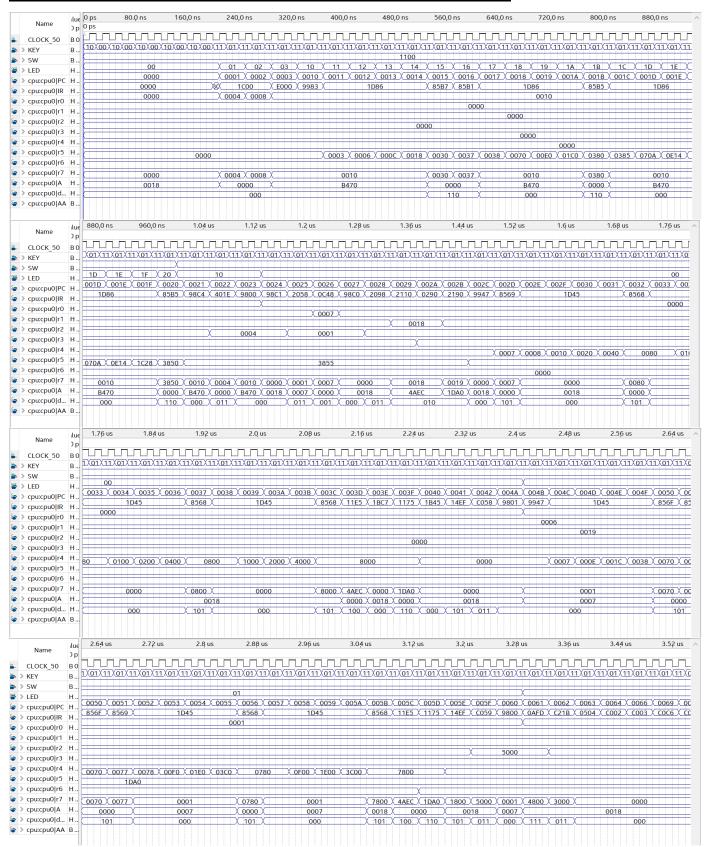
D6E8: -14.90625 (This should be the Minimum Value)

45A0: 3.40625

Full Simulation Results:



Test 2 Zoomed In Until Final Results of Simulation Are Generated:



	Name	ιluε	3.52 us	3.6 us	3.68 us	3.76 us	3.84 us	3.92 us	4.Q us	4.08 us	4.16 us	4.2,4 us	4.32 us	4.4 us ^
) р В 0								пппп	пппп		ппп	
<u> </u>	CLOCK_50 KEY	В 0			11X01X11X01X									
> >		В												
₩>	LED	н	V 0060 V 0007	V 0000 V 0000	V 000D V 000F	V 0004 V 006	V 0067 V 004	0 V 0030 V 003	V 003D V 003F	V 003F V 0030	V 0031 V 0033	V 0022 V 0024	V 0035 V 00	26 \ 0027 \ 00
	cpu:cpu0 PC				X 008D X 008E X C00A X C1C4			X 2190 X 994		1D45	X 8568		D45	X 8568 X
	cpu:cpu0 IR cpu:cpu0 r0													
	cpu:cpu0 r1				X									00
	cpu:cpu0 r2			****						3000				001A
	cpu:cpu0 r3									3000				4AEC
	cpu:cpu0 r4 cpu:cpu0 r5		1	800					X 0007 X 0008	X 0010 X 0020	X 0040 X 00	080 X 0100	X 0200 X 04	00 X 0800
	cpu:cpu0 r6							4800						
	cpu:cpu0 r7			X 0019 X 0006	X 0005 X	0000		X 001A X 000) X 0007 X	0000	X 0080	X o	0000	X 0800 X
		н		X 1DA0 X 0	0000 X	0018	8	X A75B X 001		0018	X 0000	X		0018
	cpu:cpu0 d cpu:cpu0 AA			X 010 X (001 X	000		X 010 X 000	X 101 X	000	X 101	X(000	101
• /	сра.сраојяя	Б												
		ılue	4.4 us	4.48 us	4.56 us	4.64 us	4.72 us	4.8 us	4.88 us	4.96 us	5.04 us	5.12 us	5.2 us	5.28 us ^
	Name) p												
<u>in</u> _	CLOCK_50	ВО												
	KEY	B	ALVITABLET		1X01X11X01X11	IVATVITVATY	117017117017				IVATVITVATYT	ואמואוואמואן		I VII VOI VII VOI
	SW LED	н							00					
	cpu:cpu0 PC			0039 X 003A 1D45	003B X 003C X									
	cpu:cpu0 IR		3568 X	1043	V 8368 Y	TIES / TBC7	<u>∧ 11/3 ∧ 1845</u>	∧ 14EF ∧ CU58	0000 C21B	X 0504 X C0C6 X	COUS A COCE	€004 ∧ 0290	∧ UC48 X COO	M ∧ C1C4 ∧ C10
	cpu:cpu0 r0		0005										X	
	cpu:cpu0 r1		001A										X	
	cpu:cpu0 r3		4AEC					X 4	000 X					
	cpu:cpu0 r4			1000 X 2000	4000 X	8000		X				4000		
	cpu:cpu0 r5						A75B							
	cpu:cpu0 r7		0800 X	0000	Y 8000 Y	4AEC Y 0000	X A75B X 0000	X 4000	X 0000 X C000	V	0000	Y 001A	X 0005 X 000	V4 V
	cpu:cpu0 A	н	0018	0000	X 8000 X	0000 X 0018		4000		018	0000		X 0000 X 385	
	cpu:cpu0 d		101 X	000	X 101 X	100 000	X 110 X 000	X 101 X 011	X 111 X 011	X	000	X 010	X 001	
•	cpu:cpu0 AA	\ В												
							<u> </u>							
			5.36 us	5.44 us	5.52 us	5.6 us	5.68 us							
	Name	ilue				'	0.00	5.76 us	5.8 ₄ us	5.92 us	6.Q us	6.08 us	6.16 us	6.24 us
in		Эp							J.5,7 43	5.92 us				6.24 us
<u>i</u>	Name CLOCK_50 KEY			 11X01X11X01X	 11X01X11X01X									
>	CLOCK_50 KEY SW	Эр В 0 В В		11X01X11X01X										
⇒ >	CLOCK_50 KEY SW LED	Эр ВО В В	1X01X11X01X		11X01X11X01X X 002C X 002D	11X01X11X01	X11X01X11X01	X11X01X11X01	\ X11X01X11X01			11X01X11X01X	(11X01X11X0	7171701X11XC
	CLOCK_50 KEY SW LED cpu:cpu0 PC) р В 0 В В Н	1X01X11X01X 006A X 0067	X 0049 X 002B		11X01X11X01 X 002E X 002I	X11X01X11X01	X11X01X11X01	\ X11X01X11X01		11X01X11X01X X 0038 X 0039	11X01X11X01X	(11)X01)X11X0 3 X 003C X 00	7171701X11XC
* > * > * * > * * * * * * * * * * * * *	CLOCK_50 KEY SW LED) р В 0 В В Н Н	1X01X11X01X 006A X 0067	X 0049 X 002B	X 002¢ X 002D	11X01X11X01 X 002E X 002I	X11X01X11X01 FX 0030 X 003	X11X01X11X01 1 X 0032 X 003	X11X01X11X01X 3 X 0034 X 0035	11X01X11X01X X 0036 X 0037	11X01X11X01X X 0038 X 0039	X 003A X 003B	(11)X01)X11X0 3 X 003C X 00	D1X11X01X11XC
* > > > > > > > > > > > > > > > > > > >	CLOCK_50 KEY SW LED cpu:cpu0 PC cpu:cpu0 IR cpu:cpu0 r0 cpu:cpu0 r1) р В 0 В Н Н Н	1X01X11X01X 006A X 0067	X 0049 X 002B	X 002¢ X 002D	11X01X11X01 X 002E X 002I	X11X01X11X01 FX 0030 X 003	X11X01X11X01 1 X 0032 X 003	X11X01X11X01X 3 X 0034 X 0035	11X01X11X01X X 0036 X 0037	11X01X11X01X X 0038 X 0039	X 003A X 003B	(11)X01)X11X0 3 X 003C X 00	D1X11X01X11XC
# > # > # > # > # > # > # > # >	CLOCK_50 KEY SW LED cpu:cpu0 PC cpu:cpu0 R cpu:cpu0 r0 cpu:cpu0 r1 cpu:cpu0 r2	Эр Во В Н Н Н Н	1X01X11X01X 006A X 0067	X 0049 X 002B	X 002¢ X 002D	11X01X11X01 X 002E X 002I	X11X01X11X01 FX 0030 X 003 1D45	X11X01X11X01 1 X 0032 X 003	X11X01X11X01X 3 X 0034 X 0035	11X01X11X01X X 0036 X 0037	11X01X11X01X X 0038 X 0039	X 003A X 003B	(11)X01)X11X0 3 X 003C X 00	D1X11X01X11XC
	CLOCK_50 KEY SW LED cpu:cpu0 PC cpu:cpu0 IR cpu:cpu0 r0 cpu:cpu0 r1	Эр Во В Н Н Н Н Н	1X01X11X01X 006A X 0067	X 0049 X 002B	X 002C X 002D X 9947 X 8569	11X01X11X01 X 002E X 002E X	X11X01X11X01 X11X01X11X01 EX 0030 X 003 1045	X11X01X11X01 1 X 0032 X 003 X 8568 X	X11X01X11X01X 3 X 0034 X 0035 1045	(11X01X11X01X X 0036 X 0037 X 8568	11X01X11X01X X 0038 X 0039 X 11	11X01X11X01X X 003A X 003B	(11X01X11X0 3 X 003C X 00 X 8568 X 11	23D X 003E X 00 25 X 1BC7 X 11
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	Name	ılue	7.12 us	7.2 us	7.28 us	7.36 us	7.44 us	7.52 us	7.6 us	7.68 us	7.76 us	7.8 ₄ us	7.92 us	8.0 us ^
n_) p B0												
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	cpu:cpu0 IR cpu:cpu0 r0													
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in_	CLOCK_50	ВО												
	KEY	В	11X01X11X01X	11X01X11X01X	11X01X11X01X	(11X01X11X0 ⁻	1X11X01X11X0	1X11X01X11X0	1X11X01X11X01	X <u>11X01X11X01</u> X	11X01X11X01X1	1X01X11X01	X11X01X11X0	1X11X01X11X
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## > > > > > > > > > > > > > > > > > >	Name CLOCK_50 KEY SW LED cpurcpu0 PC cpurcpu0 r0 cpurcpu0 r1 cpurcpu0 r3 cpurcpu0 r4 cpurcpu0 r5 cpurcpu0 r4 cpurcpu0 r5 cpurcpu0 r5 cpurcpu0 r5 cpurcpu0 r5 cpurcpu0 r5 cpurcpu0 A Name CLOCK_50 KEY SW LED cpurcpu0 R	llue) p B 0 H H H H B B 0 B 0 B 0 B 0 H H	(11X01X11X01) 2 X 0043 X 0044 3 X 0AFD X C211 4000 X 40000 X 40000 X 1111 X 011 9.76 us 11X01X11X01X X 0032 X 0033 X 8568 X 4 0080	11X01X11X01 4 X 0047 X 004 3 X 0504 X COC 3 X 0504 X COC 3 X 0504 X COC 11X01X11X01 1X01X11X01 1X01X1X01 1X01X1X01 1X01X1X01 1X01X1X01 1X01X1X01 1X01X1X01 1X01X1X01 1X01X1X01 1X01X1X01 1X01X1X01 1X01X1X01 1X01X1X01 1X01X1X01 1X01X1X01 1X01X1X01 1X01X1X01 1X01X1 1X01X1X01 1X01X1X01 1	X11X01X11X01 8 X 0066 X 006 6 X C003 X C0C 0000 0000 9.92 us (11X01X11X01) X 8566 001C	X11X01X11X0 99 X 0087 X 00 66 X C004 X 0. 44 X 00 X 10.0 us X11X01X11X0 7 X 0038 X 00 3 X 00002 00000 X 10	01X11X01X11X 08B X 008C X 0 290 X 0C4B X C 101C X 0003 X 0 756 X 0000 110 X 001 10.08 us 11.01 X 11.01 11.01 X 11.01 11.01 X 11.01 11.01 X 10.01 10.05 Us 10.05	01X11X01X11X 08D X 008E X 0 000A X C1C4 X C 000A X C1C4 X C 0002 X X X 10.16 us 21X11X01X11X(6) 23B X 003C X 00 X 8568 X 1	01X11X01X11X0 08A X 006A X 00 100 X C1C5 X 0000 0018 0000 10.24 us 10.24 us 01X11X01X11X01 03D X 003E X 003 E5 X 1BC7 X 117 0000 0000 0018 0000 0018 0000 0018 0000 0018 0000 0018 0000 0018 0000 0018 0000 0018 0000 0018 0000 0000 0018 0000 0018 0000 0018 0000 0018 0000 0018 0000 0018 0000 0018 0000 0018 0000 0018 0000 0018 0000 0018 0000 0018 0000 0018 0000 0000 0018 00000 00000 00000 0000	X001 X001 X001 X001 X001 X001 X001 X001	X11X01X11X01X B X 002C X 002D O X 9947 X 8569 X 0000 X 0007 X 0000 X 0007 B X 0018 X 0000 O X 000 X 101 10,4 us (11X01X11X01X X 0042 X 0043 X 0058 X 0AFD	10.48 us 11.X01.X11.X01 X 0008 X 000	00 2F \ 0030 \ 0 1D45 0000 0000 0000 0000 0018 0000 10.56 us X11\X01\X11\X6 7 \ 0048 \ X6 4 \ COC6 \ X6 6003	031 X 0032 X X 8568 X 040 X 0080 X X 0080 X X 0000 X X 101 X 10.64 us ^ 11.64 us ^ 12.11101X11
##	Name CLOCK_50 KEY SW LED cpurcpu0 PC cpurcpu0 r0 cpurcpu0 r1 cpurcpu0 r3 cpurcpu0 r4 cpurcpu0 r5 cpurcpu0 r4 cpurcpu0 r5 cpurcpu0 r6 cpurcpu0 r6 cpurcpu0 r6 cpurcpu0 r6 cpurcpu0 r6 cpurcpu0 AA Name CLOCK_50 KEY SW LED cpurcpu0 r1 cpurcpu0 r2 cpurcpu0 r3 cpurcpu0 r3 cpurcpu0 r3 cpurcpu0 r3 cpurcpu0 r4 cpurcpu0 r2 cpurcpu0 r4 cpurcpu0 r4 cpurcpu0 r6 cpurcpu0 r6 cpurcpu0 r7 cpurcpu0 r6 cpurcpu0 r7 cpurcpu0 r6 cpurcpu0 r7 cpurcpu0 r6 cpurcpu0 r	llue	(11X01X11X01) (11X01X11X01) (11X01X11X01) (11X01X11X01X (11X01X1X01X	11X01X11X01 20X 20X 20X 20X 20X 20X 20X 20X	X11X01X11X01 8 X 0066 X 006 6 X C003 X C00 0000 0000 9.92 us (11X01X11X01) 3 X 0036 X 0037 X 8568 0010 X 0800 (10X11X01) (10X1X11X01) (10X11X01) (X11X01X11X0 X11X01X11X0 X11X01X11X0 44 X00 X8 X11X01X11X0 7 X 0038 X 00 3 X 00002 00002 00000 X 100 00018	01X11X01X11X 088 X 008C X 0 290 X 0C48 X C X X X 0000 01C X 0003 X 0 756 X 0000 110 X 001 10.08 us 11X11X01X11XC 139 X 003A X 0C 1045 000 X 2000 X 4C	01X11X01X11X 08D X 008E X 0 000A X C1C4 X C	01X11X01X11X0 01X11X01X11X0 08A X 006A X 00 100 X C1C5 X 0000 0018 000 0018 000 10.24 us 11X11X01X11X01 11X11X01X11X01 155 X 18C7 X 117 8000 066 003 X 0000 X 066 000 X 0018 X 000	10.32 us 10.32 us 10.32 us 10.32 us 10.32 us 10.32 us 10.34 us 10.35 us 10.35 us	X11X01X11X01X B X 002C X 002D 0 X 9947 X 8569 X 00007 X 00007 B X 0018 X 0000 0 X 0000 X 101 10.4 us X 0042 X 0043 X 0042 X 0043 X 0042 X 0043 X 0042 X 0043 X 0040 X 0000	10.48 us 10.48 us 10.48 us 10.48 us 10.48 us 10.48 us	00 PF X 0030 X 0 1D45 0000 0000 0000 0000 10.56 us 10.56 us 7 X 0048 X 00 4 X COC6 X CO	01\(\)11\(\)01\(\)11\(\)031\(\)0032\(\)\(\)\(\)\(\)\(\)\(\)\(\)\(\)\(\)\(\
##	Name CLOCK_50 KEY SW LED cpuccpu0 PC cpucpu0 r1 cpuccpu0 r2 cpuccpu0 r3 cpuccpu0 r3 cpuccpu0 r4 cpuccpu0 r4 cpuccpu0 r5 cpuccpu0 r4 cpuccpu0 r5 cpuccpu0 r6 cpuccpu0 r7 cpuccpu0 AA Name CLOCK_50 KEY SW LED cpuccpu0 R	Luce 2 ps B B B B B B B B B B B B B B B B B B	(11X01X11X01) 2 X 0043 X 0044 3 X 0AFD X C211 4000 X 4000 X 0000 X 111 X 011 9.76 us 11X01X11X01X X 0032 X 0033 X 8568 X X 0080 X 0080	11X01X11X01 4 X 0047 X 004 3 X 0504 X COC 3 X 0504 X COC 3 X 0504 X COC 11X01X11X01 1X01X11X01 1X01X1X01 1X01X1X01 1X01X1X01 1X01X1X01 1X01X1X01 1X01X1X01 1X01X1X01 1X01X1X01 1X01X1X01 1X01X1X01 1X01X1X01 1X01X1X01 1X01X1X01 1X01X1X01 1X01X1X01 1X01X1X01 1X01X1 1X01X1X01 1X01X1X01 1	X11X01X11X01 8 X 0066 X 006 6 X C003 X C0C 0000 0000 9.92 us (11X01X11X01) X 8568 001E	X11X01X11X0 X11X01X11X0 X11X01X11X0 44 X00 X8 X11X01X11X0 7 X 0038 X 00 3 X 00002 00002 00000 X 100 00018	01X11X01X11X 08B X 008C X 0 290 X 0C4B X C 101C X 0003 X 0 756 X 0000 110 X 001 10.08 us 11.01 X 11.01 11.01 X 11.01 11.01 X 11.01 11.01 X 10.01 10.05 Us 10.05	01X11X01X11X 08D X 008E X 0 000A X C1C4 X C	0000 0000 0000 0000 0000 0000 0018 0000 10.24 us 10.211100111101 0000 0018 0000 0018 0000 0018 0000 0018 0000 0018 0000 0018	10.32 us 10.32 us 10.32 us 10.32 us 10.32 us 10.32 us 10.34 us 10.35 us 10.35 us	X11X01X11X01X B X 002C X 002D 0 X 9947 X 8569 X 00007 X 00007 B X 0018 X 0000 0 X 0000 X 101 10.4 us X 0042 X 0043 X 0042 X 0043 X 0042 X 0043 X 0042 X 0043 X 0040 X 0000	10.48 us 10.48 us 10.48 us 10.48 us 10.48 us 10.48 us	00 PF X 0030 X 0 1D45 0000 0000 0000 0000 10.56 us 10.56 us 7 X 0048 X 00 4 X COC6 X CO	031 X 0032 X X 8568 X 040 X 0080 X X 0080 X X 0000 X X 101 X 10.64 us ^ 11.64 us ^ 12.11101X11

CLOCK_50) p												
> KEY	В	1X01X11X01X	11 (01) 11 (0	1X11X01X11X01	(11X01X11X01	X11X01X11X01	X11X01X11X01	X11X01X11X01	X11X01X11X01	X11X01X11X01	(11)(01)(11)(01	X11X01X11X0	1X11X01X
> sw	В												
> LED	Н.,												
> cpu:cpu0 PC	Н.,			8C X 008D X 008E 48 X C00A X C1C4									
> cpu:cpu0 IR		COC6 / COO4	\ 0290 \ 0C	48 A COUA A CTC4	1 × C100 × C1C	3 \ C102	X 2190 X 994	7 \ 8369 \	1D45	X 8568	*	1D45	X 8568
> cpu:cpu0 r0				X									
> cpu:cpu0 r1			X										
> cpu:cpu0 r2									C000				
> cpu:cpu0 r3 > cpu:cpu0 r4													
> cpu:cpu0 r5			4000					X 0007 X 000	8 X 0010 X 002	0 X 0040 X (0080 X 010	0 X 0200 X 04	00 X 0
> cpu:cpu0 r6							X						
> cpu:cpu0 r7	1 1	•	0000 X 001D X 00	03 Y 0001 Y	000	0	X 001E X 0000	2 Y 0007 Y	0000	X 0080	, 	0000	X 0800
> cpu:cpu0 A	114		X D6E8 X 00		001		X 45A0 X 001		0018	X 0000		0000	0000
> cpu:cpu0 d	н		X 010 X	001 X	000		X 010 X 000		000	X 101	X	000	X 101
> cpu:cpu0 AA	В												
Name	ılue	11.52 us	11.6 us	11.68 us	11.76 us	11.84 us	11.92 us	12.0 us	12.Q8 us	12.16 us	12.24 us	12.32 us	12.4 u
	Эр В0	1			пппп	пппп		пппп	пппп	пппп	пппп		ппп
	В			X11X01X11X01X									X11X01X1
	В												
	н.,							X					
> cpu:cpu0 PC	н			A X 003B X 003C									
> cpu:cpu0 IR	н	8568 X	1D45	₹ 8568	∧ 11E3 ↓ 1BC7	<u> </u>	5 X 14EF X C058	<u> </u>	^1	D45	X 856F X 8569	<u>'</u>	1D45
> cpu:cpu0 r0								0001					
> cpu:cpu0 r1							0	01E					
> cpu:cpu0 r2													0000
> cpu:cpu0 r3 > cpu:cpu0 r4													
> cpu:cpu0 r4 > cpu:cpu0 r5		0800	X 1000 X 200	0 X 4000 X	8000	X	0000		X 0007 X 000E	X 001C X 0038	<u> </u>		
> cpu:cpu0 r6													45A0
> cpu:cpu0 r7		0800 X	0000	X 8000	X 60D3 X 0000	X 45A0 X	0000		0001		X 0070 X 0077	X	0001
> cpu:cpu0 A		0018			X 0000 X 0018		0018	X	0007		X 0000		0007
	lu II		000	X 101		X 110 X 000		X T	000		X 101	X T	000
		101											
	В	12.4 us	12.48 us	12.56 us	12.64 us	12.72 us	12.8 us	12.88 us	12.96 us	13.Q4 us	13.12 us	13.2 us	13.28 u
> cpu:cpu0 AA Name CLOCK_50	llue) p B O	12.4 us	12.48 us	12.56 us	12.64 us	12.7,2 us	12.8 us						13.28 u
Name CLOCK_50 KEY	B ilue) p B0	12.4 us	12.48 us		12.64 us	12.7,2 us	12.8 us						13.28 u
Name CLOCK_50 KEY SW LED	llue) p B 0 B B H	12.4 us \(\text{\tint{\text{\tint{\text{\tint{\text{\tint{\text{\text{\text{\text{\text{\text{\tin\text{\texit{\text{\texi}\text{\text{\texi}\text{\texit{\texit{\texi}\tint{\ti}\text{\texit{\texit{\texit{\texit{\texi\tin}\tint{\texitit{\texi{\texi{\texi{\texi{\texi{\texi{\texi\tint{\ti}}}\tiint{\t	12.48 us 1X01X11X01X	(11X01X11X01X1	12.64 us	12.7,2 us	12.8 us	1X01X11X01X	11X01X11X01X1	1X01X11X01X1	1X01X11X01X	 11X01X11X01	13.28 u
Name CLOCK_50 KEY SW LED cpu:cpu0 PC	B lue) p B0 B H H	12.4 us (01\(11\(\) 01\(\) 1 00054\(\) 0055\(\)	12.48 us 1X01X11X01X 1 0056 X 0057		12.64 us 12.04 us 12.01	12.7,2 us 11.7,2 us 11.7,01,7,11,7,11,7,1	12.8 us 11.X01X11X01X1 X 005E X 005F	1X01X11X01X 1X01X11X01X X 0060 X 0061	11X01X11X01X1 X 0062 X 0063	11X01X11X01X1 X 0064 X 0066	1X01X11X01X	111X01X11X01 X 008B X 0080	13.28 u
Name CLOCK_50 KEY SW LED CUCK_50	B Ilue) p B0 B B H H	12.4 us (01\(11\(\) 01\(\) 1 00054\(\) 0055\(\)	12.48 us 1X01X11X01X 1 0056 X 0057 8568 X	(11X01X11X01X1 (1X01X11X01X1 (X 0058 X 0059)	12.64 us 12.04 us 12.01	12.7,2 us 11.7,2 us 11.7,01,7,11,7,11,7,1	12.8 us	1X01X11X01X 1X01X11X01X X 0060 X 0061	11X01X11X01X1 X 0062 X 0063	11X01X11X01X1 X 0064 X 0066	1X01X11X01X	111X01X11X01 X 008B X 0080	13.28 u
Name CLOCK_50 > KEY > SW > LED > cpu:cpu0 PC > cpu:cpu0 R > cpu:cpu0 r0	B B B B H H	12.4 us \(\sqrt{1}\text{1}\text{1}\text{1}\text{2}\text{1}\text{2}\text{1}\text{2}\text{2}\text{1}\text{2}\text{2}\text{2}\text{2}\text{3}\text{2}\text{2}\text{3}\text{2}\text{3}\text{5}\text{2}\text{5}\text{3}\text{5}\text{3}\text{5}\text{3}\text{5}\text{3}\text{5}\text{3}\text{5}\text{3}\text{5}\text{3}\text{5}\te	12.48 us 1X01X11X01X 1 0056 X 0057 8568 X	(11X01X11X01X1 (1X01X11X01X1)	12.64 us 12.04 us 12.01	12.7,2 us 11.7,2 us 11.7,01,7,11,7,11,7,1	12.8 us 11.X01X11X01X1 X 005E X 005F	1X01X11X01X 1X01X11X01X X 0060 X 0061	11X01X11X01X1 X 0062 X 0063	11X01X11X01X1 X 0064 X 0066	1X01X11X01X	111X01X11X01 X 008B X 0080	13.28 u
Name CLOCK_50 > KEY > SW > LED > cpu:cpu0 PC > cpu:cpu0 PC > cpucpu0 r0 > cpucpu0 r1	B B B B H H H	12.4 us \(\sqrt{1}\text{1}\text{1}\text{1}\text{2}\text{1}\text{2}\text{1}\text{2}\text{2}\text{1}\text{2}\text{2}\text{2}\text{2}\text{3}\text{2}\text{2}\text{3}\text{2}\text{3}\text{5}\text{2}\text{5}\text{3}\text{5}\text{3}\text{5}\text{3}\text{5}\text{3}\text{5}\text{3}\text{5}\text{3}\text{5}\text{3}\text{5}\te	12.48 us 1X01X11X01X 1 0056 X 0057 8568 X	(11X01X11X01X1 (1X01X11X01X1)	12.64 us 12.04 us 12.01	12.7,2 us 11.7,2 us 11.7,01,7,11,7,11,7,1	12.8 us 11.X01X11X01X1 X 005E X 005F	1X01X11X01X 1X01X11X01X X 0060 X 0061	11X01X11X01X1 X 0062 X 0063	X 0064 X 0066 X 0002 X 0003	1X01X11X01X	111X01X11X01 X 008B X 0080	13.28 u
> cpurcpu0 AA Name	B Ilue) p B0 B H H H H	12.4 us \(\sqrt{1}\text{1}\text{1}\text{1}\text{2}\text{1}\text{2}\text{1}\text{2}\text{2}\text{1}\text{2}\text{2}\text{2}\text{2}\text{3}\text{2}\text{2}\text{3}\text{2}\text{3}\text{5}\text{2}\text{5}\text{3}\text{5}\text{3}\text{5}\text{3}\text{5}\text{3}\text{5}\text{3}\text{5}\text{3}\text{5}\text{3}\text{5}\te	12.48 us 1X01X11X01X 1 0056 X 0057 8568 X	(11X01X11X01X1 (1X01X11X01X1)	12.64 us 12.04 us 12.01	12.7,2 us 11.7,2 us 11.7,01,7,11,7,11,7,1	12.8 us 11.X01X11X01X1 X 005E X 005F	1X01X11X01X 1X01X11X01X X 0060 X 0061	11X01X11X01X1 X 0062 X 0063	11X01X11X01X1 X 0064 X 0066	1X01X11X01X	111X01X11X01 X 008B X 0080	13.28 u
Name CLOCK_50 KEY SW LED cpu:cpu0 PC cpu:cpu0 PC cpu:cpu0 r1 cpu:cpu0 r2 cpu:cpu0 r3	B lue) p B0 B H H H H H	12,4 us (01)(11)(01)(1) (00054 \(\times \) (0055) (00054 \(\times \) (0056)	12.48 us 1.X01X11X01X 1.X0056 X 0057 8568 X 01	(11X01X11X01X1 2 X 0058 X 0059 X 1D45	12.64 us 1.01 × 11 × 01 × 12 × 01 × 01 × 01 × 01 ×	12.7,2 us 11.7,2 us 11.7,01 \(\text{11} \) \(\text{12} \) \(\text{1175} \)	12.8 us 11.X01X11X01X1 X 005E X 005F	1X01X11X01X 1X01X11X01X X 0060 X 0061	11X01X11X01X1 X 0062 X 0063	X 0064 X 0066 X 0002 X 0003	1X01X11X01X	X 008B X 008C X 0290 X 0C48	13.28 u
> cpurcpu0 AA Name CLOCK_50 > KEY > SW > LEB > cpurcpu0 PC > cpurcpu0 PC > cpurcpu0 r1 > cpurcpu0 r2 > cpurcpu0 r3 > cpurcpu0 r3 > cpurcpu0 r3	B Ilue) p B 0 B H H H H H H H H	12.4 us \(\sqrt{1}\text{1}\text{1}\text{1}\text{2}\text{1}\text{2}\text{1}\text{2}\text{2}\text{1}\text{2}\text{2}\text{2}\text{2}\text{3}\text{2}\text{2}\text{3}\text{2}\text{3}\text{5}\text{2}\text{5}\text{3}\text{5}\text{3}\text{5}\text{3}\text{5}\text{3}\text{5}\text{3}\text{5}\text{3}\text{5}\text{3}\text{5}\te	12.48 us 1X01X11X01X 1 0056 X 0057 8568 X	(11X01X11X01X1 (1X01X11X01X1)	12.64 us 1.01 × 11 × 01 × 12 × 01 × 01 × 01 × 01 ×	12.7,2 us 11.7,2 us 11.7,01,7,11,7,11,7,1	12.8 us 11.X01X11X01X1 X 005E X 005F	1X01X11X01X 1X01X11X01X X 0060 X 0061	11X01X11X01X1 X 0062 X 0063	X 0064 X 0066 X 0002 X 0003	1X01X11X01X	X 008B X 008C X 0290 X 0C48	13.28 u
> cpurcpu0 AA Name	B llue Jp BO B Short Bo B H	12,4 us (01)(11)(01)(1) (00054 \(\times \) (0055) (00054 \(\times \) (0056)	12.48 us 1.X01X11X01X 1.X0056 X 0057 8568 X 01	(11X01X11X01X1 2 X 0058 X 0059 X 1D45	12.64 us 1.01 × 11 × 01 × 12 × 01 × 01 × 01 × 01 ×	12.7,2 us 11.7,2 us 11.7,01 \(\text{11} \) \(\text{12} \) \(\text{1175} \)	12.8 us 11.X01X11X01X1 X 005E X 005F	1X01X11X01X 1X01X11X01X X 0060 X 0061	11X01X11X01X1 X 0062 X 0063	X 0064 X 0066 X 0002 X 0003	1X01X11X01X	X 008B X 008C X 0290 X 0C48	13.28 u
>> cpurcpu0 AA Name CLOCK_50 >> KEY >> SW >> LED >> cpurcpu0 PC >> cpurcpu0 r0 >> cpurcpu0 r3 >> cpurcpu0 r3 >> cpurcpu0 r4 >> cpurcpu0 r6	B llue Jp BO B Jp BO B H	12.4 us \(\sqrt{01\times11\times01\times1}\) \(\sqrt{01\times11\times01\times1}\) \(\sqrt{00054\times055}\) \(\sqrt{000}\) \(\sqrt{00050}\) \(000000000000000000000000000000000000	12.48 us 1.X01X11X01X 1.X0056 X 0057 8568 X 01	(11X01X11X01X1 2 X 0058 X 0059 X 1D45	12.64 us 1.2.64 us	12.72 us 11.72 us	12.8 us 11.X01X11X01X1 X 005E X 005F	X X X X X X X X X Y X Y X Y X Y X Y X Y	11X01X11X01X1 X 0062 X 0063 X C21B X 0504	X 0064 X 0066 X 0002 X 0003	1X01X11X01X	X 008B X 008C X 0290 X 0C48	13.28 u
Name CLOCK_50 KEY SW LED CPU:CPU0 PC CPU:CPU0 PC CPU:CPU0 P1 CPU:CPU0 P1 CPU:CPU0 F1 CPU:CPU0 F3 CPU:CPU0 F3 CPU:CPU0 F3 CPU:CPU0 F3 CPU:CPU0 F3 CPU:CPU0 F5 CPU:CPU0 F5 CPU:CPU0 F5 CPU:CPU0 F5 CPU:CPU0 F5 CPU:CPU0 F5	B lue	12.4 us (01\()11\()01\()1 (00054\()0055\() (0	12.48 us 1 \(\text{11.101} \) \(11.10	(11\\01\\11\\01\\11\\01\\11\\01\\11\\01\\11\\01\\11\\01\\11\\01\\11\\01\\11\\01\\11\\01\\11\\01\\11\\01\\11\\01\\11\\01\\11\\01\\11\\01\\11\\0	12.64 us TLTLT 1X01X11X01X (005A X 005B	12.72 us 11.X01X11X01X X 005C X 005D X 11E5 X 1175 7800 X X 60D3 X 45A0 X 0000	12,8 us 11,V01X11X01X11 X 005E X 005E X 14EF X C059 X X X 4000 X 2000 X 0018	1X01X11X01X X X 0060 X 0061 X 9800 X 0AFD X X 0001 X 6000 X 0007 X	X 2000 X	X 0064 X 0066 X C002 X C003 X 2000 2000 0000 0018	1X01X11X01X	X 003B X 008C X 0290 X 0C48 X 0290 X 0C48 X 001E X 0001 X 45A0 X 0007	13.28 u
Name CLOCK_50 KEY SW LED cpu:cpu0 PC cpu:cpu0 r1 cpu:cpu0 r3 cpu:cpu0 r4 cpu:cpu0 r5 cpu:cpu0 r6 cpu:cpu0 r4 c	B llue Jp B0 T B B B H G H H G H H G H H G H H G H H G H H G H H G H H G H	12.4 us (01\()11\()01\()1 (00054\()0055\() (0	12.48 us 1.01\(\text{11}\) 1.0056 \(\text{10}\) 0.056 \(\text{10}\) 0.0780	(11X01X11X01X1 2 X 0058 X 0059 X 1D45 X 0F00 X 1E00 X	12.64 us 1.01 × 11 × 01 × 11 × 01 × 11 × 01 × 11 × 01 × 11 × 01 ×	12.72 us 11.X01X11X01X X 005C X 005D X 11E5 X 1175 7800 X X 60D3 X 45A0 X 0000	12.8 us 11.X01X11X01X1 X 005E X 005E X 14EF X C059 X X	1X01X11X01X X X 0060 X 0061 X 9800 X 0AFD X X 0001 X 6000 X 0007 X	X 2000 X	X 0064 X 0066 X C002 X C003 X C000 X	1X01X11X01X	X 003B X 008C X 0290 X 0C48 X 0290 X 0C48 X 001E X 0001 X 45A0 X 0007	13.28 u 13.28 u 13.28 u 13.28 u 13.28 u 13.28 u 14.000 x 14.000 x 14.000 x 15.0000 x 16.000 x 16.000 x 17.0000 x 18.0000 x 18.000
Name CLOCK_50 KEY SW LED cpu:cpu0 PC cpu:cpu0 r1 cpu:cpu0 r3 cpu:cpu0 r4 cpu:cpu0 r5 cpu:cpu0 r6 cpu:cpu0 r4 c	B llue Jp B0 T B B B H G H H G H H G H H G H H G H H G H H G H H G H H G H	12.4 us (01\()11\()01\()1 (00054\()0055\() (0	12.48 us 1 \(\text{11.101} \) \(11.10	(11\\01\\11\\01\\11\\01\\11\\01\\11\\01\\11\\01\\11\\01\\11\\01\\11\\01\\11\\01\\11\\01\\11\\01\\11\\01\\11\\01\\11\\01\\11\\01\\11\\01\\11\\0	12.64 us TLTLT 1X01X11X01X (005A X 005B	12.72 us 11.X01X11X01X X 005C X 005D X 11E5 X 1175 7800 X X 60D3 X 45A0 X 0000	12,8 us 11,V01X11X01X11 X 005E X 005E X 14EF X C059 X X X 4000 X 2000 X 0018	1X01X11X01X X X 0060 X 0061 X 9800 X 0AFD X X 0001 X 6000 X 0007 X	X 2000 X	X 0064 X 0066 X C002 X C003 X 2000 2000 0000 0018	1X01X11X01X	X 003B X 008C X 0290 X 0C48 X 0290 X 0C48 X 001E X 0001 X 45A0 X 0007	13.28 L \[\sqrt{11\times 1\times 1} \] \[\sqrt{008D} \times 1 \] \[\sqrt{008D} \times 2 \] \[\sqrt{000A} \] \[\sqrt{000D} \] \[\sqrt{000D} \]
Name CLOCK_50 KEY SW LED cpuscpu0 PC cpuscpu0 r1 cpuscpu0 r1 cpuscpu0 r2 cpuscpu0 r4 cpuscpu0 r5 cpuscpu0 r6 cpuscpu0 r6 cpuscpu0 r3 cpuscpu0 r4 cpuscpu0 r3 cpuscpu0 r4 cpuscpu0 r5 cpuscpu0 r6 cpuscpu0 r7 cpuscpu0 d	B	12.4 us (01\()11\()01\()1 (00054\()0055\() (0	12.48 us 1 \(\text{11.101} \) \(11.10	(11\\01\\11\\01\\11\\01\\11\\01\\11\\01\\11\\01\\11\\01\\11\\01\\11\\01\\11\\01\\11\\01\\11\\01\\11\\01\\11\\01\\11\\01\\11\\01\\11\\01\\11\\0	12.64 us TLTLT 1X01X11X01X (005A X 005B	12.72 us 11.X01X11X01X X 005C X 005D X 11E5 X 1175 7800 X X 60D3 X 45A0 X 0000	12,8 us 11,V01X11X01X11 X 005E X 005E X 14EF X C059 X X X 4000 X 2000 X 0018	1X01X11X01X X X 0060 X 0061 X 9800 X 0AFD X X 0001 X 6000 X 0007 X	X 2000 X	X 0064 X 0066 X C002 X C003 X 2000 2000 0000 0018	1X01X11X01X	X 003B X 008C X 0290 X 0C48 X 0290 X 0C48 X 001E X 0001 X 45A0 X 0007	13.28 u
Name CLOCK_50 KEY SW LED cpu:cpu0 PC cpucpu0 r1 cpu:cpu0 r3 cpucpu0 r3 cpucpu0 r4 cpucpu0 r4 cpucpu0 r5 cpucpu0 r6 cpucpu0 r7 cpucpu0 r6 cpucpu0 AA	B	12.4 us \(\sqrt{01\times11\times01\times1}\) \(\sqrt{001\times11\times01\times1}\) \(\sqrt{00054\times055}\) \(\sqrt{00056\times0}\) \(00056\ti	12.48 us 1 \(\text{1.12.48 us} \) 1 \(\text{1.12.11} \) 1 \(\text{1.0056} \times \text{0.0057} \) 1 \(\text{0.056} \times \text{0.0057} \) 0 \(\text{0.780} \times \text{0.0000} \times \text{0.0000} \text{0.0000} \text{0.0000} \text{0.0000} \text{1.3.36 us}	(11\(01\)\(11\)\(01\)\(11\)\(01\)\(11\)\(01\)\(11\)\(01\)\(11\)\(01\)\(11\)\(01\)\(11\)\(01\)\(11\)\(01\)\(11\)\(01\)\(11\)\(01\)\(11\)\(01\)\(01\)\(00\)\(00\)\(13\)\(44\)\(us\)	12.64 us 1 \(\)	12.72 us 11X01X11X01X X 005C X 005D X 11E5 X 1175 7800 X 6003 X 45A0 X 0000 X 100 X 110	12,8 us 11X01X11X01X1 X 005E X 005E X 14EF X C059 X X X 4000 X 2000 X 0018 X 101 X 011 13,68 us	X 0060 X 0061 X 9800 X 0AFD X 0001 X 6000 X 0007 X X 0007 X X 000 X 111	X 2000 X X 2011 X X 2000 X X 218 X 2000 X	X 0064 X 0066 X C002 X C003 X C000 X	1\(\)\(0.01\)\(0.01\)\(0.01\)\(0.01\)\(0.01\)\(0.004\)\(0	X 008B X 0086 X 0290 X 0C48 X 0290 X 0C48 X 001E X 0001 X 45A0 X 0007 X 010 X	13.28 u 13.28 u 13.28 u 13.28 u 13.28 u 14.10 u 14.
Name CLOCK_50 KEY SW LED cpu:cpu0 PC cpu:cpu0 r1 cpu:cpu0 r1 cpu:cpu0 r3 cpu:cpu0 r4 cpu:cpu0 r5 cpu:cpu0 r4 cpu:cpu0 r5 cpu:cpu0 A cpu:cpu0 A Cpu:cpu0 A Cpu:cpu0 A Cpu:cpu0 A Cpu:cpu0 A	B	12.4 us \(11\times 11\times 12\times 12\t	12.48 us 1\(01\)\(11\)\(0056\)\(00	(11X01X11X01X1 X 0058 X 0059 X 1D45 X 0F00 X 1E00	12.64 us 1.01 \(\) 1.00 \(\) 0.05A \(\) 0.05B \(\) 8568 2.600 \(\) \(\) 2.000 \(\) \(\) 0.018 \(\) 1.01 13.52 us	12.72 us 11X01X11X01X X 005C X 005D X 11E5 X 1175 7800 X 60D3 X 45A0 X 0000 X 100 X 110	12,8 us 11,V01X11X01X1 X 005E X 005E X 14EF X C059 X X X 4000 X 2000 X 0018 X 101 X 011 13,68 us	X X X X X X X X X X X X X X X X X X X	X 0062 X 0063 X C21B X 0504 X 2000 X X 2000 X X 011 X	0000 0000 0001 13.92 us	14.0 us	X 003B X 008G X 0290 X 0C4E X 001E X 0001 X 45A0 X 0007 X 14.Q8 us	13.28 u 13.28 u (11X01X11 X 008D X X 000A X X 0000 X 0000 X 0001 X 14.1
Name CLOCK_50 KEY SW LED cpu:cpu0 PC cpu:cpu0 r0 cpu:cpu0 r1 cpu:cpu0 r3 cpu:cpu0 r4 cpu:cpu0 r5 cpu:cpu0 r4 cpu:cpu0 r6 c	B due) p BO B H H H H H H H	12.4 us \(11\times 11\times 12\times 12\t	12.48 us 1\(01\)\(11\)\(0056\)\(00	(11X01X11X01X1 (X 0058 X 0059 X 1045 X 0050 X 1045 X 0000 X 1000 X 10000 X 1000 X 100	12.64 us 1.01 \(\) 1.00 \(\) 0.05A \(\) 0.05B \(\) 8568 2.600 \(\) \(\) 2.000 \(\) \(\) 0.018 \(\) 1.01 13.52 us	12.72 us 11X01X11X01X X 005C X 005D X 11E5 X 1175 7800 X 60D3 X 45A0 X 0000 X 100 X 110	12,8 us 11,V01X11X01X1 X 005E X 005E X 14EF X C059 X X X 4000 X 2000 X 0018 X 101 X 011 13,68 us	X X X X X X X X X X X X X X X X X X X	X 0062 X 0063 X C21B X 0504 X 2000 X X 2000 X X 011 X	0000 0000 0001 13.92 us	14.0 us	X 003B X 008G X 0290 X 0C4E X 001E X 0001 X 45A0 X 0007 X 14.Q8 us	13.28 u 13.28 u 13.28 u 13.28 u 13.28 u 14.10 14.10 14.10
Name CLOCK_50 KEY SW LED cpu:cpu0 PC cpu:cpu0 r1 cpu:cpu0 r1 cpu:cpu0 r2 cpu:cpu0 r3 cpu:cpu0 r4 cpu:cpu0 r4 cpu:cpu0 r5 cpu:cpu0 r4 cpu:cpu0 r4 cpu:cpu0 r4 cpu:cpu0 r5 cpu:cpu0 r4 cpu:cpu0 r4 cpu:cpu0 r4 cpu:cpu0 r5 cpu:cpu0 r4 cpu:cpu0 r5 cpu:cpu0 r4 cpu:cpu0 r5 cpu:cpu0 r6 cpu:cpu0 r6 cpu:cpu0 AA	B due)p BO B) B H H H H H H H B due lue lue lue lue lue lue lue	12.4 us \(11\times 11\times 11\t	12.48 us 1 \(\text{1.48 us} \) 1 \(\text{1.401} \text{1.11} \(\text{0.01} \) 1 \(\text{0.056} \times \text{0.0057} \) 8568 \(\text{0.0056} \text{0.0057} \) 0780 \(\text{0.0000} \text{0.0000} \text{0.0000} \) 13.36 us	(11X01X11X01X1 (11X01X11X01X1 (11X01X11X01X11X01 (11X01X11X01X11X01	12.64 us 1.01 \(\) 1.01 \(\) 1.01 \(\) 1.01 \(\) 1.01 \(\) 1.00 \(\) \(\) 2.668 \(\) 3.600 \(\) \(\) 2.668 \(\) 3.600 \(\) \(\) 2.668 \(\) 3.52 us 13.52 us	12.72 us 11X01X11X01X X 005C X 005D X 11E5 X 1175 7800 X 6003 X 45A0 X 0000 X 100 X 110. 13.6 us	12.8 us 11.V01X11X01X11 X 005E X 005E X 14EF X C059 X 4000 X 2000 X 0018 X 101 X 011 13.68 us	X 0060 X 0061 X 9800 X 0AFD X 0007 X 0007 X 0007 X 0007 X 111 13.76 us	X 2000 X X 011 X 13.84 us	X 0064 X 0066 X 0006 X 0000 X 0000 0000	14.0 us	X 003B X 008G X 0290 X 024E X 001E X 0001 X 45A0 X 0007 X 010 X 01	13.28 u 13.28 u 13.28 u 13.28 u 13.28 u 14.10 14.10 14.10 14.10 14.11 14.11
Name CLOCK_50 KEY SW LED cpu:cpu0 PC cpucpu0 P1 cpu:cpu0 r1 cpu:cpu0 r3 cpu:cpu0 r4 cpu:cpu0 r5 cpu:cpu0 r5 cpu:cpu0 r4 cpu:cpu0 r4 cpu:cpu0 r5 cpu:cpu0 r5 cpu:cpu0 r4 cpu:cpu0 r5 cpu:cpu0 AA Name CLOCK_50 KEY SW LED	B due	12.4 us \(11\times 11\times 12\times 12\t	12.48 us 1\(\text{01\text{\te}\text{\texic}\text{\tex{\text{\text{\text{\text{\text{\text{\text{\text{\text{\text{\tex	(11X01X11X01X1 X 0058 X 0059 X 1045	12.64 us 1.01 \ 1.101 \ 1.101 \ 0.101 \ 0.05A \ 0.05B \	12.72 us 11X01X11X01X X 005C X 005D X 11E5 X 1175 7800 X 0000 X 0000 X 100 X 110 13.6 us 13.7 us	12,8 us 11,V01X11X01X11 X 005E X 005E X 14EF X C059 X X X 4000 X 2000 X 0018 X 101 X 011 13,68 us 13,101 X 111X01	X 0001 X 6000 X 0001 X 6000 X 0000 X 111 13.76 us 111X01X11X01 00 9 X 009A X 009	X 2000 X X 2000 X X 2000 X X 2000 X X 211 X 2000 X X 211 X 2000 X X 211 X 2000 X X 2000 X	X 0064 X 0066 X 0002 X 0002 X 0003 X 0000 0000 0000 0	14.0 us 1.001 × 11.0 us 1.1.0 us	X 003B X 008G X 0290 X 0C4E X 001E X 0001 X 45A0 X 0007 X 010 X 01	13.28 u 13.28 u 13.28 u 13.28 u 13.28 u 13.28 u 14.10 14.1
Name CLOCK_50 KEY SW LED CRUCK_50 CRUCK_50 KEY SW LED CRUCK_50 KEY SW LED CRUCK_50 SW LED CRUCK_50 CRUCK_50 SW LED	B due) p BO B H	12.4 us \(11\times 11\times 12\times 12\t	12.48 us 1\(\text{01\text{\te}\text{\texic}\text{\tex{\text{\text{\text{\text{\text{\text{\text{\text{\text{\text{\tex	(11X01X11X01X1 (11X01X11X01X1 (11X01X11X01X11X01 (11X01X11X01X11X01	12.64 us 1.01 \ 1.101 \ 1.101 \ 0.101 \ 0.05A \ 0.05B \	12.72 us 11X01X11X01X X 005C X 005D X 11E5 X 1175 7800 X 0000 X 0000 X 100 X 110 13.6 us 13.7 us	12,8 us 11,V01X11X01X11 X 005E X 005E X 14EF X C059 X X X 4000 X 2000 X 0018 X 101 X 011 13,68 us 13,101 X 111X01	X 0001 X 6000 X 0001 X 6000 X 0001 X 6000 X 0007 X 000 X 111 13.76 us 111\(01\) 111\(01\) 10 9 \(009\) X 009 7 \(8569\) X	X 2000 X X 011 X 13.84 us	X 0064 X 0066 X 0006 X 0000 X 0000 0000	14.0 us 1.001 × 11.0 us 1.1.0 us	X 003B X 008G X 0290 X 024E X 001E X 0001 X 45A0 X 0007 X 010 X 01	13.28 u 13.28 u 13.28 u 13.28 u 13.28 u 14.10 14.10 14.10 14.10 14.11 14.11
Name CLOCK_50 NEEY SW LED CRUICEPUO PC CRUICEPUO CRUI	B due) p B0 B H	12.4 us \(11\times 11\times 12\times 12\t	12.48 us 1X01X11X01X 1 0056 X 0057 8568 X 01 0780 0780 X 0000 X 101 X 13.36 us (11X01X11X0 X 0090 X 00	(11X01X11X01X1 (X 0058 X 0059) 1D45 (X 0F00 X 1E00) 0001 0007 000 13.44 us (X 11X01X11X01 191 X 10092 X 009 (X 1 X 2058 X 004)	12.64 us	12.72 us 11X01X11X01X X 005C X 005D X 11E5 X 1175 7800 X 0000 X 0000 X 100 X 110 13.6 us 13.7 us	12,8 us 11,V01X11X01X11 X 005E X 005E X 14EF X C059 X X X 4000 X 2000 X 0018 X 101 X 011 13,68 us 13,101 X 111X01	X 0001 X 6000 X 0001 X 6000 X 0000 X 111 13.76 us 111X01X11X01 00 9 X 009A X 009	X 2000 X X 2000 X X 2000 X X 2000 X X 211 X 2000 X X 211 X 2000 X X 211 X 2000 X X 2000 X	X 0064 X 0066 X 0002 X 0002 X 0003 X 0000 0000 0000 0	14.0 us 1.001 × 11.0 us 1.1.0 us	X 003B X 008G X 0290 X 0C4E X 001E X 0001 X 45A0 X 0007 X 010 X 01	13.28 u 13.28 u 13.28 u 13.28 u 13.28 u 13.28 u 14.10 14.1
Name CLOCK_50 KEY SW LED CPUCCPUO 10 CPUCCPUO 10 CPUCCPUO 15 CPUCCPUO 15 CPUCCPUO 16 CPUCCPUO 17 CPUCCPUO 16 CPUCCPUO 17 CPUCCPUO 16 CPUCCPUO 17 CPUCCPUO 16 CPUCCPUO 17	B due) p BO H	12.4 us \(11\times 11\times 12\times 12\t	12.48 us 1 \(\)	11X01X11X01X1 2X 0058 X 0059 X 1045 1045 X 0F00 X 1E00 X 1000 X 1000 X 10007 0007 0000 13.44 us 11X11X01X11X01 11X11X01X11X01 11X11X01X11X01 11X1X01X11X01 11X1X01X11X01 11X1X01X11X01 11X1X01X11X01 11X1X01X11X01 11X1X01X11X01 11X1X01X11X01 11X1X01X11X01 1XX1X01X11X01 1XX1X01X1X01 1XX1X01X11X01 1XX1X01X1X1X01 1XXXXXXXX	12.64 us	12.72 us 11X01X11X01X X 005C X 005D X 11E5 X 1175 7800 X 6003 X 45A0 X 0000 X 100 X 110 13.6 us 13.6 us	12,8 us 11,V01X11X01X11 X 005E X 005E X 14EF X C059 X X X 4000 X 2000 X 0018 X 101 X 011 13,68 us 13,101 X 111X01	X 0001 X 6000 X 0001 X 6000 X 0001 X 6000 X 0007 X 000 X 111 13.76 us 111\(01\) 111\(01\) 10 9 \(009\) X 009 7 \(8569\) X	X 2000 X X 2000 X X 2000 X X 2000 X X 211 X 2000 X X 211 X 2000 X X 211 X 2000 X X 2000 X	X 0064 X 0066 X 0002 X 0002 X 0003 X 0000 0000 0000 0	14.0 us 1.001 × 11.0 us 1.1.0 us	X 003B X 008G X 0290 X 0C4E X 001E X 0001 X 45A0 X 0007 X 010 X 01	13.28 u 13.28 u 13.28 u 13.28 u 13.28 u 13.28 u 14.10 14.1
Name CLOCK_50 KEY SW LED CPUCCPU0 PC CPUCCPU0 T1 CPUCCPU0 T3 CPUCCPU0 T4 CPUCCPU0 T4 CPUCCPU0 T5 CPUCCPU0 T6 CPUCCPU0 T1 CPUCCPU0 T1	B due D D D D D D D D D	12.4 us \(11\times 11\times 12\times 12\t	12.48 us 1X01X11X01X 1 0056 X 0057 8568 X 01 0780 0780 X 0000 X 101 X 13.36 us (11X01X11X0 X 0090 X 00	(11X01X11X01X1 (X) (0058 X 0059 X 005	12.64 us 1.01 \ 1.101	12.72 us 11X01X11X01X X 005C X 005D X 11E5 X 1175 7800 X 0000 X 0000 X 100 X 110 13.6 us 13.7 us	12,8 us 11,V01X11X01X11 X 005E X 005E X 14EF X C059 X X X 4000 X 2000 X 0018 X 101 X 011 13,68 us 13,101 X 111X01	X 0001 X 6000 X 0001 X 6000 X 0001 X 6000 X 0007 X 000 X 111 13.76 us 111\(01\) 111\(01\) 10 9 \(009\) X 009 7 \(8569\) X	X 2000 X X 2000 X X 2000 X X 2000 X X 211 X 2000 X X 211 X 2000 X X 211 X 2000 X X 2000 X	X 0064 X 0066 X 0002 X 0002 X 0003 X 0000 0000 0000 0	14.0 us 1.001 × 11.0 us 1.1.0 us	X 003B X 008G X 0290 X 0C4E X 001E X 0001 X 45A0 X 0007 X 010 X 01	13.28 u 13.28 u 13.28 u 13.28 u 13.28 u 13.28 u 14.10 14.10 14.10 14.10 14.11 14.11 14.11 14.10 14.1
Name CLOCK_50 KEY SW LED CRUCCHUGIPC C	B due Jp BO B H H H GH H H H H H H H H H H H H H	12.4 us \(11\times 11\times 12\times 12\t	12.48 us 1\(01\)\(11\)\(01\)\(11\)\(0056\) \(0056	(11X01X11X01X1 (X) (0058 X 0059 X 005	12.64 us 1.01 \ 1.101	12.72 us 11X01X11X01X X 005C X 005D X 11E5 X 1175 7800 X 6003 X 45A0 X 0000 X 100 X 110 13.6 us 13.6 us	12,8 us 11,V01X11X01X11 X 005E X 005E X 14EF X C059 X X X 4000 X 2000 X 0018 X 101 X 011 13,68 us 13,101 X 111X01	X 0001 X 6000 X 0001 X 6000 X 0001 X 6000 X 0007 X 000 X 111 13.76 us 111\(01\) 111\(01\) 10 9 \(009\) X 009 7 \(8569\) X	X 2000 X X 2000 X X 2000 X X 2000 X X 211 X 2000 X X 211 X 2000 X X 211 X 2000 X X 2000 X	X 0064 X 0066 X 0002 X 0002 X 0003 X 0000 0000 0000 0	14.0 us 1.001 × 11.0 us 1.1.0 us	X 003B X 008G X 0290 X 0C4E X 001E X 0001 X 45A0 X 0007 X 010 X 01	13.28 u 13.28 u 13.28 u 13.28 u 13.28 u 13.28 u 14.10 14.1
> cpurcpu0 AA Name	B due DP BO B H H H H JP B due H	12.4 us \(11\times 11\times 12\times 12\t	12.48 us 1\(01\)\(11\)\(01\)\(11\)\(0056\)\(0056\)\(0057\)\(8568\)\(011\) 0780\\ 0780\\ \(0780\)\(101\)\(11\)\(0000\)\(101\)\(11\)\(0000\)	(11X01X11X01X1 (X) (0058 X 0059 X 005	12.64 us 1.01 \ 1.101	12.72 us 11X01X11X01X X 005C X 005D X 11E5 X 1175 7800 X 6003 X 45A0 X 0000 X 100 X 110 13.6 us 13.6 us	12,8 us 11,V01X11X01X11 X 005E X 005E X 14EF X C059 X X X 4000 X 2000 X 0018 X 101 X 011 13,68 us 13,101 X 111X01	X 0001 X 6000 X 0007 X 0007 X 0007 X 0007 X 0007 X 0007 X 111 X 01 X 11 X 01 X 0	X 2000 X X 2000 X X 2000 X X 2000 X X 211 X 2000 X X 211 X 2000 X X 211 X 2000 X X 2000 X	0000 0000 0001 0000 0018 000 13.92 us 17.17(01)(11)(01) 000 0018 000 0018	14.0 us 11.001 × 11.	X 003B X 008G X 0290 X 0C4E X 001E X 0001 X 45A0 X 0007 X 010 X 01	13.28 u 13.28 u 13.28 u 13.28 u 13.28 u 13.28 u 14.10 1 14.10 1 14.10 1 14.10 1 14.10 1 14.10 1 14.10 1 14.10 1 14.10 1 15.10 1 16.
> cpurcpu0 AA Name	B	12.4 us \[\(\)	12.48 us 1\(01\)\(11\)\(01\)\(11\)\(0056\)\(0056\)\(0057\)\(8568\)\(011\) 0780\\ 0780\\ \(0780\)\(101\)\(11\)\(0000\)\(101\)\(11\)\(0000\)	(11X01X11X01X1 (X) (0058 X 0059 X 005	12.64 us \(\text{1.01} \text{1.1} \text{0.01} \text{1.1} \text{0.01} \text{2.1} \\ \(\text{0.05A} \text{ \text{0.05B}} \) \(\text{3.000} \text{ \text{2.05B}} \) \(\text{3.000} \text{ \text{2.05B}} \) \(\text{3.000} \text{3.001B} \) \(\text{3.001} \text{3.001} \text{3.001} \text{3.000} \text{3.000} \) \(\text{3.000} \tex	12.72 us 11.X01X11X01X X 005C X 005D X 11E5 X 1175 7800 X 60D3 X 45A0 X 0000 X 100 X 110 13.6 us 13.6 us 13.6 us 2.110 X 02 X 0018	12,8 us 11,V01X11X01X11 X 005E X 005E X 14EF X C059 X X X 4000 X 2000 X 0018 X 101 X 011 13,68 us 13,101 X 111X01	X 0001 X 6000 X 0007 X 0007 X 0007 X 0007 X 0007 X 0007 X 111 X 01 X 11 X 01 X 0	X 2000 X X 2011 X 13.84 us 13.84 us 13.85 us 14.85 us 15.85 us 16.85 us 17.85 us	0000 0000 0001 0000 0018 000 13.92 us 17.17(01)(11)(01) 000 0018 000 0018	14.0 us 11.001 × 11.	X 008B X 008G X 0290 X 0C48 X 0290 X 0C48 X 001E X 0001 X 45A0 X 0007 X 010 X	13.28 u 13.28 u 13.28 u 13.28 u 13.28 u 13.28 u 14.10 1 14.10 1 14.10 1 14.10 1 14.10 1 14.10 1 14.10 1 14.10 1 14.10 1 15.10 1 16.
Name	B	12.4 us \[\(\sqrt{11\times 01\times 1} \) \[\(\sqrt{01\times 11\times 01\times 1} \) \[\(\sqrt{0054\times 0055\times 5} \) \[\(\sqrt{0056\times 0065\times 0066\times 1} \) \[\(\sqrt{0066\times 0066\times 0066\times 1} \) \[\(\sqrt{0066\times 0066\times 0066\times 0066\times 1} \) \[\(0066\times 0066	12.48 us 1X01X11X01X 1 0056 X 0057 8568 X 01 0780 0780 X 0000 X 101 X 11X01X11X0 EX 0090 X 00 X 0002	(11X01X11X01X1 2X 0058 X 0059 X 1D45 1D45 X 0F00 X 1E00 X	12.64 us	12.72 us 11X01X11X01X X 005C X 005D X 11E5 X 1175 7800 X 0000 X 100 X 110 13,6 us 13,6 us 13,6 us 13,6 us X 11X01X11X0 X 0018 X 0018	12,8 us 11,01,11,01,11 X 005E X 005E X 14EF X C059 X X 0018 X 101 X 011 13,68 us 1,111,01,11,101 13,70 0098 X 009 90 X 2190 X 994	X 0001 X 6000 X 0001 X 6000 X 0007 X 000 X 0000 X 000 X 0007 X 000 X 0000 X 000	X 2000 X X 2000 X X 2000 X X 2011 X X 2000 X X 2010 X 2000 X	X 0064 X 0066 X 0002 X 0003 X 0000 X 0000 X 0000 X 13.92 us X 111 X 01 X 11 X 01	14.0 us 11.001 × 11.001 × 11.0 us 12.0040 × 00040 ×	X 008B X 008G X 0290 X 0290 X 0C48 X 001E X 0001 X 45A0 X 0007 X 45A0 X 0007 X 14.08 us 14.08 us 11.00A2 X 00 1D.45	13.28 u 14.10 14.10 14.10 14.10 14.11 14.11 14.11 14.11 14.10 14.10 14.10 14.10 14.10 15.11 16.11 17.11
> cpurcpu0 AA Name	B due) B B H G. H	12.4 us \[\(\)	12.48 us 1 \(\)	11X01X11X01X1 2X 0058 X 0059 X 1045 1045 X 0F00 X 1E00 X 1007 0007 0007 000 X 13.44 us 11X11X01X11X01 11X11X01X11X01 11X11X01X11X01 11X11X01X11X01 11X1X01X11X01 11X1X01X11 1XX1X01X11X01 1XXXXXXXX	12.64 us 1 \(\)	12.72 us 11X01X11X01X X 005C X 005D X 11E5 X 1175 7800 X 6003 X 45A0 X 0000 X 100 X 110 13.6 us 13.6 us 13.6 us 25 X 0096 X 00 28 X 2110 X 02 X 0018 4 0000 X 0018	12,8 us 11X01X11X01X1 X 005E X 005E X 14EF X C059 X X 4000 X 2000 X 0018 X 101 X 011 13,68 us 1X11X01X11X01 97 X 0098 X 009 90 X 2190 X 994 X X X X X X X X X X X X X X X X X X X	X	X 2000 X X 2000 X X 2000 X X 211 X 2000 X X 211 X 2000 X X 211 X 2000 X X 2	00000000000000000000000000000000000000	14.0 us 14.0 us 14.0 us EX.00A0 X.00A 8 X.	X 008B X 008G X 0290 X 0C48 X 0290 X 0C48 X 001E X 0001 X 45A0 X 0007 X 010 X	13.28 u 14.10 14.10 14.10 14.10 14.10 14.10 14.10 14.10 15.10 16.10
> cpurcpu0 AA Name CLOCK_50 > KEY > SW > LED > cpurcpu0 PC > cpurcpu0 R > cpurcpu0 r1 > cpurcpu0 r2 > cpurcpu0 r3 > cpurcpu0 r4 > cpurcpu0 r5 > cpurcpu0 r6 > cpurcpu0 r3 > cpurcpu0 r3 > cpurcpu0 r4 > cpurcpu0 r5 > cpurcpu0 r5 > cpurcpu0 A	B	12.4 us \(\sqrt{01\times11\times01\times1}\) \(\sqrt{01\times11\times01\times1}\) \(\sqrt{00054\times055\times5}\) \(\sqrt{0005}\) \(\sqrt{0000}\) \(\sqrt{0000}\) \(\sqrt{0000}\) \(\sqrt{0000}\) \(\sqrt{0000}\) \(\sqrt{0000}\) \(\sqrt{0000}\) \(\sqrt{0000}\)	12.48 us 1\(01\)\(11\)\(01\)\(11\)\(0056\) \(0056	(11X01X11X01X1 2X 0058 X 0059 X 1D45 1D45 X 0F00 X 1E00 X	12.64 us 1.01 × 11 × 01 × 11 × 01 × 11 × 01 × 11 × 01 × 11 × 01 ×	12.72 us 11X01X11X01X X 005C X 005D X 11E5 X 1175 7800 X 60D3 X 45A0 X 0000 X 100 X 110 13.6 us 13.6 us 13.6 us 25 X 0096 X 00 88 X 2110 X 02 X 0018 X 0018 X 4AEC	12,8 us 11,01,11,01,11 X 005E X 005F X 14EF X C059 X X 0018 X 101 X 011 13,68 us 17,11,01,11,101 13,68 us 27,0098,009 90,0098,009 90,0098,009 10,0098,009 10,0098,009 10,0098,009 10,0098,009 10,0098,009 10,0098,009 10,0098,009 10,0098,009 10,0098,009 10,0098,009 10,0098,009 10,0098,009 10,0098,009 10,0098,009	X 0001 X 0000 X 00007 X 00007 X 00007 X 0000 X 00007 X 8 X 00000 X 00000 X 00000 X 00007 X 00000 X 000000	X 2000 X X 2000 X X 2000 X X 2011 X X 2000 X X 2010 X 2000 X	X 0064 X 0066 X 0002 X 0003 X 0000 X 0000 X 0000 X 13.92 us X 111 X 01 X 11 X 01	14.0 us 1.001 × 11 × 01 × 01 × 01 × 01 × 01 × 01	X 008B X 008G X 0290 X 0290 X 0C48 X 001E X 0001 X 45A0 X 0007 X 45A0 X 0007 X 14.08 us 14.08 us 11.00A2 X 00 1D.45	13.28 u 14.10 14.10 14.10 14.10 14.11 14.11 14.11 14.11 14.10 14.10 14.10 14.10 14.10 15.11 16.11 17.11

	News	ılue	14.16 us	14.24 us	14.32 us	14.4 us	14.48 us	14.56 us	14.64 us	14.72 us	14.8 us	14.88 us	14.96 us	15.04 us 🗷
	Name	Эp												
in_	CLOCK_50 KEY	B 0						X11X01X11X01X						
	> SW	В												
	> LED	н			VV				,					
	> cpu:cpu0 PC		X 00A4 X 00A5 X 8568 X	X 00A6 X 00A7 1D45				D X 00AE X 00AF 5 X 14EF X C058			X 00BB X 00B	8C X 00BD X 00B X 856F X 856		0 X 00C1 X 0 1D45
	> cpu:cpu0 IR		A 8368 A	1043		N TIES N IBCZ	A 11/3 A 164	3 A 14EF A C038	X 9801 X 9947	^	043		9 ^	1043
	> cpu:cpu0 r0 > cpu:cpu0 r1								00	006				
	> cpu:cpu0 r2									0019				
	> cpu:cpu0 r3						0000							
	> cpu:cpu0 r4		X 0800	X 1000 X 2000	X 4000 X	8000	X	0000		X 0007 X 000E	X 001C X 003	88 X 0070 X 007	7 X 0078 X 00F	0 X 01E0 X 0
	> cpu:cpu0 r5												1DA0	
	cpu:cpu0 r6 cpu:cpu0 r7		X 0800 X	0000	V 0000	X 1456 X 0000	V 1040 V	0000		0001		0000	-	0001
		н	0018	0000	8000	X 4AEC X 0000 X 0000 X 0018		0000		0001		X 0070 X 007 X 0000		0001
	> cpu:cpu0 d		X 101 X	000	X 101	X 100 X 000	X 110 X 00	O X 101 X 011	X	000		X 101		000
*	> cpu:cpu0 AA	В												
			15.Q4 us	15.12 us	15.2 us	15.28 us	15.36 us	15.44 us	15.52 us	15.6 us	15.68 us	15.76 us	15.84 us	15.92 u ^
	Name	ılue O p		15. 12 us	13.2 us	13.46 us	13.30 us	13. 44 us	13.32 us	13.p us	13.00 us	15.70 us	15.q4 us	13.92 u ^
in	CLOCK 50	ВО												
=	> KEY	В	X11X01X11X01	X11X01X11X01	X11X01X11X01	1X11X01X11X01	X11X01X11X0)1X11X01X11X01		<u> </u>	X11X01X11X0	01X11X01X11X0)1X11X01X11X0	1X11X01X11
	> SW	В		01					0000					
	> LED > cpu:cpu0 PC	Н) X 00C1 X 00C		4 X 00C5 X 000	C6 X 00C7 X 00C	8 X 00C9 X 00	OCA X 00CB X 00C	C X 00CD X 00CI	X 00CF X 00E	00 X 00D1 X 00	DD3 X 00D6 X 00)F4 X 00F8 X 00	F9 X OOFA X
	> cpu:cpu0 FC		1D45	X 8568 X	1D45	X 856	8 X 11E5 X 11	75 X 14EF X C05	9 X 9800 X 0AFI	X C21B X 050	04 X C002 X C0	003 X C0C6 X C0	004 X 0290 X 0C	48 X C00A X
	> cpu:cpu0 r0			0001					 					
	> cpu:cpu0 r1												<u> </u>	
	> cpu:cpu0 r2 > cpu:cpu0 r3								5000	X				
	> cpu:cpu0 r3) X 01E0 X 03C	0 X 0780	V 0500 V 450	2000	7000	4AEC					1000	
	> cpu:cpu0 r5		J X 01E0 X 03C	0 A 0/80	X 0F00 X 1E0	00 × 3C00 ×	7800						1800	
	> cpu:cpu0 r6						X							
*	> cpu:cpu0 r7 > cpu:cpu0 A	Н	0001	X 0780 X	0001			0A0 X 1800 X 500		X 3000 X		000	X 0019 X 00	
	> cpu:cpu0 A			X 0000 X X 101 X	0007	X 001		0018 10 × 101 × 01	X 0007 X	Y 011 Y	0018	00	X 1DA0 X X 010 X	0000 X 001 X
	> cpu:cpu0 AA				000									
		1	15.92 us	16.0 us	16.Q8 us	16.16 us	16 34 116	46.00		16.49 με	16.56 us	46.64		
		ilue	Total do	10.p us	10.00 03	10. ţ0 us	16.24 us	16.32 us	16.4 us	16.48 us	10.30 us	16.64 us	16.72 us	16.8 us ^
	Name) p												
in_	CLOCK_50) p B 0												
	CLOCK_50 > KEY) р В 0 В												
>	CLOCK_50) p B 0	1X01X11X01X1	1X01X11X01X	11X01X11X01X	11X01X11X01X1	1X01X11X01	(11X01X11X01X1	1X01X11X01X1	1X01X11X01X1	11X01X11X01	(11X01X11X01X		 11X01X11Xi
* :	CLOCK_50 > KEY > SW > LED > cpu:cpu0 PC	Эр Во В В Н	1X01X11X01X1 (00FA X 00FB)	1X01X11X01X	11X01X11X01X X 00D4 X 00B6	11X01X11X01X1 X 0098 X 0099	1X01X11X01 X 009A X 009B	(11X01X11X01X1 3 X 009C X 009D)	1X01X11X01X1 009E X 009F	1X01X11X01X1	11X01X11X01) X 00A2 X 00A3	(11X01X11X01X 3 X 00A4 X 00A5	11X01X11X01X 3 X 00A6 X 00A7	 11X01X11Xi
	CLOCK_50 > KEY > SW > LED > cpu:cpu0 PC > cpu:cpu0 IR	Эр Во В Н Н	1X01X11X01X1 (00FA X 00FB)	1X01X11X01X	11X01X11X01X X 00D4 X 00B6	11X01X11X01X1	1X01X11X01 X 009A X 009B	(11X01X11X01X1	1X01X11X01X1	1X01X11X01X1	11X01X11X01	(11X01X11X01X		 11X01X11Xi
	CLOCK_50 > KEY > SW > LED > cpu:cpu0 PC > cpu:cpu0 IR > cpu:cpu0 r0	Эр В В Н Н	1X01X11X01X1 (00FA X 00FB)	1X01X11X01X	11X01X11X01X X 00D4 X 00B6	11X01X11X01X1 X 0098 X 0099	1X01X11X01 X 009A X 009B	(11X01X11X01X1 3 X 009C X 009D)	1X01X11X01X1 009E X 009F	1X01X11X01X1	11X01X11X01) X 00A2 X 00A3	(11X01X11X01X 3 X 00A4 X 00A5 X 8568 X	(11X01X11X01X 11X01X11X01X 1X 00A6 X 00A7 1D45	 11X01X11Xi
	CLOCK_50 > KEY > SW > LED > cpu:cpu0 PC > cpu:cpu0 IR	Эр Во В Н Н Н	1X01X11X01X1 (00FA X 00FB)	1X01X11X01X	11X01X11X01X X 00D4 X 00B6	11X01X11X01X1 X 0098 X 0099	1X01X11X01 X 009A X 009B	(11X01X11X01X1 3 X 009C X 009D 1D45	1X01X11X01X1 009E X 009F	1X01X11X01X1	11X01X11X01) X 00A2 X 00A3	(11X01X11X01X 3 X 00A4 X 00A5 X 8568 X	(11X01X11X01X 11X01X11X01X 1X 00A6 X 00A7 1D45	 11X01X11Xi
	CLOCK_50 KEY SW LED cpuccpu0 PC cpuccpu0 IR cpuccpu0 r1 cpuccpu0 r2 cpuccpu0 r3	Эр В В Н Н Н Н	1X01X11X01X1 (00FA X 00FB)	1X01X11X01X	11X01X11X01X X 00D4 X 00B6	11X01X11X01X1 X 0098 X 0099	1X01X11X01 X 009A X 009B	(11X01X11X01X1 3 X 009C X 009D)	1X01X11X01X1 009E X 009F	1X01X11X01X1	11X01X11X01) X 00A2 X 00A3	(11X01X11X01X 3 X 00A4 X 00A5 X 8568 X	(11X01X11X01X 11X01X11X01X 1X 00A6 X 00A7 1D45	 11X01X11Xi
	CLOCK_50 > KEY > SW > LED > cpuccpu0 PC > cpuccpu0 r1 > cpuccpu0 r1 > cpuccpu0 r2 > cpuccpu0 r3 > cpuccpu0 r3	Эр во в н н н н н	1X01X11X01X1 (00FA X 00FB)	1X01X11X01X	11X01X11X01X X 00D4 X 00B6	11X01X11X01X1 X 0098 X 0099	1X01X11X01 X009A X 009E X 8569 X	(11X01X11X01X1 3 X 009C X 009D 1D45	1\(\)01\(\)11\(\)01\(\)1 (\)009E\(\)\(009E\(\)	1X01X11X01X1 0000 X 0001 10	11X01X11X01) X 00A2 X 00A3	(11\(01\(11\(01\))) (11\(01\)(11\(01\)) (004\(004\)(004\)(005\) (005\(005\)(005\)	(11X01X11X01X 11X01X11X01X 1X 00A6 X 00A7 1D45	11X01X11Xi X 00A8 X 0i X 8:
	CLOCK_50 > KEY > SW > LED > cpuccpu0 PC > cpuccpu0 In > cpuccpu0 r1 > cpuccpu0 r2 > cpuccpu0 r3 > cpuccpu0 r4 > cpuccpu0 r4 > cpuccpu0 r5 > cpuccpu0 r6	Эр В Н Н Н Н Н Н Н	1X01X11X01X1 1X01X11X01X1 (00FA X 00FB X (C00A X C1C4)	1X01X11X01X	X 0004 X 0086 X C102	11X01X11X01X1 X 0098 X 0099 X 2190 X 9947	1X01X11X01 X009A X 009E X 8569 X	(11X01X11X01X1 8 X 009C X 009D X 1D45	1\(\)01\(\)11\(\)01\(\)1 (\)009E\(\)\(009E\(\)	1X01X11X01X1 0000 X 0001 10	11X01X11X01 00042 X 00043 0045	(11\01\11\01) 3\0004\0005	(11X01X11X01X X 00A6 X 00A7 1D45	11X01X11Xi X 00A8 X 0i X 8:
	CLOCK_50 > KEY > SW > LED > cpuccpu0 PC > cpuccpu0 r1 > cpuccpu0 r1 > cpuccpu0 r2 > cpucpu0 r3 > cpuccpu0 r4 > cpucpu0 r4 > cpucpu0 r5 > cpucpu0 r6	D P B O B B H H H H H H H H	1X01X11X01X1 (00FA X 00FB X 00FB X 000A X C1C4 X 000A X C1C4 X 000A X 0	1X01X11X01X	X 0004 X 0086 X C102	11X01X11X01X1 X 0098 X 0099 X 2190 X 9947	1X01X11X01 X009A X 009E X 8569 X	(11X01X11X01X1 8 X 009C X 009D X 1D45	1\(\)01\(\)11\(\)01\(\)1 (\)009E\(\)\(009E\(\)	00A0 X 00A1 1101X11X01X1	11X01X11X01 00042 X 00043 0045	(11\01\11\01) 3\0004\0005	(11X01X11X01X X 00A6 X 00A7 1D45	11X01X11Xi X 00A8 X 0i X 8:
	CLOCK_50 > KEY > SW > LED > cpu:cpu0 PC > cpu:cpu0 r0 > cpu:cpu0 r1 > cpu:cpu0 r2 > cpu:cpu0 r3 > cpu:cpu0 r4 > cpu:cpu0 r5 > cpu:cpu0 r5 > cpu:cpu0 r5 > cpu:cpu0 r5 > cpu:cpu0 r6 > cpu:cpu0 r7	Эр В В Н	1X01X11X01X1 (00FA X 00FB X 00FB X 000FA X 01C4 X	1X01X11X01X 1X01X11X01X (00F7 X 00D7 (C100 X C1C5	X 0004 X 0086 X C102	X 0098 X 0099 X 2190 X 9947 X 2190 X 9947 X 2190 X 9947 X 2190 X 0018 X	1X01X11X01X X 009A X 009E X 8569 X X 0007 X 000E X 0007 X X 0000 X	3X 009C X 009D 1D45 3000 3X 0010 X 002D 0000 0018	1X01X11X01X1 (009E X 009F X 8568 X 8568 X 0040 X 009	00A0 X 00A1 1001X11X01X1 100A0 X 00A1 100A0 100A	X 0200 X 0400	(11\01\11\01\) 3\\0004\\0005\0005\\0005\\0005\\0005\\0005\\0005\\0005\\0005\\0005\\0005\\0005\\0005\\0005\\0005\\0005\\0005\\0005\\0005\000	(11X01X11X01X (11X01X1X01X (11X01X01X (11X01X01X (11X01X1X01X (11X01	11X01X11Xi X 00A8 X 0i X 8:
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	1	18.56 us 18.64 us	18.72 us	18.8 us	18.88 us	18.96 us	19.Q4 us	19.12 us	19.2 us	19.28 us	19.36 us	19.44 us
Name	ılue) p	10.30 43										15.44 05
CLOCK_50 KEY	B 0	X01X11X01X11X01X11X0			11X01X11X01X1						11X01X11X01X	11X01X11X0
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> cpu:cpu0 IR	н	1B45 X 14EF X C058 X OAI	FD X C21B X 0504	X C002 X C0C6	X C003 X C0C6 X	C004 X 0290 X	0C48 X C00	A X C1C4 X C100	X C1C5 X	C102 X 2190	X 9947 X 8569	
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Name	ilue	19.44 us 19.52 us	19.6 us	19.68 us	19.76 us	10.04	40.03		20.00	20.16 us	20.24	20.32 us ^
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> KEY > SW > LED	B 0 B B H		1)(11)(01)(11)(01)	\\\\(11\X\)\(11\X\X\)\(11\X\X\)\(11\X\)\(11\X\X\)\(11\X\X\)\(11\X\X\X\X\X\X\X\X\X\X	11X01X11X01X1	1X01X11X01X1	1X01X11X01	X11X01X11X01	(11)(01)(11)(01)	X11X01X11X01X	11X01X11X01X	11X01X11XC
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 ⇒ > KEY ⇒ > SW ⇒ > LED ⇒ > cpuxcpu0]PC ⇒ > cpuxcpu0]IR ⇒ > cpuxcpu0]r1 ⇒ > cpuxcpu0]r2 ⇒ > cpuxcpu0]r3 ⇒ > cpuxcpu0]r3 ⇒ > cpuxcpu0]r4 	B 0 B B H H H H H H	1X01X11X01X11X01X11X0 009B X 009C X 009D X 00 1D45 00 00 000	1X11X01X11X01 9E X 009F X 00AG X 8568 X 40 X 0080	X11X01X11X01X D X 00A1 X 00A2 1D45 X 0100 X 0200	(11X01X11X01X1 X 00A3 X 00A4 X 8568) 12X 0400 X 08	1\(\sigma \) \(\sigma \) \(\si	1X01X11X01 00A7 X 00A 45 2000 X 400	X11X01X11X01 8 X 00A9 X 00A6 X 8568 X 11E5	(11X01X11X01 (X 00AB X 00AB X 1BC7 X 117! 8000 X 8000 X	X11X01X11X01X X 00AD X 00AE X X 1845 X 14EE	X 00AF X 00B7 X C058 X 9801 0 001C X 4000	11X01X11X0 X X X X X X X X X X X X X X X X X X X
\$\begin{array}{c}\$ > KEY\$ \$\begin{array}{c}\$ > SW\$ \$\end{array}\$ > Cpuccpu0]rG\$ \$\begin{array}{c}\$ > cpuccpu0]rG\$ \$\begin{array}{c}\$ > cpuccpu0]r3\$ \$\begin{array}{c}\$ > cpuccpu0]r3\$ \$\begin{array}{c}\$ > cpuccpu0]r3\$ \$\begin{array}{c}\$ > cpuccpu0]r5\$ \$\begin{array}{c}\$ > cpuccpu0]r5\$ \$\begin{array}{c}\$ > cpuccpu0]r3\$ \$\begin{array}{c}\$ > cpuccpu0]r3\$ \$\begin{array}{c}\$ > cpuccpu0]r3\$ \$\begin{array}{c}\$ > cpuccpu0]r4\$ \$\begin{array}{c}\$ > cpuccpu0]r3\$ \$\begin{array}{c}\$ > cpuccpu0]r4\$ \$\begin{array}{c}\$ > cpuccpu0]r5\$ \$\begin{array}{c}\$ > cpuccpu0]r5\$ \$\begin{array}{c}\$ > cpuccpu0]r5\$ \$\begin{array}{c}\$ > cpuccpu0]r4\$ \$\begin{array}{c}\$ > cpuccpu0]r5\$ \$\begin{array}{c}\$ > cpuccpu0]r4\$ \$\begin{array}{c}\$ > cpuccpu0]r4\$ \$\begin{array}{c}\$ > cpuccpu0]r5\$ \$\begin{array}{c}\$ > cpuccp	BO B B H H H H H H	1X01X11X01X11X01X11X0 C009B X 009C X 009D X 00 1D45 00 C000B X 0010 X 0020 X 00 C000B X 0010 X 0020 X 00 C000B X 0010 X 0020 X 00	9E X 009F X 00AG	(11\01\11\01\) (11\01\11\01\) (11\01\11\01\) (10\01\01\01\01\01\01\01\01\01\01\01\01\0	(11X01X11X01X1 X 000A3 X 000A4 X 8568) 1 X 0400 X 08 X 0800) 00	1X01X11X01X1 (00A5 X 00A6 X (1D 00 X 1000 X (000	00A7 X 00A 45 2000 X 400	X11X01X11X01X 8 X 00049 X 00044 X 8568 X 11E5 0 X X 8000 X A75E	(11\x\01\x\11\x\01\x\11\x\01\x\11\x\01\x\11\x\01\x\11\x\01\x\11\x\01\x\11\x\01\x\11\x\01\x\11\x\01\x\	X11X01X11X01X X 00AD X 00AE 5 X 1845 X 14EF X 5 X 0000 X 4000 5 X 0000 X 0000	X 0000 0010 X 0000 0010 X 0000 0010	11X01X11X0 X X X X X X X X X X X X X X X X X X X
\$\begin{array}{c}\$ > KEY\$ \$\begin{array}{c}\$ > SW\$ \$\end{array}\$ > Cpuccpu0]rG\$ \$\begin{array}{c}\$ > cpuccpu0]rG\$ \$\begin{array}{c}\$ > cpuccpu0]r3\$ \$\begin{array}{c}\$ > cpuccpu0]r3\$ \$\begin{array}{c}\$ > cpuccpu0]r3\$ \$\begin{array}{c}\$ > cpuccpu0]r5\$ \$\begin{array}{c}\$ > cpuccpu0]r5\$ \$\begin{array}{c}\$ > cpuccpu0]r3\$ \$\begin{array}{c}\$ > cpuccpu0]r3\$ \$\begin{array}{c}\$ > cpuccpu0]r3\$ \$\begin{array}{c}\$ > cpuccpu0]r4\$ \$\begin{array}{c}\$ > cpuccpu0]r3\$ \$\begin{array}{c}\$ > cpuccpu0]r4\$ \$\begin{array}{c}\$ > cpuccpu0]r5\$ \$\begin{array}{c}\$ > cpuccpu0]r5\$ \$\begin{array}{c}\$ > cpuccpu0]r5\$ \$\begin{array}{c}\$ > cpuccpu0]r4\$ \$\begin{array}{c}\$ > cpuccpu0]r5\$ \$\begin{array}{c}\$ > cpuccpu0]r4\$ \$\begin{array}{c}\$ > cpuccpu0]r4\$ \$\begin{array}{c}\$ > cpuccpu0]r5\$ \$\begin{array}{c}\$ > cpuccp	BO B B H H H H H H.	1X01X11X01X11X01X11X0 C009B X 009C X 009D X 00 1D45 00 C000B X 0010 X 0020 X 00 C000B X 0010 X 0020 X 00	9E X 009F X 00AG X 8568 X 40 X 0080	X11X01X11X01X D X 00A1 X 00A2 1D45 X 0100 X 0200	(11X01X11X01X1 (X 00A3 X 00A4)	1\(\)01\(\)11\(\)01\(\)11\(\)01\(\)11\(\)01\(\)11\(\)01\(\)11\(\)0	00A7 X 00A 45 2000 X 400	X11X01X11X01X 8 X 00049 X 00044 X 8568 X 11E5 0 X X 8000 X A75E	(11\x\01\x\11\x\01\x\11\x\01\x\11\x\01\x\11\x\01\x\11\x\01\x\11\x\01\x\11\x\01\x\11\x\01\x\11\x\01\x\	X11X01X11X01X X 00AD X 00AE 5 X 1845 X 14EF X 5 X 0000 X 4000	X 0000 0010 X 0000 0010 X 0000 0010	11X01X11X0 X X X X X X X X X X X X X X X X X X X
	BO B B H H H H H H.	1\(01\)\(11\)\(01\)\(11\)\(01\)\(11\)\(00\)\(11\)\(00\)\	9E X 009F X 00AG	(11\01\11\01\) (11\01\11\01\) (11\01\11\01\) (10\01\01\01\01\01\01\01\01\01\01\01\01\0	(11X01X11X01X1 X 000A3 X 000A4 X 8568) 1 X 0400 X 08 X 0800) 00	1X01X11X01X1 (00A5 X 00A6 X (1D 00 X 1000 X (000	00A7 X 00A 45 2000 X 400	X11X01X11X01X 8 X 00049 X 00044 X 8568 X 11E5 0 X X 8000 X A75E	(11\x\01\x\11\x\01\x\11\x\01\x\11\x\01\x\11\x\01\x\11\x\01\x\11\x\01\x\11\x\01\x\11\x\01\x\11\x\01\x\	X11X01X11X01X X 00AD X 00AE 5 X 1845 X 14EF X 5 X 0000 X 4000 5 X 0000 X 0000	X 0000 0010 X 0000 0010 X 0000 0010	11X01X11X0 X X X X X X X X X X X X X X X X X X X
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	BO B B H H H H H B H H H H B Idue D p B O B	1\(01\)\(11\)\(01\)\(11\)\(00)\(11\)\(00)\(11\)\(00	9E X 009F X 00AG X 8568 X 40 X 0080 X 0080 X X 0080 X X 0000 X X 1011 X	X 0100 X 0200 20.56 us	(11\(\)\(01\(\)\(11\(\)\(01\(\)\(11\(\)\(01\(\)\(11\(\)\(01\(\	1001\(\)11\(\)01\(\)11\(\)01\(\)11\(\)01\(\)11\(\)01\(\)11\(\)01\(\)11\(\)00\(00A7 X 00A 45 2000 X 400 00.8 us	X11X01X11X01 8 X 00A9 X 00AA X 8568 X 11E5 0 X X 8000 X A75E X 0000 X 101 X 100 20.88 us	(11\x\01\x\11\x\01\x\11\x\01\x\11\x\01\x\11\x\01\x\11\x\01\x\11\x\01\x\11\x\01\x\11\x\01\x\11\x\01\x\11\x\01\x\11\x\01\x\11\x\01\x\	X11X01X11X01X X10X01X11X01X X X X X X X X X X X X X X X X X X X X	X 0000 X 0000 X 0000 X 0000 X 0000 X 0000 X 0000 D18 X 011 X	11X01X11XC X
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	ilue	21.2 us	21.28 us	21.36 us	21.44 u	s 21.52 u:	s 21.6 us	21.68 us	21.76 us	21.84 us	21.92 us	22.0 us	22.08 us
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> cpu:cpu0 AA Name CLOCK_50 > KEY > SW > LED > cpu:cpu0 PC > cpu:cpu0 r1 > cpu:cpu0 r2 > cpu:cpu0 r3 > cpu:cpu0 r4 > cpu:cpu0 r4 > cpu:cpu0 r5	B lue) p B0 B H H H H	22.96 us 11X01X11X01 X 00BC X 00B X 856	23.Q4 us \[\(\sum_{\text{\color}} \sum_{\text{\color}} \sum_{\text{\color}} \] \[\sum_{\text{\color}} \sum_{\text{\color}} \sum_{\text{\color}} \] \[\sum_{\text{\color}} \sum_{\text{\color}} \sum_{\text{\color}} \sum_{\text{\color}} \] \[\sum_{\text{\color}} \sum_{\text{\color}} \sum_{\text{\color}} \sum_{\text{\color}} \sum_{\text{\color}} \] \[\sum_{\text{\color}} \sum_{\	23.12 us X11X01X11X FX 00C0 X C 1045	23.2 (01X11X01X 000C1 X 00C2	us 23.28 11.7017.11.7017. 11.7017.11.7017. 01. X.0003.X.0004. X.8568.X.	3 us 23.36 u 111X01X11X01X11 11X01X11X01X11 11X01X11X01X11 11X01X11X01X11 11X01X11X01X11	23.44 u (X01X11X01X11 (X01X11X01X11 (X007 X 0008 X X 8568 X	s 23.52 us X01X11X01X11X 0009 X 000A X 0 11E5 X 1175 X 1	23,6 us 01\11\01\11\01\11\00 01\11\00\00\00\00\00\00\00\00\00\00\00\0)1X11X01X11) X CDX 00CEX (23.76 us	01X11X01X11 0D3 X 00D6 X
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> cpuxcpu0 AA Name CLOCK_50 > KEY > SW > LED > cpuxcpu0 r0 > cpuxcpu0 r1 > cpuxcpu0 r2 > cpuxcpu0 r3 > cpuxcpu0 r5 > cpuxcpu0 r5 > cpuxcpu0 r6	B lue) p B0 B H H H H H H	22.96 us 111X01X11X01 X 008C X 008 X 836 X 0038 X 007	23.04 us \[\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	23.12 us X11X01X11X FX 00C0 X C 1045 0000 8 X 00F0 X C	23,2 (01X11X01X 00C1 X 00C2 0001 X 00C2	us 23.28 11.V01V.11V.01V 11.V01V.11V.01V 10.1 10.1	3 us 23.36 u 111X01X11X01X11 X 00C5 X 00C6 X 1D45 X 0F00 X 1E00 X	23.44 u 1.X01X11X01X11 0007 X 0008 X X 8568 X 3000 X X 7800 X X 0018 X	\$ 23.52 us \[\sum_ \sum_ \sum \] \[\sum_ \sum_ \sum_ \sum \] \[\sum_ \sum_ \sum_ \sum_ \sum \] \[\sum_	23.6 us 01X11X01X11X0 00CB X 00CC X 00 44EF X C059 X 98 X 70 5000 X 7000 X 00	P1X11X01X11 X CD X 00CE X (100 X 0AFD X (X X X X X X X X X X X X X X X X X X X	23.76 us LTLTLTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTT	01X11X01X11 0D3 X 00D6 X 0003 X 00C6 X
> cpuxcpu0 AA Name CLOCK_50 > KEY > SW > LED > cpuxcpu0 r0 > cpuxcpu0 r1 > cpuxcpu0 r2 > cpuxcpu0 r3 > cpuxcpu0 r5 > cpuxcpu0 r5 > cpuxcpu0 r6	B lue) p B0 B H H H H H H	22.96 us 111X01X11X01 X 008C X 008 X 836 X 0038 X 007	23,Q4 us 23,Q4 us 21,1\(\sigma\)1\(\sigma\)1\(\sigma\)1\(\sigma\)1 20,\(\sigma\)008E \(\sigma\)008E \(\sigma\) 20,\(\sigma\)077 \(\sigma\)000 20,\(\sigma\)077 \(\sigma\)0000 X	23.12 us X11X01X11X FX 00C0 X C 1D45 0000 8 X 00F0 X C	23,2 (01X11X01X 00C1 X 00C2 0001 X 00C2	us 23.26 11.X01X11X01X 01 X 0003 X 0004 X 8568 X 001 X 0780 X 0780 X X 0000 X	3 us 23.36 u 11 \(\) \	23.44 u 1.X01X11X01X11 0007 X 0008 X X 8568 X 3000 X X 7800 X X 0018 X	\$ 23.52 us \[\sum_ \sum_ \sum \] \[\sum_ \sum_ \sum_ \sum \] \[\sum_ \sum_ \sum_ \sum_ \sum \] \[\sum_	23.6 us 01\11\01\11\00 01\11\01\11\00 00CB \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	P1X11X01X11 X CD X 00CE X (100 X 0AFD X (X X X X X X X X X X X X X X X X X X X	23.76 us LTLTLTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTT	01X11X01X11 0D3 X 00D6 X 003 X 00C6 X
> cpuxcpu0 AA Name CLOCK_50 > KEY > SW > LED > cpuxcpu0 r0 > cpuxcpu0 r1 > cpuxcpu0 r2 > cpuxcpu0 r3 > cpuxcpu0 r5 > cpuxcpu0 r5 > cpuxcpu0 r6	B lue) p B0 B H H H H H H	22.96 us 11.X01X11X01 X 00BC X 00B X 856 X 0038 X 007 X 007	23.04 us X11X01X11X01 X11X01X11X01 D X 00BE X 00B F X 8569 X 0 X 0077 X 007 D6E8 4000 0 X 0077 X 0000 X 101 X	23.12 us X11X01X11X EX 00C0 X C 1045 0000 8 X 00F0 X C 0001 0007 0000	23,2 (01X11X01X 300C1 X 00C2 300C1 X 00C2 300C1 X 00C2	us 23.28 111/01/11/01/01/01 01 0003 X 0004 X 8568 X 0001 X 0780 X 0780 X 0000 X 101 X	3 us 23.36 u 11X01X11X01X11 X 00C5 X 00C6 X 1D45 X 0F00 X 1F00 X 0001 0007 000	23.44 u 1001X11X01X11 0007 X 0008 X X 8568 X 3000 X X 7800 X X 0018 X X 101 X	s 23.52 us \[\begin{align*} \text{C1.11} \\	23.6 us	D1X11X01X11) CD X 00CE X (100 X 0AFD X 1) 100 X 101 X 2000 X 1 107 X 2000 X 1 107 X 2000 X 1 108 X 111	23.76 us (01X11X01X11X 00CF X 00D2 X 0 00CF X 00D2 X 0 0000 X 0011	01X11X01X11 0D3 X 00D6 X 0003 X 00C6 X 0000
> cpu:cpu0 AA Name CLOCK_50 > KEY > SW > LED > cpu:cpu0 PC > cpu:cpu0 r1 > cpu:cpu0 r2 > cpu:cpu0 r3 > cpu:cpu0 r4 > cpu:cpu0 r4 > cpu:cpu0 r5	B lue J p B 0 B H H H H H H H H I H H I I I I I I I I I I I I I I I I I I	22.96 us 111X01X11X01 X 008C X 008 X 836 X 0038 X 007	23,Q4 us 23,Q4 us 21,1\(\sigma\)1\(\sigma\)1\(\sigma\)1\(\sigma\)1 20,\(\sigma\)008E \(\sigma\)008E \(\sigma\) 20,\(\sigma\)077 \(\sigma\)000 20,\(\sigma\)077 \(\sigma\)0000 X	23.12 us X11X01X11X FX 00C0 X C 1D45 0000 8 X 00F0 X C	23,2 (01X11X01X 00C1 X 00C2 0001 X 00C2	us 23.28 111/01/11/01/01/01 01 0003 X 0004 X 8568 X 0001 X 0780 X 0780 X 0000 X 101 X	3 us 23.36 u 11X01X11X01X11 X 00C5 X 00C6 X 1D45 X 0F00 X 1F00 X 0001 0007 000	23.44 u 1001X11X01X11 0007 X 0008 X X 8568 X 3000 X X 7800 X X 0018 X X 101 X	s 23.52 us \[\begin{align*} \text{C1.11} \\	23.6 us 01\11\01\11\00 01\11\01\11\00 00CB \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	P1X11X01X11 X CD X 00CE X (100 X 0AFD X (X X X X X X X X X X X X X X X X X X X	23.76 us LTLTLTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTT	01X11X01X11 0D3 X 00D6 X 0003 X 00C6 X 0000
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> cpurcpu0 AA Name CLOCK_50 > KEY > SW > LED > cpurcpu0 PC > cpurcpu0 r0 > cpurcpu0 r1 > cpurcpu0 r3 > cpurcpu0 r3 > cpurcpu0 r4 > cpurcpu0 r3 > cpurcpu0 r4 > cpurcpu0 r3 > cpurcpu0 r4 > cpurcpu0 r5 > cpurcpu0 r6 > cpurcpu0 r7 > cpurcpu0 AA Name CLOCK_50	B lue J p B 0 B H H H H H H H H I H H I I I I I I I I I I I I I I I I I I	22.96 us 11.X01X11X01 X 00BC X 00B X 856 X 856 X 0038 X 007 X 007 X 007	23.94 us 23.94 us 23.94 us 23.92 us 23.92 us	23.12 us X11X01X11X EX 00C0 X C 1D45 0000 8 X 00F0 X C 0001 0007 0000 24,0 us	23,2 (01X11X01X 00C1 X 00C2 00C1 X 00C2 000C1 X 00C2	us 23.28 111X01X11X01X 111X01X11X01X 101 X 00003 X 00004 X 8568 X 1001 X 0780 X 0780 X 0780 X 0780 X 101 X	3 us 23.36 u 111\(\times 01\)\(\times 11\)\(\times 01\)\(\times 11\)\(\times 01\)\(\times 11\)\(\times 0005\)\(\times 0005\)\(\times 0005\)\(\times 0001\)\(\times 0007\)\(\times 0000\) us 24.24 us	23.44 u 1X01X11X01X11 00C7 X 00C8 X X 8568 X 3C00 X X 7800 X X 0018 X X 101 X	\$ 23.52 us \[\sum_{\text{\ti}\text{\texi{\text{\texi{\text{\texi{\text{\text{\text{\texi{\text{\texi{\text{\texi{\texi{\texi{\text{\texi{\texi{\texi{\texi{\texi{\texi{\texi\texi{\texi{\texi{\texi{\texi{\texi{\texi{\texi{\texi{\tirit}\texi{\texi{\texi	23.6 us (01\11\01\11\01\11\00 00CB \ 00CC \ 00 14EF \ \ C059 \ 98 \times 70 0000 \ \ 7000 \ 00 0018 \ 00 0011 \ 0111 \ 01 24.48 us	D1X11X01X11 CD X 00CE X (100 X 00ED X (100	23.76 us (01\11\01\11\01\11\01\11\01\11\01\11\01\11\01\0	0000 0000 0000
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> cpurcpu0 AA Name CLOCK_50 > KEY > SW > LED > cpurcpu0 FC > cpurcpu0 r0 > cpurcpu0 r1 > cpurcpu0 r3 > cpurcpu0 r3 > cpurcpu0 r4 > cpurcpu0 r4 > cpurcpu0 r5 > cpurcpu0 r6 > cpurcpu0 r6 > cpurcpu0 r7 > cpurcpu0 r6 > cpurcpu0 r6 > cpurcpu0 r6 > cpurcpu0 r7 > cpurcpu0 AA Name CLOCK_50 > KEY > SW > LED > cpurcpu0 RA	B Ilue D p B 0 B H H H H H H H B B 0 B 0 B B B H	22.96 us 111X01X11X01 X 00BC X 00B X 856 X 0038 X 007 X 007 X 007 23.84 us 1X01X11X01 C 0006 X 00F4	23.Q4 us \[\sum_1 \su	23.12 us X11X01X11X FX 00C0 X C 1D45 0000 8 X 00F0 X C 0001 0007 000 24.0 us	23,2 (01X11X01X) (01X11X01X) (01X11X01X) (01X11X01X) (01X11X01X1) (01X11X01X1) (01X11X01X1) (01X11X01X1) (01X11X01X1) (01X11X01X1)	us 23.28 111/01/11/01/01 01 001 0003 \ 0004 0001 0000 \ 00000 \ 00000 0000 \ 00000 \ 00000 0000 \ 00000 \ 00000 0000 \ 00000 \	3 us 23.36 u 11.X01X11X01X11 X 0005 X 0006 X 1D45 X 0F00 X 1F00 X 0001 0007 000 us 24.24 us 1X01X11X01X11	23.44 u 1001X11X01X11 0007X 0008 X X 8568 X 3000 X X 7800 X X 0018 X X 101 X \$ 24.32 us	\$ 23.52 us \[\sqrt{11} \sqrt{11} \text{Vol X11} \text{Vol X11} \\ 00009 \text{Vol COCA \text{X} (} \\ 11E5 \text{X 1175 \text{X} :} \\ 7800 \text{X} \\ A75B \text{X D6E8 \text{X} :} \\ 00000 \text{X 110 \text{X} :} \\ 100 \text{X 110 \text{X} :} \\ 100 \text{X 111 \text{X} :} \\ 01 \text{X 11 \text{X 11 \text{X} :} \\ 0000 \text{X 110 \text{X} :} \\ 0001 \text{X 11 \text{X 11 \text{X} :} \\ 0001 \text{X 11 \text{X 11 \text{X} :} \\ 0000 \text{X 1 \text{X 11 \text{X} :} \\ 0000 \text{X 0 \text{X 0 \text{X 11 \text{X} :} \\ 0000 X 0 \text{X	23.6 us 01\(11\)\(01\)\(11\)\(11\)\(01\)\(11\)\	DIX11X01X11 CD X 00CE X (100 X 0AFD X (10	23.76 us (01\11\01\11\01\11\01\11\01\11\01\11\01\0	0000 0000 0000 0000 0000 0000 0000 0000 0000
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