Mixed Data-Type Circuit Modeling: The Ideal Diode

John Rugis

***Abstract*— This article presents a mixed numeric plus Boolean data-type algebraic representation that can be used to characterize certain non-linear ideal circuit components for the purpose of sparse matrix circuit modeling. The first part of this article introduces the concept of and some features of a mixed data-type algebra in the context of electronics. Then a mixed data-type characterization for the ideal diode is presented. Finally the mixed data-type models of several example circuits are explored.**

I. INTRODUCTION

THe use of mixed data-type expressions, although not commonly used in mathematics of electronics engineering, is included in the syntax of the C and C++ computer programming languages [1], [2], [3]. We will build on that source as well as on the notational conventions and syntax used in discrete and foundational mathematics [4] to develop a mixed data-type algebra for circuit modeling.

In most engineering contexts it is implicitly understood that the data-type of a constant or unknown variable is a real number. The algebraic expressions that use these variables include operators that are defined for real numbers, such as "+" for addition and the blank no symbol at all for multiplication. The resultant data-type of an algebraic expression such as $a+b$ is then subsequently understood to be a real number. This is symbolically indicated by $(a+b) \in \mathbb{R}$. When it is said that division by zero is not defined it means that whatever the result of division by zero is, it is not a real number.

Additionally, the specialized engineering context of logic circuit design employs the Boolean "true" or "false" data-type[1]. The Boolean data-type as used in engineering has its own collection of operators including "+" for logical OR and "$\times$" (or again no symbol at all) for logical AND. In this context the resultant data-type of an algebraic expression such as $a+b$ is understood to be Boolean. This is symbolically indicated by $(a+b) \in \mathbb{B}$. The reuse and redefinition of operator symbols for different data-types is known as *operator overloading*.

II. MIXED DATA-TYPE EXPRESSIONS

It is possible to construct mixed data-type expressions if we define rules for automatic *type conversion*. To avoid ambiguity we will for the most part not overload operators in this presentation. We will use the logical operator symbol set from pure mathematics which includes, for example, "$\wedge$" for logical AND and "$\vee$" for logical OR.

Operator	Operation	Arguments		Result
+	addition	numeric	numeric	numeric
-	subtraction	numeric	numeric	numeric
-	negation	numeric	none	numeric
(blank)	multiplication	numeric	numeric	numeric
/	division	numeric	numeric	numeric
$<$	less than	numeric	numeric	boolean
$>$	greater than	numeric	numeric	boolean
$=$	equal to	numeric	numeric	boolean
$\wedge$	and	boolean	boolean	boolean
$\vee$	or	boolean	boolean	boolean
$\oplus$	exclusive or	boolean	boolean	boolean
$\Rightarrow$	implication	boolean	boolean	boolean

TABLE I
OPERATORS

We define a type conversion scheme in which the Boolean data-type is converted to a numeric data type. The type conversion is automatically invoked whenever an operator requires a real number but has been given a Boolean value. The type conversion rule is quite simple:

> *When required, convert the Boolean "true" to the real number 1 and the Boolean "false" to the real number 0.*

This is the only type conversion that will be required in the application presented in this article.

Given a real number type variable a and a Boolean variable b, again consider the algebraic expression $a+b$. Since the + operator is now only defined for real numbers it is necessary to convert the Boolean type variable b to a numeric value for expression to be defined. If, for example, the value of a is 5 and the value of b is true, the value of the expression $a+b$ is 6. The expression has a resultant real number data-type.

The operators "+" for addition and "$\wedge$" for logical AND are *binary operators* in the sense that they take two inputs. The addition operator takes two numeric input values and produces one numeric output value. The logical AND operator takes two Boolean input values and produces one Boolean output value. Somewhat differently, the greater-than operator "$>$" takes two numeric input values and produces one Boolean output value. So, using our type conversion rule, the resultant data-type of the expression $c\,(a>b)$ is numeric. If, for example, the value of a is 2, the value of b is 1 and the value of c is 5, the value of the expression $c\,(a>b)$ is 5.

Table 1 gives a summary of all the operators that we will use. Note that we have overloaded the "$-$" operator, using it

The author is with the Department of Electrical and Computer Engineering at Manukau Institute of Technology in Auckland, New Zealand.

[1]The Boolean data-type is alternatively sometimes thought of as a binary numeric data-type.

as the symbol for both the binary operation subtraction and for the unary operation negation.

Using our notational convention as defined so far, the expression $i = v/R$, where $(i, v, R) \in \mathbb{R}$, evaluates to a Boolean data-type, and as such could be either true or false. If we are intending to make a statement of Ohm's Law, what we would actually want to say is that for all possible values of i, v and R this expression is always true. A statement consisting of an *always true* boolean expression is known as a *tautology*. The symbol $\vDash$ is used to indicate that the statement it precedes is a tautology. Ohm's Law expressed as tautological statement is:

$$\vDash (i = v/R)$$

For the sake of brevity we will often omit the symbol $\vDash$ and refer to a tautological statement simply as a *statement* to distinguish it from an *expression*.

Expressions in the following form will reoccur later in this article:

$$rx + sy = c$$
$$\text{where } (r, s) \in \mathbb{B},\ (x, y, c) \in \mathbb{R}$$
$$\text{and } \vDash (r \oplus s)$$

In this case we will refer to the boolean variables r and s as *selectors* since they effectively select one of the numeric variables x or y as being equal to the constant number c.

III. Characteristic statements

Electronic devices as mathematical entities are defined by their characteristic tautological statements [5]. From this perspective Ohm's Law is simply the characterization statement for the resistor device. Device characteristic statements are the building blocks that we use to create circuit models. A circuit model is also, in turn, as a whole, a larger compound tautological statement.

When doing circuit modeling with a sparse matrix [5], as we will in this article, it is easier to work with the matrix formulation of device characteristic statements. For the resistor device as an example we have:

$$\begin{bmatrix} 1 & -R \end{bmatrix} \begin{bmatrix} v \\ i \end{bmatrix} = 0$$

Next we will use mixed data-type statements to characterize the ideal diode.

IV. The ideal diode

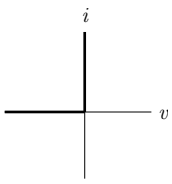

Fig. 1. Diode characteristic vi curve.

Figure 1 is a plot of the characteristic vi curve for an ideal diode. This curve is clearly non-linear. Additionally, because the curve is 'L' shaped and aligned with both axis, it cannot be represented as a piece-wise linear function. However, it is possible to build a mixed data-type representation based on the observations that:

1) either the voltage or the current is zero,
2) if the current is zero then the voltage is less than or equal to zero,
3) and if the voltage is zero then the current is greater than or equal to zero.

These observations can be represented symbolically with the mixed data-type expressions:

$$(v = 0) \vee (i = 0)$$
$$(i = 0) \Rightarrow (v \leq 0)$$
$$(v = 0) \Rightarrow (i \geq 0)$$

These three expressions can be combined to give a single complete mixed data-type characteristic statement for the ideal diode:

$$\vDash \Big(\big((v = 0) \vee (i = 0) \big) \wedge \big((i = 0) \Rightarrow (v \leq 0) \big) \wedge \big((v = 0) \Rightarrow (i \geq 0) \big) \Big)$$

The ideal diode can also be equivalently characterized using selector notation and the following collection of statements:

$$rv + si = 0 \quad (1)$$
$$r \oplus s \quad (2)$$
$$(i = 0) \Rightarrow (v \leq 0) \quad (3)$$
$$(v = 0) \Rightarrow (i \geq 0) \quad (4)$$

In matrix form equations (1) and (2) become:

$$\begin{bmatrix} r & s \end{bmatrix} \begin{bmatrix} v \\ i \end{bmatrix} = 0 \quad (5)$$
$$\text{where } \begin{bmatrix} r & s \end{bmatrix} \in \left\{ \begin{bmatrix} 0 & 1 \end{bmatrix}, \begin{bmatrix} 1 & 0 \end{bmatrix} \right\} \quad (6)$$

Note that when the diode current is non-zero we say that the diode is *forward biased* and when the voltage is non-zero we say that the diode is *reverse biased*.

V. Circuit modeling with the ideal diode

The next goal will be to use the mixed data-type characterization of the ideal diode as a building block in a circuit model.

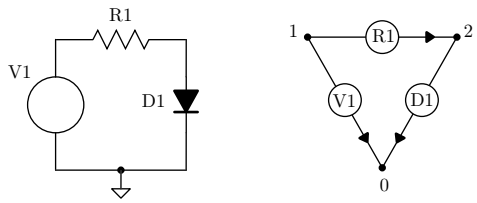

Fig. 2. Example circuit.

A. Single diode example.

Figure 2 shows schematic, a digraph, and a netlist for an example circuit. An electrical engineer could readily produce mathematical statements for the diode voltage drop and diode current by inspection for this simple circuit. What we seek however is a general method for finding solutions that proceeds mechanically in a way that is conducive to computer implementation.

Using the method and conventions given in [5], the symbolic sparse matrix model in the form $[\mathbf{T}|\mathbf{u}]$ for this example is:

$$\left[\begin{array}{cccccccc|c} 0 & 0 & 0 & 0 & 0 & 1 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & -1 & 1 & 0 \\ -1 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ -1 & 1 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & V_{V1} \\ 0 & 0 & 0 & 1 & 0 & 0 & -R_{R1} & 0 & 0 \\ 0 & 0 & 0 & 0 & r_{D1} & 0 & 0 & s_{D1} & 0 \end{array}\right] \quad (7)$$

Note that selectors for the diode have been included in the model thereby creating a mixed data-type augmented matrix. As a first check for the existence of solutions, we calculate[1] the determinant of the left-hand side of the augmented matrix and get the result:

$$\det \mathbf{T} = s_{D1} - r_{D1} R_{R1}$$

Solutions to the model exist only when the determinant is non-zero. Remembering the selector cases given in equation (6), we begin the construction of a solutions table by listing all of the possible selector values along with the associated determinant value:

$[\, r_{D1} \;\; s_{D1} \,]$	$\det \mathbf{T}$
$[\, 0 \;\; 1 \,]$	1
$[\, 1 \;\; 0 \,]$	$-R_{R1}$

To insure that the determinant is non-zero, we need to append a constraint to the second row in the solutions table:

$[\, r_{D1} \;\; s_{D1} \,]$	$\det \mathbf{T}$	constraints
$[\, 0 \;\; 1 \,]$	1	none
$[\, 1 \;\; 0 \,]$	$-R_{R1}$	$R_{R1} > 0$

Note that we have also taken into account the global constraint that all resistors are non-negative.

Solving the model matrix (7) symbolically for the diode voltage drop and diode current solution variables yields:

$$v_{D1} = \frac{s_{D1} V_{V1}}{\det \mathbf{T}}$$

$$i_{D1} = \frac{-r_{D1} V_{V1}}{\det \mathbf{T}}$$

[1]The author has used the software package *Maple* [6] to assist with many of the symbolic calculations in this article.

We refine the solutions table by adding a column for each of the desired solution variables and removing the now redundant determinant column:

$[\, r_{D1} \;\; s_{D1} \,]$	constraints	v_{D1}	i_{D1}
$[\, 0 \;\; 1 \,]$	none	V_{V1}	0
$[\, 1 \;\; 0 \,]$	$R_{R1} > 0$	0	V_{V1}/R_{R1}

Note that at this stage we could have added a column for any other desired solution variable such as, for example, resistor current. Next we remove the redundant selectors column and include any additional constraints based on the implication of the diode characterization statements (3) and (4):

constraints	v_{D1}	i_{D1}
$v_{D1} \leq 0$	V_{V1}	0
$i_{D1} \geq 0, R_{R1} > 0$	0	V_{V1}/R_{R1}

Finally we seek to express everything in the constraints column in a form that does not contain any of the solution variables. In the first solution row we have the constraint $v_{D1} \leq 0$. But since the second column gives $v_{D1} = V_{V1}$ this constraint can be equivalently expressed as $V_{V1} \leq 0$. In a similar manner we also replace the first constraint in the second row. The complete solutions table for the sample circuit is:

constraints	v_{D1}	i_{D1}
$V_{V1} \leq 0$	V_{V1}	0
$V_{V1} \geq 0, R_{R1} > 0$	0	V_{V1}/R_{R1}

Note that there is a case under which the model does not give a solution, namely when $V_{V1} > 0$ and $R_{R1} = 0$. In this case the problem is that a zero value resistor would result in an infinite current.

All of the diode voltage drop and diode current solutions for this example circuit are therefore given by the equivalent single complete mixed data-type statement:

$$\vDash \Big(\big((V_{V1} \leq 0) \implies (v_{D1} = V_{V1}) \wedge (i_{D1} = 0) \big) \wedge$$
$$\big((V_{V1} > 0) \wedge (R_{R1} > 0) \implies (v_{D1} = 0) \wedge (i_{D1} = V_{V1}/R_{R1}) \big) \Big)$$

Notice that in this statement we have removed the overlap in cases where $V_{V1} = 0$.

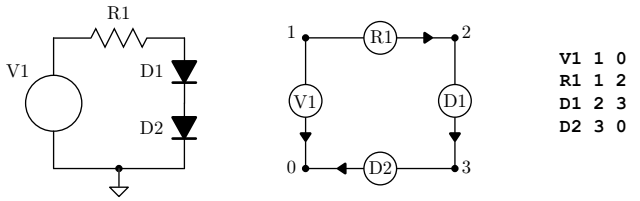

Fig. 3. Example circuit.

B. A series diode example.

Figure 3 shows schematic, a digraph, and a netlist for a series diode example circuit. Proceeding as before, the determinant for the model is given by:

$$\det \mathbf{T} = -s_{D2} r_{D1} - s_{D1} r_{D2} + r_{D1} r_{D2} R_{R1}$$

Construction of the solutions table begins as a list of all of the possible selector cases along with the associated determinant value:

$[\, r_{D1} \;\; s_{D1} \;\; r_{D2} \;\; s_{D2} \,]$	$\det \mathbf{T}$
$[\, 0 \;\; 1 \;\; 0 \;\; 1 \,]$	0
$[\, 0 \;\; 1 \;\; 1 \;\; 0 \,]$	-1
$[\, 1 \;\; 0 \;\; 0 \;\; 1 \,]$	-1
$[\, 1 \;\; 0 \;\; 1 \;\; 0 \,]$	R_{R1}

Solutions occur only when the determinant is non-zero, so we delete the first row and append constraints as required:

$[\, r_{D1} \;\; s_{D1} \;\; r_{D2} \;\; s_{D2} \,]$	$\det \mathbf{T}$	constraints
$[\, 0 \;\; 1 \;\; 1 \;\; 0 \,]$	-1	none
$[\, 1 \;\; 0 \;\; 0 \;\; 1 \,]$	-1	none
$[\, 1 \;\; 0 \;\; 1 \;\; 0 \,]$	R_{R1}	$R_{R1} > 0$

Solving the model matrix symbolically for the diode voltage drop and diode current solution variables yields:

$$v_{D1} = \frac{-s_{D1} r_{D2} V_{V1}}{\det \mathbf{T}}$$

$$i_{D1} = \frac{r_{D1} r_{D2} V_{V1}}{\det \mathbf{T}}$$

$$v_{D2} = \frac{-r_{D1} s_{D2} V_{V1}}{\det \mathbf{T}}$$

$$i_{D2} = \frac{r_{D1} r_{D2} V_{V1}}{\det \mathbf{T}}$$

We refine the solutions table by removing both the selectors column and the determinant column and adding a column for each of the desired solution variables:

constraints	v_{D1}	i_{D1}	v_{D2}	i_{D2}
none	V_{V1}	0	0	0
none	0	0	V_{V1}	0
$R_{R1} > 0$	0	V_{V1}/R_{R1}	0	V_{V1}/R_{R1}

Next we update the constraints based on the diode characterization implications:

constraints	v_{D1}	i_{D1}	v_{D2}	i_{D2}
$v_{D1} \leq 0$	V_{V1}	0	0	0
$v_{D2} \leq 0$	0	0	V_{V1}	0
$i_{D1} \geq 0$, $i_{D2} \geq 0$, $R_{R1} > 0$	0	V_{V1}/R_{R1}	0	V_{V1}/R_{R1}

After expressing everything in the constraints column in a form that does not contain any of the solution variables we have:

constraints	v_{D1}	i_{D1}	v_{D2}	i_{D2}
$V_{V1} \leq 0$	V_{V1}	0	0	0
$V_{V1} \leq 0$	0	0	V_{V1}	0
$V_{V1} \geq 0$, $R_{R1} > 0$	0	V_{V1}/R_{R1}	0	V_{V1}/R_{R1}

The first two rows contradict each other except when $V_{V1} = 0$. We can remove the contradiction by tightening the constraints and combining the first two rows. The completed solutions table is:

constraints	v_{D1}	i_{D1}	v_{D2}	i_{D2}
$V_{V1} = 0$	0	0	0	0
$V_{V1} \geq 0$, $R_{R1} > 0$	0	V_{V1}/R_{R1}	0	V_{V1}/R_{R1}

There are cases under which the model does not give a solution. When $V_{V1} < 0$ the voltage at the node common to the diodes is apparently not well-defined. This problem could be resolved in practice by simply not using series ideal diodes in the model. Replacing series diodes with a single ideal diode gives a more comprehensive and overall no less informative solution. When $V_{V1} > 0$ and $R_{R1} = 0$ there is still a problem however with the resultant infinite current.

All of the diode voltage drop and diode current solutions for this example circuit are given by the single complete mixed data-type statement:

$$\begin{aligned} \vDash \Big(\big((V_{V1} = 0) \implies (v_{D1} = i_{D1} = v_{D2} = i_{D2} = 0) \big) \wedge \\ \big((V_{V1} > 0) \wedge (R_{R1} > 0) \implies \\ (v_{D1} = v_{D2} = 0) \wedge (i_{D1} = i_{D2} = V_{V1}/R_{R1}) \big) \Big) \end{aligned}$$

Notice that we have removed the overlap in cases where $V_{V1} = 0$.

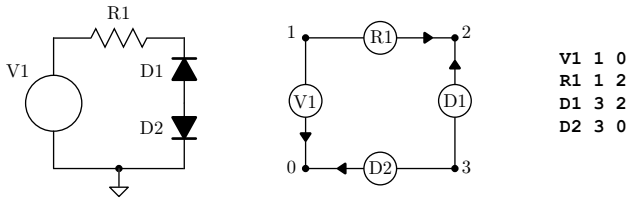

Fig. 4. Example circuit.

C. A back-to-back diode example.

Figure 4 shows schematic, a digraph, and a netlist for a back-to-back diode example circuit. The determinant and the beginning solutions table for the model are the same as in the previous example:

$$\det \mathbf{T} = -s_{D2} r_{D1} - s_{D1} r_{D2} + r_{D1} r_{D2} R_{R1}$$

$[\, r_{D1} \;\; s_{D1} \;\; r_{D2} \;\; s_{D2} \,]$	$\det \mathbf{T}$
$[\, 0 \;\; 1 \;\; 0 \;\; 1 \,]$	0
$[\, 0 \;\; 1 \;\; 1 \;\; 0 \,]$	-1
$[\, 1 \;\; 0 \;\; 0 \;\; 1 \,]$	-1
$[\, 1 \;\; 0 \;\; 1 \;\; 0 \,]$	R_{R1}

As in the previous example we delete the first row and append constraints as required:

$[\, r_{D1} \;\; s_{D1} \;\; r_{D2} \;\; s_{D2} \,]$	$\det \mathbf{T}$	constraints
$[\, 0 \;\; 1 \;\; 1 \;\; 0 \,]$	-1	none
$[\, 1 \;\; 0 \;\; 0 \;\; 1 \,]$	-1	none
$[\, 1 \;\; 0 \;\; 1 \;\; 0 \,]$	R_{R1}	$R_{R1} > 0$

Solving the model matrix symbolically for the diode voltage drop and diode current solution variables yields:

$$v_{D1} = \frac{s_{D1} r_{D2} V_{V1}}{\det \mathbf{T}}$$

$$i_{D1} = \frac{-r_{D1} r_{D2} V_{V1}}{\det \mathbf{T}}$$

$$v_{D2} = \frac{-r_{D1} s_{D2} V_{V1}}{\det \mathbf{T}}$$

$$i_{D2} = \frac{r_{D1} r_{D2} V_{V1}}{\det \mathbf{T}}$$

We refine the solutions table by removing both the selectors column and the determinant column and adding a column for each of the desired solution variables:

constraints	v_{D1}	i_{D1}	v_{D2}	i_{D2}
none	$-V_{V1}$	0	0	0
none	0	0	V_{V1}	0
$R_{R1} > 0$	0	V_{V1}/R_{R1}	0	$-V_{V1}/R_{R1}$

Next we update the constraints based on the diode characterization implications:

constraints	v_{D1}	i_{D1}	v_{D2}	i_{D2}
$v_{D1} \leq 0$	$-V_{V1}$	0	0	0
$v_{D2} \leq 0$	0	0	V_{V1}	0
$i_{D1} \geq 0$, $i_{D2} \geq 0$, $R_{R1} > 0$	0	V_{V1}/R_{R1}	0	$-V_{V1}/R_{R1}$

After expressing everything in the constraints column in a form that does not contain any of the solution variables we have:

constraints	v_{D1}	i_{D1}	v_{D2}	i_{D2}
$V_{V1} \geq 0$	$-V_{V1}$	0	0	0
$V_{V1} \leq 0$	0	0	V_{V1}	0
$V_{V1} \geq 0$, $V_{V1} \leq 0$, $R_{R1} > 0$	0	V_{V1}/R_{R1}	0	$-V_{V1}/R_{R1}$

Combining constraints in the third row gives:

constraints	v_{D1}	i_{D1}	v_{D2}	i_{D2}
$V_{V1} \geq 0$	$-V_{V1}$	0	0	0
$V_{V1} \leq 0$	0	0	V_{V1}	0
$V_{V1} = 0$, $R_{R1} > 0$	0	0	0	0

But since the case represented by the third row is also given in both the first and second row, we can delete the third row. The final solutions table is:

constraints	v_{D1}	i_{D1}	v_{D2}	i_{D2}
$V_{V1} \geq 0$	$-V_{V1}$	0	0	0
$V_{V1} \leq 0$	0	0	V_{V1}	0

The model gives solutions for all cases. Note that there are no conditions under which current flows in this circuit.

All of the diode voltage drop and diode current solutions for this example circuit are given by the single complete mixed data-type statement:

$$\begin{aligned} \vDash \Big(&\big((V_{V1}{=}0) \implies (v_{D1}{=}i_{D1}{=}v_{D2}{=}i_{D2}{=}0)\big) \wedge \\ &\big((V_{V1}{>}0) \implies (v_{D1}{=}{-}V_{V1}) \wedge (i_{D1}{=}i_{D2}{=}v_{D2}{=}0) \wedge \\ &\big((V_{V1}{<}0) \implies (v_{D2}{=}V_{V1}) \wedge (i_{D1}{=}i_{D2}{=}v_{D1}{=}0)\big)\Big) \end{aligned}$$

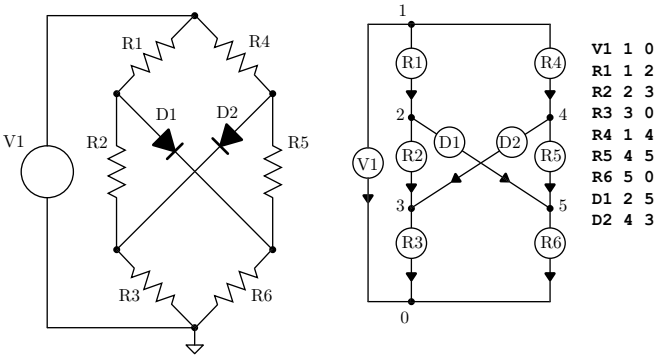

Fig. 5. Example circuit.

D. A more complex example with two diodes.

Figure 5 shows schematic, a digraph, and a netlist for another example circuit. It is relatively easy to identify by inspection the conditions under which both diodes would be forward biased (ie: current is non-zero). But let's ask a somewhat more difficult question:

Under what conditions, if any, will diode $D1$ be forward biased and diode $D2$ be reverse biased?

To answer this question we will concentrate only on the one required row in the solutions table. The row associated with the case where diode $D1$ current is non-zero and diode $D2$ voltage is non-zero is the row in which:

$$[\, r_{D1} \;\; s_{D1} \;\; r_{D2} \;\; s_{D2} \,] = [\, 1 \;\; 0 \;\; 0 \;\; 1 \,]$$

The determinant evaluated for this row is given by:

$$\begin{aligned} \det \mathbf{T} = {} & R_{R1}(R_{R2} + R_{R3})(R_{R4} + R_{R5} + R_{R6}) + \\ & R_{R6}(R_{R4} + R_{R5})(R_{R1} + R_{R2} + R_{R3}) \end{aligned}$$

Note that because resistors have non-negative values, the determinant is also non-negative. There are a number of combinations of zero valued resistors that will cause the determinant to be zero. This row will therefore not give a

solution under any of the following conditions:

$$R_{R1} + R_{R2} + R_{R3} = 0 \quad (8)$$
$$R_{R4} + R_{R5} + R_{R6} = 0 \quad (9)$$
$$R_{R1} + R_{R4} + R_{R5} = 0 \quad (10)$$
$$R_{R2} + R_{R3} + R_{R6} = 0 \quad (11)$$
$$R_{R1} + R_{R6} = 0 \quad (12)$$
$$R_{R2} + R_{R3} + R_{R4} + R_{R5} = 0 \quad (13)$$

We continue by considering the voltage and current associated with diode $D2$ as evaluated for the row under consideration:

$$v_{D2} = V_{V1}(R_{R1}R_{R2}R_{R5} + R_{R1}R_{R2}R_{R6} + R_{R1}R_{R3}R_{R5} + R_{R1}R_{R5}R_{R6} + R_{R2}R_{R4}R_{R6} + R_{R2}R_{R5}R_{R6})/\det \mathbf{T}$$

But since the current i_{D2} is evaluated to be zero, the diode characteristic implication (3) states that voltage v_{D2} must be less than or equal to zero. Because the determinant is positive and resistors have non-negative values, this in turn implies that

$$V_{V1} \leq 0 \quad (14)$$

and this becomes a new constraint for the row.

Now we consider the current and voltage associated with diode $D1$ as evaluated for this row:

$$i_{D1} = V_{V1}(R_{R2}R_{R4} + R_{R2}R_{R5} + R_{R3}R_{R4} + R_{R3}R_{R5} - R_{R1}R_{R6})/\det \mathbf{T}$$

But since the voltage v_{D1} is evaluated to be zero, the diode characteristic implication (4) states that i_{D1} is therefore greater than or equal to zero. Since we already have the determinant positive and V_{V1} less than or equal to zero, for this row to give a solution we must therefore have:

$$(R_{R2}R_{R4} + R_{R2}R_{R5} + R_{R3}R_{R4} + R_{R3}R_{R5} - R_{R1}R_{R6}) \leq 0$$

After rearranging we have:

$$R_{R1}R_{R6} \geq (R_{R2}R_{R4} + R_{R2}R_{R5} + R_{R3}R_{R4} + R_{R3}R_{R5}) \quad (15)$$

Remember that what we are seeking according to the original question are the conditions under which the current through diode $D1$ is *greater* than zero. Combining statements (14) and (15) we have as the final answer:

Diode $D1$ will be forward biased and diode $D2$ will be reverse biased whenever:

$$(V_{V1} < 0) \wedge \big(R_{R1}R_{R6} > (R_{R2}R_{R4} + R_{R2}R_{R5} + R_{R3}R_{R4} + R_{R3}R_{R5})\big)$$

and none of the expressions (8) through (13) are true.

The result can be checked by exploring a modified circuit in which $R1$ and $R6$ have been removed. Removing $R1$ and $R6$ effectively sets their value to infinity in which case the statement (15) will most certainly be true. Figure 6 shows the circuit with $R1$ and $R6$ removed. It is clear by inspection that diode $D1$ will be forward biased and diode $D2$ will be reverse biased when V_{V1} is negative.

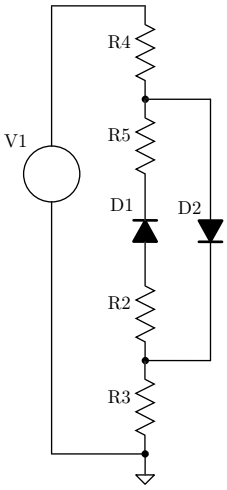

Fig. 6. Modified circuit.

VI. A SUMMARY OF THE METHOD

The method that we used to extract information from the sparse matrix circuit model when it contains one or more ideal diodes can be summarized as follows:

1) Build the augmented sparse matrix including selector entries for the diodes.
2) Construct a solutions table with a row for each of the selector cases. Add columns for all of the diode voltages and currents. Add a column for each of any other desired solution variable.
3) Calculate the symbolic determinant of the sparse matrix.
4) Evaluate the determinant for each row. Remove any rows in which the determinant is identically zero. Append constraints to rows as required to insure that the determinant is never zero.
5) Solve the augmented sparse matrix symbolically .
6) Evaluate each solution variable in each row of the solutions table.
7) Update the constraints in each row as required by the diode characteristic implications.
8) Restate the constraints in terms that do not include any of the solution variables.
9) Combine each row of the solutions table in a final solutions statement that removes any overlapping cases.

VII. CONCLUSION

We have presented a mixed data-type characterization for the (non-linear) ideal diode. This characterization can be used with a generalized sparse matrix circuit model and symbolic mixed data-type solutions can be extracted from the resulting model. The process of extracting solutions proceeds mechanically, using only the rules of mathematics and mathematical logic.

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REFERENCES

[1] B. W. Kernighan and D. M. Ritchie, *The C Programming Language*. New Jersey: Prentice-Hall, 1978.
[2] S. C. Dewhurst and K. T. Stark, *Programming in C+*. New Jersey: Prentice-Hall, 1989.
[3] B. Stroustrup, *The C++ Programming Language*, 3rd ed. Massachusetts: Addison-Wesley, 1997.
[4] S. Grantham, *Discrete and Foundational Mathematics*. Idaho: Boise State University, August 1999.
[5] J. Rugis, "Symbolic circuit modeling and simulation: An introduction," *Article Preprint*, January 2004.
[6] *Maple 6*, Waterloo Maple Inc., January 2000, computer program and documentation.

email: jrugis@manukau.ac.nz