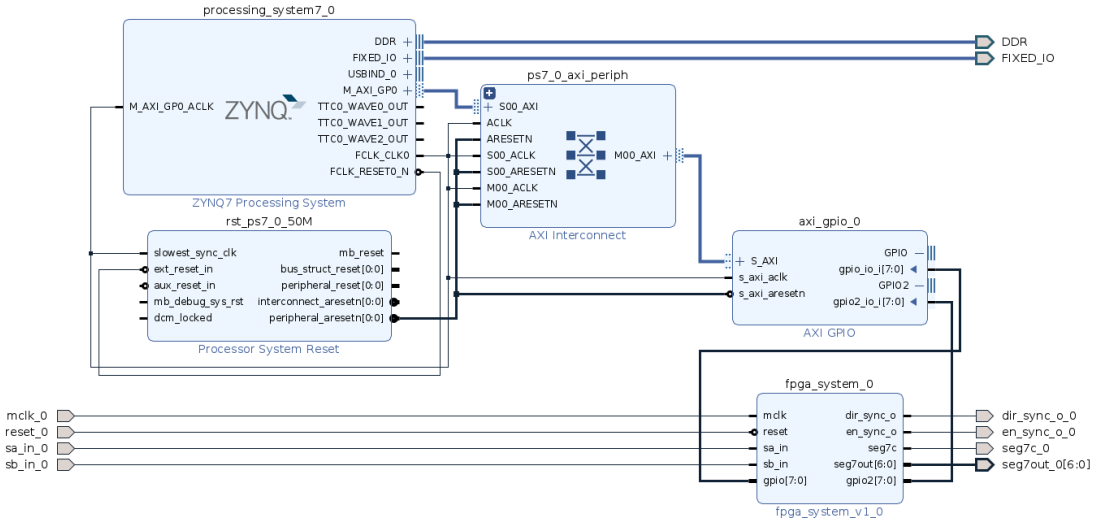
Optional: Add an Integrated Logic Analyzer(ILA) to you block design

Part 1: This part can be done when you have completed step 20 on page 39 in the Modified UG1165 (i.e. before creating the HDL wrapper).

An integrated logic analyzer (ILA) can be added at this stage to enable viewing the actual values of our signals in the implemented design. While it is running in on the FPGA!
We will use it to probe the two 8-bit vectors between our FPGA System and the Processor system. You can add more for other signals aswell if you want.

Before adding the ILA the Block Design should look something like diagram below:



To add an ILA to the design:

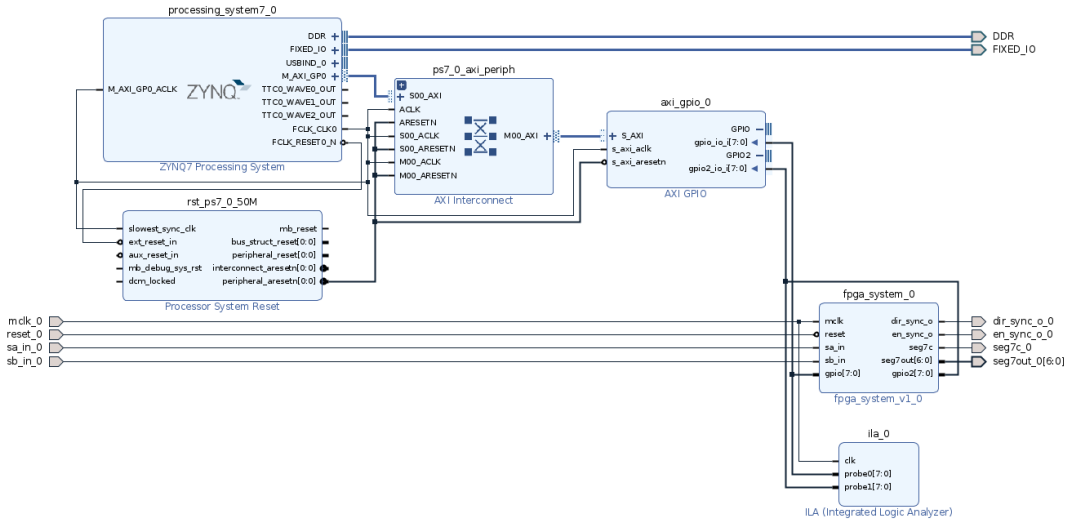
1. Press the '+' (Add IP) Like you did to add the others IPs previously.
2. Search for ILA and add ILA (Integrated Logic Analyzer)
3. An ILA block will now show up in your design. Double click this block to customize it in the following way:
   (a) Monitor type: Native
   (b) Number of probes: 2
   (c) Sample Data Depth: 4096
   (d) In the Probe_Ports tab. Set the bit width for both probes to 8.

4. Now the ILA is customized to probe two 8-bit signals with a sample depth of 4096. If you want to add for other signals: add a probe of the signal you want to probe, and set the bit width accordingly.

5. Drag and drop you mclk signal to the clk port of the ILA. This port determines when the ILA samples the probes.

6. Drag and drop signals you want to probe (GPIO and GPIO2) to the probe0 and probe1 of the ILA.

With the ILA the block design should look something like this:



Now, with the ILA as a part of the design. When the device is programmed in Vivado a new tab to interact with the ILA should show up in the Hardware Manager.
Continue with the modified UG1165 page 40 step 24, (Creating a HDL Wrapper).

Part 2:
This part can be done when you have completed Step 7 on page 46 in the modified UG1165. We will diverge from UG1165 at step 8 when we program the FPGA.
To interact with the ILA we will use the Vivado Hardware Manager GUI. And we need to program the FPGA part of the ZYNQ 7000 through Vivado, not through Vitis which UG1165 want us to. By default, Vitis will program the FPGA when we run on hardware. We do not want this, since we want to interact with the ILA.
To program design with ILA:

1. In Vivado: Open Hardware Manager in Vivado and program FPGA as normal.

2. In Vitis: Click the Run dropdown menu and click 'Run Configurations...'

3. In this new Run Configurations window, select the Target Setup tab, and uncheck the two buttons: 'Reset entire system' and 'Program FPGA'.

When the FPGA is programmed trough Vivado and the Run Configurations are modified. You may run the appication in Vitis by selecting Run as -¿ Launch on Hardware.
While the application is running go back into Vivado and trigger the ILA by pressing the play button. You may setup triggers to so that the ILA only triggers when a specific condition in the probes are met.
When the ILA is triggered you may view the actual value of the signals inside the FPGA!