```
#-----------------------------------------------------------
# Vivado v2015.4 (64-bit)
# SW Build 1412921 on Wed Nov 18 09:44:32 MST 2015
# IP Build 1412160 on Tue Nov 17 13:47:24 MST 2015
# Start of session at: Tue May  3 09:49:57 2016
# Process ID: 2711
# Current directory:
/home/jrvgnzlz/EE_316_Labs/Lab_7_Vivado/project_7/project_7.runs/
synth_1
# Command line: vivado -log Top.vds -mode batch -messageDb
vivado.pb -notrace -source Top.tcl
# Log file:
/home/jrvgnzlz/EE_316_Labs/Lab_7_Vivado/project_7/project_7.runs/
synth_1/Top.vds
# Journal file:
/home/jrvgnzlz/EE_316_Labs/Lab_7_Vivado/project_7/project_7.runs/
synth_1/vivado.jou
#-----------------------------------------------------------
source Top.tcl -notrace
Command: synth_design -top Top -part xc7a35tcpg236-1
Starting synth_design
Attempting to get a license for feature 'Synthesis' and/or device
'xc7a35t'
INFO: [Common 17-349] Got license for feature 'Synthesis' and/or
device 'xc7a35t'
---------------------------------------------------------------
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Starting RTL Elaboration : Time (s): cpu = 00:00:09 ; elapsed =
00:00:09 . Memory (MB): peak = 1022.914 ; gain = 178.766 ; free
physical = 1350 ; free virtual = 31369
---------------------------------------------------------------
---------------
INFO: [Synth 8-638] synthesizing module 'Top'
[/home/jrvgnzlz/EE_316_Labs/Lab_7_Vivado/top.vhd:20]
INFO: [Synth 8-3491] module 'clock_divider' declared at
'/home/jrvgnzlz/EE_316_Labs/Lab_7_Vivado/clock_div.vhd:10' bound
to instance 'clock_div_inst' of component 'clock_divider'
[/home/jrvgnzlz/EE_316_Labs/Lab_7_Vivado/top.vhd:41]
INFO: [Synth 8-638] synthesizing module 'clock_divider'
[/home/jrvgnzlz/EE_316_Labs/Lab_7_Vivado/clock_div.vhd:17]
INFO: [Synth 8-256] done synthesizing module 'clock_divider'
(1#1) [/home/jrvgnzlz/EE_316_Labs/Lab_7_Vivado/clock_div.vhd:17]
INFO: [Synth 8-3491] module 'Product_Sum' declared at
```

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'/home/jrvgnzlz/EE_316_Labs/Lab_7/Problem_20.vhd:13' bound to
instance 'Arbitrary_Name' of component 'Product_Sum'
[/home/jrvgnzlz/EE_316_Labs/Lab_7_Vivado/top.vhd:42]
INFO: [Synth 8-638] synthesizing module 'Product_Sum'
[/home/jrvgnzlz/EE_316_Labs/Lab_7/Problem_20.vhd:21]
WARNING: [Synth 8-614] signal 'Nextstate' is read in the process
but is not in the sensitivity list
[/home/jrvgnzlz/EE_316_Labs/Lab_7/Problem_20.vhd:165]
INFO: [Synth 8-256] done synthesizing module 'Product_Sum' (2#1)
[/home/jrvgnzlz/EE_316_Labs/Lab_7/Problem_20.vhd:21]
INFO: [Synth 8-256] done synthesizing module 'Top' (3#1)
[/home/jrvgnzlz/EE_316_Labs/Lab_7_Vivado/top.vhd:20]
---------------------------------------------------------------
---------------
Finished RTL Elaboration : Time (s): cpu = 00:00:10 ; elapsed =
00:00:11 . Memory (MB): peak = 1062.297 ; gain = 218.148 ; free
physical = 1303 ; free virtual = 31323
---------------------------------------------------------------
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Report Check Netlist:
+------+------------------+-------+---------+-------+------------
------+
|      |Item              |Errors |Warnings |Status |Description
     |
+------+------------------+-------+---------+-------+------------
------+
|1     |multi_driven_nets |      0|        0|Passed |Multi driven
nets |
+------+------------------+-------+---------+-------+------------
------+
---------------------------------------------------------------
---------------
Finished RTL Optimization Phase 1 : Time (s): cpu = 00:00:11 ;
elapsed = 00:00:11 . Memory (MB): peak = 1062.297 ; gain =
218.148 ; free physical = 1306 ; free virtual = 31323
---------------------------------------------------------------
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INFO: [Device 21-403] Loading part xc7a35tcpg236-1
INFO: [Project 1-570] Preparing netlist for logic optimization

Processing XDC Constraints
Initializing timing engine
```

```
Parsing XDC File
[/home/jrvgnzlz/EE_316_Labs/Lab_7_Vivado/Basys3_Master.xdc]
Finished Parsing XDC File
[/home/jrvgnzlz/EE_316_Labs/Lab_7_Vivado/Basys3_Master.xdc]
INFO: [Project 1-236] Implementation specific constraints were
found while reading constraint file
[/home/jrvgnzlz/EE_316_Labs/Lab_7_Vivado/Basys3_Master.xdc].
These constraints will be ignored for synthesis but will be used
in implementation. Impacted constraints are listed in the file
[.Xil/Top_propImpl.xdc].
Resolution: To avoid this warning, move constraints listed in
[.Xil/Top_propImpl.xdc] to another XDC file and exclude this new
file from synthesis with the used_in_synthesis property (File
Properties dialog in GUI) and re-run elaboration/synthesis.
Completed Processing XDC Constraints

INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

Constraint Validation Runtime : Time (s): cpu = 00:00:00 ;
elapsed = 00:00:00.01 . Memory (MB): peak = 1349.484 ; gain =
0.000 ; free physical = 1084 ; free virtual = 31098
INFO: Launching helper process for spawning children vivado
processes
INFO: Helper process launched with PID 2723
---------------------------------------------------------------
---------------
Finished Constraint Validation : Time (s): cpu = 00:00:23 ;
elapsed = 00:00:23 . Memory (MB): peak = 1349.488 ; gain =
505.340 ; free physical = 1068 ; free virtual = 31082
---------------------------------------------------------------
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---------------------------------------------------------------
---------------
Start Loading Part and Timing Information
---------------------------------------------------------------
---------------
Loading part: xc7a35tcpg236-1
---------------------------------------------------------------
---------------
Finished Loading Part and Timing Information : Time (s): cpu =
00:00:23 ; elapsed = 00:00:23 . Memory (MB): peak = 1349.488 ;
gain = 505.340 ; free physical = 1068 ; free virtual = 31082
```

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---------------------------------------------------------------------
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---------------------------------------------------------------------
---------------
Start Applying 'set_property' XDC Constraints
---------------------------------------------------------------------
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---------------------------------------------------------------------
---------------
Finished applying 'set_property' XDC Constraints : Time (s): cpu
= 00:00:23 ; elapsed = 00:00:23 . Memory (MB): peak = 1349.488 ;
gain = 505.340 ; free physical = 1068 ; free virtual = 31082
---------------------------------------------------------------------
---------------
INFO: [Synth 8-5545] ROM "gen_clk" won't be mapped to RAM because
address size (29) is larger than maximum supported(25)
INFO: [Synth 8-5544] ROM "ACC" won't be mapped to Block RAM
because address size (3) smaller than threshold (5)
INFO: [Synth 8-5544] ROM "add_4" won't be mapped to Block RAM
because address size (3) smaller than threshold (5)
INFO: [Synth 8-5544] ROM "add_9" won't be mapped to Block RAM
because address size (3) smaller than threshold (5)
INFO: [Synth 8-5544] ROM "add_4_out" won't be mapped to Block RAM
because address size (2) smaller than threshold (5)
INFO: [Synth 8-5544] ROM "add_9_out" won't be mapped to Block RAM
because address size (2) smaller than threshold (5)
---------------------------------------------------------------------
---------------
Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:23 ;
elapsed = 00:00:23 . Memory (MB): peak = 1349.488 ; gain =
505.340 ; free physical = 1056 ; free virtual = 31070
---------------------------------------------------------------------
---------------

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
---------------------------------------------------------------------
---------------
Start RTL Component Statistics
---------------------------------------------------------------------
```

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---------------
Detailed RTL Component Info :
+---Adders :
       2 Input     29 Bit       Adders := 1
       2 Input      9 Bit       Adders := 1
       2 Input      5 Bit       Adders := 3
+---Registers :
                   29 Bit    Registers := 1
                    9 Bit    Registers := 2
                    5 Bit    Registers := 2
                    4 Bit    Registers := 1
                    3 Bit    Registers := 1
                    1 Bit    Registers := 1
+---Muxes :
       2 Input      9 Bit        Muxes := 5
       2 Input      5 Bit        Muxes := 8
      11 Input      5 Bit        Muxes := 1
       2 Input      4 Bit        Muxes := 1
       2 Input      3 Bit        Muxes := 2
      11 Input      3 Bit        Muxes := 1
       2 Input      2 Bit        Muxes := 1
      11 Input      2 Bit        Muxes := 1
      11 Input      1 Bit        Muxes := 2
       2 Input      1 Bit        Muxes := 4
---------------------------------------------------------------
---------------
Finished RTL Component Statistics
---------------------------------------------------------------
---------------
---------------------------------------------------------------
---------------
Start RTL Hierarchical Component Statistics
---------------------------------------------------------------
---------------
Hierarchical RTL Component report
Module clock_divider
Detailed RTL Component Info :
+---Adders :
       2 Input     29 Bit       Adders := 1
+---Registers :
                   29 Bit    Registers := 1
                    1 Bit    Registers := 1
Module Product_Sum
```

```
Detailed RTL Component Info :
+---Adders :
       2 Input      9 Bit       Adders := 1
       2 Input      5 Bit       Adders := 3
+---Registers :
                    9 Bit    Registers := 2
                    5 Bit    Registers := 2
                    4 Bit    Registers := 1
                    3 Bit    Registers := 1
+---Muxes :
       2 Input      9 Bit        Muxes := 5
       2 Input      5 Bit        Muxes := 8
      11 Input      5 Bit        Muxes := 1
       2 Input      4 Bit        Muxes := 1
       2 Input      3 Bit        Muxes := 2
      11 Input      3 Bit        Muxes := 1
       2 Input      2 Bit        Muxes := 1
      11 Input      2 Bit        Muxes := 1
      11 Input      1 Bit        Muxes := 2
       2 Input      1 Bit        Muxes := 4
---------------------------------------------------------------
---------------
Finished RTL Hierarchical Component Statistics
---------------------------------------------------------------
---------------
---------------------------------------------------------------
---------------
Start Part Resource Summary
---------------------------------------------------------------
---------------
Part Resources:
DSPs: 90 (col length:60)
BRAMs: 100 (col length: RAMB18 60 RAMB36 30)
---------------------------------------------------------------
---------------
Finished Part Resource Summary
---------------------------------------------------------------
---------------
Start Parallel Synthesis Optimization  : Time (s): cpu = 00:00:23
; elapsed = 00:00:24 . Memory (MB): peak = 1349.492 ; gain =
505.344 ; free physical = 1056 ; free virtual = 31070
---------------------------------------------------------------
---------------
```

```
Start Cross Boundary Optimization
---------------------------------------------------------------------
---------------
INFO: [Synth 8-5544] ROM "Arbitrary_Name/ACC" won't be mapped to
Block RAM because address size (3) smaller than threshold (5)
INFO: [Synth 8-5545] ROM "clock_div_inst/gen_clk" won't be mapped
to RAM because address size (29) is larger than maximum
supported(25)
---------------------------------------------------------------------
---------------
Finished Cross Boundary Optimization : Time (s): cpu = 00:00:24 ;
elapsed = 00:00:24 . Memory (MB): peak = 1349.492 ; gain =
505.344 ; free physical = 1058 ; free virtual = 31072
---------------------------------------------------------------------
---------------
Finished Parallel Reinference  : Time (s): cpu = 00:00:24 ;
elapsed = 00:00:24 . Memory (MB): peak = 1349.492 ; gain =
505.344 ; free physical = 1058 ; free virtual = 31072

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
---------------------------------------------------------------------
---------------
Start Area Optimization
---------------------------------------------------------------------
---------------
WARNING: [Synth 8-3332] Sequential element
(\Arbitrary_Name/State_reg[4]_P ) is unused and will be removed
from module Top.
WARNING: [Synth 8-3332] Sequential element
(\Arbitrary_Name/State_reg[3]_P ) is unused and will be removed
from module Top.
WARNING: [Synth 8-3332] Sequential element
(\Arbitrary_Name/State_reg[2]_P ) is unused and will be removed
from module Top.
WARNING: [Synth 8-3332] Sequential element
(\Arbitrary_Name/State_reg[1]_P ) is unused and will be removed
from module Top.
WARNING: [Synth 8-3332] Sequential element
(\Arbitrary_Name/State_reg[0]_P ) is unused and will be removed
```

```
from module Top.
------------------------------------------------------------------------
---------------
Finished Area Optimization : Time (s): cpu = 00:00:25 ; elapsed =
00:00:25 . Memory (MB): peak = 1349.492 ; gain = 505.344 ; free
physical = 1049 ; free virtual = 31063
------------------------------------------------------------------------
---------------
Finished Parallel Area Optimization  : Time (s): cpu = 00:00:25 ;
elapsed = 00:00:25 . Memory (MB): peak = 1349.492 ; gain =
505.344 ; free physical = 1049 ; free virtual = 31063

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
------------------------------------------------------------------------
---------------
Start Timing Optimization
------------------------------------------------------------------------
---------------
------------------------------------------------------------------------
---------------
Start Applying XDC Timing Constraints
------------------------------------------------------------------------
---------------
------------------------------------------------------------------------
---------------
Finished Applying XDC Timing Constraints : Time (s): cpu =
00:00:38 ; elapsed = 00:00:38 . Memory (MB): peak = 1349.492 ;
gain = 505.344 ; free physical = 1063 ; free virtual = 31077
------------------------------------------------------------------------
---------------
------------------------------------------------------------------------
---------------
Finished Timing Optimization : Time (s): cpu = 00:00:38 ; elapsed
= 00:00:38 . Memory (MB): peak = 1349.492 ; gain = 505.344 ; free
physical = 1066 ; free virtual = 31076
------------------------------------------------------------------------
---------------

Report RTL Partitions:
```

```
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
-------------------------------------------------------------------
---------------
Start Technology Mapping
-------------------------------------------------------------------
---------------
-------------------------------------------------------------------
---------------
Finished Technology Mapping : Time (s): cpu = 00:00:38 ; elapsed
= 00:00:38 . Memory (MB): peak = 1349.492 ; gain = 505.344 ; free
physical = 1066 ; free virtual = 31076
-------------------------------------------------------------------
---------------
Finished Parallel Technology Mapping Optimization  : Time (s):
cpu = 00:00:38 ; elapsed = 00:00:38 . Memory (MB): peak =
1349.492 ; gain = 505.344 ; free physical = 1066 ; free virtual =
31076

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
Finished Parallel Synthesis Optimization  : Time (s): cpu =
00:00:38 ; elapsed = 00:00:38 . Memory (MB): peak = 1349.492 ;
gain = 505.344 ; free physical = 1066 ; free virtual = 31076
-------------------------------------------------------------------
---------------
Start IO Insertion
-------------------------------------------------------------------
---------------
-------------------------------------------------------------------
---------------
Start Flattening Before IO Insertion
-------------------------------------------------------------------
---------------
-------------------------------------------------------------------
---------------
Finished Flattening Before IO Insertion
-------------------------------------------------------------------
```

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------------------------------------------------------------
---------------
Start Final Netlist Cleanup
------------------------------------------------------------
---------------
------------------------------------------------------------
---------------
Finished Final Netlist Cleanup
------------------------------------------------------------
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------------------------------------------------------------
---------------
Finished IO Insertion : Time (s): cpu = 00:00:39 ; elapsed =
00:00:39 . Memory (MB): peak = 1349.492 ; gain = 505.344 ; free
physical = 1066 ; free virtual = 31076
------------------------------------------------------------
---------------

Report Check Netlist:
+------+-----------------+-------+---------+-------+-----------
------+
|      |Item             |Errors |Warnings |Status |Description
     |
+------+-----------------+-------+---------+-------+-----------
------+
|1     |multi_driven_nets |      0|        0|Passed |Multi driven
nets |
+------+-----------------+-------+---------+-------+-----------
------+
------------------------------------------------------------
---------------
Start Renaming Generated Instances
------------------------------------------------------------
---------------
------------------------------------------------------------
---------------
Finished Renaming Generated Instances : Time (s): cpu = 00:00:39
; elapsed = 00:00:39 . Memory (MB): peak = 1349.492 ; gain =
505.344 ; free physical = 1066 ; free virtual = 31076
------------------------------------------------------------
---------------
```

```
Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
-------------------------------------------------------------------
---------------
Start Rebuilding User Hierarchy
-------------------------------------------------------------------
---------------
-------------------------------------------------------------------
---------------
Finished Rebuilding User Hierarchy : Time (s): cpu = 00:00:39 ;
elapsed = 00:00:39 . Memory (MB): peak = 1349.492 ; gain =
505.344 ; free physical = 1066 ; free virtual = 31076
-------------------------------------------------------------------
---------------
-------------------------------------------------------------------
---------------
Start Renaming Generated Ports
-------------------------------------------------------------------
---------------
-------------------------------------------------------------------
---------------
Finished Renaming Generated Ports : Time (s): cpu = 00:00:39 ;
elapsed = 00:00:39 . Memory (MB): peak = 1349.492 ; gain =
505.344 ; free physical = 1066 ; free virtual = 31076
-------------------------------------------------------------------
---------------
-------------------------------------------------------------------
---------------
Start Handling Custom Attributes
-------------------------------------------------------------------
---------------
-------------------------------------------------------------------
---------------
Finished Handling Custom Attributes : Time (s): cpu = 00:00:39 ;
elapsed = 00:00:39 . Memory (MB): peak = 1349.492 ; gain =
505.344 ; free physical = 1062 ; free virtual = 31072
-------------------------------------------------------------------
---------------
-------------------------------------------------------------------
---------------
```

```
Start Renaming Generated Nets
---------------------------------------------------------------------
---------------
---------------------------------------------------------------------
---------------
Finished Renaming Generated Nets : Time (s): cpu = 00:00:39 ;
elapsed = 00:00:39 . Memory (MB): peak = 1349.492 ; gain =
505.344 ; free physical = 1062 ; free virtual = 31072
---------------------------------------------------------------------
---------------
---------------------------------------------------------------------
---------------
Start Writing Synthesis Report
---------------------------------------------------------------------
---------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-------+------+
|      |Cell   |Count |
+------+-------+------+
|1     |BUFG   |     2|
|2     |CARRY4 |    10|
|3     |LUT1   |    34|
|4     |LUT2   |     8|
|5     |LUT3   |     3|
|6     |LUT4   |    14|
|7     |LUT5   |    10|
|8     |LUT6   |    21|
|9     |FDCE   |    14|
|10    |FDRE   |    51|
|11    |IBUF   |    14|
|12    |OBUF   |    10|
+------+-------+------+

Report Instance Areas:
+------+-----------------+--------------+------+
|      |Instance         |Module        |Cells |
```

```
+------+-----------------+--------------+------+
|1     |top              |              |   191|
|2     |  Arbitrary_Name |Product_Sum   |    90|
|3     |  clock_div_inst |clock_divider |    75|
+------+-----------------+--------------+------+
------------------------------------------------------------------
---------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:39 ;
elapsed = 00:00:39 . Memory (MB): peak = 1349.492 ; gain =
505.344 ; free physical = 1062 ; free virtual = 31072
------------------------------------------------------------------
---------------
Synthesis finished with 0 errors, 0 critical warnings and 5
warnings.
Synthesis Optimization Runtime : Time (s): cpu = 00:00:30 ;
elapsed = 00:00:30 . Memory (MB): peak = 1349.492 ; gain =
100.387 ; free physical = 1074 ; free virtual = 31084
Synthesis Optimization Complete : Time (s): cpu = 00:00:39 ;
elapsed = 00:00:39 . Memory (MB): peak = 1349.492 ; gain =
505.344 ; free physical = 1074 ; free virtual = 31084
INFO: [Project 1-571] Translating synthesized netlist
INFO: [Netlist 29-17] Analyzing 24 Unisim elements for replacemen
INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU
seconds
INFO: [Project 1-570] Preparing netlist for logic optimization
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

INFO: [Common 17-83] Releasing license: Synthesis
28 Infos, 6 Warnings, 0 Critical Warnings and 0 Errors
encountered.
synth_design completed successfully
synth_design: Time (s): cpu = 00:00:37 ; elapsed = 00:00:37 .
Memory (MB): peak = 1349.492 ; gain = 434.008 ; free physical =
1074 ; free virtual = 31084
report_utilization: Time (s): cpu = 00:00:00.22 ; elapsed =
00:00:00.25 . Memory (MB): peak = 1381.504 ; gain = 0.000 ; free
physical = 1072 ; free virtual = 31082
INFO: [Common 17-206] Exiting Vivado at Tue May  3 09:50:45
2016...
```