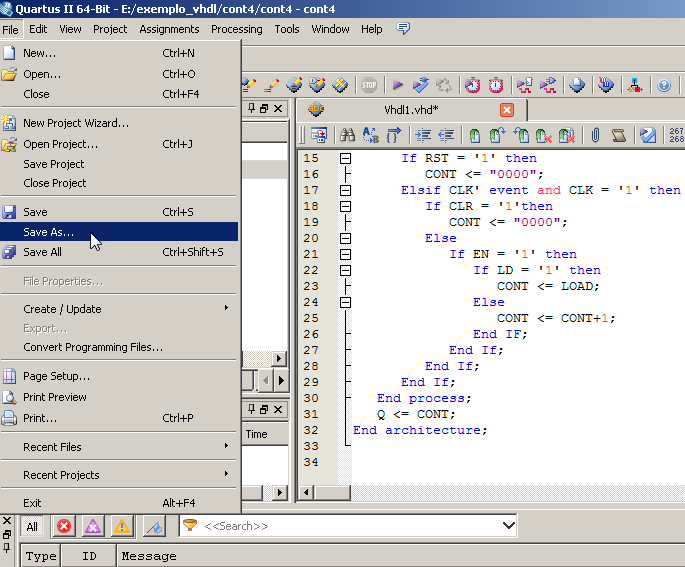
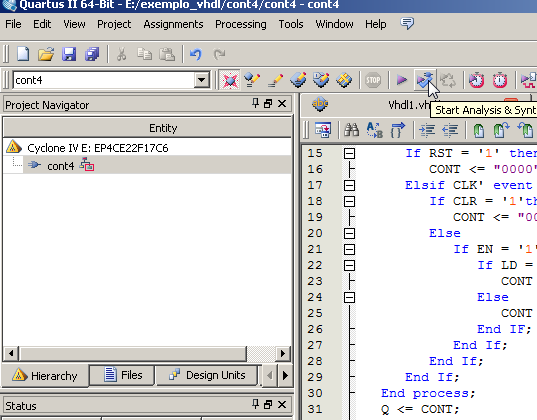


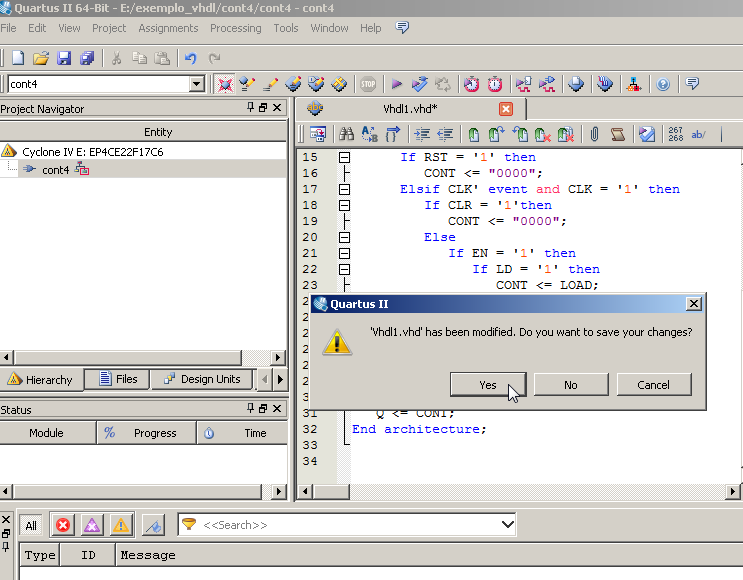
Copiar o código abaixo para o novo arquivo vhdl.

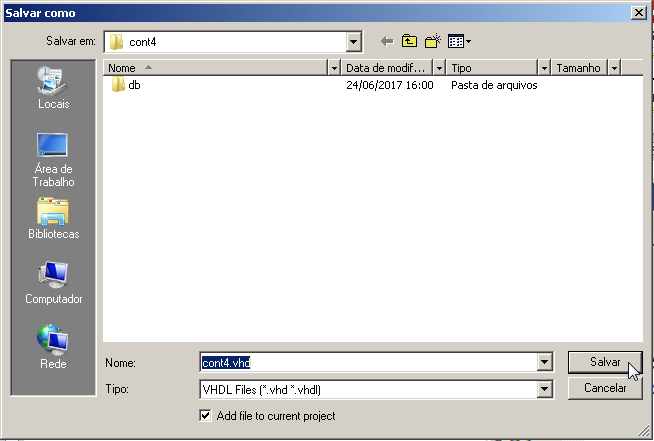
Library IEEE;  
use IEEE.std\_logic\_1164.all;  
use IEEE.numeric\_std.all;

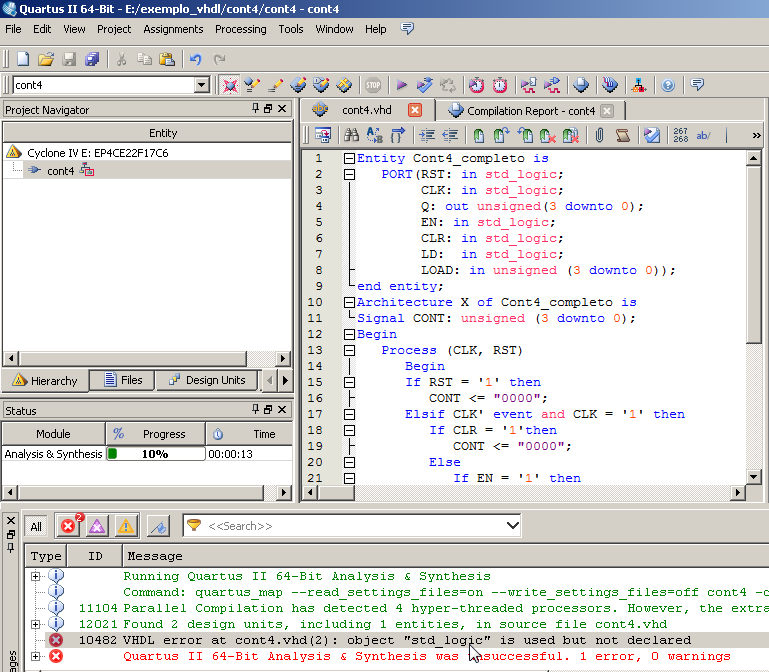
Entity Cont4\_completo is  
 PORT(RST: in std\_logic;  
 CLK: in std\_logic;  
 Q: out unsigned(3 downto 0);  
 EN: in std\_logic;  
 CLR: in std\_logic;  
 LD: in std\_logic;  
 LOAD: in unsigned (3 downto 0));  
end entity;   
Architecture X of Cont4\_completo is  
Signal CONT: unsigned (3 downto 0);  
Begin  
 Process (CLK, RST)  
 Begin  
 If RST = '1' then  
 CONT <= "0000";  
 Elsif CLK' event and CLK = '1' then  
 If CLR = '1'then  
 CONT <= "0000";  
 Else  
 If EN = '1' then  
 If LD = '1' then  
 CONT <= LOAD;  
 Else  
 CONT <= CONT+1;  
 End IF;  
 End If;  
 End If;  
 End If;  
 End process;  
 Q <= CONT;  
End architecture;





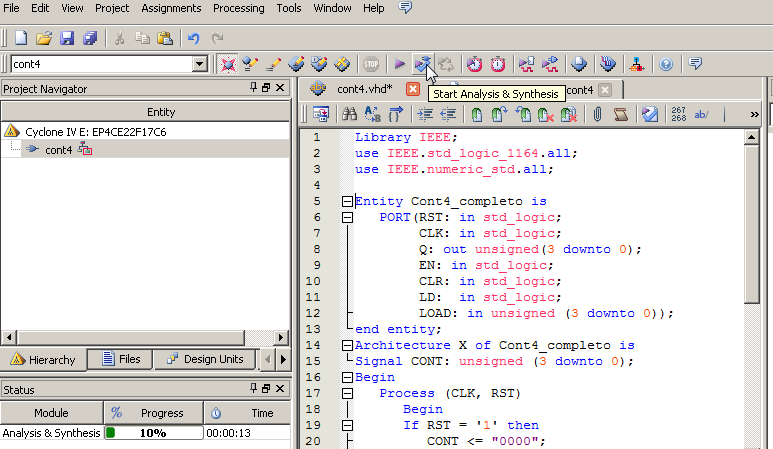


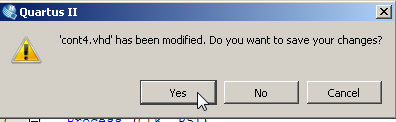


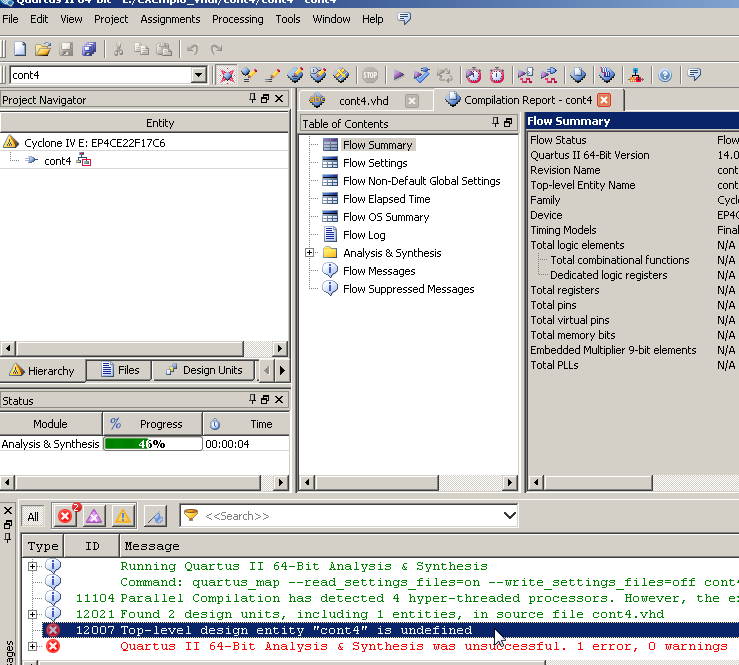


Faltaram as linhas relativas às bibliotecas

Library IEEE;  
use IEEE.std\_logic\_1164.all;  
use IEEE.numeric\_std.all;

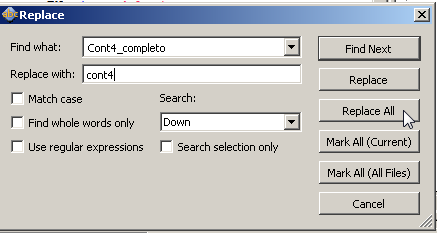


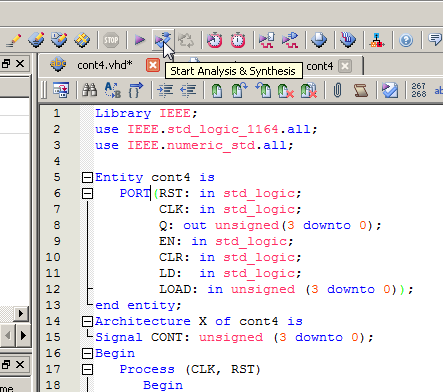


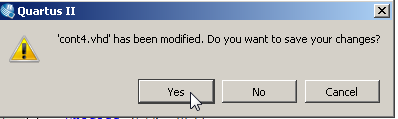


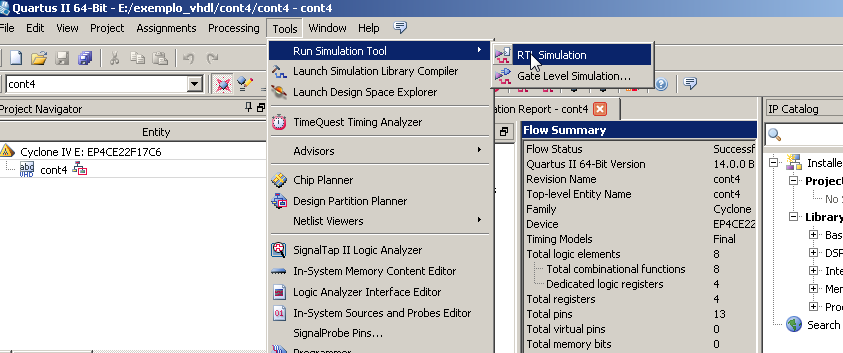
O problema é que o projeto chama-se “cont4”, mas a entidade e arquitetura chama-se “cont4\_completo”. Substituir e recompilar.

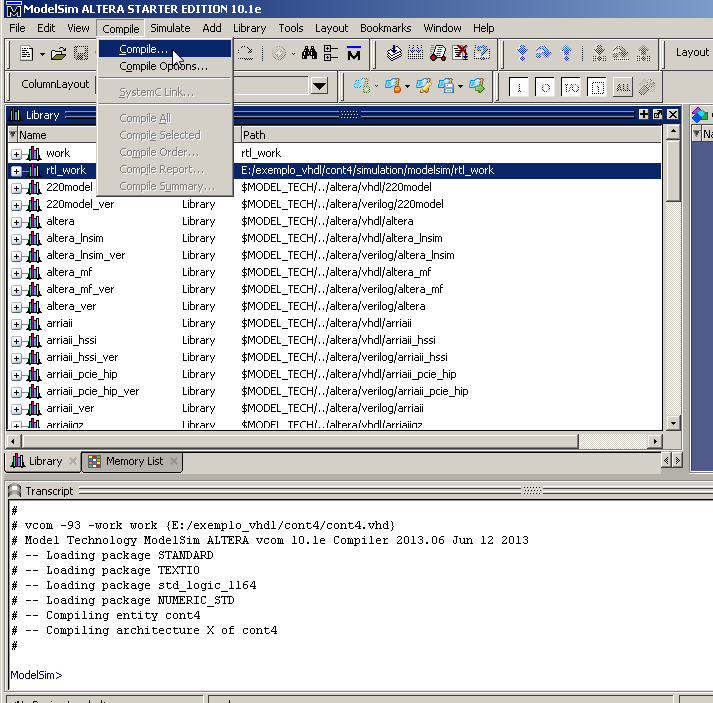
CONTROL H (replace)

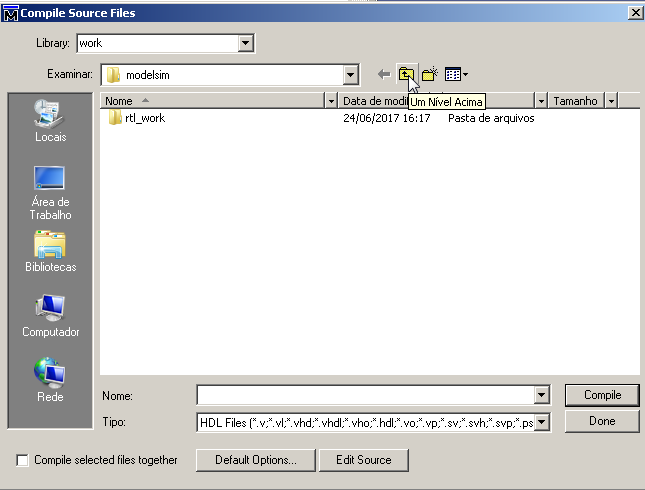


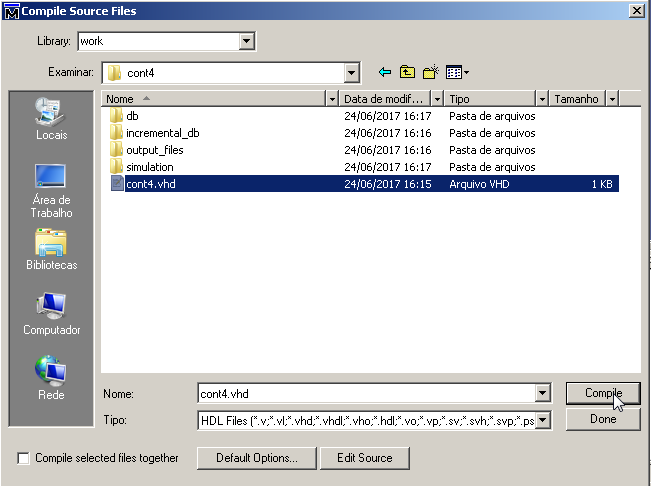


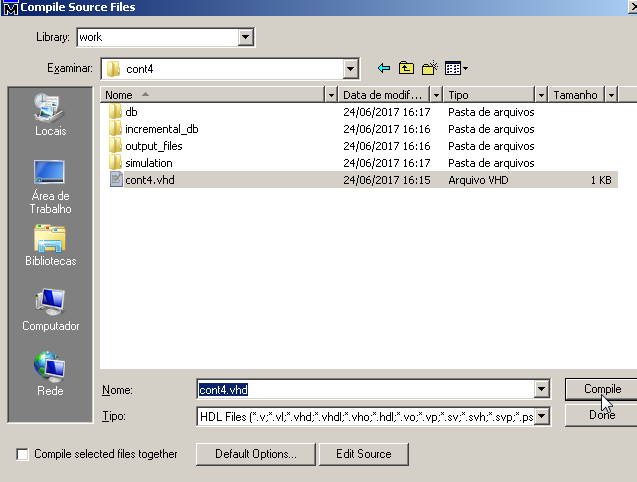


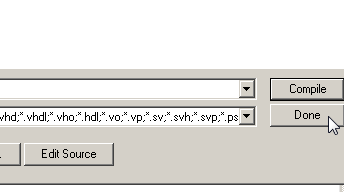


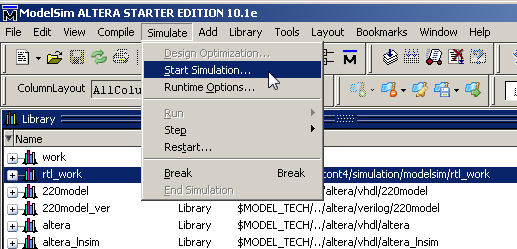


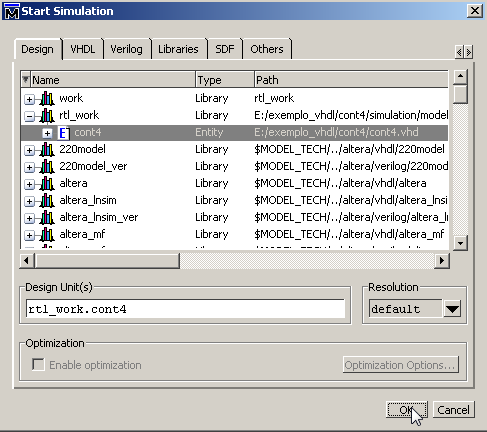


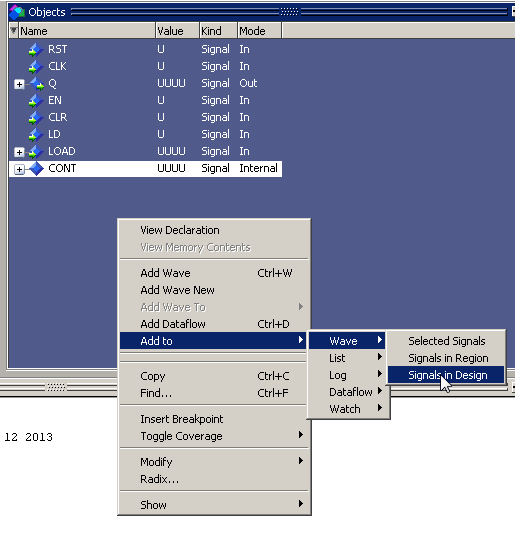


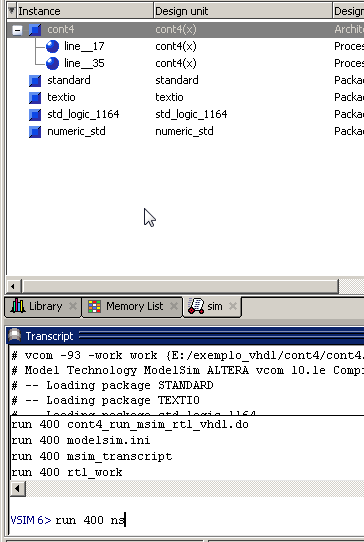


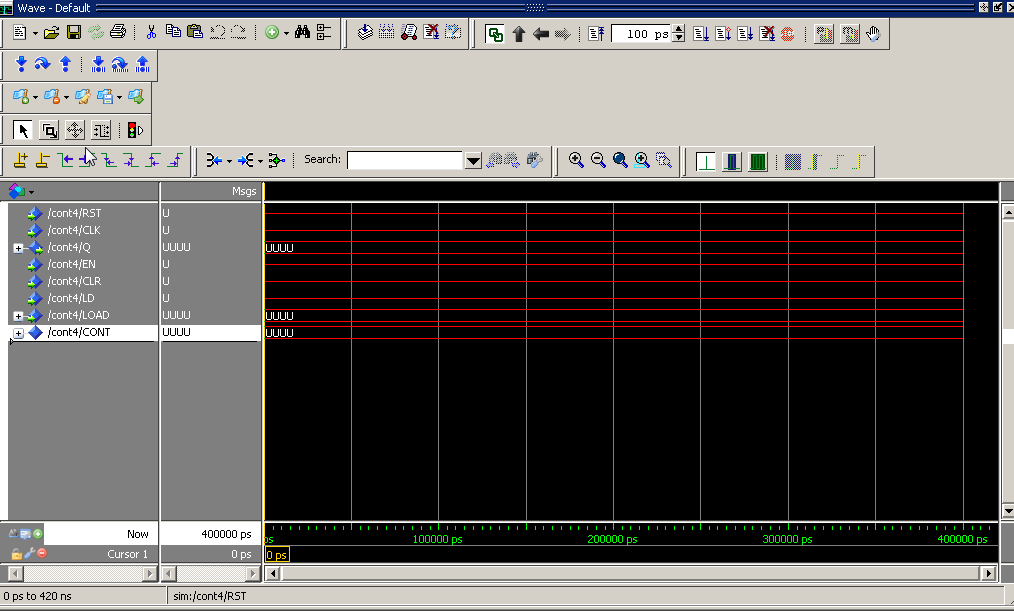




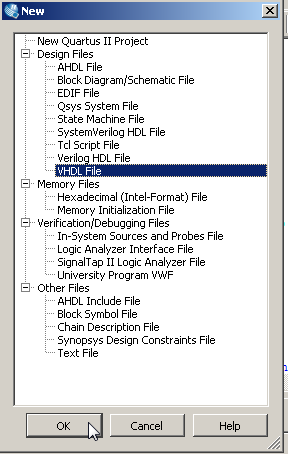


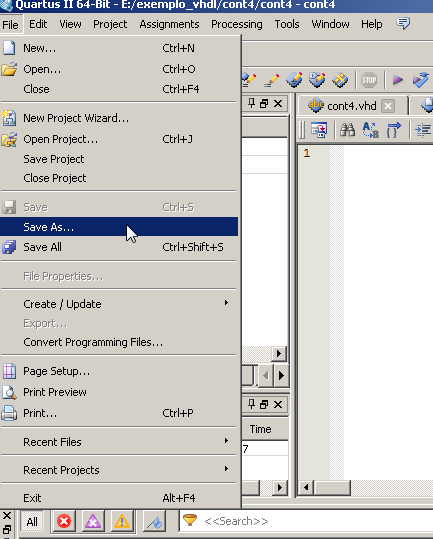






Construir o testbench





Salvar como cont4\_tb.vhd

Cabeçalho do arquivo

Library IEEE;  
use IEEE.std\_logic\_1164.all;  
use IEEE.numeric\_std.all;

Entity cont4\_tb is  
end entity;

architecture nome\_qualquer of cont4\_tb is

component cont4 is  
 PORT(RST: in std\_logic;  
 CLK: in std\_logic;  
 Q: out unsigned(3 downto 0);  
 EN: in std\_logic;  
 CLR: in std\_logic;  
 LD: in std\_logic;  
 LOAD: in unsigned (3 downto 0));  
end component;

begin  
 DUT: cont4  
 port map  
 (CLK => clk,  
 Q => Q,  
 EN => EN,  
 CLR=> clr  
 LD => ld  
 LOAD:load);

process  
 begin  
 clk <= ‘0’;  
 wait for 15 ns;  
 clk <= ‘1’;  
 wait for 15 ns;  
 end process;   
end architecture;

