Team

06 October 2014 16:10

Progress

No.	Function	Comment	Schematic	Comment	People	Layout	Comment	People
1	Inverter		Done			Done		
2	Ring oscillator	7.7MHz	Done	7.73MHz	cc6g11, jm15g13	Done	7.76MHz	ss4g13
3	4-bit adder		Done	V1.0	ss4g13	Done	V1.0	ss4g13
4	Sequence recogniser	11100101	Done	V2.0	yz39g13, jm15g13	Done	V1.0	jm15g13
5.1	Hamming encoder		Done	V1.0	yz39g13	Done	V1.0	ss4g13, jm15g13
5.2	Hamming decoder		Done	V2.0	yz39g13	Done	V2.0	yz39g13, ss4g13
Full	Full chip integration		Done	V1.0	yz39g13	Done	V1.0	yz39g13

Timeline

ID	Time	Type	Comment
cc6g11	06/10	Schematic	Finished ring oscillator
yz39g13	06/10	Schematic	Finished sequence recogniser
yz39g13	07/10	Schematic	Updated sequence recogniser by a mistake spotted by jm15g13
jm15g13	07/10	Schematic	Adjusted ring oscillator for new OrCAD library
yz39g13	07/10	Schematic	Finished shift register, decoder ALU, decoder error corrector
ss4g13	08/10	Layout	Finished ring oscillator, 7.76MHz
ss4g13	08/10	Layout	Finished shift register for decoder
yz39g13	08/10	Schematic	Finished decoder state machine
yz39g13	08/10	Layout	Finished decoder ALU, decoder error corrector
ss4g13	08/10	Layout	Finished decoder state machine
jm15g13	08/10	Layout	Finished sequence recogniser, but failed on simulation
yz39g13	09/10	Schematic	Finished encoder
ss4g13	09/10	Layout	Finished encoder state machine
ss4g13	10/10	Both	Finished 4-bit adder
yz39g13	10/10	Layout	Finished decoder output buffer, combined decoder
jm15g13	10/10	Layout	Fixed sequence recogniser
yz39g13	10/10	Schematic	Finished decoder output buffer, combined decoder
jm15g13	11/10	Layout	Finished encoder
yz39g13	11/10	Both	Finished full chip integration, not simulated yet
yz39g13	13/10	Both	Finished full chip integration simulation
yz39g13	17/10	Both	Update decoder design so it will only need 8 cycles
yz39g13	18/10	Schematic	Tested by Il Bagatto and Il Matto
yz39g13	20/10	Both	Submitted
yz39g13	23/10	Schematic	Modified for submission

Team J

ID	Name	Or
yz39g13	Yubo Zhi	Norman
cc6g11	Christopher Carville	
yl3c11	Yushuo Liu	Jeremy
jm15g13	Jiuxi Meng	Clark
ss4g13	Shuai Shao	David
dh1g14	Diwen Hu	

Sequence recogniser

06 October 2014 19:10

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From <https://secure.ecs.soton.ac.uk/notes/elec2205/D2/current/html/D2_Specification_2014_v3.html>

Right	D	S2	S1	S0	S2'	S1'	S0'	MATCH'
	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	1	0
	0	0	0	1	0	0	0	0
1	1	0	0	1	0	1	0	0
	0	0	1	0	0	0	0	0
1	1	0	1	0	0	1	1	0
0	0	0	1	1	1	0	0	0
	1	0	1	1	0	1	1	0
0	0	1	0	0	1	0	1	0
	1	1	0	0	0	0	1	0
	0	1	0	1	0	0	0	0
1	1	1	0	1	1	1	0	0
0	0	1	1	0	1	1	1	0
	1	1	1	0	0	1	0	0
	0	1	1	1	0	0	0	0
1	1	1	1	1	0	0	1	1

*MATCH' is a D-type flip-flop buffer for MATCH signal

S0'

S1S0\DS2	00	01	11	10
00		1	1	1
01				
11			1	1
10		1		1

$S0' = \sim D \cdot S2 \cdot \sim S0 + D \cdot \sim S1 \cdot \sim S0 + D \cdot S1 \cdot S0 + D \cdot \sim S2 \cdot S1$

S1'

S1S0\DS2	00	01	11	10
00				
01			1	1
11				1
10		1	1	1

$S1' = D \cdot \sim S1 \cdot S0 + D \cdot \sim S2 \cdot S1 + S2 \cdot S1 \cdot \sim S0$

S2'

S1S0\DS2	00	01	11	10
00		1		
01			1	
11	1			
10		1		

$S2' = \sim D \cdot S2 \cdot \sim S1 \cdot \sim S0 + D \cdot S2 \cdot \sim S1 \cdot S0 + \sim D \cdot \sim S2 \cdot S1 \cdot S0 + \sim D \cdot S2 \cdot S1 \cdot \sim S0$

$MATCH' = D \cdot S2 \cdot S1 \cdot S0$

Hamming encoder

06 October 2014 00:24

Input	clk, n_reset, start, [3:0] in
Output	strobe, out

State transition

Start	S2	S1	S0	S2'	S1'	S0'	OUT'	eStrobe
0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	1	1	0
X	0	0	1	0	1	0	1	1
X	0	1	0	0	1	1	1	0
X	0	1	1	1	0	0	1	0
X	1	0	0	1	0	1	1	0
X	1	0	1	1	1	0	1	0
X	1	1	0	1	1	1	1	0
X	1	1	1	0	0	0	1	0

Data/Bin	Data/Dec	Code/Bin	Code/Hex
0000	0	00010101	15
0001	1	00000010	2
0010	2	01001001	49
0011	3	01011110	5E
0100	4	01100100	64
0101	5	01110011	73
0110	6	00111000	38
0111	7	00101111	2F
1000	8	11010000	D0
1001	9	11000111	C7
1010	10	10001100	8C
1011	11	10011011	9B
1100	12	10100001	A1
1101	13	10110110	B6
1110	14	11111101	FD
1111	15	11101010	EA

$$OUT' = D + S2 + S1 + S0$$
$$eStrobe = \sim S2 \cdot \sim S1 \cdot S0$$

S2'

S0\S2S1	00	01	11	10
0			1	1
1		1		1

$$S2' = S2 \cdot \sim S0 + S2 \cdot \sim S1 + \sim S2 \cdot S1 \cdot S0$$

S1'

S0\S2S1	00	01	11	10
0		1	1	
1	1			1

$$S1' = S1 \cdot \sim S0 + \sim S1 \cdot S0 = S0 \oplus S1$$

S0'

S1S0\DS2	00	01	11	10
00		1	1	1
01				
11				
10	1	1	1	1

$$S0' = S1 \cdot \sim S0 + D \cdot \sim S0 + S2 \cdot \sim S0$$

Algorithm

B7	D3
B6	$D1 \oplus D2 \oplus D3$
B5	D2
B4	$\overline{D0 \oplus D2 \oplus D1}$
B3	D1
B2	$\overline{D0 \oplus D1 \oplus D3}$
B1	D0
B0	$\overline{D0 \oplus D2 \oplus D3}$

S0\S2S1	00	01	11	10
0			1	
1	?	?	?	?

$$D10 = S2 \cdot S1$$

S0\S2S1	00	01	11	10
0		1		
1	?	?	?	?

$$D12 = \sim S2 \cdot S1$$

S0\S2S1	00	01	11	10
0				1
1	?	?	?	?

$$D13 = S2 \cdot \sim S1$$

Hamming encoder algorithm

06 October 2014 01:44

Truth table

Number	D3	D2	D1	D0	B0	B2	B4	B6
0	0	0	0	0	1	1	1	0
1	0	0	0	1	0	0	0	0
2	0	0	1	0	1	0	0	1
3	0	0	1	1	0	1	1	1
4	0	1	0	0	0	1	0	1
5	0	1	0	1	1	0	1	1
6	0	1	1	0	0	0	1	0
7	0	1	1	1	1	1	0	0
8	1	0	0	0	0	0	1	1
9	1	0	0	1	1	1	0	1
10	1	0	1	0	0	1	0	0
11	1	0	1	1	1	0	1	0
12	1	1	0	0	1	0	0	0
13	1	1	0	1	0	1	1	0
14	1	1	1	0	1	1	1	1
15	1	1	1	1	0	0	0	1

B0

D1D0\D3D2	00	01	11	10
00	1		1	
01		1		1
11		1		1
10	1		1	

Function

$out = \overline{D3} \cdot \overline{D2} \cdot \overline{D0} + \overline{D3} \cdot D2 \cdot D0 + D3 \cdot D2 \cdot \overline{D0} + D3 \cdot \overline{D2} \cdot D0$

$out = \overline{D3} \cdot (\overline{D2} \cdot \overline{D0} + D2 \cdot D0) + D3 \cdot (D2 \cdot \overline{D0} + \overline{D2} \cdot D0)$

$out = \overline{D3} \cdot \overline{(D2 \oplus D0)} + D3 \cdot (D2 \oplus D0)$

$out = \overline{D0 \oplus D2 \oplus D3}$

B2

D1D0\D3D2	00	01	11	10
00	1	1		
01			1	1
11	1	1		
10			1	1

Function

$out = \overline{D0 \oplus D1 \oplus D3}$

B4

D1D0\D3D2	00	01	11	10
00	1			1
01		1	1	
11	1			1
10		1	1	

Function

$out = \overline{D0 \oplus D1 \oplus D2}$

B6

D1D0\D3D2	00	01	11	10
00		1		1
01		1		1
11	1		1	
10	1		1	

Function

$out = D1 \oplus D2 \oplus D3$

Summary

B7	D3
B6	$D1 \oplus D2 \oplus D3$
B5	D2
B4	$\overline{D0 \oplus D1 \oplus D2}$
B3	D1
B2	$\overline{D0 \oplus D1 \oplus D3}$
B1	D0
B0	$\overline{D0 \oplus D2 \oplus D3}$

Hamming decoder

07 October 2014 21:30

State

dStrobe	S2	S1	S0	S2'	S1'	S0'	OUT_
0	0	0	0	0	0	0	0
1	0	0	0	0	0	1	0
X	0	0	1	0	1	0	0
X	0	1	0	0	1	1	0
X	0	1	1	1	0	0	0
X	1	0	0	1	0	1	0
X	1	0	1	1	1	0	0
X	1	1	0	1	1	1	0
X	1	1	1	0	0	0	1

S2'

S0\S2S1	00	01	11	10
0			1	1
1		1		1

$S2' = S2 \cdot {\sim}S0 + S2 \cdot {\sim}S1 + {\sim}S2 \cdot S1 \cdot S0$

S1'

S0\S2S1	00	01	11	10
0		1	1	
1	1			1

$S1' = S1 \cdot {\sim}S0 + {\sim}S1 \cdot S0 = S0 \oplus S1$

Valid check

AB\DC	00	01	11	10
00	1	1		
01	1	1		
11	1	1	1	
10	1	1		

$V = {\sim}D + ABCD$

$OUT = S2 \cdot S1 \cdot S0$

S0'

S1S0\DS2	00	01	11	10
00		1	1	1
01				
11				
10	1	1	1	1

$S0' = S1 \cdot {\sim}S0 + D \cdot {\sim}S0 + S2 \cdot {\sim}S0$