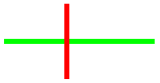
IC Design

- Transistors

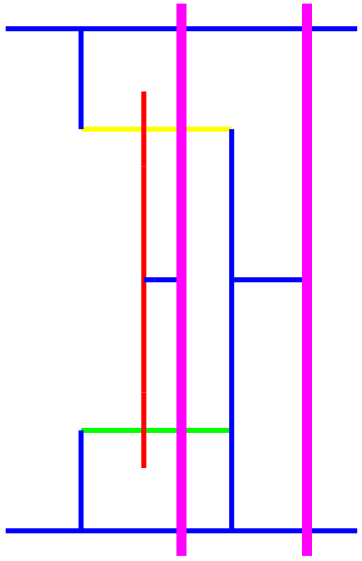


- PMOS and NMOS[1]

[1] see ELEC3221 IC Design notes for lots more detail

IC Design

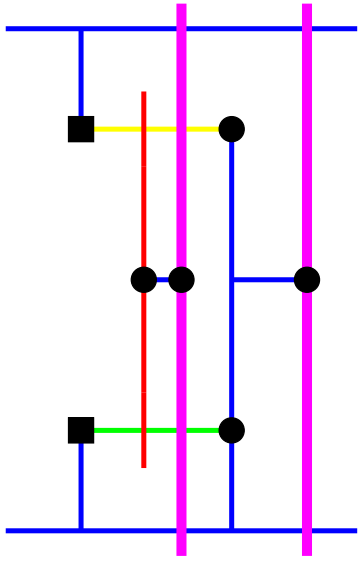
- Transistors
- Wiring



- Touching/crossing wires on the same metal layer connect
- Touching/crossing wires on the different metal layers do not connect

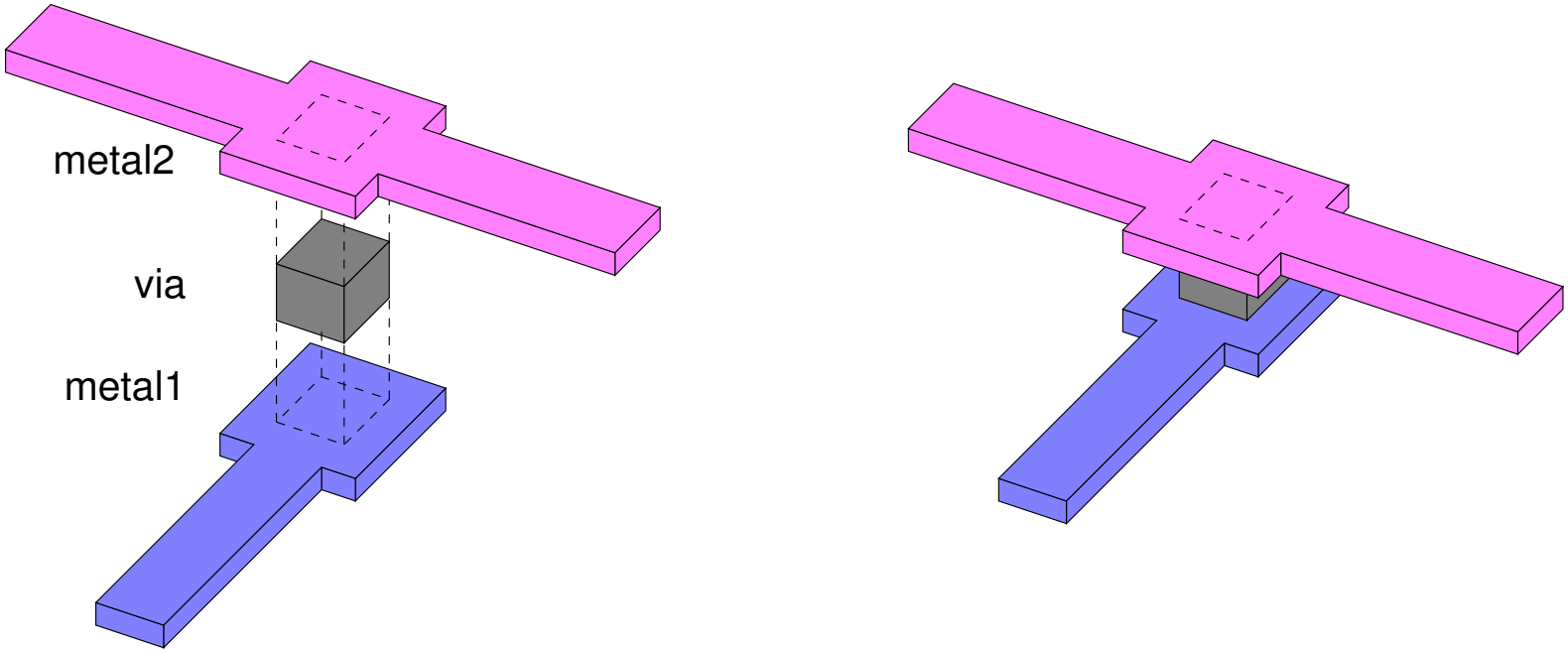
IC Design

- Transistors
- Wiring
- Contacts/Vias



- Connections may be explicitly added between adjacent layers
  e.g. metal1 and metal2

IC Design



- metal1 to metal2 connection is made with the addition of a via

IC Design

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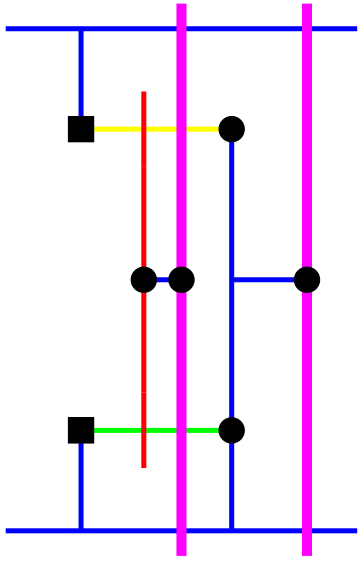
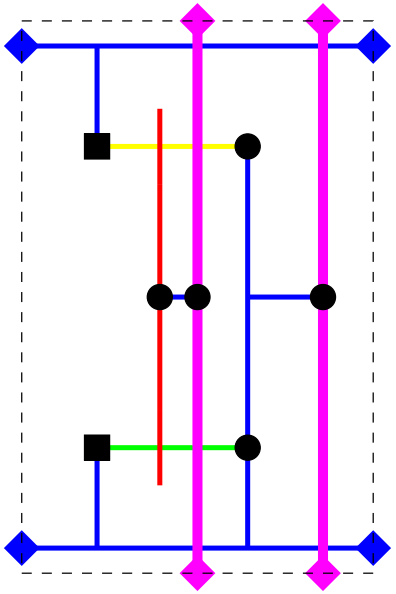
- Contacts/Vias



- Connections may be explicitly added between adjacent layers
  e.g. metal1 and metal2

IC Design - Hierarchy

- Transistors
- Wiring
- Contacts/Vias
- Ports

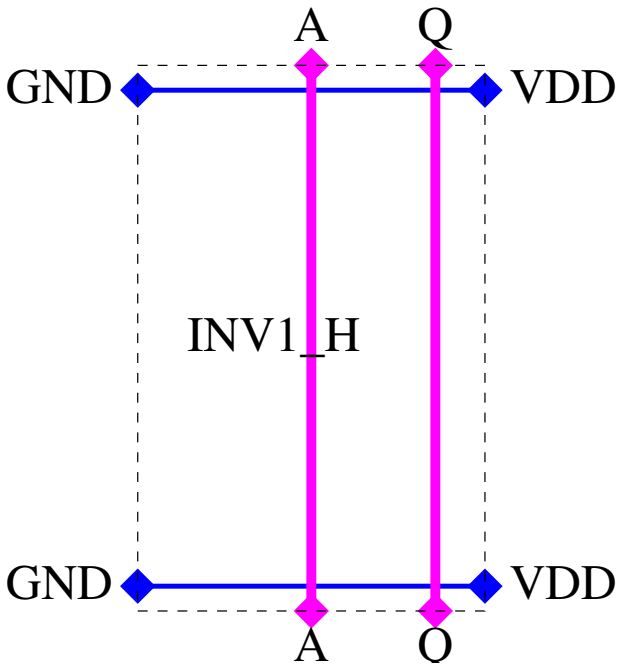


- The ports of a cell define where connections to the rest of the circuit can be made.[2]

[2]connections made to other parts of the cell and wires overlapping the cell boundary represent violations of hierarchy rules and can lead to unpredictable results

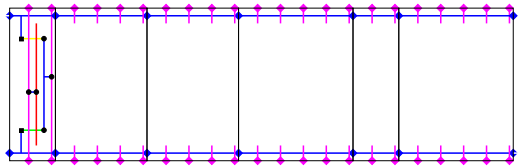
IC Design - Standard Cells

- Abstract View



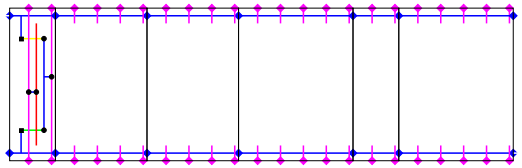
- Often the standard cell designers supply only an abstract (black box) view and a simulation model to the users of the standard cell library.

Placement



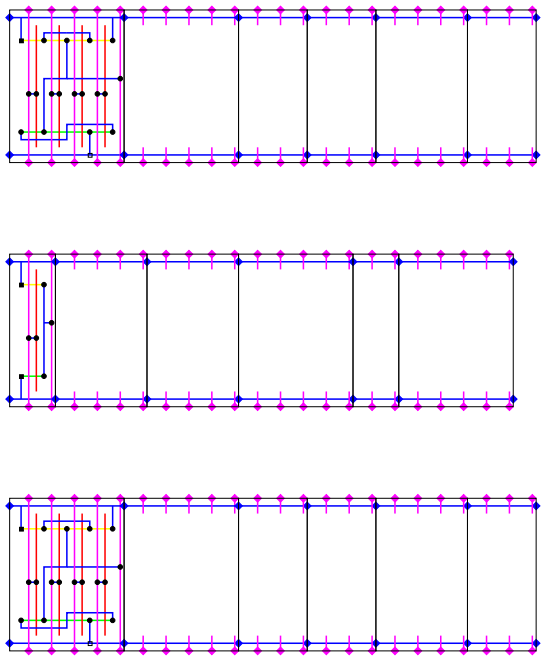
Butting of cells allows for easy routing of power and ground.

Placement



Cells are placed in one or several equal length lines.

Placement



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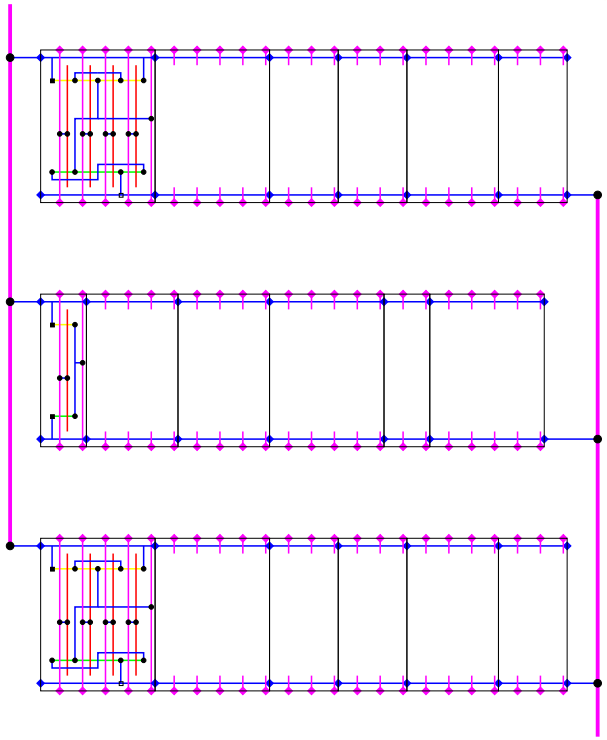
Placement



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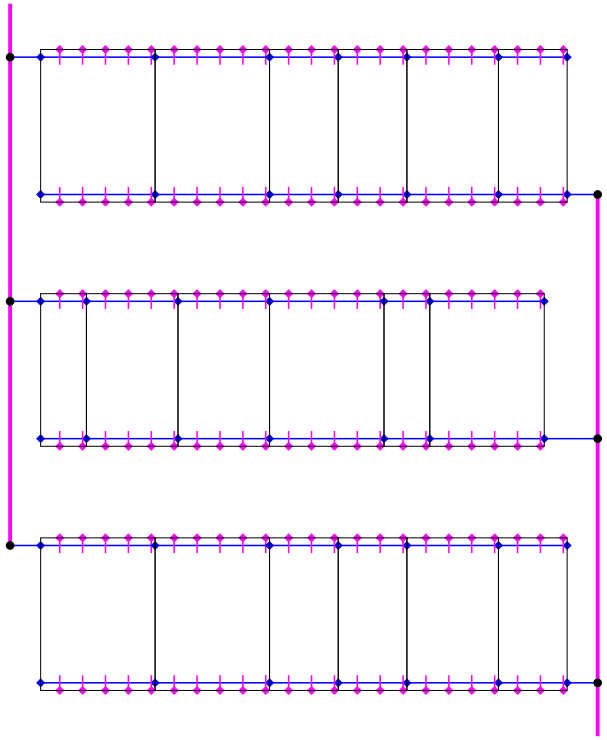
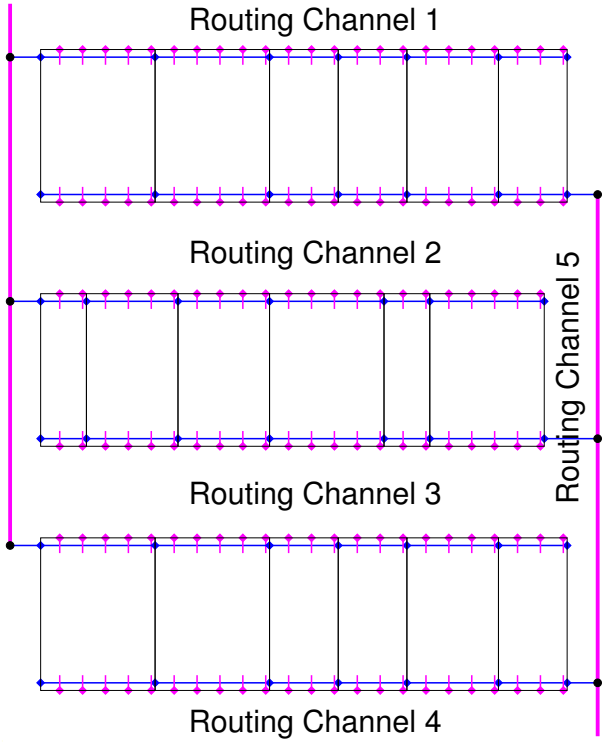
Routing



In the routing channels between the cells we route metal1 horizontally and metal2 vertically.

Routing



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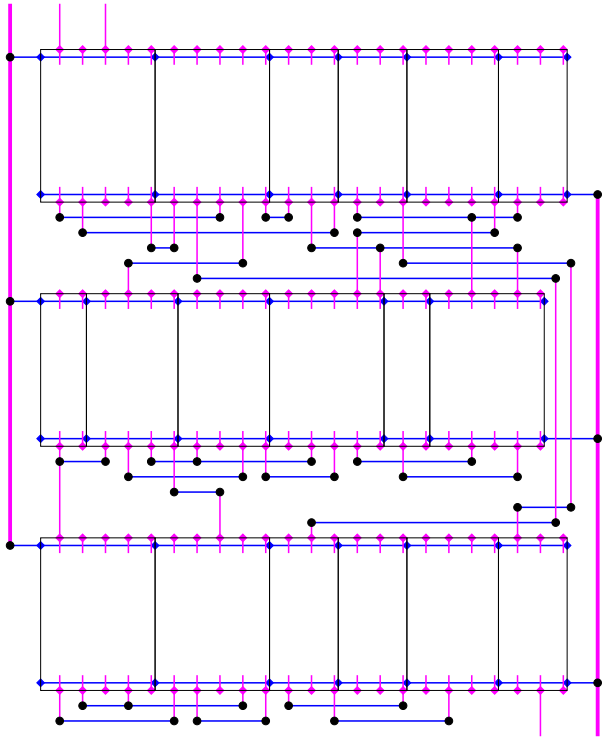

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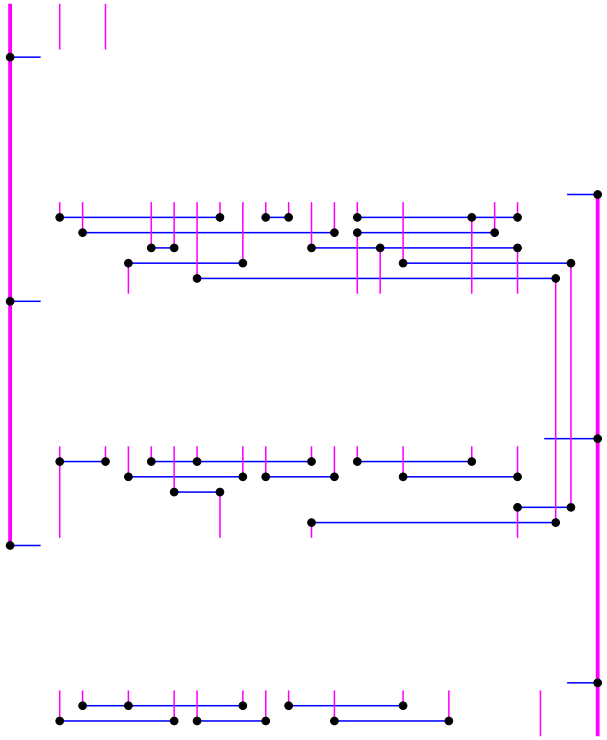

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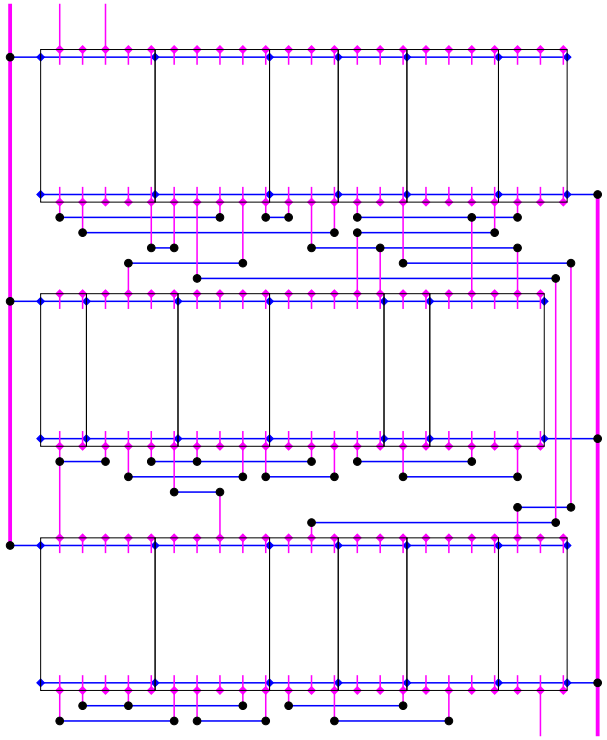

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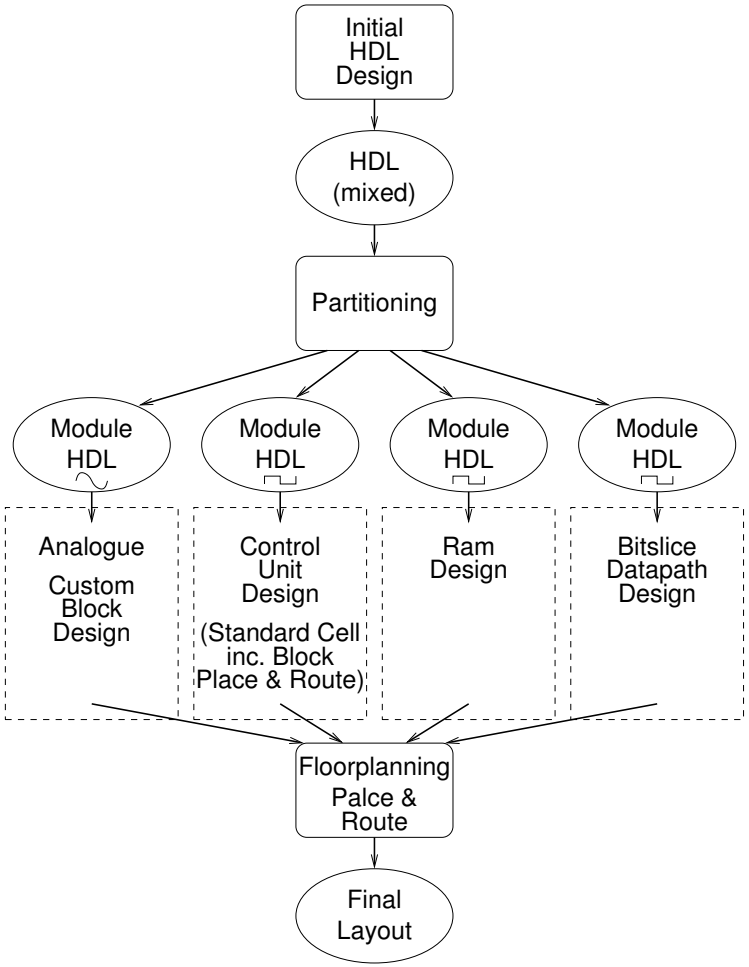
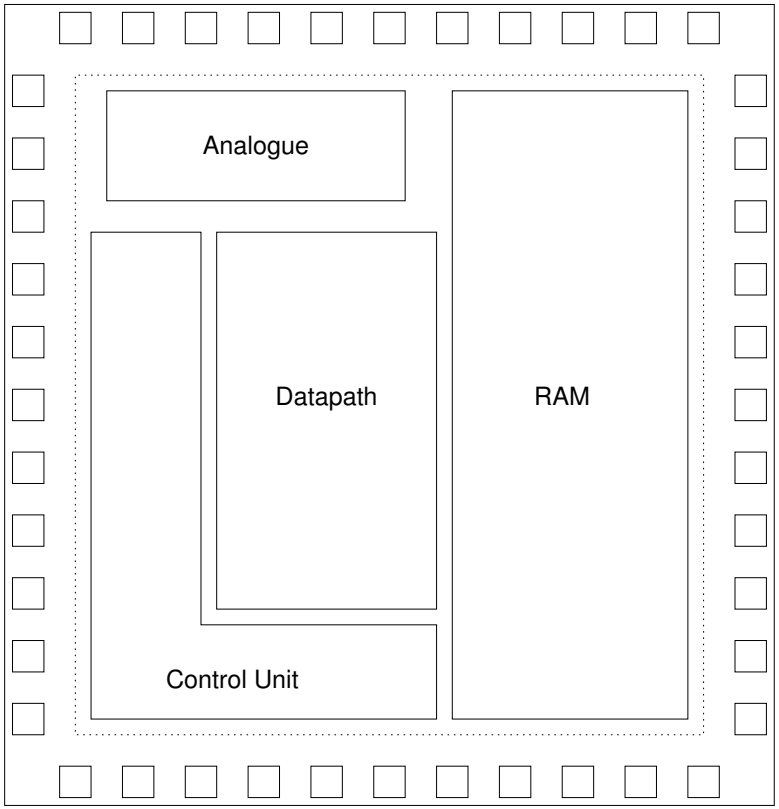
Full Chip Design within Flexible Pad Ring



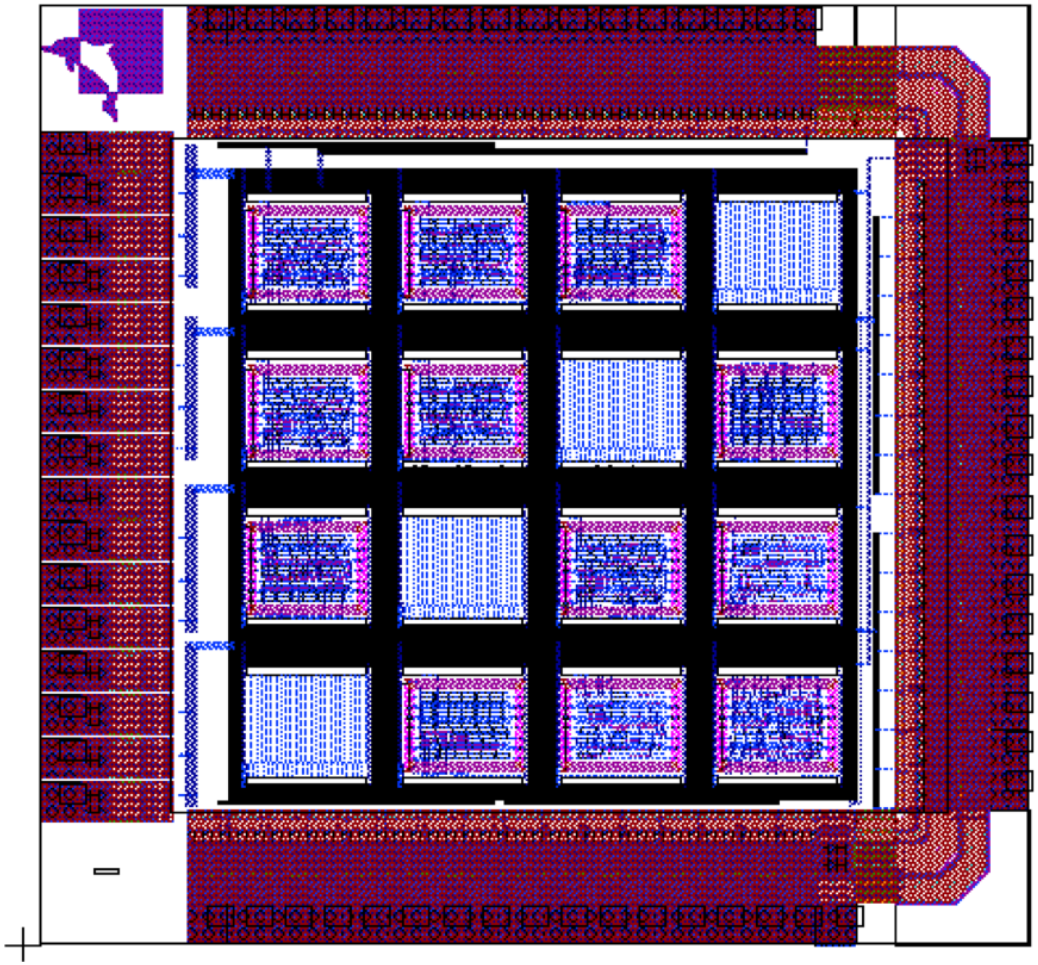


- Partitioning - Floor Planning

ECS SuperChip

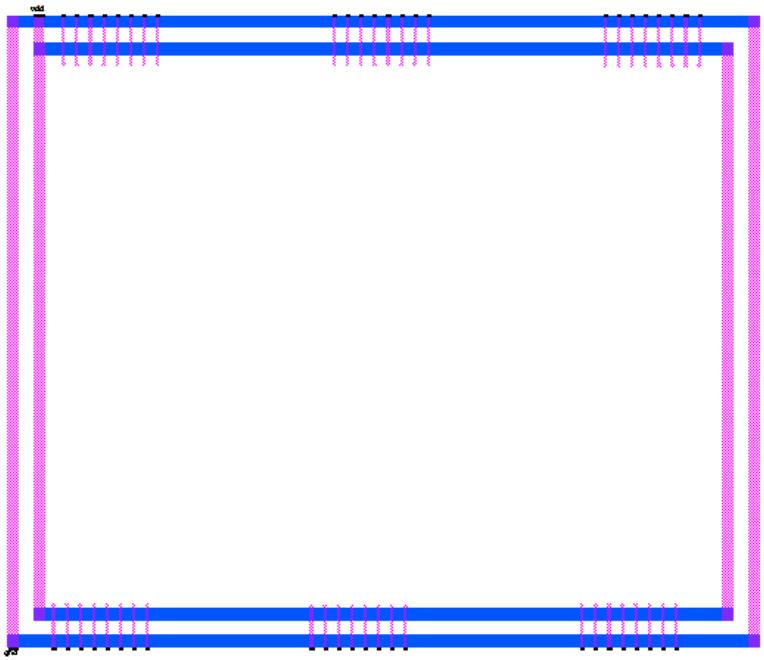
Die Size: 2.5mm $\times$ 2.4mm

Technology: AMS 0.35μm



- Multi-project chip with fixed area for each team.

ECS SuperChip Max Project Size: $250\mu m \times 200\mu m$ 16 Projects Per Chip



- Team design fits within "D2_DESIGN_IO" cell[3]
- Provides access to 24 inputs (A0-A23) at the top and 24 outputs (Q0-Q23) at the bottom

[3]only connections to the (inner) VDD ring or the (outer) GND ring may overlap the padring