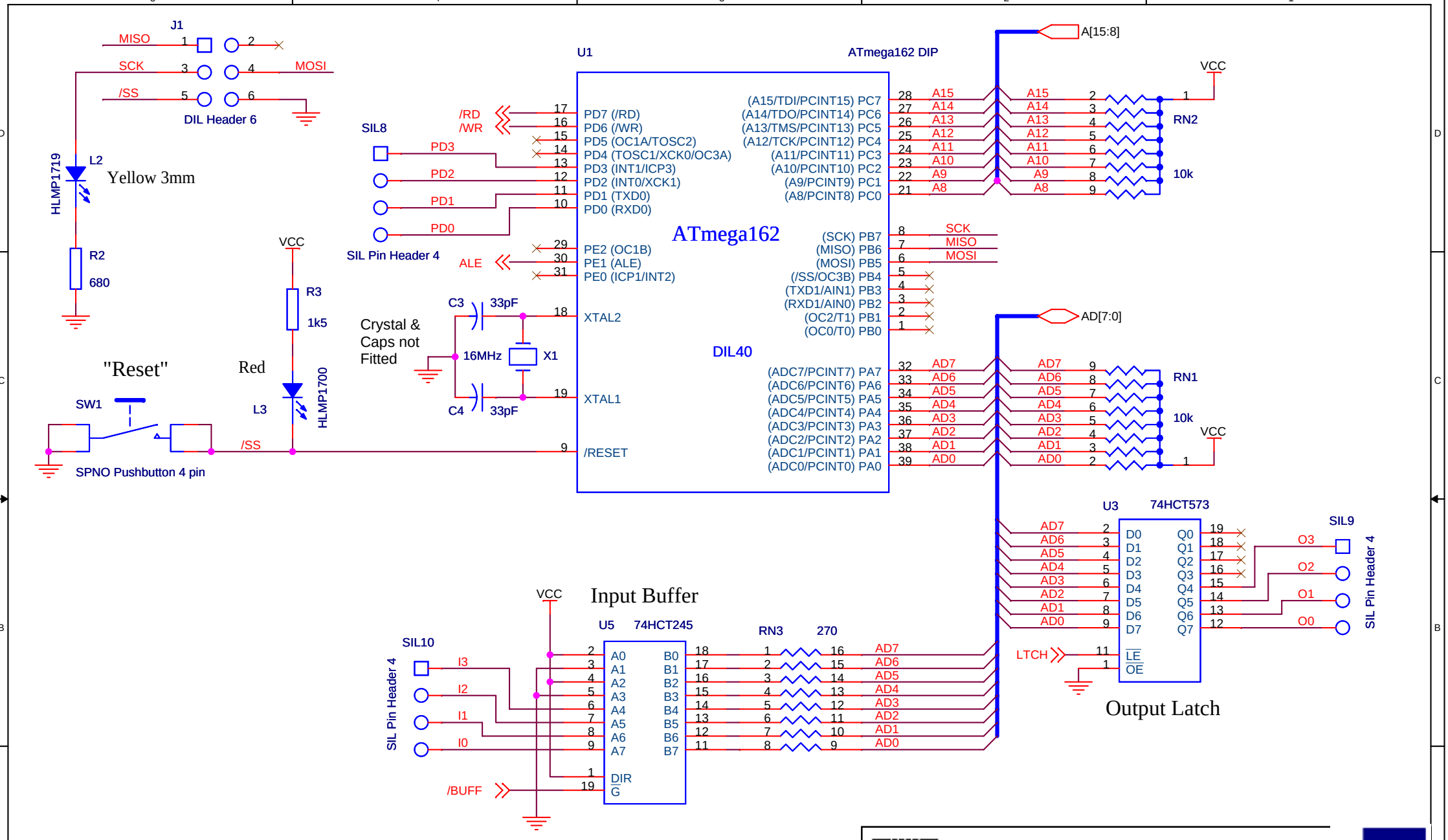

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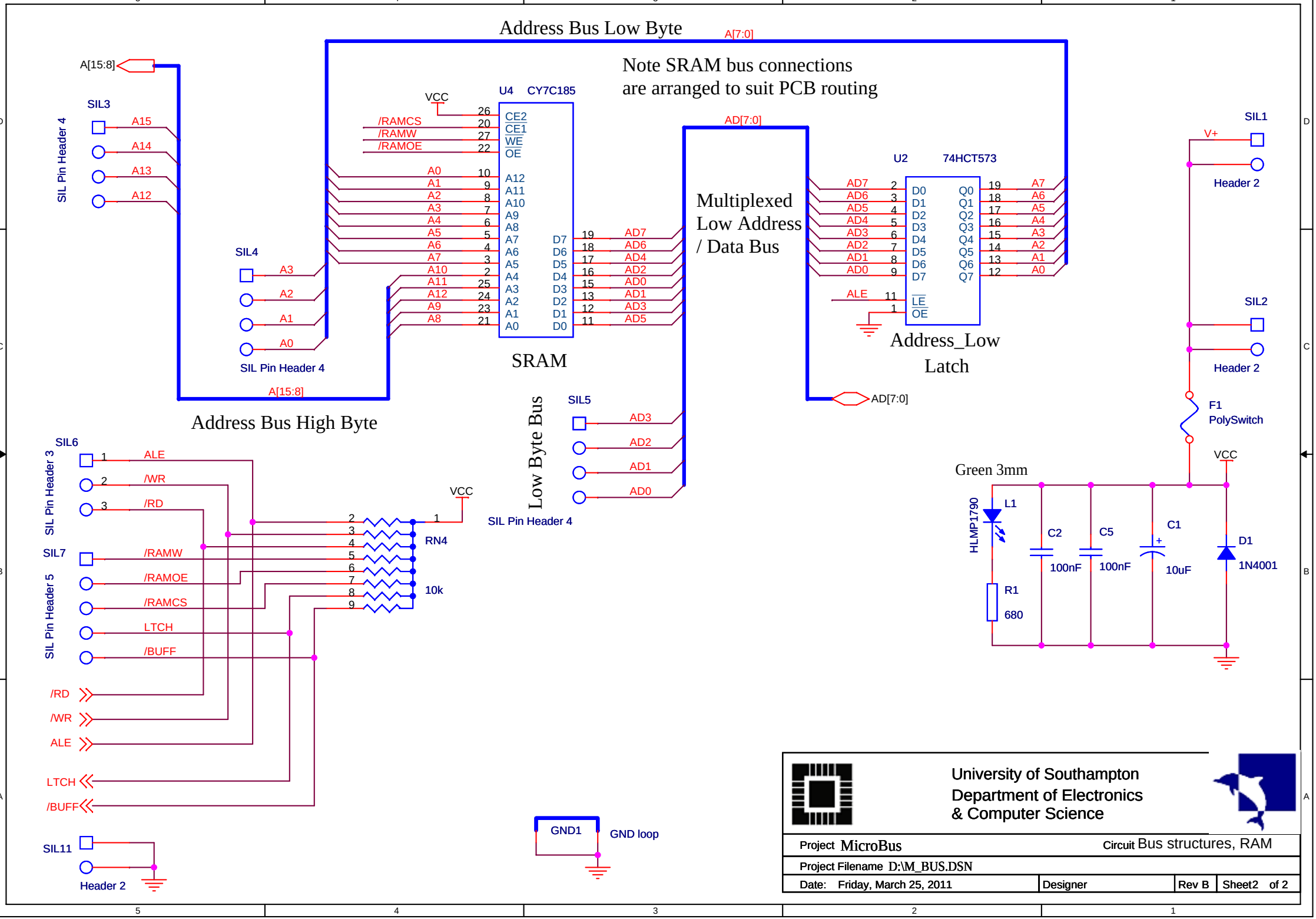
Project MicroBus		Circuit AVR, buffer, latch	
Project Filename D:\M_BUS.DSN			
Date: Friday, March 25, 2011	Designer	Rev B	Sheet1 of 1


Address Bus Low Byte
A[7:0]
Note SRAM bus connections
are arranged to suit PCB routing
A[15:8]
SIL3
SIL Pin Header 4
A15
A14
A13
A12
SIL4
A3
A2
A1
A0
SIL Pin Header 4
A[15:8]
Address Bus High Byte
VCC
U4 CY7C185
/RAMCS
/RAMW
/RAMOE
CE2
CE1
WE
OE
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
D7
D6
D5
D4
D3
D2
D1
D0
SRAM
AD[7:0]
Multiplexed
Low Address
/ Data Bus
Low Byte Bus
SIL5
AD3
AD2
AD1
AD0
SIL Pin Header 4
U2 74HCT573
D0
D1
D2
D3
D4
D5
D6
D7
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
LE
OE
ALE
Address_Low
Latch
AD[7:0]
SIL1
V+
Header 2
SIL2
Header 2
F1
PolySwitch
VCC
Green 3mm
HLMP1790
L1
R1
680
C2
100nF
C5
100nF
C1
10uF
D1
1N4001
SIL6
SIL Pin Header 3
ALE
/WR
/RD
SIL7
SIL Pin Header 5
/RAMW
/RAMOE
/RAMCS
LTCH
/BUFF
VCC
RN4
10k
/RD
/WR
ALE
LTCH
/BUFF
SIL11
Header 2
GND1
GND loop
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& Computer Science
Project MicroBus
Circuit Bus structures, RAM
Project Filename D:\M_BUS.DSN
Date: Friday, March 25, 2011
Designer
Rev B
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