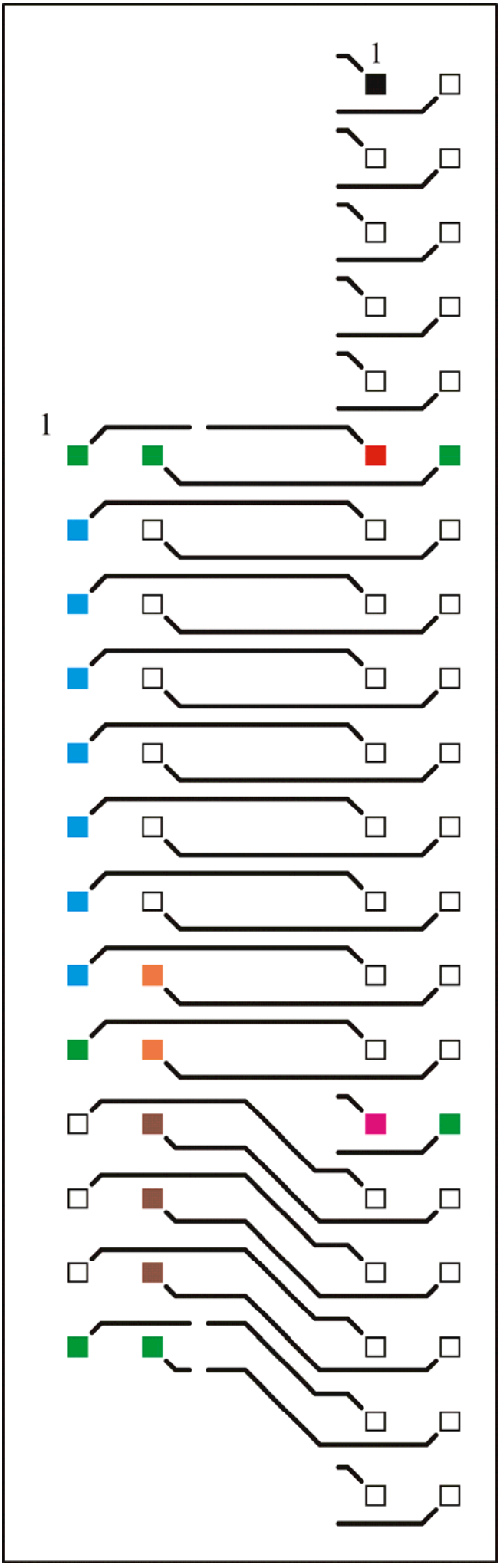
Connecting ECS lift to Terasic DE0 FPGA board

26 way connector pin	Lift signal	40 way connector pin	DE0 J4 signal	DE0 J5 signal
1	Gnd	-	-	-
2	Gnd	12	Gnd	Gnd
3	/Call0 (out)	13	GPIO0_D8	GPIO1_D8
4	-	14	GPIO0_D9	GPIO1_D9
5	/Call1 (out)	15	GPIO0_D10	GPIO1_D10
6	-	16	GPIO0_D11	GPIO1_D11
7	/Call2 (out)	17	GPIO0_D12	GPIO1_D12
8	-	18	GPIO0_D13	GPIO1_D13
9	/Bottom (out)	19	GPIO0_CLKOUT0	GPIO1_CLKOUT0
10	-	20	GPIO0_D14	GPIO1_D14
11	/Middle_minus (out)	21	GPIO0_CLKOUT1	GPIO1_CLKOUT1
12	-	22	GPIO0_D15	GPIO1_D15
13	/Middle_plus (out)	23	GPIO0_D16	GPIO1_D16
14	-	24	GPIO0_D17	GPIO1_D17
15	/Top (out)	25	GPIO0_D18	GPIO1_D18
16	Motor direction (in)	26	GPIO0_D19	GPIO1_D19
17	Gnd	27	GPIO0_D20	GPIO1_D20
18	Motor /enable (in)	28	GPIO0_D21	GPIO1_D21
19	-	31	GPIO0_D22	GPIO1_D22
20	/Indicator 2 (in)	32	GPIO0_D23	GPIO1_D23
21	-	33	GPIO0_D24	GPIO1_D24
22	/Indicator 1 (in)	34	GPIO0_D25	GPIO1_D25
23	-	35	GPIO0_D26	GPIO1_D26
24	/Indicator 0 (in)	36	GPIO0_D27	GPIO1_D27
25	Gnd	-	-	-
26	Gnd	-	-	-

The cable is constructed by fitting 40-way ribbon cable with a 40-way IDC line socket. Cores 1:10, 29:30 and 39:40 are cut of at the 40-way connector end, so that the remaining 26 cores can be fitted with a 26-way IDC latched header. Cores 11, 37 and 38 then have segments removed so that signals on 26-way pins 1, 25 and 26 are not connected through.

GPIOx_CLKOUTy pins need to be standard I/O, not PLL clock outputs. All used DE0 pins need to be suited to TTL-compatible 5V logic levels – this may mean setting outputs to be open-drain. Open-drain outputs will drive the lift indicator and motor /enable inputs correctly, but there is no pullup on the motor direction input, so this must have drive in the HI state sufficient to deliver a TTL-compatible HI.

Tim Forcer, 2009 November 23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