Multi-stage Amplifier Design

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Abstract: The objective of this exercise was to design a multi-stage amplifier with overall gain of 6. The amplifier contain two stages, a common emitter stage for amplify, followed by a common collector stage for reduce output impedance. The component values was first calculated by models and formulas, then verified and adjusted by simulation using LTspice. Finally the circuit had been built during the lab, with each stage and overall input impedance, output impedance, voltage gain evaluated. There were some differences in these values from simulation, but they all in the acceptable range, indicates the design was successful.

1. Introduction

Bipolar junction transistor amplifiers were used widely, but the gain of bipolar junction transistors was not controllable and the same across all transistors, therefore amplifier circuits like common emitter amplifier with emitter bias resistor which can produce controllable stable gain was introduced. In this exercise, a multi-stage amplifier was designed. The first stage, a common emitter stage is used for produce the required voltage gain of 6, and it has large input impedance. The second stage, a common collector stage, with a voltage gain of almost unity, works as an output buffer, effectively reduced the output impedance, enable the amplifier to drive more load without affect the gain. Large signal model and small signal model were used for gain, impedances and component value calculations. Then LTspice simulation tool was used for verify of component values, operation points, estimation of gain and bandwidth. Finally the circuit was been built in the laboratory, and operation point voltages, input impedance, output impedance, gain and bandwidth measured using digital multimeter and oscilloscope.

2. Basic design

The bipolar junction transistor (BJT) used in this exercise is BC547, with schematic described by Figure 1.

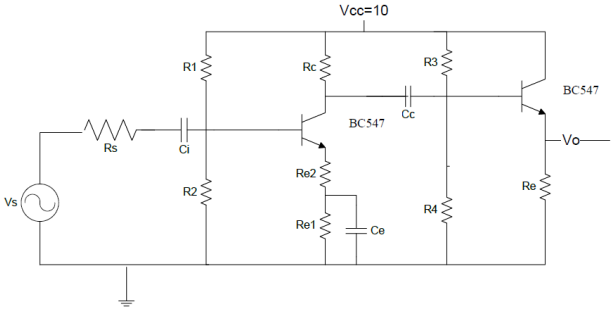

Figure 1: Overall schematic of the multi-stage amplifier (adapted from [1])

The transistor has a gain of 200. V_s and R_s modelled the input signal and source impedance, C_i is the input coupling capacitor, together with bias resistors R_1, R_2, R_e1, R_e2, load resistor R_c, emitter decoupling capacitor C_e, output coupling capacitor C_c and transistor 1 created the first stage. Bias resistors R_3, R_4, R_e and transistor 2 created the second stage.

3. Second stage design

The common collector stage was designed first.

3.1 Choose collector current

Equation (1) from basic characteristic of BJTs states for a smaller collector current, base current would also be smaller. And the base current should not affect the base voltage bias, as in relationship (8), R_3 and R_4 can be bigger for smaller base current, results in a larger input impedance. Therefore a small collector current of about $1mA$ should be appropriate.

$$I_c = \beta I_b \tag{1}$$

$$I_{R_{3,4}} \gg I_{b2} \tag{2}$$

3.2 Determine output quiescent point

From basic equation (3) of BJTs, for a small I_b, I_e was approximately the same as I_c.

$$I_e = I_c + I_b = (1+\beta) I_b \tag{3}$$

As show in the schematic Figure 1, using KVL, R_e is related to I_{c2} by equation (4).

$$V_{cc} = V_{CE2} + I_{e2} R_e$$

$$R_e = \frac{V_{cc} - V_{CE2}}{I_{e2}} \approx \frac{V_{cc} - V_{CE2}}{I_{c2}} \tag{4}$$

From transistor BC547 datasheet, $V_{BE2} = 0.66V$ at $I_{c2} = 1mA$. Therefore to have full output swing at V_{B2} and

V_{E2}, the average of these two voltages should be $\frac{V_{cc}}{2}$ as in equation (5).

$$\frac{V_{B2}+V_{E2}}{2} = \frac{V_{cc}}{2}$$
$$V_{E2} = \frac{V_{cc}-V_{BE}}{2} \approx 4.67V \tag{5}$$

3.3 Choose resistor R_e

By Ohms law, R_e could be calculated as in equation (6).

$$R_e = \frac{V_{E2}}{I_{e2}} \approx 4.67k\Omega \tag{6}$$

For standard E12 series resistors, choose $R_e = 4.7k\Omega$.

3.4 Determine bias resistor R3 and R4

Base current I_{b2} must not affect bias voltage determined by R_3 and R_4, as in equation (7).

$$I_{b2} = \frac{I_{e2}}{\beta+1} = \frac{V_{E2}}{R_e(\beta+1)} \approx 4.94\mu A$$
$$I_{R_{3,4}} > 10I_{b2} \approx 49.4\mu A \gg I_{b2} \tag{7}$$

Apply KVL as in equation (8) and bias conditions as (9), R_4 chosen to be $100k\Omega$ in E12 series, while R_3 calculated as in (10) to be $82k\Omega$.

$$I_{R_{3,4}} = \frac{V_{cc}}{R_3+R_4} \tag{8}$$
$$V_{B2} = V_{E2}+V_{BE} \approx 5.33$$
$$R_4 = \frac{V_{B2}}{I_{R_{3,4}}} \approx 108k\Omega \tag{9}$$
$$R_3 = \frac{V_{cc}-V_{B2}}{I_{R_{3,4}}} \approx 94.5k\Omega \tag{10}$$

3.5 Estimate gain, input impedance and output impedance

To estimate these parameters, use hybrid pi small signal model shown in Figure 2.

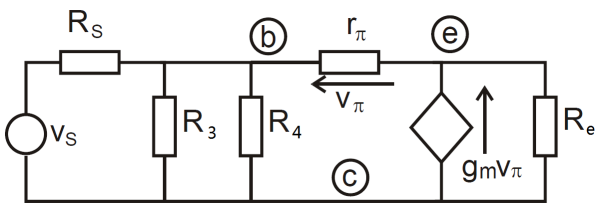

Figure 2: Small signal model of common collector stage (adapted from [3])

For simplicity, consider V_B as input voltage, R_{in} as input resistance from V_B, R_{in}, R_3, R_4 and R_s form a potential divider described by equation (11).

$$R_i = \left(\frac{1}{R_3}+\frac{1}{R_4}+\frac{1}{R_{in}}\right)^{-1}$$
$$V_B = V_S\frac{R_i}{R_i+R_S} \tag{11}$$

By using BJT characteristic r_π described by (12) and KCL analysis at emitter described by (13):

$$r_\pi = \frac{\beta}{g_m} \tag{12}$$
$$g_m(V_E-V_B)+\frac{V_E-V_B}{r_\pi}+\frac{V_E}{R_e} = 0 \tag{13}$$

Equation for gain (14) and input impedance (15) can be therefore analysed:

$$A = \frac{V_E}{V_S} = \frac{R_i}{R_i+R_S}\frac{V_E}{V_B} = \frac{R_i}{R_i+R_S}\frac{R_e(1+\beta)}{r_\pi+R_e(1+\beta)} \tag{14}$$
$$I_b = \frac{V_B-V_E}{r_\pi} = \frac{V_B}{r_\pi+R_e(1+\beta)}$$
$$R_{in} = \frac{V_B}{I_b} = r_\pi+R_e(1+\beta)$$
$$R_i = \left(\frac{1}{R_3}+\frac{1}{R_4}+\frac{1}{r_\pi+R_e(1+\beta)}\right)^{-1} \tag{15}$$

Calculate g_m and r_π from I_c:

$$g_m = \frac{qI_c}{kT} \approx 38.6I_c \tag{16}$$
$$r_\pi = \frac{\beta}{g_m} \approx \frac{5.175}{I_c} \approx 5.2k\Omega \tag{17}$$

Use source impedance for function generator $R_S \approx 50\Omega$, put values in equation for gain (14): $A \approx 0.99$, input impedance (15): $R_i \approx 43k\Omega$.

To calculate output impedance, consider a current source at output and the impact of the circuit on the current source as in Figure 3, where $R'_S = R_S \| R_3 \| R_4$.

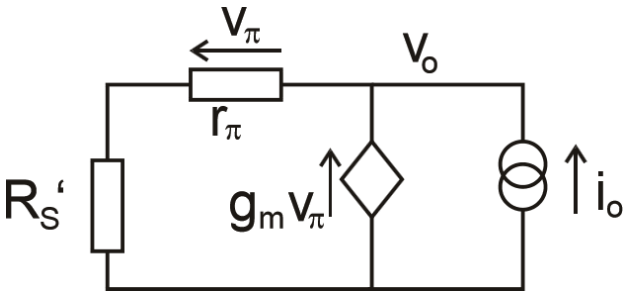

Figure 3: Simplified small signal model of common collector for calculate output impedance (adapted from [3])

Solving the system described by KCL analysis at emitter (18), V_π from potential divider (19):

$$i_o + g_m V_\pi - \frac{V_o}{R'_S + r_\pi} = 0 \tag{18}$$

$$V_\pi = -\frac{V_o r_\pi}{R'_S + r_\pi} \tag{19}$$

Output impedance can be therefore analysed by (20).

$$R_o = \frac{V_o}{I_o} = \frac{R'_S + r_\pi}{1+\beta} \tag{20}$$

Use source impedance for function generator $R_S \approx 50\Omega$, put values in equation for output impedance: $R_o \approx 26.1\Omega$.

4. First stage design

The common emitter stage need to be designed after common collector stage, because in order to avoid loading between two stages, output impedance of common emitter stage should be much less than input impedance of common collector stage as described by (21).

$$R_{o1} < \frac{R_{in2}}{10} \approx 4.3k\Omega \tag{21}$$

4.1 Determine load resistor R_c

The load resistor R_c of common emitter stage equals to the output impedance, so choose $R_c = 3.9k\Omega$.

4.2 Estimate gain and input impedance

To estimate these parameters, use hybrid pi small signal model shown in Figure 4.

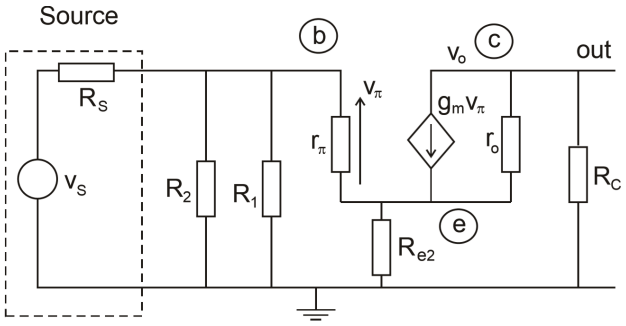

Figure 4: Small signal model of common emitter stage (adapted from [2])

Solving the system described by KVL analysis of V_c (22), KCL analysis at emitter (23), gain can be descibed as (24).

$$V_c = -g_m (V_b - V_e) R_c \tag{22}$$

$$\frac{V_e}{R_{e2}} + \frac{V_e - V_b}{r_\pi} - g_m (V_b - V_e) = 0 \tag{23}$$

$$A = \frac{V_c}{V_b} = \frac{-\beta R_c}{r_\pi + R_{e2}(1+\beta)} \tag{24}$$

If $R_{e2}\beta$ is large, gain can be approximated by (25).

$$A \approx -\frac{R_c}{R_{e2}} \tag{25}$$

Equation (26) described input impedance at base terminal:

$$R_b = \frac{V_b}{I_b} = \frac{V_b}{\frac{V_b - V_e}{r_\pi}} = r_\pi + R_{e2}(1+\beta) \tag{26}$$

Therefore total input impedance can be described as (27).

$$R_{in} = R_1 \| R_2 \| R_b = \left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{r_\pi + R_{e2}(1+\beta)} \right)^{-1} \tag{27}$$

4.3 Determine bias resistor R_{e2}

Had determined $R_{o1} = R_c = 3.9k\Omega$, gain of common collector stage should be approximately 0.91.

Desired gain is 6, so common emitter stage should have a gain of approximately 6.59.

By solving equation (25), $R_{e2} \approx 592\Omega$, choose $R_{e2} = 560\Omega$.

4.4 Determine bias resistor R_{e1} and V_{CE1}

To have maximum swing at the output of the common emitter stage, $V_{C1} = \frac{V_{cc}}{2} = 5V$.

Therefore collector current I_{c1} can be determined by (28).

$$I_{c1} = \frac{V_{cc} - V_{C1}}{R_c} \approx 1.28mA \tag{28}$$

Choose R_{e1} to be 470Ω, V_{CE} can be therefore determined by (29) using KVL.

$$\begin{aligned} I_{e1} &= I_{c1}\left(1 + \frac{1}{\beta}\right) \approx 1.29mA \\ V_{CE1} &= V_C - I_{e1}(R_{e1} + R_{e2}) \approx 3.67V \end{aligned} \tag{29}$$

4.5 Determine bias resistors R_1 and R_2

Solving bias condition described by V_{B1} (30), input impedance specification (31), potential divider (32):

$$V_{B1} = V_{C1} - V_{CE1} \approx 1.33V \tag{30}$$

$$r_\pi \approx 4.04k\Omega$$

$$R_{in} = \left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{r_\pi + R_{e2}(1+\beta)} \right)^{-1} \leq 40k\Omega \tag{31}$$

$$\frac{V_{B1}}{V_{cc}} = \frac{R_2}{R_1 + R_2} \tag{32}$$

In E12 series, choose $R_1 = 390k\Omega$ and $R_2 = 100k\Omega$.

4.6 Determine emitter decoupling capacitor C_e

Apply equation (33), choose $f = 1\text{kHz}$, $C_e \geq 5.02\mu\text{F}$.

$$C_e \geq \frac{10}{2\pi f \left(R_{e1} \| \left(R_{e2} + \frac{r_{\pi 1}}{\beta+1} + \frac{R_1 \| R_2}{\beta+1} \right) \right)} \tag{33}$$

4.7 Determine input coupling capacitor C_i

Apply equation (34), choose $f = 1\text{kHz}$, $R_S = 50\Omega$ from function generator, $C_i \geq 33.6\text{nF}$.

$$C_i \geq \frac{10}{2\pi f\left(R_S + R_1 \| R_2 \| \left(r_{\pi 1} + (\beta+1)R_{e2}\right)\right)} \tag{34}$$

5. Multi-stage design

The overall gain of multi-stage amplifier calculated from equation (14) and equation (24) is -6.10, within specification.

The overall input impedance of multi-stage amplifier from equation (31) is $47k\Omega$, within specification.

The overall output impedance of multi-stage amplifier from $R_{o1} = R_c$ and equation (20) is 43Ω, within specification.

6. SPICE simulation

After determined the parameters of components, the circuit was simulated by using LTspice software.

Quiescent voltage analysed from simulation as shown in Figure 5, there were some difference from calculated value, but still acceptable.

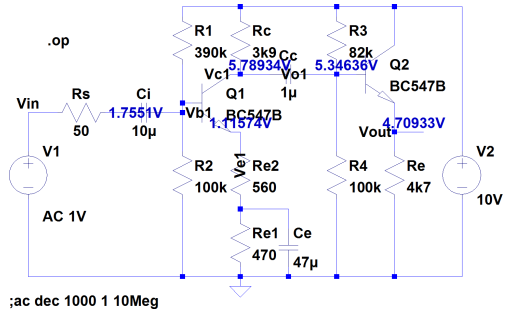

Figure 5: LTspice operation point analysis of multi-stage amplifier

Frequency response analysed from simulation as shown in Figure 6, mind-band gain was 6.04, bandwidth was 10.7MHz.

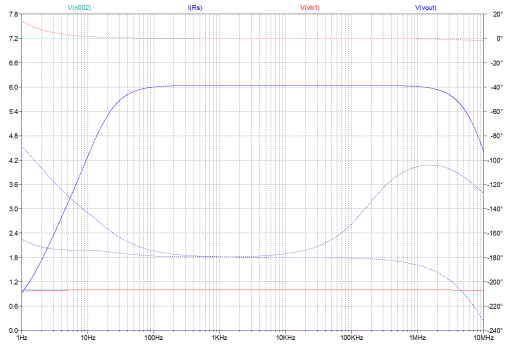

Figure 6: LTspice frequency response analysis of multi-stage amplifier

7. Laboratory work

7.1 Measuring gain

Mid-band gain can be easily measured by setup a function generator at input terminal, in sine wave mode with mid-band frequency (e.g. $f = 1\text{kHz}$), then use an oscilloscope to measure the amplitude of output signal voltage, gain $A = \frac{V_{out}}{V_{in}}$.

7.2 Measuring input impedance

Input impedance can be measured by connect a potentiometer in series with input terminal as shown in Figure 7, then adjust the potentiometer until amplitude of signal at input terminal become half of original signal, the input resistance is approximately the same as the resistance of the potentiometer.

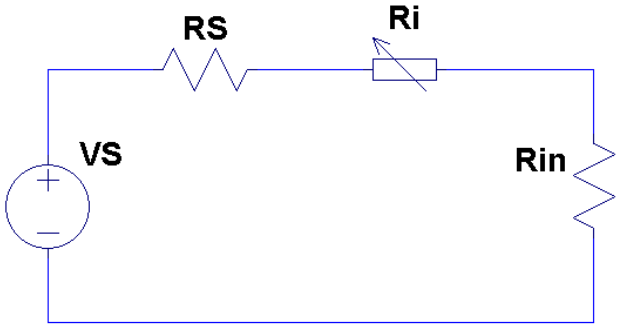

Figure 7: Input impedance measuring

7.3 Measuring output impedance

Output impedance can be measured at the same way, by connect a load potentiometer at output terminal as shown in Figure 8, then adjust the potentiometer until amplitude of signal at output terminal become half of original signal, the output resistance is approximately the same as the resistance of the potentiometer.

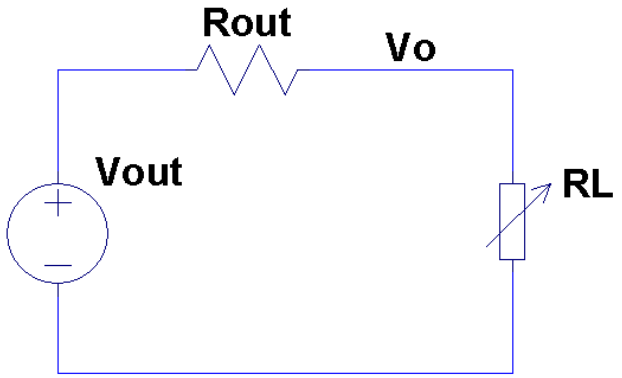

Figure 8: Output impedance measuring

7.4 Measuring quiescent point

Quiescent voltage was measured firstly, as shown in Table 1, not much difference from simulation values.

Table 1: Quiescent voltage measured in laboratory

Voltage	Simulation	Measurement
Vc1	5.789	5.71
Vb1	1.755	1.766
Ve1	1.116	1.132
Vc2	10	9.99
Vb2	5.346	5.34
Ve2	4.709	4.72

7.5 Measuring first stage

By using the method described above, the mid-band gain of first stage as shown in Figure 9, was $A \approx \frac{6.60}{1.02} = 6.47$.

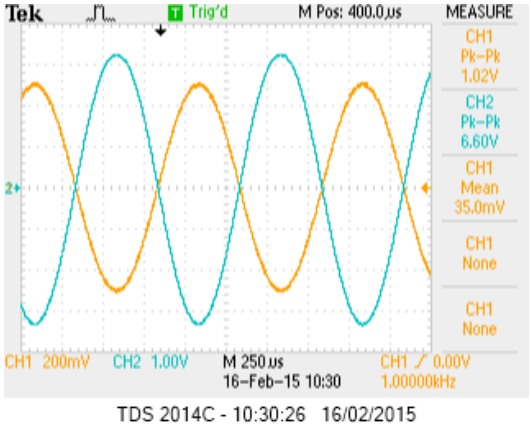

Figure 9: Mid-band gain measurement of first stage, oscilloscope screen capture of input signal at CH1, output signal at CH2

The input impedance is $R_{in} \approx R_i = 60.1k\Omega$, when input signal amplitude became half the signal from function generator as shown in Figure 10.

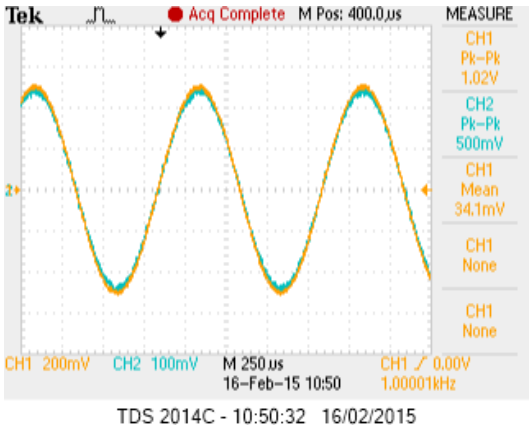

Figure 10: Input impedance measurement of first stage, oscilloscope screen capture of half input signal amplitude

The output impedance is $R_{out} \approx R_L = 3.84k\Omega$, when output signal amplitude became half the original signal as shown in Figure 11.

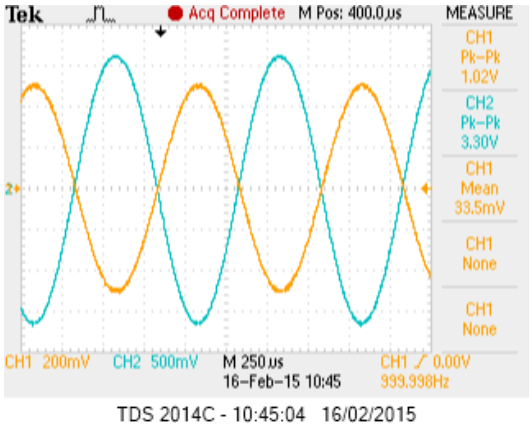

Figure 11: Output impedance measurement of first stage, oscilloscope screen capture of half output signal amplitude from original output signal shown in Figure 9

By measuring voltage gain at different frequencies, the frequency response analysis can be plotted as shown in Figure 12, bandwidth ≈ 2MHz.

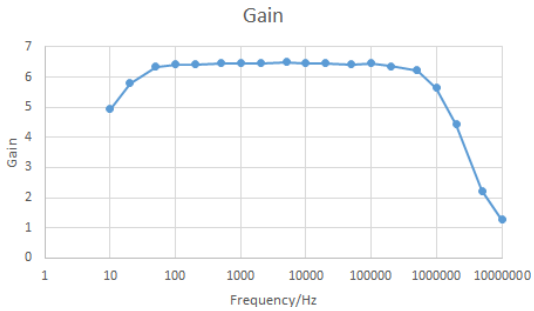

Figure 12: Frequency response analysis, produced from measuring voltage gain at different frequencies

Mid-band gain of first stage with C_e removed measured as shown in Figure 13, was $A \approx \frac{3.72}{1.02} = 3.65$. From equation (24), R_{e2} become approximately doubled, therefore gain approximately halved.

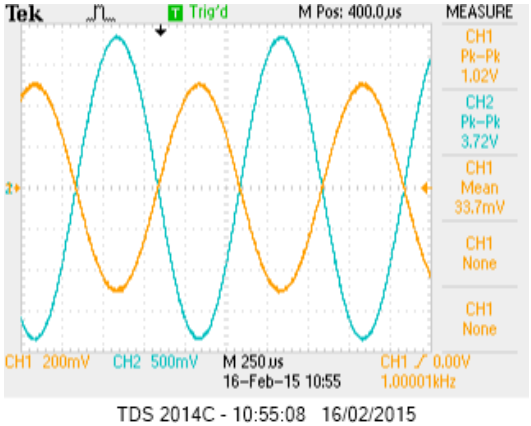

Figure 13: Mid-band gain measurement of first stage, after C_e removed

Mid-band gain of first stage with C_e bypassed R_{e1} and R_{e2}

measured as shown in Figure 14, was $A \approx \frac{7.20}{63.2\times10^{-3}} = 114$. From equation (24), gain from transistor is only affected by $\frac{R_c}{R_{\pi 1}} \approx 0.975$.

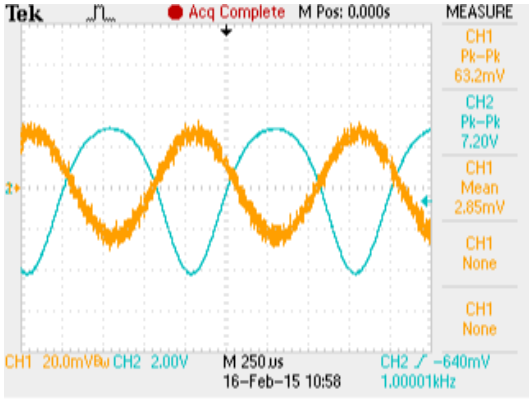

Figure 14: Mid-band gain measurement of first stage, after emitter resistance totally bypassed by C_e

7.6 Measuring second stage

By using the method described above, the mid-band gain of second stage as shown in Figure 15, was $A \approx \frac{5.00}{5.04} = 0.99$.

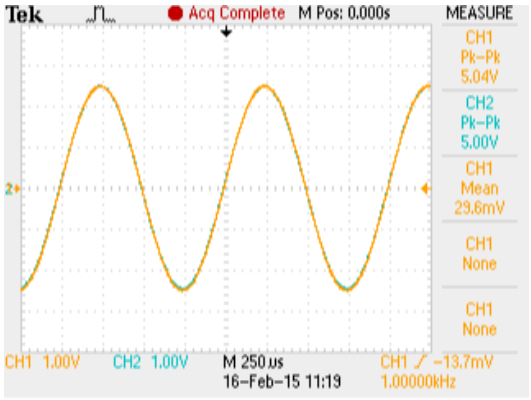

Figure 15: Mid-band gain measurement of second stage, oscilloscope screen capture of input signal at CH1, output signal at CH2

The input impedance is $R_{in} \approx R_i = 44.7k\Omega$, when input signal amplitude became half the signal from function generator as shown in Figure 16.

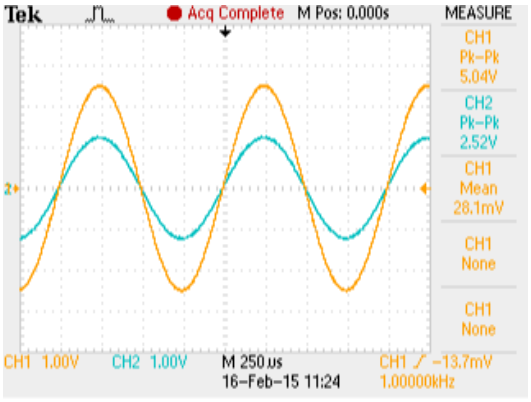

Figure 16: Input impedance measurement of second stage, oscilloscope screen capture of half input signal amplitude

The output impedance is $R_{out} \approx R_L = 152.3\Omega$, when output signal amplitude became half the original signal as shown in Figure 17.

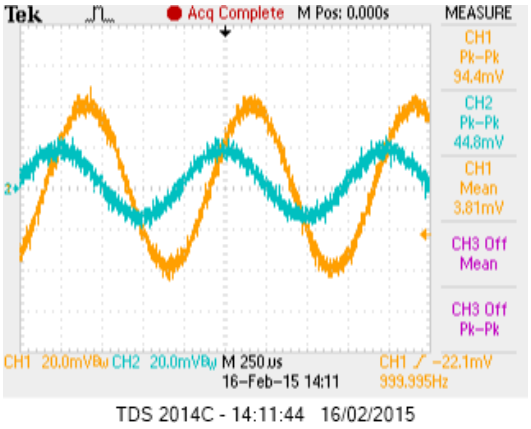

Figure 17: Output impedance measurement of second stage, oscilloscope screen capture of half output signal amplitude from input signal (gain ≈ 1)

7.7 Measuring multi-stage amplifier

By using the method described above, the mid-band gain of multi-stage stage as shown in Figure 18, was $A \approx \frac{6.04}{1.02} = 5.92$.

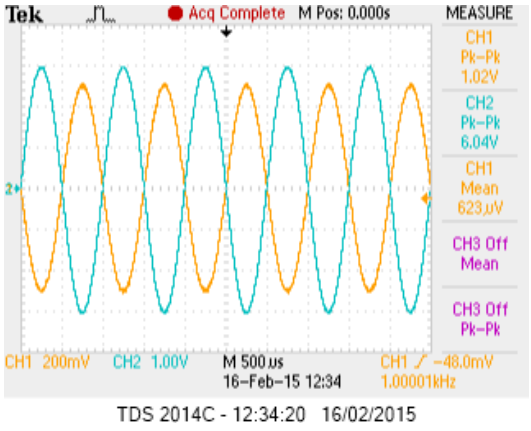

Figure 18: Mid-band gain measurement of multi-stage amplifier, oscilloscope screen capture of input signal at CH1, output signal at CH2

The input impedance is $R_{in} \approx R_i = 60.0k\Omega$, when input signal amplitude became half the signal from function generator as shown in Figure 19.

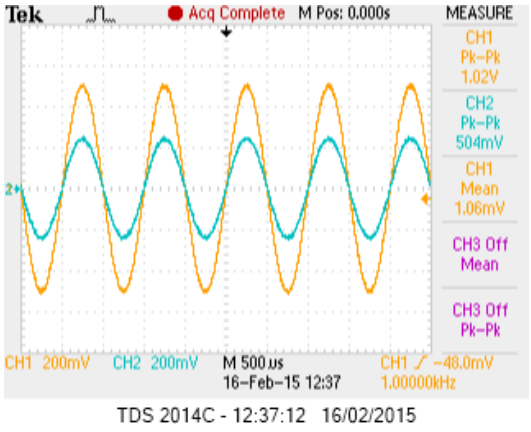

Figure 19: Input impedance measurement of multi-stage amplifier, oscilloscope screen capture of half input signal amplitude

To avoid clipping, the amplitude of input signal reduced as in Figure 20.

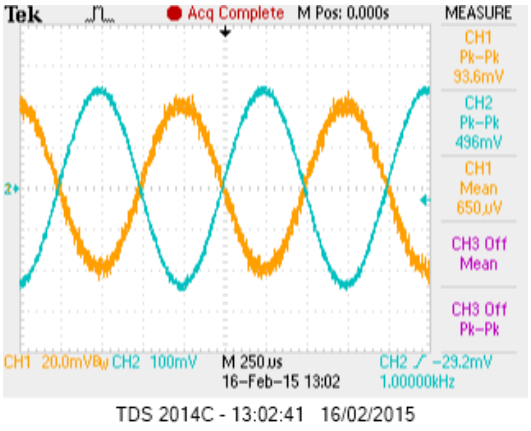

Figure 20: Mid-band gain measurement of multi-stage amplifier, at reduced input signal amplitude

The output impedance is $R_{out} \approx R_L = 180.1\Omega$, when output signal amplitude became half the original signal as shown in Figure 21.

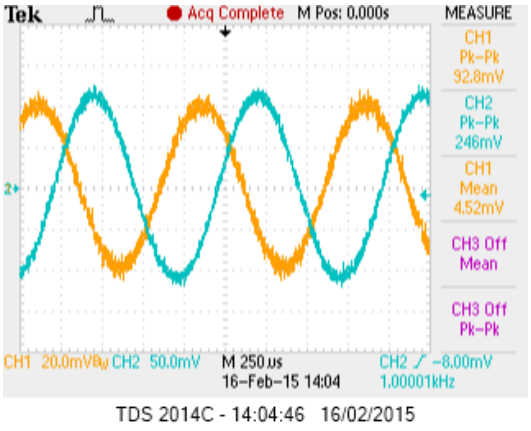

Figure 21: Output impedance measurement of multi-stage amplifier, oscilloscope screen capture of half output signal amplitude from original output signal shown in Figure 20

8. Reflection

There were some differences in values of quiescent voltage, gain, input and output impedance from calculated, simulation and measured values, but still acceptable. And the overall gain $A = 5.92 \approx 6$, input impedance $R_{in} = 60.0k\Omega > 40k\Omega$ and output impedance $R_{out} = 180.1\Omega < 1.3k\Omega$ were all within the specifications, therefore the design was succeed.

References

[1] Sasan Mahmodi "Circuit Design" [*Online*]. Available: https://secure.ecs.soton.ac.uk/notes/elec2205/D3/d3coursework2.pdf

[2] Peter Wilson "Lecture slides A" [*Online*]. Available: https://secure.ecs.soton.ac.uk/notes_so/elec2216/notes/elec2216_slides_1.pdf

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