# Sequence recogniser

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- 11100101

From <https://secure.ecs.soton.ac.uk/notes/elec2205/D2/current/html/D2_Specification_2014_v3.html>

| Right | D | S2 | S1 | S0 | S2' | S1' | S0' | MATCH' |
|---|---|---|---|---|---|---|---|---|
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 |
| | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 |

*MATCH' is a D-type flip-flop buffer for MATCH signal

S0'

| S1S0\DS2 | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | | 1 | 1 | 1 |
| 01 | | | | |
| 11 | | | 1 | 1 |
| 10 | | 1 | | 1 |

$S0' = \sim D \cdot S2 \cdot \sim S0 + D \cdot \sim S1 \cdot \sim S0 + D \cdot S1 \cdot S0 + D \cdot \sim S2 \cdot S1$

S1'

| S1S0\DS2 | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | | | | |
| 01 | | | 1 | 1 |
| 11 | | | | 1 |
| 10 | | 1 | 1 | 1 |

$S1' = D \cdot \sim S1 \cdot S0 + D \cdot \sim S2 \cdot S1 + S2 \cdot S1 \cdot \sim S0$

S2'

| S1S0\DS2 | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | | 1 | | |
| 01 | | | 1 | |
| 11 | 1 | | | |
| 10 | | 1 | | |

$S2' = \sim D \cdot S2 \cdot \sim S1 \cdot \sim S0 + D \cdot S2 \cdot \sim S1 \cdot S0 + \sim D \cdot \sim S2 \cdot S1 \cdot S0 + \sim D \cdot S2 \cdot S1 \cdot \sim S0$

$MATCH' = D \cdot S2 \cdot S1 \cdot S0$