D1 SystemVerilog Design of a Sequential Multiplier

Introduction

This exercise is done individually and the assessment is:

- By formal report describing the final design, its development, implementation and testing.
- By results recorded on the Design Completion Form, available from the ELEC2014 notes intranet site.

One full day of supervised laboratory time has been allocated for this exercise, comprising both laboratory sessions: am from 10:00 to 13:00 and pm from 14:00 to 17:00.

Specification

The objective of this exercise is to design a complete n-bit, where n>=4, unsigned binary sequential multiplier and implement it on a MachXO2 CPLD. The controller should be written in SystemVerilog, simulated in Modelsim, synthesised in Synplify Pro (which is a part of ispDiamond) and implemented on a MachXO2 CPLD using ispDiamond. The multiplier must implement the SHIFT & ADD algorithm shown in Figure 1. An example of 3-bit multiplication sequence is shown in Figure 2.

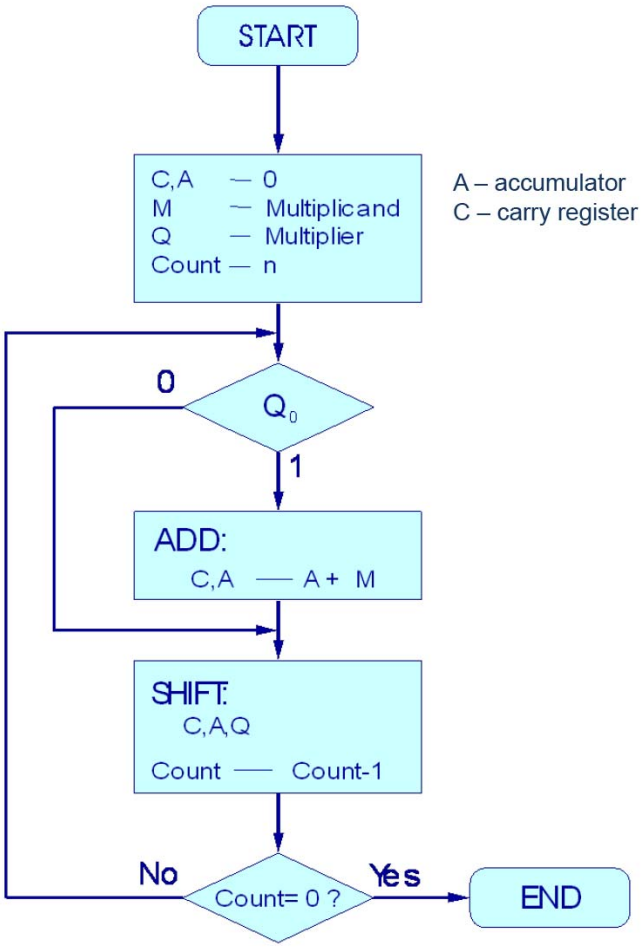

Figure 1. SHIFT-ADD binary multiplication algorithm.

The D1 briefing lecture slides describe the SHIFT & ADD algorithm in detail, provide an application example and some coding suggestions in SystemVerilog. A block diagram of the system and required input output signals are shown in Figure 3. It is permissible to combine the ADD and SHIFT signals into a single signal in case you decide to implement the shift and add operations in a single clock cycle. You may also add an active low asynchronous reset input (nreset) to the SHIFT & ADD sequencer if you wish.

	M=	1	1	1	(M=7)			
	C	A			Q = 5			
	0	0	0	0	1	0	1	Initial Values
	0	1	1	1	1	0	1	ADD: A := A+M
	0	0	1	1	1	1	0	SHIFT (cycle 1)
	0	0	0	1	1	1	1	SHIFT (cycle 2)
	1	0	0	0	1	1	1	ADD: A:=A+M
	0	1	0	0	0	1	1	SHIFT (cycle 3)
A,Q=	0	**1**	**0**	**0**	**0**	**1**	**1**	**= 35**

Figure 2. Example of a 3-bit multiplication sequence where M=7 and Q=5.

The operation of the system is as follows:

- when the START signal is asserted (you can choose whether you want to make it active high or active low), the system begins the multiplication of two n-bit input numbers in unsigned binary: M - the multiplicand and Q - the multiplier.

- on completion of the multiplication sequence, the system stops, asserts the active high output READY and displays the 2n-bit product of M and Q in the registers A and Q.

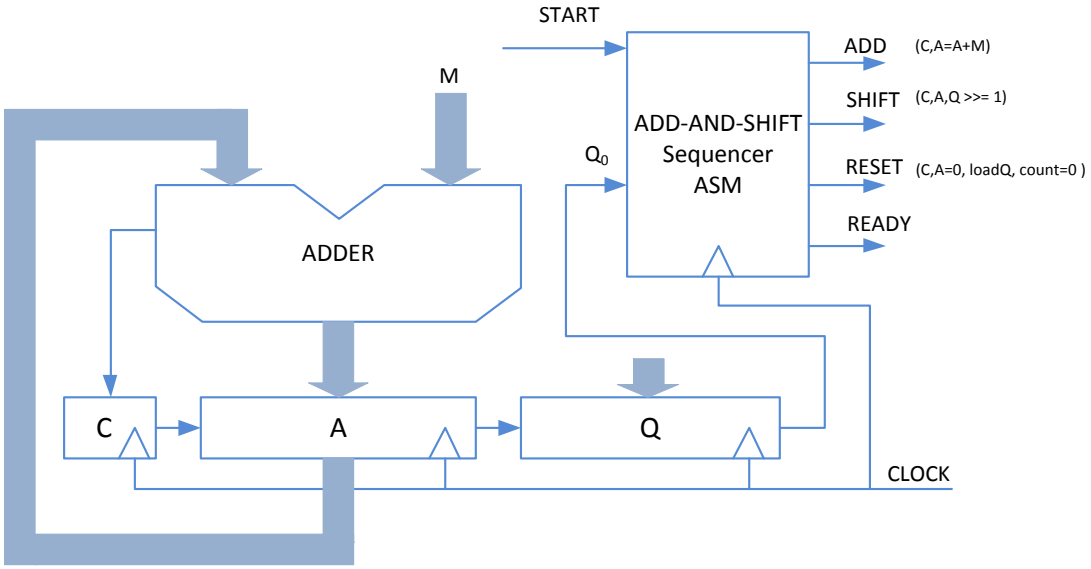

Figure 3. Sequential multiplier block diagram .

The system must work correctly with the internal MachXO2 clock of about 25MHz.

Design strategy

Develop an ASM chart of the sequencer using techniques discussed during your First Year. You can use the ASM suggested in the briefing lecture slides. Pay attention to any unspecified states and ensure that your design will never enter such a mode. Develop SystemVerilog code and a separate testbench for each module in your design. Also write a testbench for the whole design. Read the MachXO CPLD Synthesis Walk-Through document available on the ELEC2202 webpage which explains the CPLD design steps and associated software tools. Synthesise each module separately and test it in the laboratory using the MachXO switches and LEDs. Demonstrate your modules and the whole design using a very slow clock which you can derive from the fast MachXO2 clock using a counter. Carry out all the design work before you come to the laboratory. Build the circuit and verify its operation. You will be issued with a development kit an ispLattice MachXO2 mini kit and an interface board which provides a conversion between the 3.3V logic of the MachXO2 mini kit and the 5V logic of the Digital Testbed. This will allow you to use the Digital Test Bed in your tests. Documentation about the interface Board (BB4MM) and Lattice MachXO kit can be found in the PLD area on the Electronics Laboratory pages: https://secure.ecs.soton.ac.uk/notes/ellabs/databook/pld/. You should use the Digital Testbed's facilities to simulate the lamps, clocks, switches and buttons to verify and demonstrate your design. Ensure that you complete all the requirements on the Design Completion Form, except the last two which are optional and extend the specification. The Design Completion Form should be incorporated into your formal report.

Formal report

The formal report must be submitted by 4pm on the fifth working day (i.e. one week) after the laboratory. Submit through C-BASS and ECS front office. An electronic copy and one paper copy of the report are required. The report should not exceed 2000 words in length. It must contain a full discussion of your design, including the final circuit diagrams, sequencer ASM chart, Modelsim simulation results and any SystemVerilog source code of the PLDs . All source files must be packaged in a zip file and submitted electronically as a separate file at the same time. The reports will normally be marked and returned to you before the end of term, so that any feedback s can be incorporated into later reports. Bonus marks will be given for extended specification and implementation of novel concepts.

tjk, 16 Oct'13