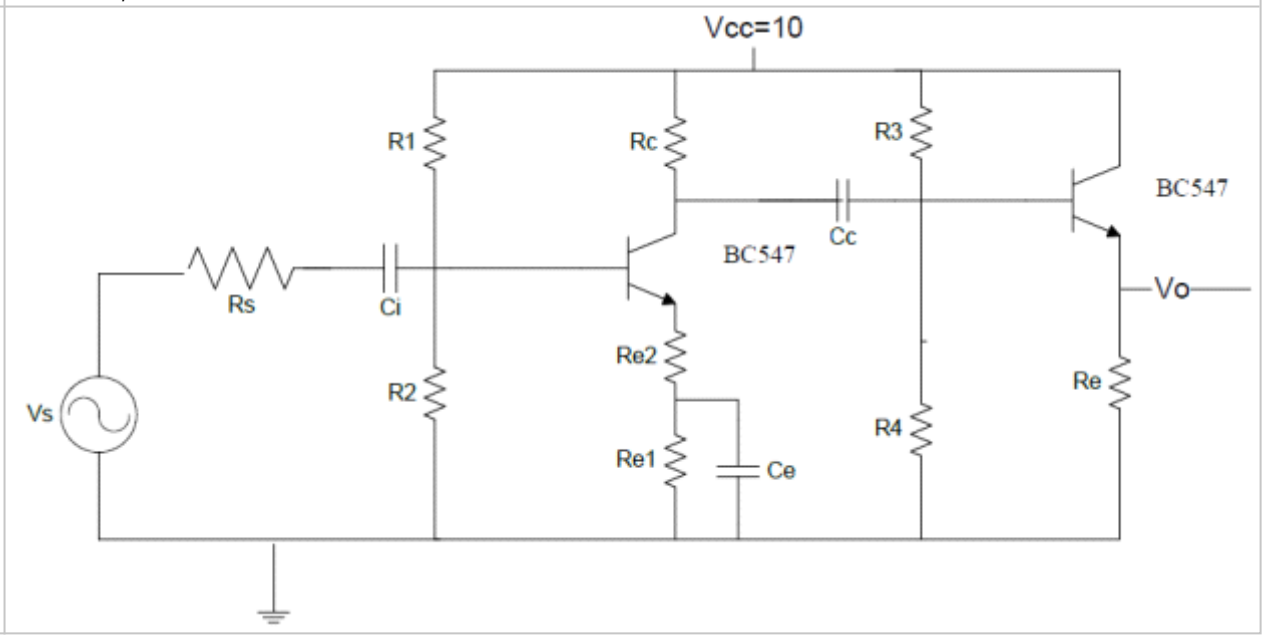
D3

12 February 2015 16:42

Overall gain	6 ± 0.6
Input impedance	$> 40 \pm 4k\Omega$
Output impedance	$< 1.3 \pm 0.13k\Omega$
Supply voltage	$0, V_{cc} = 10V$
BJT	NPN, BC547, $\beta = 200$.
Circuit	

Remember the output impedance of the first stage should at least be 10x less than the input impedance of the second stage to avoid loading between two stages.

Operation points

V	Simulation	Measurement
Vc1	5.789	5.71
Vb1	1.755	1.766
Ve1	1.116	1.132
Vc2	10	9.99
Vb2	5.346	5.34
Ve2	4.709	4.72

Stage	Gain	Input impedance	Output impedance
1st	6.47	60.1k	3.84k
2nd	0.992	44.7k	152.3
Multi	5.92	60.0k	180.1