A method to design the two stage amplifier of the D3 course work:

Our strategy here is to start the design with the second stage (the common collector stage) of the amplifier. Having calculated all the elements of the second stage, we then proceed to design the first stage. It is not compulsory to follow the design method proposed here, however if you decide to choose another design method, you need to explain step by step in great details what you are doing and why you are doing it.
On the other hand, if you decide to follow the design method discussed in this document, then you need to explain in your report how the equations are derived and what approximations are made.
Remark: For BC547 transistors, the current gain β can be considered to be around 200 for the current collectors between 1 to 5 mAs.

1) Choose a reasonable value for I_{C2} (current collector of the second stage)
2) For a maximum swing in the output of the second stage, choose $V_{E2} = V_{CE2} = V_{CC}/2$
3) Then calculate V_{b2} and I_{b2}
4) Calculate $I_{R_{3,4}}$ so that $I_{R_{3,4}} >> I_{b2}$ (e.g. $I_{R_{3,4}} \approx 10 I_{b2}$)
5) Ignore the DC base current of this transistor ($I_{R_{3,4}} >> I_{b2}$ thus $I_{b2} \approx 0$) and calculate R_3 and R_4 using the following equations:

$$I_{R_{3,4}} = \frac{V_{cc}}{R_3 + R_4} \tag{1}$$

$$R_4 = \frac{V_{b2}}{I_{R_{3,4}}} \tag{2}$$

6) Then $R_e = \frac{V_{E2}}{I_{C2}}$
7) Verify R_{o2} (the output impedance of the second stage) is less than 150 Ω
8) Calculate $r_{\pi 2} = \beta \frac{V_T}{I_{c2}}$ and R_{in2} (the input impedance of the second stage)
9) Calculate R_c using (3) (R_{o1} is the output impedance of the first stage):

$$R_{in2} \geq 10 R_{o1} \tag{3}$$

10) Calculate R_{e2} using $G \approx \frac{R_c}{R_{e2}} = 6$
11) Calculate $R_1 \| R_2$ using (4):

$$R_{in} = R_1 \| R_2 \| (\beta + 1) R_{e2} \geq 40 k\Omega \tag{4}$$

12) Write the maximum swing requirement for the output of the first stage:
13) Choose a reasonable DC collector current for the first stage, I_{C1}
14) Calculate the DC voltage for V_{CE1} by using condition (12)
15) Calculate R_{e1} by using a DC KVL in the output of the first stage:
16) Calculate V_{b1}
17) Calculate R_1 and R_2 using equation(5) and the fact that $R_1 \| R_2$ is already known from stage (11)

$$\frac{V_{b1}}{V_{CC}} = \frac{R_2}{R_1 + R_2} \tag{5}$$

18) Choose C_e to satisfy inequality (6) (f = *1 kHz*)

$$C_e \geq \frac{10}{2\pi\ f\left(R_{e1}\left\|\left(R_{e2}+\frac{r_{\pi 1}}{\beta+1}+\frac{R_1\|R_2}{\beta+1}\right)\right.\right)} \tag{6}$$

19) Choose C_i to satisfy inequality (7) (f = *1 kHz*)

$$C_i \geq \frac{10}{2\pi\ f\left(R_s+R_1\|R_2\|\left(r_{\pi 1}+(\beta+1)R_{e2}\right)\right)} \tag{7}$$