

# Switch-mode Light Dimmer Using Multivibrators

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**Abstract—** The objective of this design project is to understand astable and monostable circuits, design and implement a light bulb dimmer using op-amps, capacitors, and resistors to create multivibrators.

**Keywords—** astable, monostable, multivibrator, op-amps, buffer

## I. INTRODUCTION

The project was designed with the given specifications for the student. The specifications for this was to reach a frequency of 500 Hz and it should have a minimum and maximum duty cycle of 35% and 85%. This project was also made by following the exercise from the laboratory 4 of EEE 148 as a guide to create the astable and monostable part of the circuit. The schematic and the equations were taken from that exercise to create the circuit of this project. The materials used were also based on that exercise, where it used LM358 op-amps, capacitors, resistors, and 1N4007 diodes. An additional TIP31C was added to act as a switch in the loading stage.

## II. METHODOLOGY

There were multiple steps taken that were necessary to complete this project.

### A. Astable Multivibrator Design

In this part, the specified frequency must be achieved which is 500 Hz. To calculate the values of the Astable part, calculations must be set to the period of the circuit which is 2 milliseconds. The equations used to calculate the values of the Astable Multivibrator are shown below.

$$f = \frac{1}{T} \quad (1)$$

$$\beta = \frac{R2}{R1 + R2} \quad (2)$$

$$T = 2RC \times \ln\left(\frac{1+\beta}{1-\beta}\right) \quad (3)$$

To solve the values of the resistors it must be noted that the capacitor value was set to 0.1uF for this part of the design and for all the succeeding parts due to unavailability of other values of capacitors. The values for R1 and R2 were set to 12k ohms and 10k ohms due to their availability in the lab. With that, it was calculated that the value for R is 10k ohms to get the desired frequency. Shown in figures 1, 2, and 3 are the full schematic

of the Astable stage, the waveform generated, and the results in LTSpice.

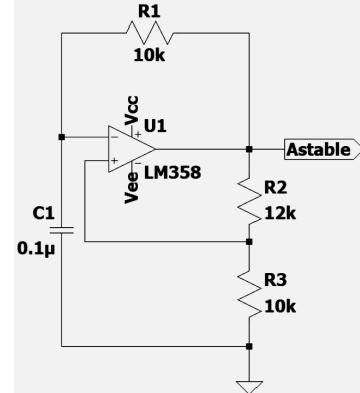


Fig. 1 Astable op-amp multivibrator schematic design

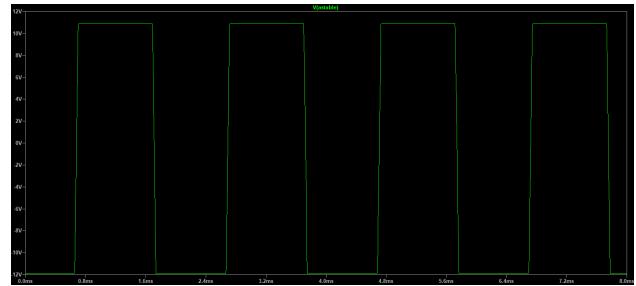


Fig. 2 Astable waveform generated in LTSpice

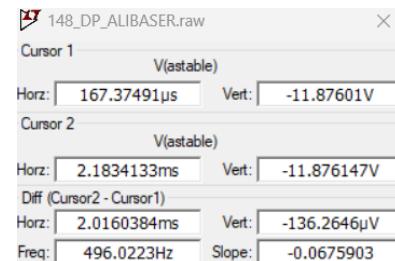


Fig. 3 Astable period and frequency values generated in LTSpice

As you can see from the figure, the values are not exactly equal to the values desired but since the difference is small and in the range of  $\pm 10$  Hz, the values generated are accepted for this project.

### B. Monostable Multivibrator Design

In this stage of the project, the specified duty cycle must be met. To solve the values for the monostable stage, some values from the equations of the laboratory 4 of EEE 148 were set and assumed already. The period is set to 2 milliseconds, and the duty cycles were 35% and

85%. With those values, the timing period was also set to 0.7 milliseconds and 1.7 milliseconds. The equation used for solving the values of the Monostable Multivibrator are shown below.

$$T_{Timing\ Period} = RC \times \ln(1 + \frac{R_1}{R_2}) \quad (4)$$

The values of R and R1 were set already to 5.1k ohms and 50k ohms. Those values were chosen in a trial-and-error way and through using the equation 4 to verify if it will work in the circuit. The value of R2 that was solved when the duty cycle is around 85% was 1.8k ohms. When the duty cycle is 35% it is around 15.5k ohms.

It was decided to put the 100k ohm potentiometer in before the calculated value for the R2 resistor when it is in 85% duty cycle and must be paralleled to another resistor with a value of 16k ohms to achieve the 15.5k ohms when the value of the potentiometer is 100k ohms. The value of the paralleled resistor will be added to the R1 value to achieve the desired 35% duty cycle. The other function of the potentiometer is to short the 16k ohms resistor when the potentiometer is set 0 ohms, so it can achieve the 85% duty cycle. The schematic diagram for the whole stage is shown in figure 4. The waveform and the results are also shown in figure 5 and 6. It must be noted that there was a margin of error of  $\pm 5\%$  in each duty cycle and it can be seen in the results generated that the values are not exact but it was in the range of the error and it was acceptable.

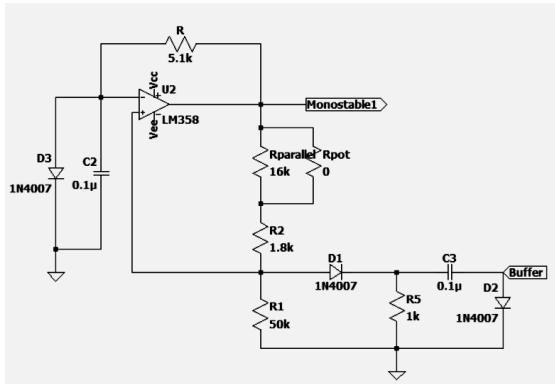


Fig. 4 Monostable op-amp multivibrator schematic design

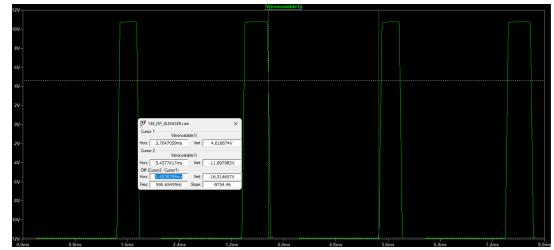


Fig. 5 Monostable waveform generated for 85% duty cycle

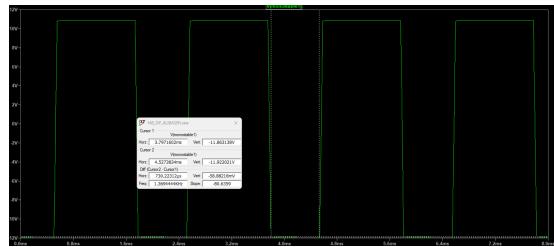


Fig. 6 Monostable waveform generated for 35% duty cycle

### C. Buffer

In order to prevent too much current from the source of a signal, a buffer stage must be added in between the astable stage and monostable stage and in between the monostable stage and the loading stage. It is also to isolate the previous stage or one section to the next stage. The op-amp implementation for the buffer stage is shown below in figure 7.

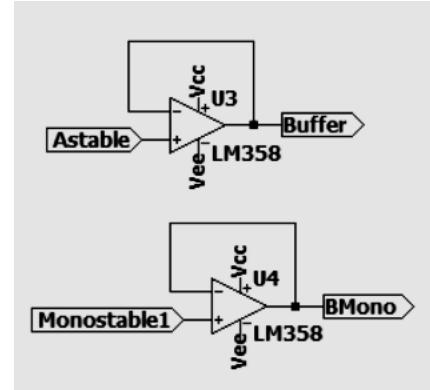


Fig. 7 Buffer schematic diagram between each stages

### D. Loading Stage

To transform the signal from the cascaded circuit, the loading stage was implemented. A light bulb was used to observe its behavior. In the LTSpice implementation shown in figure 8, a 5 ohm resistor acting as the light bulb was put in between the input voltage and the TIP31C transistor.

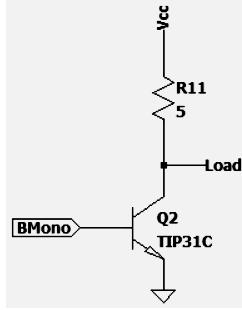


Fig. 8 LTSpice schematic diagram of the loading stage

### III. RESULTS AND DISCUSSION

After the hardware implementation of the circuits shown in LTSpice. It will be shown that there were some adjustments made to the values of the resistors to adjust to their availability in the laboratory and to the real-life values. The difference of the simulated and hardware implementation were not too big to be significant. The values of the resistors in real-life or hardware implementation were in standard values of the resistors. Shown in figure 9 is the hardware implementation of the actual circuit.

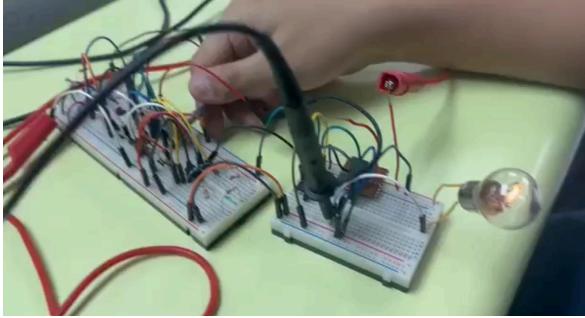


Fig. 9 Hardware implementation of the design project

The results were observed in an oscilloscope to see if the specified frequency and duty cycles were met. The plots are shown in figures 10 and 11 where it can be observed that the specified values are met. The observed frequency of the hardware implementation is in the range of 490-500 Hz and the observed duty cycles were 34.4% and 81.68%. Since there was a  $\pm 10$  Hz margin of error in the frequency and  $\pm 5\%$  margin of error for the duty cycle, the observed results were acceptable.

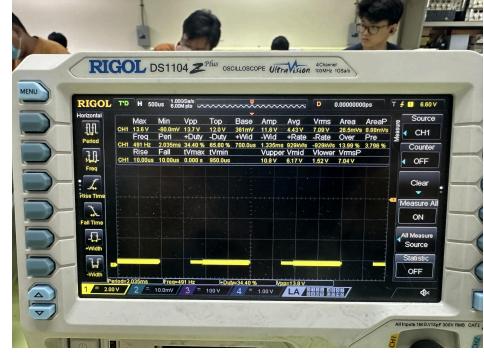


Fig. 10 Minimum duty cycle shown in the monostable stage



Fig. 11 Maximum duty cycle shown in the monostable stage

When the output of the monostable stage was added to the loading stage, the expected behavior of the light bulb was observed. In the minimum duty cycle, the light in the bulb is low and the light is high when it is in the maximum duty cycle.

### IV. CONCLUSION

The design made by the student was successful in following the specifications provided to them. It was also shown that using multivibrators as light dimmers can be effective.

The equations used from the previous laboratory activities and the solved values for the missing values were crucial to create the whole design. Simulating it first in LTSpice was essential to prevent damages in the laboratory. However, it was also noted that simulations and calculations do not always align perfectly with the actual hardware, requiring adjustments to the circuit. Therefore, designing a system like this requires an understanding of the behavior of each circuit stage.

### REFERENCES

- [1] UP Electrical and Electronics Engineering, *EEE 148 Laboratory Exercise 4, 2024*